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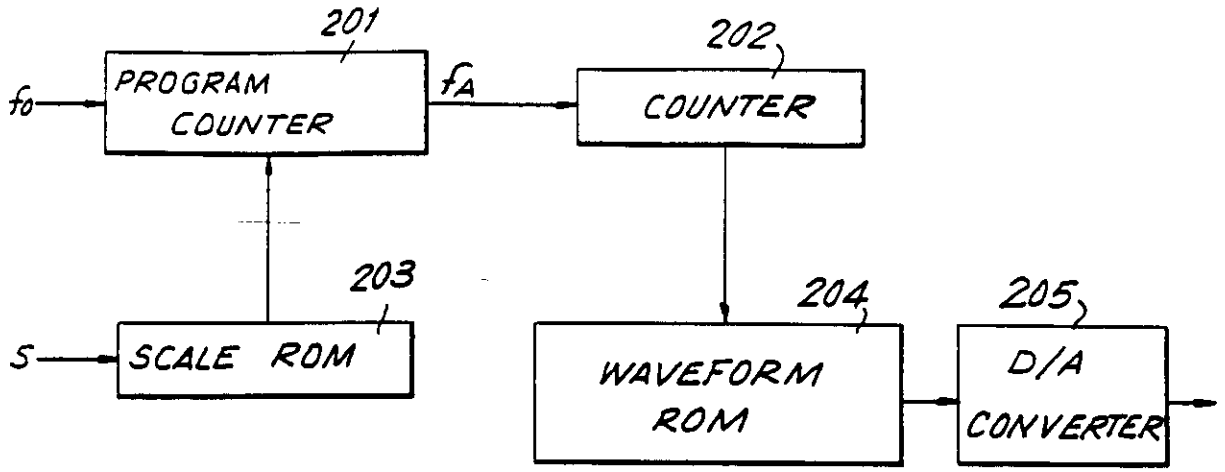
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FIG. 2



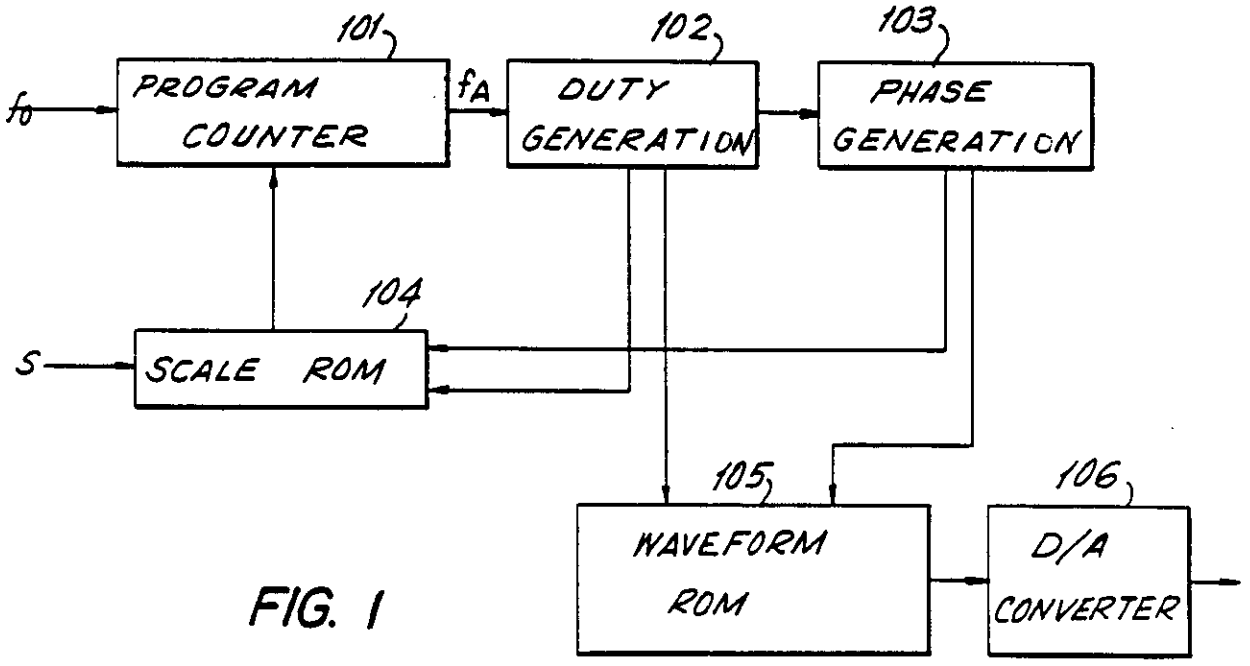


FIG. 1

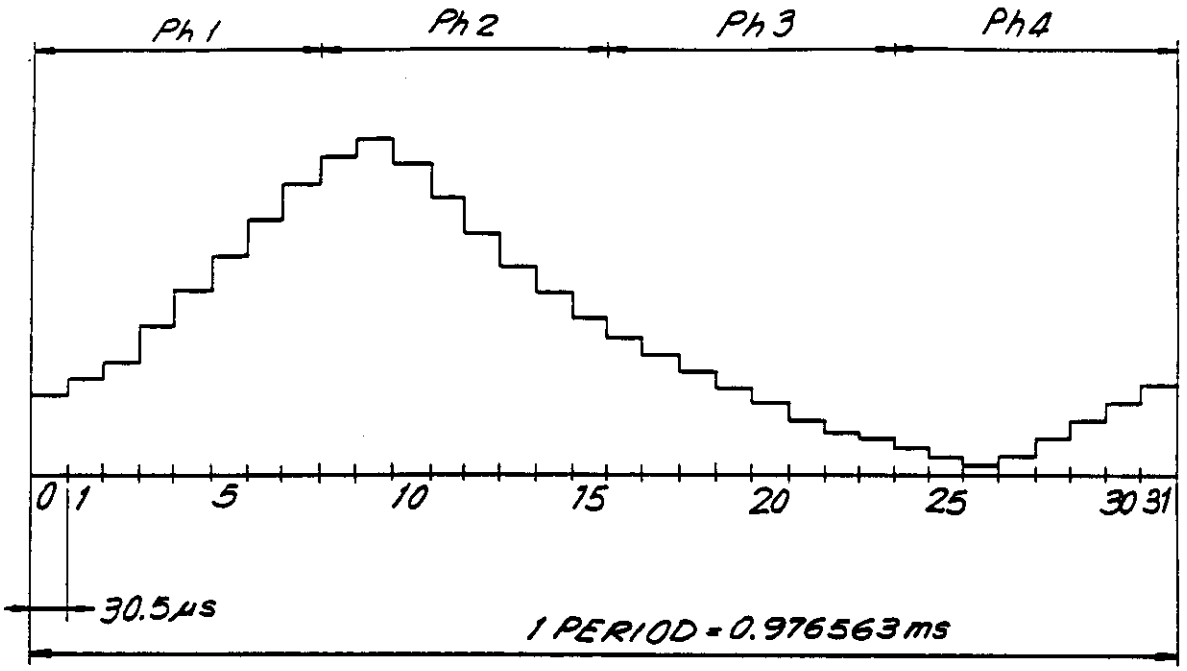
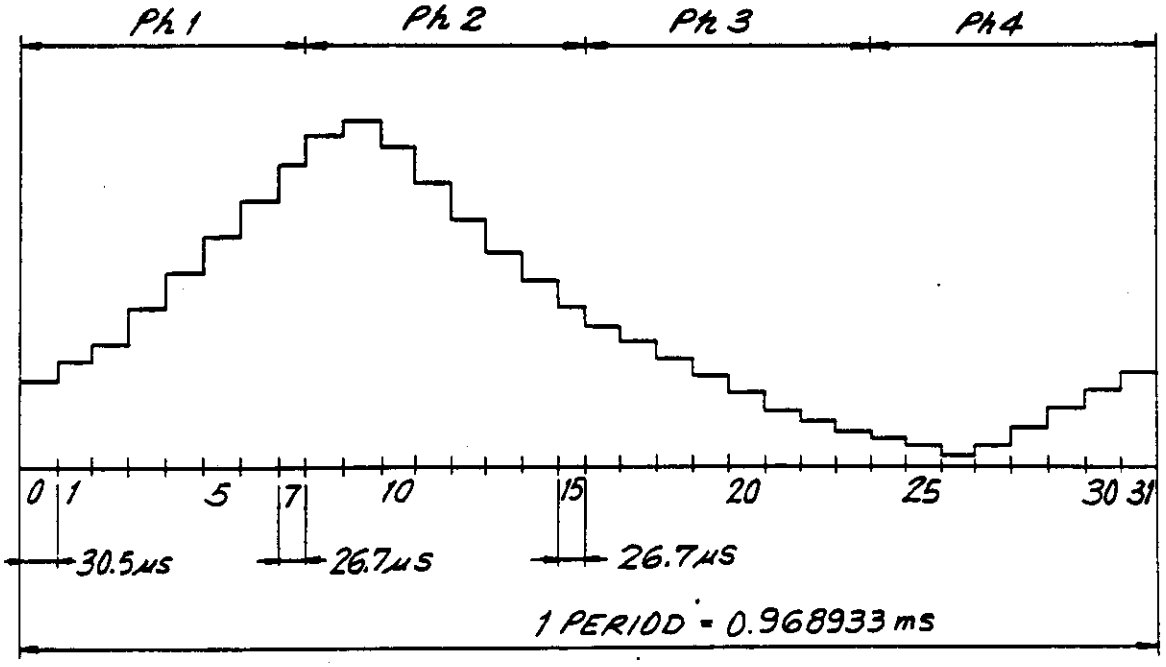

Ph 1
Ph 2
Ph 3
Ph 4
0 1 5 10 15 20 25 30 31
30.5µs
1 PERIOD = 0.976563 ms

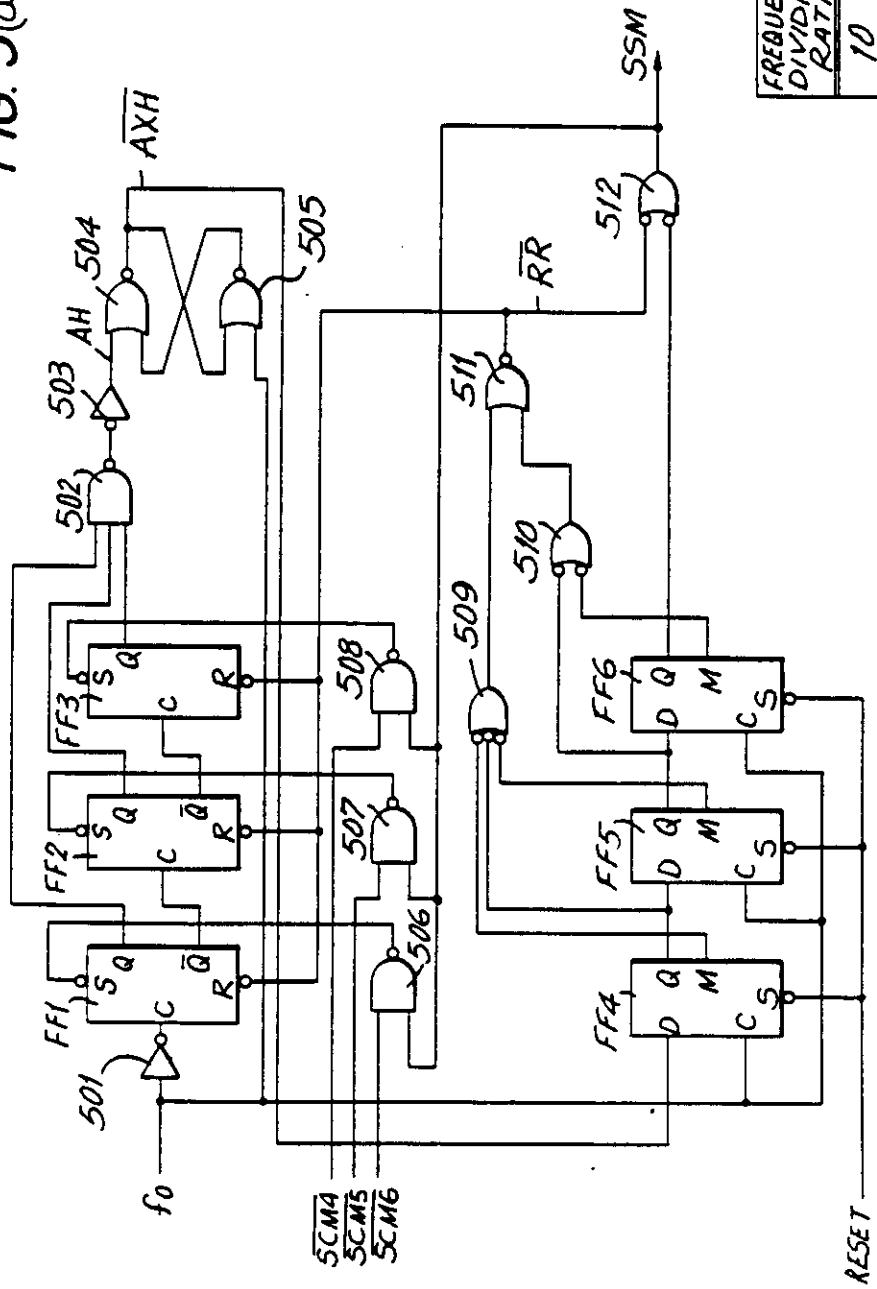
FIG. 3

FIG. 4


Ph 1
Ph 2
Ph 3
Ph 4
0 1 5 7 10 15 20 25 30 31
30.5µs
26.7µs
26.7µs
1 PERIOD = 0.968933 ms

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FIG. 5(a)



FREQUENCY DIVIDING RATIO	SCM4	SCM5	SCM6
10	1	1	1
9	0	1	1
8	1	0	1
7	0	0	1
6	1	1	0
5	0	1	0
4	1	0	0
3	0	0	0

FIG. 5 (b)

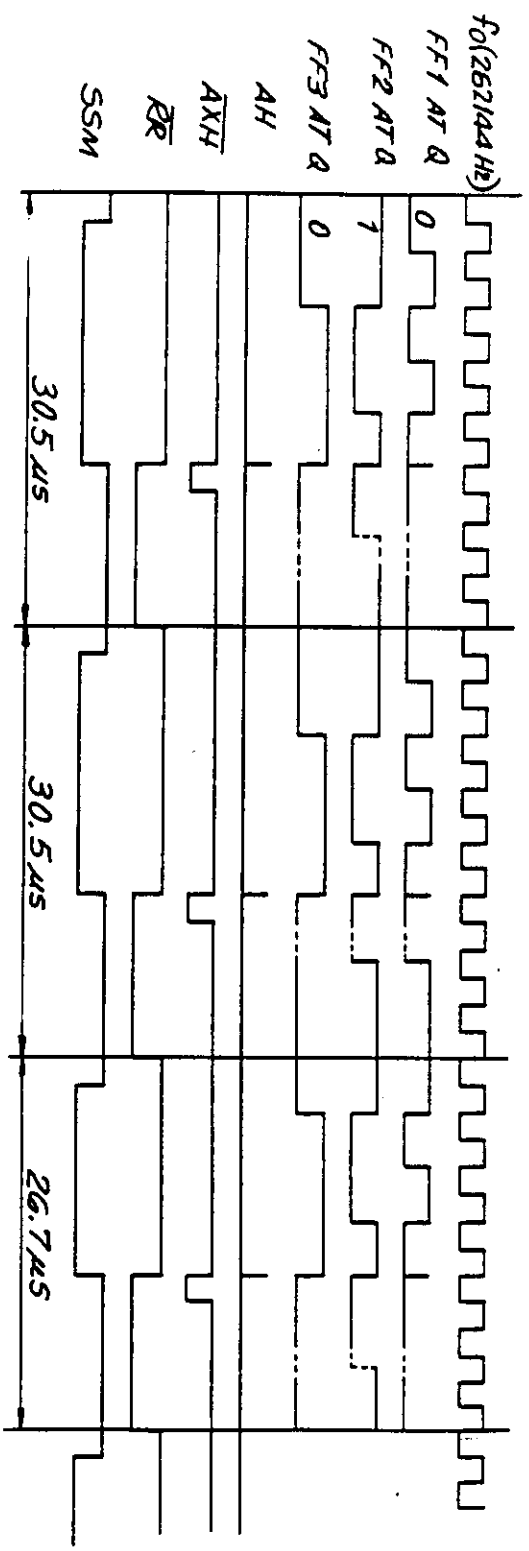

fo(262144 Hz)
FF1 AT Q
FF2 AT Q
FF3 AT Q
AH
AXH
ŘR
SSM
0
1
0
30.5 µs
30.5 µs
26.7 µs

FIG. 5(c)

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FIG. 6 (a)

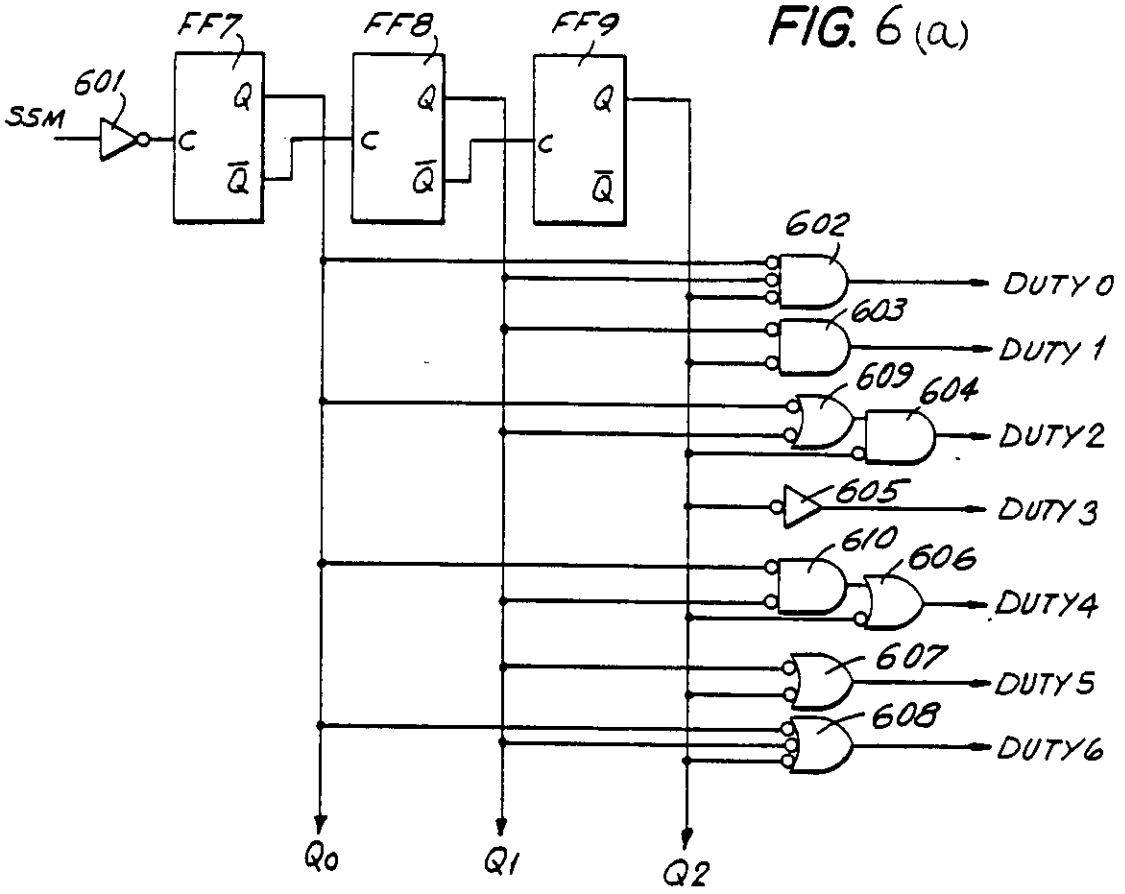
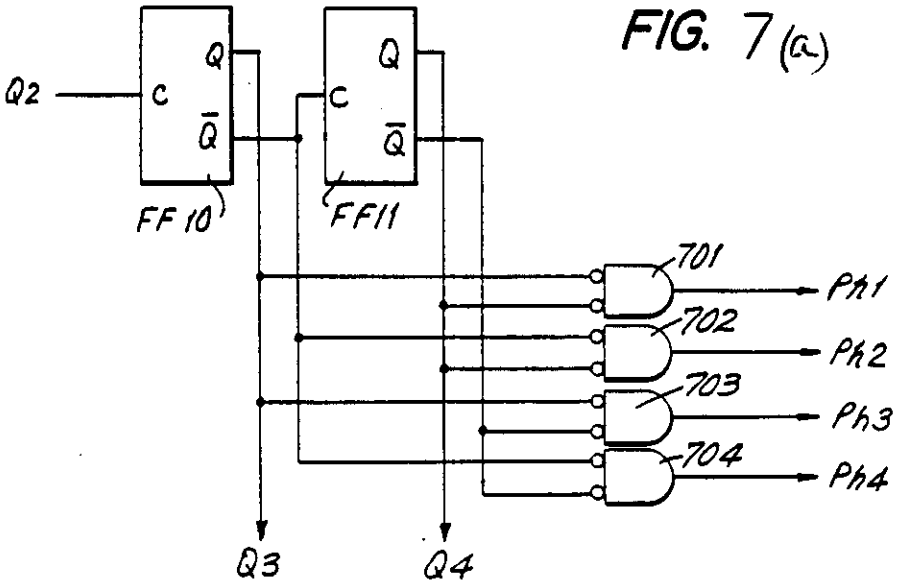


FIG. 7 (a)



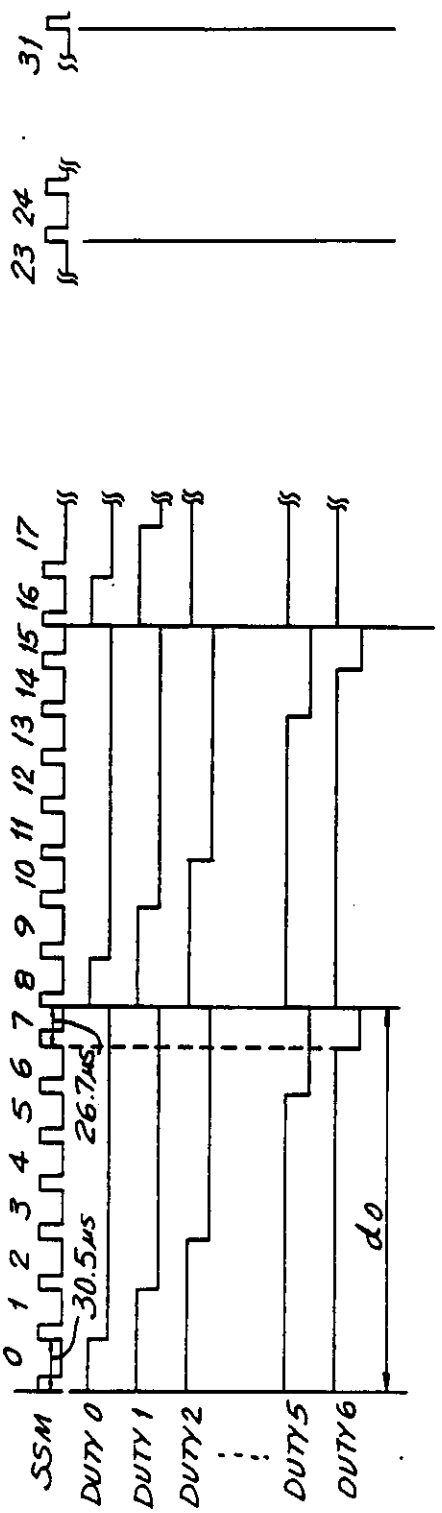

SSM
DUTY 0
DUTY 1
DUTY 2
DUTY 5
DUTY 6
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
30.5μs
26.7μs
d0
23 24
31

FIG. 6(b)

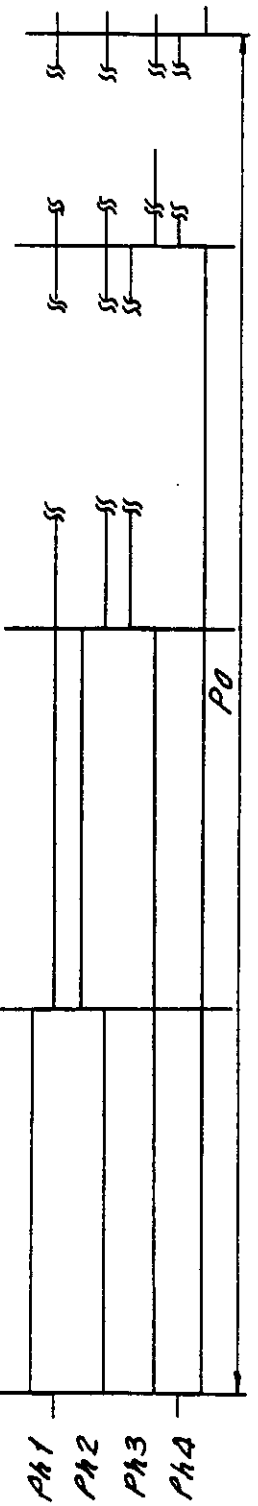
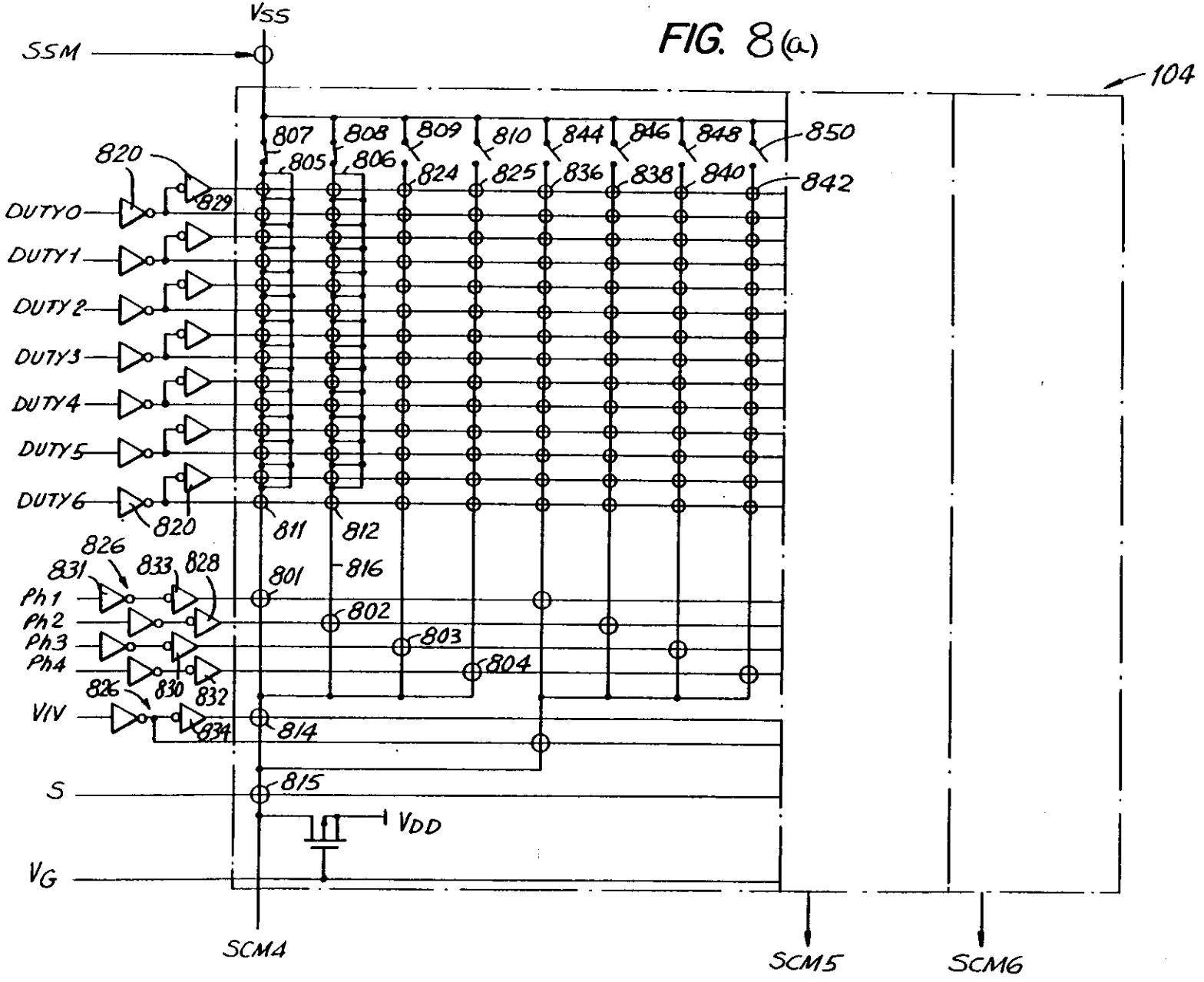

PH1
PH2
PH3
PH4
P0

FIG. 7(b)

FIG. 8(a)



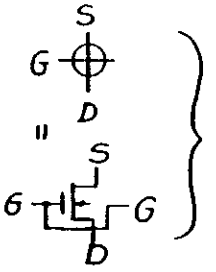


FIG. 8(b)

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METHOD AND APPARATUS FOR GENERATING SOUND WAVEFORM SIGNALS

The present invention relates to a method and apparatus for generating sound waveform signals for providing various types of sound from a sound synthesizer.

Conventionally, sound waveform signals have been generated by using a circuit, such as the one shown in Figure 2, wherein sound waveform data is read from a storage circuit 204 and is subjected to digital/analog conversion (D/A conversion) in a D/A converter 205 for supply to an electrical/acoustic converter (not shown), which produces musical tones.

More particularly, the circuit shown in Figure 2 comprises a scale ROM 203, in which an address is selected by a data signal S whose content varies according to the pitch of a musical tone and whose content is changed at intervals determined by the length of the tone. Data on a frequency dividing ratio stored in the selected address is supplied to a program counter 201, which is adapted to effect variable frequency division of a clock signal, having a predetermined frequency f_0, in accordance with such data. Thus, an N fold output having a frequency and a period (the period being 1/frequency) corresponding to the pitch of the sound is obtained from the program counter 201 for a length of time corresponding to the length of the sound in response to the data signal S.

The waveform ROM 204 stores data on sound waveforms for various different tones, such as the tone of a violin, the tone of a guitar, etc., this data having been programmed in the ROM in advance in accor-

dance with the user's usage and preferance. Addresses in the waveform ROM 204 are selected by a counter 202, which counts according to a numerical notation system based on the number N. Therefore, the counter 202 counts on the basis of an N fold clock cycle and for every number N of clock pulses input to the counter, an output representing one waveform is provided to the D/A converter 205. The period for reading the data for one waveform corresponds to the pitch of the sound, and the data for this one waveform is read repeatedly, thereby making it possible to obtain a frequency corresponding to the pitch of the sound.

Thus, conventionally, an original frequency is divided in dependence upon the data signal S for designating a musical note, and an analog sound signal is produced repeatedly at a frequency determined by the desired sound.

As described above, the waveform data is stored in the ROM 204, and the data is repeatedly read out at a predetermined frequency for D/A conversion. Now, the musical tone produced can be changed in terms of the quality of the sound by varying the number of divisions of the waveform made in the direction of its time axis and its amplitude for generating the data stored in the ROM 204, i.e. by varying the resolution. In order to increase the resolution in the direction of the time axis, it is necessary in the conventional arrangement to increase the original frequency by a corresponding margin, i.e. to increase the frequency f_0 of the clock signal input to the program counter 201. For example, if the period for reading the data for one waveform of the sound is divided into 32 equal timing intervals in the direction of the time axis so as to obtain an output of 1,024 Hz, then the minimum value required for the

original frequency f_0 becomes 32,768 Hz. Furthermore, if vibratos of $\pm$ 1% are added to the frequency of 1,024 Hz, a program counter having a resolution of 10 Hz also becomes necessary, and the original frequency f_0 must then satisfy the following formula:

$$\frac{f_0}{32 \times (n-1)} - \frac{f_0}{32 \times n} \leq 10 \text{ (Hz)}$$

where f_0 is the original frequency and n is a maximum dividing capacity of the program counter. If this formula is calculated we have f_0 approximately equal to 5.2 MHz when $n = 128$.

Thus, it has hitherto been necessary to set the original frequency to a large level and to store in the scale ROM 203 data on a frequency dividing ratio for dividing such a high frequency to a frequency in which 1,024 Hz is shifted by $\pm$ 1% to enable the program counter 201 to effect fine frequency division to 1,024 Hz $\pm$ 1%.

However, if a high original frequency such as 5.2 MHz is used, it becomes difficult to incorporate or attach a stable CR oscillator or the like in or outside an integrated circuit containing the circuitry shown in Figure 2. In addition, since it is necessary to increase the frequency dividing capacity of the program counter, another drawback arises in that the circuit configuration of the program counter itself becomes large. Furthermore, since the oscillation frequency is high, the power consumption by the oscillator and the program counter increases.

It is an object of the present invention, at least in its preferred form, to provide an arrangement for

generating sound waveform signals, which is capable of using an oscillator having a low frequency for obtaining a vibrato frequency requiring a high resolution.

According to one aspect of the present invention to which, there is provided a method of generating sound waveform signals in which waveform data is stored in storage means and is repeatedly read from said storage means at a frequency corresponding to the pitch of the sound, said method comprising the steps of dividing a predetermined period for reading said waveform data by a given number for generating a corresponding number of timing intervals of a predetermined length, and changing the length of an arbitrarily selected one or plurality of the timing intervals to make fine adjustment of said predetermined reading period and thereby to make fine adjustment of said frequency.

According to another aspect of the present invention, there is provided apparatus for generating sound waveform signals, comprising first storage means for storing waveform data, and means for repeatedly reading the waveform data from the first storage means at a frequency corresponding to the pitch of a sound, the reading means comprising second storage means for storing data representing a frequency dividing ratio, variable frequency dividing means for receiving a clock signal having a predetermined frequency and for dividing the predetermined frequency in accordance with the data in the second storage means for generating pulses to increment the addresses in the first storage means, and

control means arranged to co-operate with the second storage means so as to change the frequency dividing ratio of the variable frequency dividing means during an arbitrary section of the period for reading the waveform data.

In the preferred embodiment, the control means of the apparatus comprises a program counter, which is capable of providing a vibrato frequency even with a small circuit configuration.

The invention will be described further, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of apparatus in accordance with the present invention;

Figure 2 is a block diagram of a conventional arrangement;

Figure 3 is a diagram illustrating one example of a sound waveform signal generated in the conventional arrangement;

Figure 4 is a diagram illustrating an example of a sound waveform signal generated in accordance with the present invention;

Figure 5 (a) is a circuit diagram illustrating an example of the program counter shown in Figure 1;

Figure 5 (b) is a chart illustrating a frequency dividing ratio of the program counter with respect to input data;

Figure 5 (c) is a timing chart for signals generated in the program counter;

Figure 6 (a) is a circuit diagram illustrating an example of the duty generating circuit shown in Figure 1;

Figure 6 (b) is a timing chart for signals generated in the duty generating circuit;

Figure 7 (a) is a circuit diagram illustrating an example of the phase generating circuit shown in Figure 1;

Figure 7 (b) is a timing chart for signals generated in the phase generating circuit; and

Figure 8 is a diagram illustrating an example of the scale ROM shown in Figure 1.

Referring now to Figure 1, waveform data is stored in a waveform ROM 105. The ROM 105 is generally accessed at a predetermined frequency f_A in response to an output from a program counter 101, which receives as input clock pulses having a predetermined frequency f_0 and which divides the frequency f_0 according to an output from a scale ROM 104 for producing pulses having the frequency f_A. In the present invention, however, the output from the scale ROM 104 may be changed in a k-th timing interval, corresponding to the duration of the k-th pulse, during the access of one period of the waveform from the ROM 105, thereby changing the frequency dividing ratio of the program counter 101 instantly. In consequence, the frequency f_A of the pulses from the scale ROM 104 is instantly changed for the duration of a single pulse. If the waveform ROM 105 is accessed on the basis of this pulse, and the resulting output is subjected to D/A conversion by a D/A converter 106, the sound waveform signal produced will momentarily have a different frequency. This can better be understood by a comparison of Figures 3 and 4.

Figure 3 shows an output from the D/A converter 205 in the conventional arrangement shown in Figure 2 when the scale ROM 203 is accessed purely on the basis of the data signal S. In this example, it is assumed that f_A = 1,024 Hz and a period T (namely $1/f_A$) is equal to 0.976563 milli-seconds (mS). Figure 4 shows an

output from the D/A converter 106, in accordance with the present invention, wherein a seventh and a fifteenth timing interval of the waveform period are made shorter by $1/f_0$. In this example, the frequency of the musical tone obtained in the case of the Figure 3 arrangement is 1/0.976563 milli-seconds which is approximately 1,024 Hz. The frequency of the musical tone obtained in the case of the Figure 4 arrangement is 1/0.968933 milli-seconds which is approximately equal to 1,032 Hz. The difference between the two frequencies is 8 Hz, corresponding to approximately 0.8% of 1,024 Hz. In this instance, the frequency in accordance with the present invention is increased by +0.8%, but if the seventh and the fifteenth timing intervals are instead elongated by $1/f_0$, the frequency of the musical tone is reduced to 1,016 Hz. By changing the frequency of the waveform signal to 1,032 Hz and 1,016 Hz at a frequency of several Hz to 10 Hz, the musical tone obtained sounds as if vibratos are applied to the basic tone having the frequency of 1,024 Hz.

Figures 5 (a) to 5 (c), Figures 6 (a) and 6 (b), Figures 7 (a) and 7 (b), and Figures 8 (a) and 8 (b) illustrate examples of the circuitry within the respective blocks shown in Figure 1.

Figure 5 (a) shows an example of the program counter 101 shown in Figure 1, wherein the frequency f_0 is set at 262,144 Hz. Signals $\overline{SCM4}$ to $\overline{SCM6}$ are received from the scale ROM 104, which is shown in detail in Figure 8 and which, in Figure 8, is shown as generating output signals SCM4 to SCM6 of opposite phase to the signals $\overline{SCM4}$ to $\overline{SCM6}$. The frequency dividing ratio of the program counter 101 is determined in dependence upon the signals SCM4 to SCM6 in compliance with the table shown in Figure 5 (b), and changes at a

certain timing so as to effect fine adjustment of the output frequency of the counter 101 in accordance with an important feature of the present invention.

Figure 5 (c) shows the timing of the various signals produced during operation of the program counter 101. First, a case is considered where ($\overline{SCM4}$, $\overline{SCM5}$, $\overline{SCM6}$) = (1, 0, 1), i.e. ($\overline{SCM4}$, $\overline{SCM5}$, $\overline{SCM6}$) = (0, 1, 0). Flip-flops (hereinafter referred to generally as FF) FF1 to FF3 constitute an up counter, and the signals at their respective Q terminals change sequentially from (0, 1, 0) to (1, 1, 0), (0, 0, 1), (1, 0, 1), (0, 1, 1) and (1, 1, 1). However, instantaneously as the Q terminals become (1, 1, 1), a signal AH provided at an output of an invertor 503 coupled to the Q terminals by way of a NAND gate 502 becomes a spike, and a signal $\overline{A\ X\ H}$ at the output of a latch constituting NOR gates 504 and 505 forms a pulse.

Subsequently, this signal $\overline{A\ X\ H}$ is delayed by the flip-flops FF4 to FF6, NAND gates 509, 510 and NOR gate 511 to cause a signal $\overline{RR}$ to become low for a time corresponding to three clock pulses of the frequency f_o. The signal $\overline{RR}$ is applied to a NOR gate 512 together with the signal at the Q terminal of the flip-flop FF6, and a signal SSM, which remains high for a duration corresponding to 3.5 clock pulses of the frequency f_o, is produced at the output of the NOR gate 512. When the signal SSM is high, a MOS transistor of the scale ROM 104 connected to a power source V_{ss} as shown in Figure 8 is turned ON. The MOS transistor is therefore operated intermittently so that a current flows intermittently to the scale ROM 104, which reduces the power consumption to a low level. It goes without saying that the ROM 104 may be operated constantly, and in that case the flip-flops FF4 to FF6 are not required. In addition, when

the signal $\overline{RR}$ is low, this re-sets the flip-flops FF1 to FF3. When the signal $\overline{RR}$ changes again to high, counting is carried out once more.

Accordingly, during an initial timing interval shown in Figure 5 (c), the counting cycle of the flip-flops FF1 to FF3 corresponds to eight clock pulses of the frequency f_0. The period of the signal $\overline{RR}$ corresponds also to eight clock pulses of the frequency f_0 and is 30.5 micro-seconds (μs), and the period of the signal SSM, which is synchronised with the signal $\overline{RR}$, is also 30.5 micro-seconds. In the next timing interval, the counting cycle again corresponds to eight clock pulses. However, the third timing interval is based on seven clock pulses of the frequency f_0 which means that the period of the signal SSM is 26.7 micro-seconds. The third timing interval shown in Figure 5 (c) corresponds to the seventh or fifteenth timing interval along the abscissa in Figure 4.

When it is desired to change the frequency dividing ratio in the program counter 101, the output signals SCM4 to SCM6 from the scale ROM 104 are varied to change the initial values of the up counter provided by the flip-flops FF1 to FF3, which changes the frequency dividing ratio. In the case of the third timing interval shown in Figure 5 (c), since (SCM4, SCM5, SCM6) = (0, 0, 1), the Q terminals of the flip-flops FF1 to FF3 are set to (1, 1, 0). Since counting is then started from this state, rather than from (0, 1, 0), the frequency dividing ratio changes. The timing for the change is controlled by the duty generating circuit 102 and the phase-generating circuit 103.

The duty generating circuit 102 is adapted to generate a duty ratio based on multiples of eight clock

pulses of the frequency f_o for controlling the data from the scale ROM 104. As shown in Figure 6 (a), the duty generating circuit 102 comprises flip-flops FF7 to FF9 and logic gates 602 to 608 arranged so as to form seven timing signals, Duty 0 to Duty 6. The signal SSM, i.e. the output of the aforementioned program counter 101, is passed through the flip-flops FF7 to FF9 so as to be subjected to binary frequency division, and the outputs therefrom are de-coded by the logic gates 602 to 608 to generate the timing signals Duty 0 to Duty 6. As shown in Figure 6 (b), when the time period d0 is assumed to be one period, the signal Duty 0 has a duty ratio of 1/8, the signal Duty 1 has a duty ratio of 2/8, ..., and the signal Duty 6 has a duty ratio of 7/8.

For instance, in the example shown in Figure 4, the sound waveform signal is obtained by basing the counting cycle of the counter 101 on eight clock pulses of the frequency f_o during the noughth to the sixth timing intervals, and by basing this counting cycle on seven clock pulses in the seventh timing interval. When the seventh timing interval arrives, the signal Duty 6 becomes low and the signals SCM4 to SCM6 are changed over to alter the counting cycle.

Referring now to Figure 7 (a) and 7 (b), a description will be given of the phase generating circuit 103. This phase generating circuit 103 is arranged such that the frequency of an output signal Q2 of the duty generating circuit 102 is divided by flip-flops FF10 and FF11 to generate pulse signals Ph1 to Ph4. If the time period P0 is assumed to be one period in this instance, the signals Ph1 to Ph4 have the same frequency and duty ratio, and only their phases are different. These signals are obtained by de-coding the

outputs of the flip-flops FF10 and FF11 by means of NOR gates 701 to 704. The signals Ph1 to Ph4 correspond with the sections Ph1 to Ph4 shown in Figure 3 of the period of the waveform signal, and the time duration of the pulse of each signal (when the signal is high) corresponds to one quarter of the period of the waveform for a certain musical note. The signals Ph1 to Ph4 are also used in the reading timing for the scale ROM 104.

Referring now to Figures 8 (a) and 8 (b), a description will be given of the scale ROM 104. In these Figures, the portions marked by circles represent n-channel MOS transistors for generating the output signals SCM4 to SCM6. The signals Duty 0 to Duty 6 are input to gates of a series of memory cell transistors 811 and 812. Normally, data is programmed in the scale ROM 104 by means of conductive wiring in such a manner that ON/OFF control of only one MOS transistor 811 by any of the signals Duty 0 to Duty 6 is possible with respect to any one line 813. Furthermore, the respective lines are selected or not selected by the phase signals Ph1 to Ph4, and further selection is then carried out with respect to a high frequency and a low frequency by a signal VIV having a vibrato frequency. In addition, selection is effected within the ROM 104 by the musical data signal S (also shown in Figure 1). The selected output is then delivered to the program counter 101.

An example will now be given of a case where a waveform signal for a musical note as shown in Figure 4 is to be created. As far as the scale ROM 104 is concerned, a detailed description is given of the generation of the signal SCM4 only, but both the signals SCM5 and SCM6 are provided in a similar manner. If it is assumed that no vibrato is required, then

VIV = H (High), and the right hand portion of the section of the ROM 104 for generating the signal SCM4 is not employed. First, data is programmed in the ROM 104 by rendering certain lines therein conductive by means of wires and switches 805 to 810. In this instance, the switches 807 and 808 are set to be ON and the switches 809 and 810 are set to be OFF. The data is programmed in advance by short circuiting the sources and drains of the MOS transistors 811, 812 by means of the wires 805, 806. The short circuited transistors become void. Thus, only the last of the signals 811 and 812 are effective with respect to the signal SCM4 and these receive the signal Duty 6 applied to the gates thereof. Accordingly, during the time duration when the signal Duty 6 is high, i.e. during the timing intervals 0 to 6, the transistor 811 is set to be OFF. Concurrently, a node 813 is being charged by a power source V_{DD} under the control of a signal V_G, and a high level output is obtained for the signal SCM4. This corresponds to a 1 given in the column for the signal SCM4 in the table of Figure 5 (b). Subsequently, in the eighth timing interval, the transistor 811 is turned ON as the signal Duty 6 becomes low, and the node 813 discharges so that the level of the signal SCM4 becomes low. Throughout this time, the signal Ph1 is high, and a transistor 801 which is responsive to this signal is set to be ON. Transistors 814 and 815 are also set to be ON by the signals VIV and S, thus enabling the signal SCM4 to become low. This corresponds to a 0 in the column for the signal SCM4 in the table of Figure 5 (b). When the signal Ph2 is high, i.e. during the timing intervals 8 to 15, the operation is similar to that obtaining during the high level of the signal Ph1. When the signals Ph3 and Ph4 are high,

i.e. during the timing intervals 16 to 31, the output level of the signal SCM4 does not become low, however, since the switches 809 and 810 are set to be OFF. When the switches 809 and 810 are OFF and the signals Ph3 and Ph4 are high, the output level of the signal SCM4 becomes unconditionally high and so the timing intervals in each cycle of eight such intervals are all of equal length.

When vibratos are to be applied to the musical tone, clock pulses having a vibrato frequency (e.g. 4 to 16 Hz) obtained by dividing the original frequency are supplied as the signal VIV. In the example of Figure 4 described up until now, the average frequency dividing ratio during the high level phase of the signal PH1 can be expressed as follows:

$$\text{Average frequency dividing ratio} = \frac{8 \times 7 + 7 \times 1}{8} = 7.875$$

Similarly, the average frequency dividing ratio in the high level phase of the signal Ph2 is equal to 7.875, but the average frequency dividing ratio during the high level phases of the signals Ph3 and Ph4 is equal to 8, so that the overall average frequency dividing ratio in one waveform period can be expressed as follows:

$$\text{Overall average frequency dividing ratio} = \frac{7.875 \times 2 + 8 \times 2}{4} = 7.9375$$

If it is assumed that the original frequency f_0 is 262,144 kHz, then the average frequency can be expressed as

$$\text{Average frequency} = \frac{262144}{7.9375 \times 32} = 1032.06 \text{ Hz}$$

This corresponds to the situation in which +8 Hz is added to a basic frequency of 1,024 Hz, so that a resolution of approximately 0.8% is obtained. Accordingly, it becomes possible to apply vibratos of $\pm$0.8% with respect to one tone by outputting a frequency of 1,032 Hz while the signal VIV is at a high level and a frequency of 1,016 Hz while the signal VIV is at a low level. In other words, if the basic frequency of a single tone is 1,024 Hz, then this can be changed to 1,016 Hz and 1,032 Hz for very short durations in accordance with the present invention, so that a vibratory sound can be produced and the tone, which is heard, assumes a state in which vibratos are applied thereto.

It should be noted that in the scale ROM 104 shown in Figure 8, only a configuration for generating vibratos for one tone is shown. If a plurality of tones, e.g. eight tones, are required as in the case of a musical tone generator, three bit signals S are required and eight configurations are required for the signals SSM4, SSM5 and SSM6 respectively.

In addition, the flip-flops FF7 to FF11 shown in Figures 6 (a) and 7 (a) correspond to the counter 202 in the conventional example shown in Figure 2. Accordingly, addresses in the waveform ROM 105 are accessed by means of the signals Q0 to Q2 in Figure 6 (a) and the signals Q3 and Q4 in Figure 7. The signals Q0 to Q4 are de-coded by a de-coder incorporated in the waveform ROM

105 to select an address, and a five bit data signal is output. The capacity of the ROM 105 is 25 x 5 = 160 bits.

As described above, in accordance with the present invention, it becomes possible to effect frequency division having a resolution of 1 or below by changing the frequency dividing ratio of the program counter 101 in a series of timing intervals. Although the period of the waveform signal is instantly altered by a very small amount (of the order of micro-seconds) the sound generated is not heard by human ears as being a disturbance of the basic tone. In addition, although in the above described embodiment a description has been given of a musical note generating apparatus, it goes without saying that the present invention can be applied to speech and various alarm generating apparatus as well.

Although conventionally a clock signal of 5.2 MHz of there-abouts has hitherto been necessary, by virtue of the present invention it is possible to employ a low frequency clock signal of 262 kHz. Thus, whereas a signal of 5.2 MHz requires a crystal oscillator for its production, a signal of 262 kHz can be realised using a CR oscillator. This permits a substantial reduction in cost. In addition, if a calculation is made on the basis of a simple frequency ratio, power consumption to which an oscillation frequency contributes is 1/20, producing a significant advantage in a musical note generating apparatus which is powered by a battery cell.

Furthermore, a small programmable counter can be used since a pseudo-shifted frequency can be obtained simply by changing data on the frequency dividing ratio and a programmable counter having a large circuit configuration, which is capable of dividing a frequency

to finely shifted frequencies, is not needed.

Moreover, although, when a radio frequency is being processed, it is difficult to obtain an output with good characteristics from a programmable counter, in this invention improved output characteristics are obtained since a low frequency suffices.

C L A I M S

1. A method of generating sound waveform signals in which waveform data is stored in storage means and is repeatedly read from said storage means at a frequency corresponding to the pitch of the sound, said method comprising the steps of dividing a predetermined period for reading said waveform data by a given number for generating a corresponding number of timing intervals of a predetermined length, and changing the length of an arbitrarily selected one or plurality of the timing intervals to make fine adjustment of said predetermined reading period and thereby to make fine adjustment of said frequency.

2. A method according to claim 1, wherein the step of changing the length comprises changing the length of the or each arbitrarily selected timing interval to longer or shorter than the predetermined length so as to create an adjusted frequency which is closely adjacent said frequency, and wherein said waveform data is read occasionally at said adjusted frequency by repeating the change in the length of the timing intervals there-by to add vibratos to the sound.

3. A method according to claim 2, wherein said predetermined period corresponds to the period of a note of music, and said two frequencies are formed with respect to one note.

4. Apparatus for generating sound waveform signals, comprising first storage means for storing waveform data, and means for repeatedly reading the waveform data from the first storage means, the reading means comprising second storage means for storing data representing a frequency dividing ratio, variable frequency dividing means for receiving a clock signal

having a predetermined frequency and for dividing the predetermined frequency in accordance with the data in the second storage means for generating pulses to increment the addresses in the first storage means, and control means arranged to co-operate with the second storage means so as to change the frequency dividing ratio of the variable frequency dividing means during an arbitrary section of the period for reading the waveform data.

5. Apparatus according to claim 4, wherein the control means comprises a first circuit responsive to the pulses output by the variable frequency dividing means for generating a plurality of first signals having mutually different duty ratios, and a second circuit responsive to the pulses output by the variable frequency dividing means for generating a plurality of second signals, and wherein the second storage means is responsive to a combination of the first and second signals and stored data for changing the frequency dividing ratio of the variable frequency dividing means.

6. Apparatus according to claim 5, wherein said second storage means comprises a ROM having a plurality of memory cell MOS transistors connected in series and arranged such that gate electrodes thereof receive respectively the first signals and the first signals inverted, the memory cell MOS transistors being pre-programmed to set the conductive states thereof for providing the storage data, and the ROM having a further plurality of MOS transistors arranged to be controlled by the second signals for outputting the storage data.

7. Apparatus according to claim 5 or 6, wherein each of the second signals represents a respective section of the period for reading the waveform data, and wherein

the first signals comprise pulses having different durations generated in the course of each such section.

8. Apparatus according to any of claims 4 to 7, wherein the control means comprise counting means functioning as an address counter for the second storage means.

9. Apparatus according to any of claims 4 to 8, wherein the control means are arranged to co-operate with the second storage means so as to change the frequency dividing ratio of the variable frequency dividing means occasionally to a greater and a lesser value whereby to add vibratos to the sound.

10. Apparatus according to claim 4 wherein the control means includes a first circuit comprising a first counting means for counting the pulses from the variable frequency dividing means and further comprising a first de-coding means for de-coding a counting content so as to generate a plurality of first signals.

11. Apparatus according to claim 10, wherein the control means includes a second circuit comprising a second counting means for counting output from the first counting means and further comprising a second de-coding means for de-coding a counting content so as to generate a plurality of second signals.

12. Apparatus according to claim 11, wherein the first and second counting means function as an address counter for the second storage means.

13. Apparatus according to claim 11, wherein the first signals have mutually different duty ratios, the second signals comprise pulses, each representing a respective

section of the period for reading the waveform data, and wherein the second storage means is responsive to a combination of the first and second signals for changing the frequency dividing ratio of the variable frequency dividing means.

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