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(54) Title: MATERIAL AND METHOD FOR ROUGHNESS REDUCTION OF SUBSTRATES

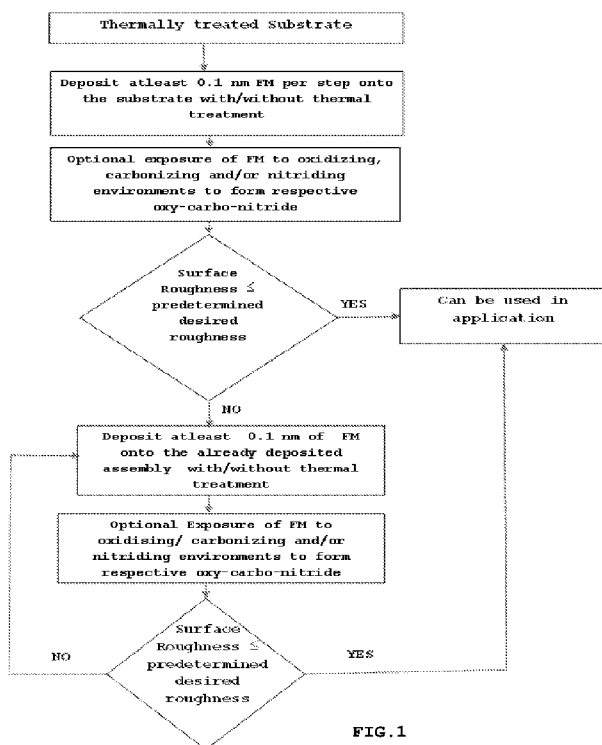


FIG. 1

(57) Abstract: The present invention relates to a requirement of substrates with a smooth surface. It also relates to the method which reduces the surface roughness of a substrate (metal carbide, nitride, oxide, carbonitride, oxycarbide, oxynitride, oxy carbonitride, semiconductor (silicon), metal or an inorganic crystal metal). The method consists of depositing a filler material (FM) and further subjecting the layer to thermal treatment with or without optional exposure to oxidizing, carbonizing and/or nitriding environments. The filler material is selected from metals such as Zinc (Zn), Magnesium (Mg), Aluminium (Al), Titanium (Ti), Manganese (Mn), Chromium (Cr), Germanium (Ge), Niobium (Nb), Tantalum (Ta), Hafnium (Hf), Zirconium (Zr), Vanadium (V), Calcium (Ca), Gallium (Ga), Indium (In), and Tin (Sn) or a combination thereof.

LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE,
SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, KM, ML, MR, NE, SN, TD, TG).

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- *as to the identity of the inventor (Rule 4.17(i))*
- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *of inventorship (Rule 4.17(iv))*

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**Material and method for roughness reduction of
substrates**

FIELD OF THE INVENTION

[0001] The present invention relates to top surface roughness reduction of substrates by deposition process. The present disclosure also relates to the material and method of its deposition which reduces the surface roughness of a substrate.

BACKGROUND ART

[0002] Day by day the device size in the semiconductor industry keeps reducing, once the critical dimensions are reached, the surface smoothness of intricately patterned material layers on substrate surfaces play a crucial role in deciding the performance of the active layer of the devices like advanced integrated circuits (ICs). The rapid progress in solid state electronic devices would not have been possible without the development of new thin film deposition processes, improved film characteristics and superior film qualities. In order to design and manufacture a high performance integrated circuit cost effectively, the parameters of the manufacturing process need to be carefully controlled: surface roughness along with other parameters must

fall within tight limits, for devices to be free of defects.

[0003] In case of high-k dielectrics used in MOSFETs, high surface roughness of the films can promote device degradation. The smoothness of the interfaces between the high-k dielectric material and the gate (which can be polysilicon or a metal gate), high-k dielectric material and the channel material will determine the performance and reliability of the final transistors. Transparent materials for optical applications are smoothened by taking a very flat abrasive surface and rubbing the material against it until it reaches the required smoothness. The surface finish requirement for optics is two orders higher than that can be achieved by conventional machining.

[0004] In the Micro-Electro-Mechanical Systems (MEMS) and micro-electronic fields, there is frequently a need for bonding wafers together for the purpose of encapsulating structures in vacuum cavities or in cavities with controlled atmosphere. Surface roughness is a limiting factor in fusion bonding. For example, the surface roughness requirement for silicon fusion bonding is significantly less than 1 nm.

[0005] Conventional methods include, polishing techniques such as grinding, honing, lapping, super finishing, chemical etching, electrolytic polishing, chemical mechanical polishing, laser ablation, electroplating, anodizing, and plasma treatment. Such techniques would reduce the roughness of the substrate to a minimum of a few nanometers.

[0006] Depositing material on the substrate instead of removal to reduce substrate roughness in the art. One such prior art is also known US9425046 discloses a method of processing silicon germanium (SiGe) thin films to reduce surface roughness on substrates. The prior focuses on methods of roughness reduction by Si art Ge deposition followed by chemical mechanical planarization technique to achieve final desired roughness. The deposition technique used is chemical vapor deposition. This process is cumbersome and limited to single material and deposition technique.

[0007] Thus, in all the above-mentioned cases, there is a need for improved surface roughness and the methods thereof that can be used to produce high quality devices and structures. The reduction methods disclosed herein reach the required level of

smoothness of the rapidly growing semiconductor industry.

OBJECTS OF THE INVENTION

[0008] It is an object of the invention to disclose simple and effective methods for reducing the surface roughness of substrates.

[0009] It is yet another object of the invention to disclose methods that are easy to perform on large industrial scale.

SUMMARY OF THE INVENTION

[0010] To meet the objects of the invention and overcome the problems associated with the prior art, it is disclosed here a method for reducing the roughness of a free surface of a substrate by depositing a Filler Material (FM) on the substrate by sputtering or using other PVD and CVD techniques; thermal treating the deposit to a temperature of 0.5 times the melting point of FM; and repeating the above steps until a roughness of the free surface of the substrate and deposit is equal to or smaller than a predetermined value. The assembly may also be exposed to oxy-carbo-nitride environment and subjected to further thermal treatment of the entire assembly.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0011]** The drawings described herein are for illustrative purposes only of selected embodiments and not all possible implementations and are not intended to limit the scope of present disclosure.
- [0012]** Figure 1 is a Process flowchart for roughness reduction of substrates.
- [0013]** Figure 2 shows (a) typical surface with roughness of less than 2nm (b) Deposition of FM (c) After thermal treatment (d) Partial formation of FM oxy-carbo-nitride due to exposure to oxy-carbo-nitride environment or under operating conditions (e) Partial formation of FM oxy-carbo-nitride due to exposure to oxy-carbo-nitride environment or under operating conditions.
- [0014]** Figure 3 shows (a) Typical surface with primary roughness of less than 10 nm and secondary roughness of less than 2nm (b) Deposition of FM (c) After thermal treatment (d) after exposure to oxy-carbo-nitride environment (e) Deposition of FM on the assembly (f) After thermal treatment of assembly (g) after exposure to oxy-carbo-nitride environment (h) Deposition of FM (i) After thermal treatment (j) after exposure to oxy-carbo-nitride environment (k) Deposition of FM on the assembly (l) After

thermal treatment of assembly (m) after exposure to oxy-carbo-nitride environment.

[0015] Figure 4 are AFM 3D tapping mode images with scan size of $1\mu\text{m} \times 1\mu\text{m}$ of a) Bare si wafer b) Zn 1nm deposited and annealed at 100°C C) Zn 2nm deposited at 100°C .

[0016] Figure 5 are AFM 3D tapping mode images with scan size of $1\mu\text{m} \times 1\mu\text{m}$ of a) Bare glass b) Zn 1nm deposited and annealed at 100°C C) Zn 2nm deposited at 100°C .

[0017] Figure 6 are AFM 3D tapping mode images with scan size of $1\mu\text{m} \times 1\mu\text{m}$ of a) Bare si wafer b) Zn 1nm deposited and annealed at 300°C C) Zn 2nm deposited at 300°C .

[0018] Figure 7 are AFM 3D tapping mode images with scan size of $1\mu\text{m} \times 1\mu\text{m}$ of a) Bare glass b) Zn 1nm deposited and annealed at 300°C C) Zn 2nm deposited at 300°C .

DETAILED DESCRIPTION OF THE INVENTION

[0019] The present disclosure aims to provide substrates with a smooth surface. More specifically, the present disclosure relates to the materials and steps for depositing the material which reduces the surface roughness of a substrate. The substrate could be metal carbide, nitride, oxide, carbonitride, oxycarbide, oxynitride, oxy carbonitride, semiconductor (silicon), metal or an inorganic crystal metal. In some cases, the substrate might appear metallic

in bulk form but have a thin layer (which can be native or intentionally grown) of metal carbide, nitride, oxide, carbonitride, oxycarbide, oxynitride, oxycarbonitride layer on top of the said metallic substrate. For this purpose, the invention discloses methods to deposit a filler material (FM). FM would partially or fully fill the void associated with the roughness of the substrate. The filler material is selected from Zinc (Zn), Magnesium (Mg), Aluminium (Al), Titanium (Ti), Manganese (Mn), Chromium (Cr), Germanium (Ge), Niobium (Nb), Tantalum (Ta), Hafnium (Hf), Zirconium (Zr), Vanadium (V), Calcium (Ca), Gallium (Ga), Indium (In), Tin (Sn) or combinations thereof. Optimal deposition rate of FM is needed for desired roughness. Deposition of FM can be done in a single step or multiple steps based on the roughness of the substrate. In each step, at least 0.1nm of FM is deposited onto the substrate with or without thermal treatment. Exposure to suitable oxidizing, carbonizing and/or nitriding environments of the FM after each cycle of FM deposition can increase the relative transparency of the assembly. The filler material or its compounds assist in reducing the roughness of the substrate by filling up the nano corrugations (nano crevices) in the substrate, by forming an

atomically chemically graded interface with substrate.

[0020] The deposition of filler material in the exemplary embodiment presented here is performed by using sputtering. But it could be deposited using other PVD and CVD techniques where the deposition rate is in the order of a few nanometers per minute. For example, Ebeam evaporation, PLD, ALD, PEALD, and Thermal evaporation. The disclosed method can result in surface roughness of less than or equal to 0.1nm.

[0021] Figure 1 shows detailed process flow for reducing the surface roughness of substrate.

[0022] The first step is to deposit atleast 0.1nm FM onto the substrate with finite roughness with or without thermal treatment. Step two is optional, where the FM is exposed to oxidizing, carbonizing and/or nitriding environments to form their respective compounds. If the desired roughness is reached, it can be used in the application. If the desired roughness is still not reached, deposit another 0.1 nm of FM onto the already deposited substrate with or without thermal treatment. It is followed by optional exposure to oxidizing, carbonizing and/or nitriding environments to form their

respective compounds. This process is repeated until a roughness of the free surface of the substrate and deposit is equal to or smaller than a predetermined value; roughness as low as 0.1nm can be achieved.

[0023] Figures 2 and explain the different embodiments of the invention by using non-limiting exemplary methods. These examples are for the purpose of explaining the invention in detail and no means should be considered to limit the scope of the invention.

[0024] Figure 2 (a) shows a substrate with an inherent roughness of less than 2nm. The substrate has an uneven profile. (b) FM is deposited on the substrate. FM does not fill the roughness yet. (c) The assembly is thermally treated to a temperature $< 0.9 T_m$ of the FM. The amount of FM deposited should be just enough to fill the roughness of the substrate, in such case the FM fills up the nano crevices resulting in smooth surface finish. (d) Partial formation of FM oxy-carbo-nitride due to exposure to oxy-carbo-nitride environment or under operating conditions (e) Partial formation of FM oxy-carbo-nitride due to exposure to oxy-carbo-

nitride environment or under operating conditions.

[0025] Figure 3 shows an exemplary method of reducing surface roughness of a typical surface with primary roughness of less than 10 nm and secondary roughness of less than 2nm (b) Deposition of FM (c) After thermal treatment (d) after exposure to oxy-carbo-nitride environment (e) Deposition of FM on the assembly (f) After thermal treatment of assembly (g) after exposure to oxy-carbo-nitride environment (b) Deposition of FM (c) After thermal treatment (d) after exposure to oxy-carbo-nitride environment (e) Deposition of FM again on the assembly (f) After thermal treatment of assembly (g) after exposure to oxy-carbo-nitride environment (b) Deposition of FM (c) After thermal treatment (d) after exposure to oxy-carbo-nitride environment (e) Deposition of FM again on the assembly (f) After thermal treatment of assembly (g) after exposure to oxy-carbo-nitride environment. Here the figure shows a requirement of at least 4 steps, but it can be N number of steps.

[0026] In one embodiment referring to Figure 2, the substrates have roughness of less than approximately 2nm. Atleast 0.1 nm of FM is deposited on substrates with or without

thermal treatment. The assembly is thermally treated to a temperature $< 0.9 T_m$ of the FM. The amount of FM deposited should be just enough to fill the roughness of the substrate, in such case the FM fills up the nano crevices resulting in smooth surface finish. It should be noted that an excess amount of FM may not result in a smooth surface. The FM may also react with atmospheric oxy-carbo-nitride in the working atmosphere resulting in partial or complete formation of FM oxy-carbo-nitride.

[0027] In some embodiments, atleast 0.1 nm of FM is deposited on with or without thermally annealed substrates as shown in Figure 2. FM is deposited on a preheated substrate that has an inherent roughness of less than 2nm. The assembly is thermally treated to a temperature $< 0.9 T_m$ of the FM. The amount of FM deposited should be just enough to fill the roughness of the substrate, in such case the FM fills up the nano crevices resulting in smooth surface finish. It should be noted that an excess amount of FM may not result in a smooth surface. The FM substrate assembly is then thermally annealed at an oxy-carbo-nitride environment resulting in partial or complete formation of FM oxy-carbo-nitride.

[0028] In some embodiments as shown in Figure 2, at least 0.1 nm of FM is deposited on a preheated substrate that has an inherent primary roughness of approximately less than 10nm. The substrate also has a secondary roughness on the profile of the primary roughness. The assembly is thermally treated to a temperature $< 0.9 T_m$ of the FM. The FM substrate assembly is then thermally annealed in an oxy-carbo-nitride environment to form respective FM oxy-carbo-nitride. If the required surface roughness is not achieved. The steps of deposition, thermal treatment and exposure to oxy-carbo-nitride atmospheres are repeated until a roughness of the free surface of the substrate and deposit is equal to or smaller than a predetermined value. The number of steps depends on the initial roughness of the substrate and the thickness of FM deposited in each step.

[0029] The invention is further explained by means of the following examples and results.

EXAMPLE 1

[0030] Silicon wafers and glass substrates were preheated in a vacuum of around 5×10^{-6} mbar at 100°C for 15 minutes. Then zinc of nominal thickness 1 nm and 2 nm was deposited using a DC magnetron sputtering

system. The deposited substrates were annealed at 100°C for 1 hr under vacuum. From the AFM result as shown in Table 1 we can observe that zinc 1 nm gives low surface roughness of around $R_a = 0.0810$ nm and 0.105 nm for silicon wafer and glass respectively.

[0031] Figure 4 shows AFM 3D tapping mode images with scan size of $1\mu\text{m} \times 1\mu\text{m}$ of a) Bare si wafer b) Zn 1 nm deposited and annealed at 100°C C) Zn 2 nm deposited at 100°C. The Si wafer was preheated to 100°C for 15 minutes, Zinc 1 nm was deposited and then post annealed for 1hr at 100°C. Zinc 1 nm gives low roughness for silicon wafer at 100°C.

[0032] Figure 5 shows AFM 3D tapping mode images with scan size of $1\mu\text{m} \times 1\mu\text{m}$ of a) Bare glass b) Zn 1 nm deposited and annealed at 100°C C) Zn 2 nm deposited at 100°C. The glass substrates were preheated to 100°C for 15 minutes, Zinc 1 nm was deposited and then post annealed for 1hr at 100°C. Zinc 1 nm gives low roughness for glass at 100°C.

EXAMPLE 2

[0033] Silicon wafers and glass substrates were preheated in a vacuum of around 5×10^{-6} mbar to 300°C for 15 minutes. Then zinc of nominal thickness 1 nm and 2 nm was deposited using a DC magnetron sputtering

system. The deposited substrates were annealed at 300°C for 1 hr under vacuum. From the AFM result as shown in Table 1 we can observe that zinc 2 nm gives low surface roughness of around $R_a = 0.0995$ nm and 0.143 nm for silicon wafer and glass respectively.

[0034] Figure 6 shows AFM 3D tapping mode images with scan size of $1\mu\text{m} \times 1\mu\text{m}$ of a) Bare si wafer b) Zn 1 nm deposited and annealed at 300°C C) Zn 2 nm deposited at 100°C. The Si wafer was preheated to 100°C for 15 minutes, Zinc 1 nm was deposited and then post annealed for 1hr at 300°C. Zinc 2 nm gives low roughness for silicon wafer at 300°C.

[0035] Figure 7 AFM 3D tapping mode images with scan size of $1\mu\text{m} \times 1\mu\text{m}$ of a) Bare glass b) Zn 1 nm deposited and annealed at 300°C C) Zn 2 nm deposited at 100°C. The glass substrates were preheated to 100°C for 15 minutes, Zinc 1 nm was deposited and then post annealed for 1hr at 300°C. Zinc 2 nm gives low roughness for glass at 300°C.

[0036] It is noted that the peaks and valleys are greatly exaggerated in figures 2-4 with respect to the thickness of the layer to emphasize the roughness of the layer prior to the application of the Smoothing method described herein.

Table 1: AFM roughness data of Zinc deposited on substrates at different conditions

<i>Film</i>	<i>Deposition condition</i>	<i>Ra</i>
<i>Bare Si</i>	–	<i>0.571 nm</i>
<i>Zn (1)/Si</i>	<i>annealing at 100°C – 1 hr</i>	<i>0.0810 nm</i>
<i>Zn (2)/Si</i>	<i>annealing at 100°C – 1 hr</i>	<i>0.155 nm</i>
<i>Zn (1)/Si</i>	<i>annealing at 300°C – 1 hr</i>	<i>0.123 nm</i>
<i>Zn (2)/Si</i>	<i>annealing at 300°C – 1 hr</i>	<i>0.0995 nm</i>
<i>Bare glass</i>	–	<i>0.433 nm</i>
<i>Zn (1)/glass</i>	<i>annealing at 100°C – 1 hr</i>	<i>0.105 nm</i>
<i>Zn (2)/glass</i>	<i>annealing at 100°C – 1 hr</i>	<i>0.944 nm</i>
<i>Zn (1)/glass</i>	<i>annealing at 300°C – 1 hr</i>	<i>0.356 nm</i>
<i>Zn (2)/glass</i>	<i>annealing at 300°C – 1 hr</i>	<i>0.143 nm</i>

Applications

[0037] The examples described herein are for illustrative purposes only of selected embodiments and not all possible implementations and are not intended to limit the scope of present disclosure.

Roughness reduction of wafers

[0038] Silicon wafers used as a substrate in semiconductor manufacturing should have a high degree of smooth surface finish. Achieving a uniform and consistent surface finish is essential for ensuring consistent electrical and mechanical properties across the entire wafer. This is critical in semiconductor manufacturing, where uniformity directly impacts the performance and reliability of integrated circuits. Chemical mechanical polishing (CMP) of such wafers is done to achieve the required surface finish. This process involves material removal. By using the method disclosed in the invention, roughness of these wafers can be reduced to an atomic scale. The method is also not limited to Si wafers, it can be used on wafers of any metal carbide, nitride, oxide, carbonitride, oxycarbide, oxynitride, oxy carbonitride, semiconductor, metal or an inorganic crystal metal.

Roughness reduction of Glasses in Lenses

[0039] Ultra-high precision lenses are used in various applications where exceptional optical performance and precision are critical. Some common areas include scientific research instruments, medical imaging, semiconductor manufacturing, astronomy, photolithography, space

exploration, defense and surveillance, laser systems, high-end cameras and ultra-high precision lenses. Surface roughness of lenses is a critical factor in optical systems because it directly impacts the performance of the lens and, consequently, the quality of the images or signals transmitted through the system. Surface roughness affects scattering, reflection and transmission of light, aberrations, coating adherence, durability and wear resistance of lenses. Mechanical polishing of curved lenses is difficult and requires sophisticated machinery. The method disclosed in the invention can greatly reduce the time and money invested in manufacturing such lenses.

ADVANTAGES

- [0040]** Atomically flat/smooth surface can be achieved
- [0041]** Economical and durable method
- [0042]** Roughness reduction can be achieved without compromising the transparency of the assembly.
- [0043]** Easy industrial process flow integration for large scale deposition

WE CLAIM:

1. A method for reducing the roughness of a free surface of a substrate comprising following steps:

a) thermal treating the substrate to remove any contaminants or moisture present on the surface;

b) depositing a Filler Material (FM) on the substrate by sputtering or using other PVD and CVD techniques;

c) thermal treating the substrate and deposit to a temperature of 0.5 times the melting point of FM; and

d) repeating steps (b) and (c) until a roughness of the free surface of the substrate and deposit is equal to or smaller than a predetermined value.

2. The method as claimed in claim 1, wherein the substrate may be a metal carbide, nitride, oxide, carbonitride, oxycarbide, oxynitride, oxy carbonitride, semiconductor (silicon), metal or an inorganic crystal metal.

3. The method as claimed in claim 1, wherein the said FM is selected from metals such as Zinc (Zn), Magnesium (Mg), Aluminium (Al), Titanium (Ti), Manganese (Mn), Chromium (Cr), Germanium (Ge), Niobium (Nb), Tantalum (Ta), Hafnium (Hf), Zirconium (Zr), Vanadium (V), Calcium (Ca), Gallium (Ga), Indium (In), and Tin (Sn) or a combination thereof.

4. The method as claimed in claim 1, wherein the method results in surface roughness of the free surface of substrate and deposit less than or equal to 0.1 nm.

5. A method for reducing the roughness of a free surface of a substrate comprising following steps:

a) thermal treating the substrate to remove any contaminants or moisture present on the surface;

b) depositing a Filler Material (FM) on the substrate by sputtering or using other PVD and CVD techniques;

c) thermal treating the substrate and deposit to a temperature of 0.5 times the melting point of FM;

d) exposing the treated substrate and deposit to an oxy-carbo-nitride environment;

e) subjecting oxy-carbo-nitride exposed assembly to a further thermal treatment; and

f) repeating steps (b) to (e) until a roughness of the free surface of the substrate and deposit is equal to or smaller than a predetermined value.

6. The method as claimed in claim 5, wherein the substrate may be metal carbide, nitride, oxide, carbonitride, oxycarbide, oxynitride, oxy carbonitride, semiconductor (silicon), metal or an inorganic crystal metal.

7. The method as claimed in claim 5, wherein the said FM is selected from metals such as Zinc (Zn), Magnesium (Mg), Aluminium (Al), Titanium (Ti), Manganese (Mn), Chromium (Cr), Germanium (Ge), Niobium (Nb), Tantalum

(Ta), Hafnium (Hf), Zirconium (Zr), Vanadium (V), Calcium (Ca), Gallium (Ga), Indium (In), and Tin (Sn) or a combination thereof.

8. The method as claimed in claim 5, wherein the method results in surface roughness of the free surface of substrate and deposit less than or equal to 0.1 nm.

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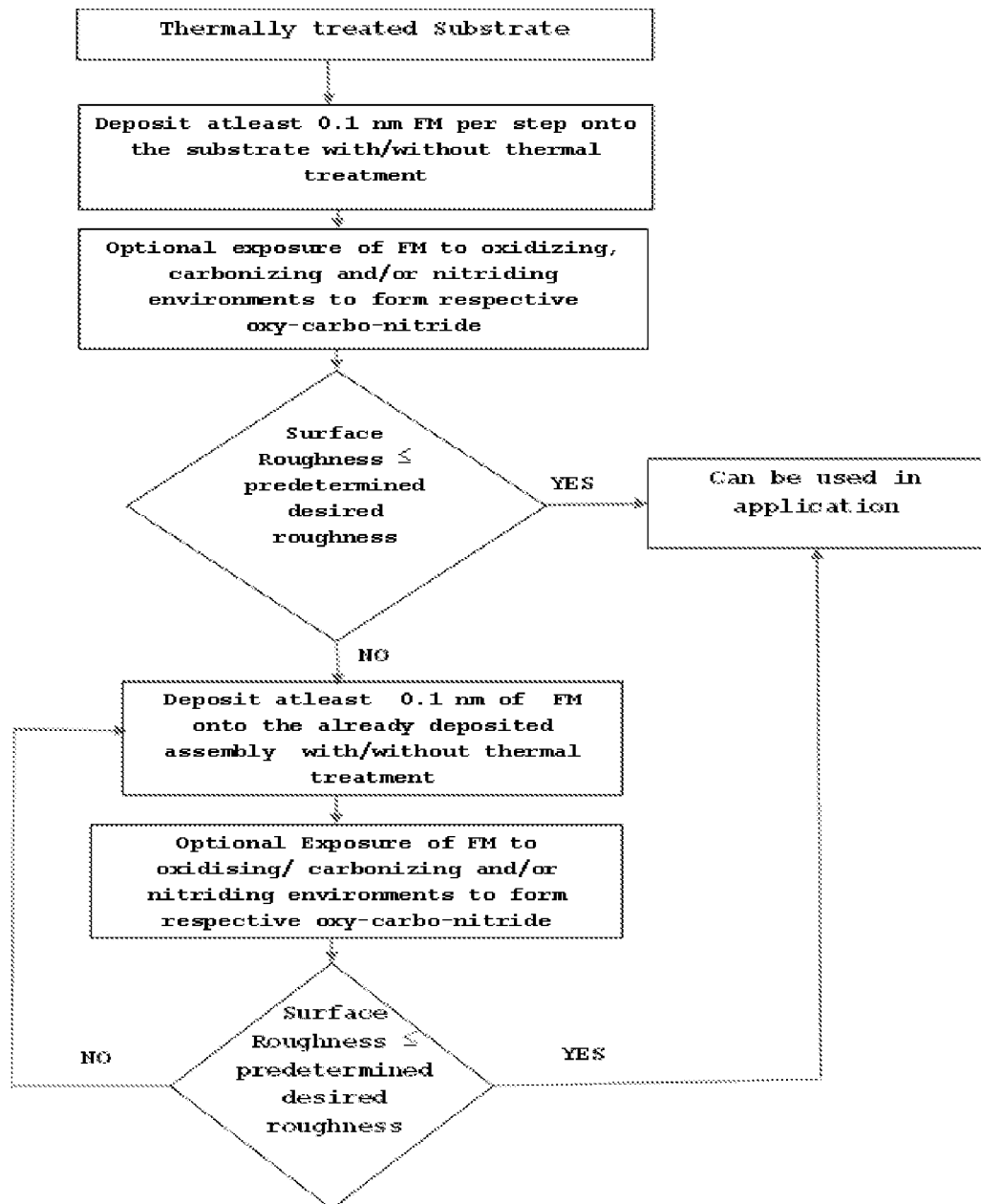


FIG. 1

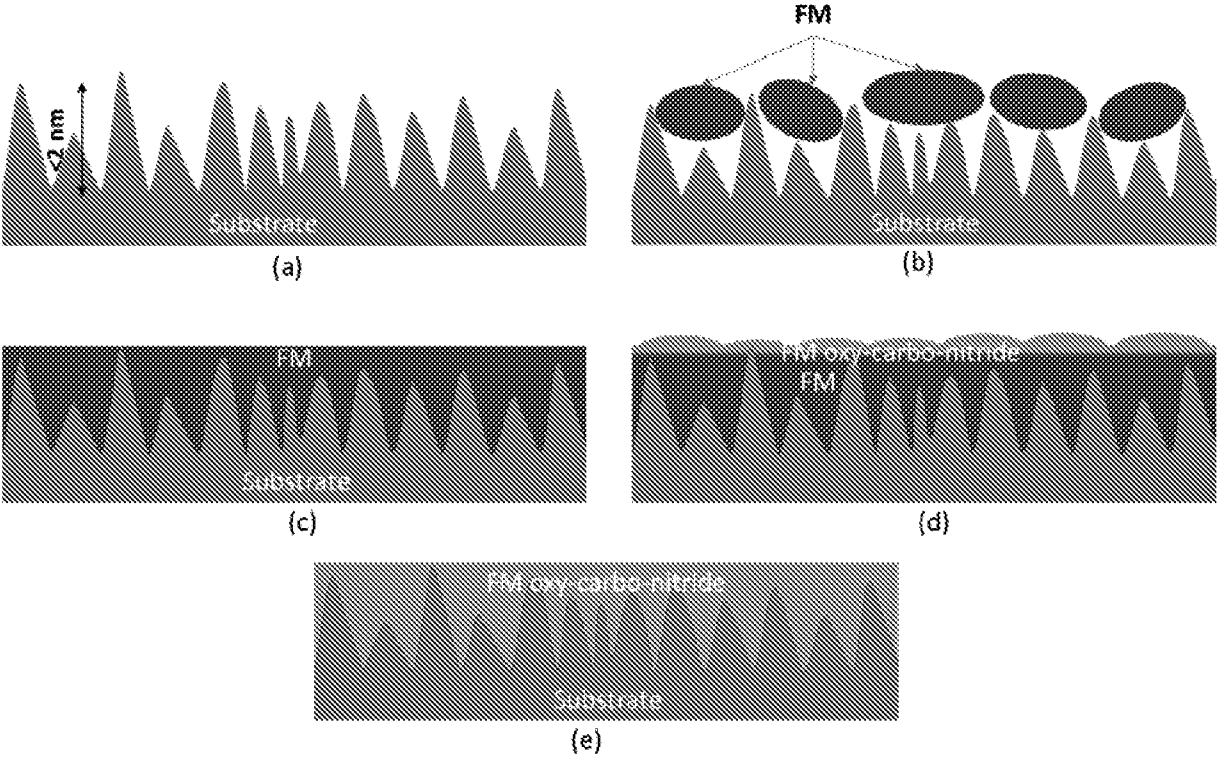


FIG. 2

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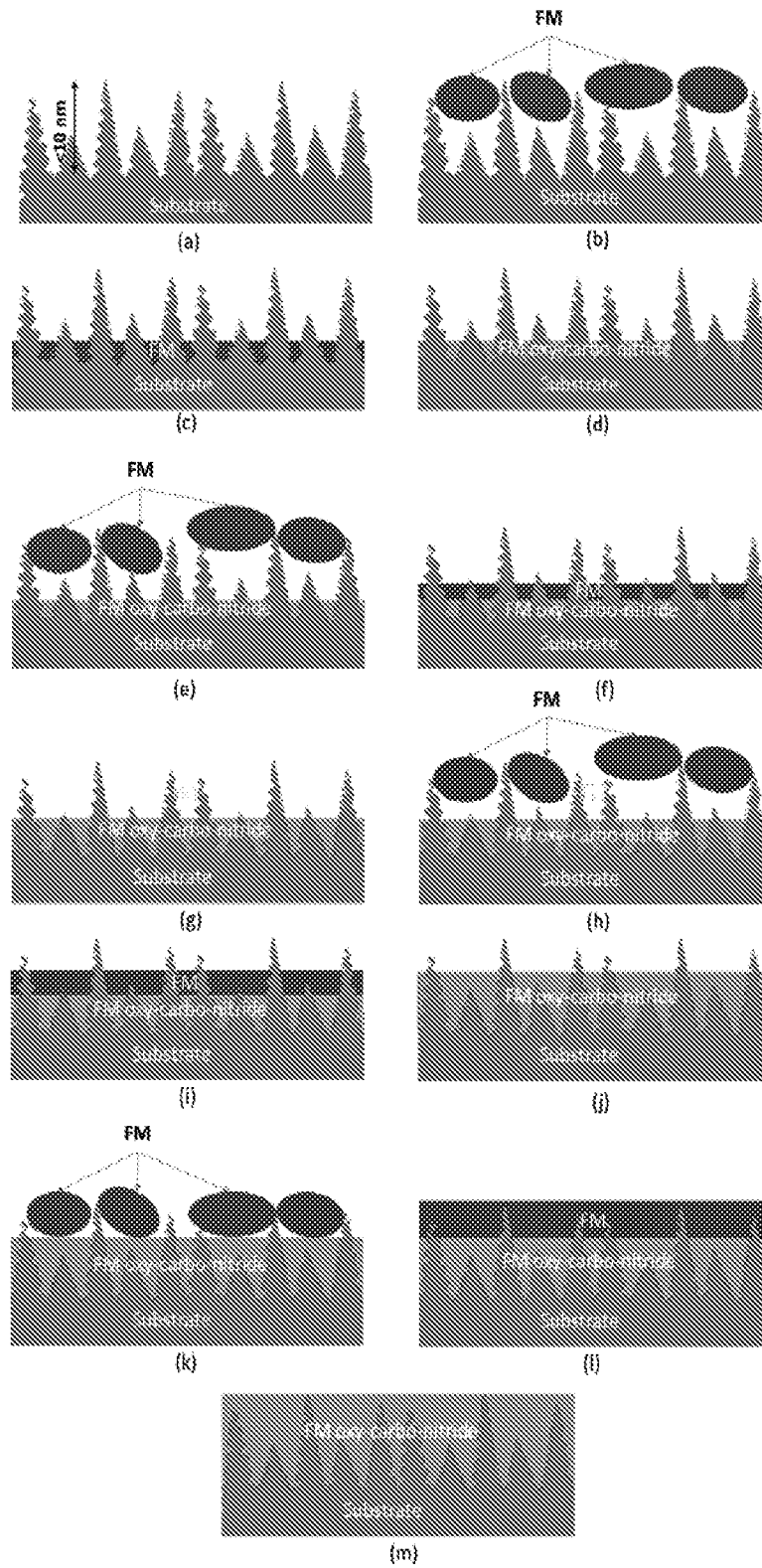


FIG. 3

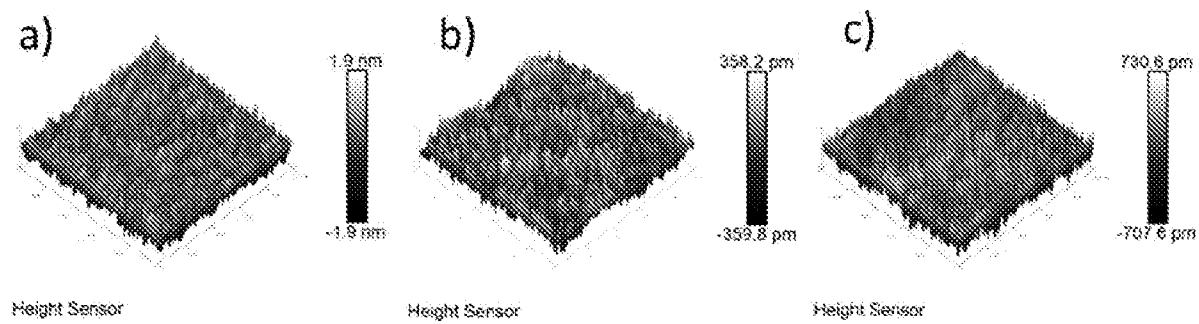


FIG. 4

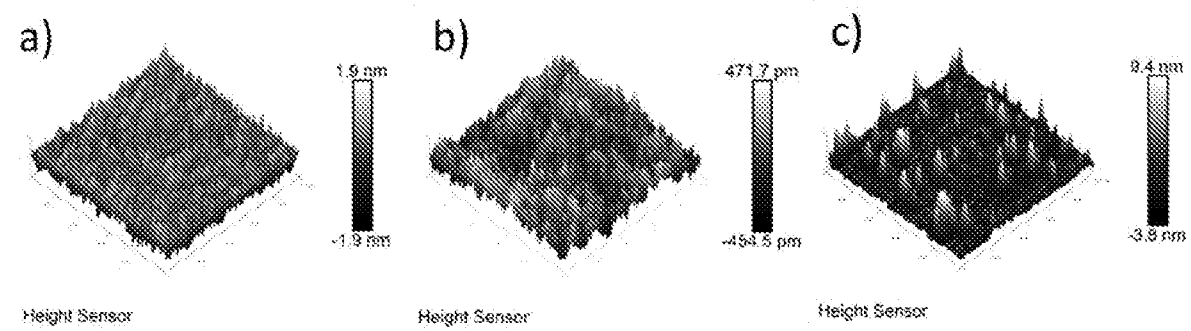


FIG. 5

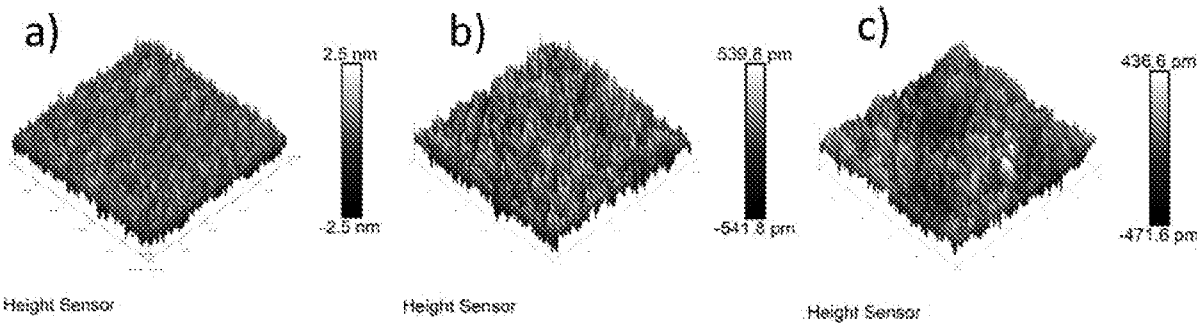


FIG. 6

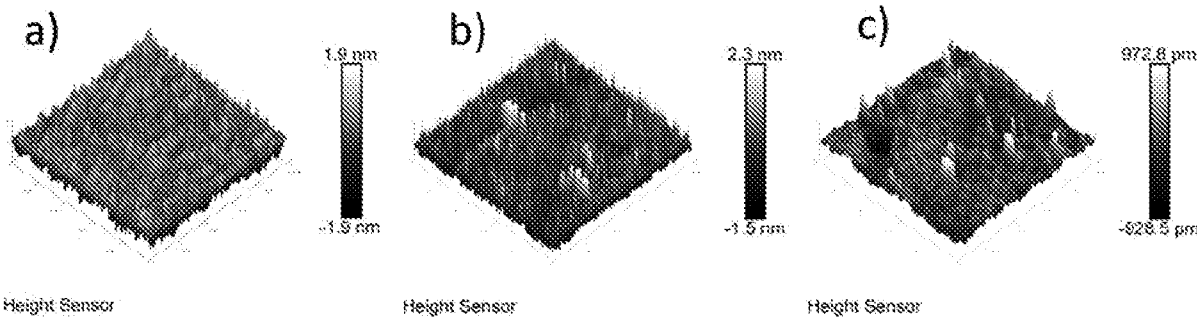


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IN2024/050184

A. CLASSIFICATION OF SUBJECT MATTER

H01L21/02, H01L21/32, H01L21/768, C23C4/02 Version=2024.01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L, C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database consulted during the international search (name of database and, where practicable, search terms used)

PatSeer, IPO Internal Database, Keywords- Filler Material, PVD, CVD, sputtering, thermal treating, reducing roughness, 0.5 times melting point

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US20060035445A1 (SOITEC SA) 16 FEBRUARY 2006 (16-02-2006) Abstract, Paragraph no. [0010-0012], [0017-0018], [0021-0023], [0045-0046]	1-8
Y	CN106601593A (WUHAN CHINA STAR OPTOELECTRONICS TECHNOLOGY CO LTD) 26 APRIL 2017 (26-04-2017) (English Translation Copy from Google Patents) abstract, description & claim 1-10	1-8
Y	KR20210080613A (APPLIED MATERIALS INC) 30 JUNE 2021 (30-06-2021) (English Translation Copy from Google Patents) abstract, Paragraph no. [0022-0035]	1-8
Y	EP2928837A2 (GUARDIAN INDUSTRIES CORP) 14 OCTOBER 2015 (14-10-2015) abstract, Paragraph no. [0015-0030]	1-8

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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