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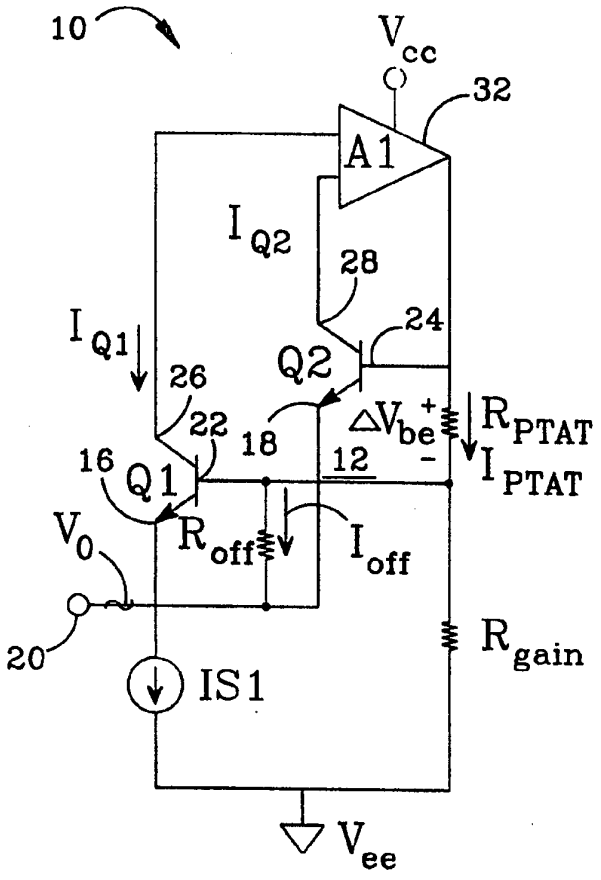
(54) Title: INTEGRATED CIRCUIT TEMPERATURE SENSOR WITH A PROGRAMMABLE OFFSET

(57) Abstract

Temperature sensor (10), with programmable offset, generates an output voltage (Vo) that is a PTAT voltage VPTAT shifted by offset voltage Voff. Band gap cell (12) generates a basic voltage across first resistor (RPTAT) to produce current (IPTAT). Second resistor (Rgain), connected between first resistor (RPTAT) and reference voltage terminal (Vee), provides voltage gain. Third resistor (Roff) is connected across the base-emitter junction of transistor (Q1) and between second resistor (Rgain) and output terminal (20) where voltage (Vo) is provided. The transistor's base-emitter voltage provides a portion of Voff. Third resistor (Roff) reduces the portion of current (IPTAT) flowing through second resistor (Rgain) to provide the remaining portion of Voff. Current source (IS1) supplies an emitter current and a current for third resistor (Roff). Offset voltage Voff is set by trimming third resistor (Roff) until voltage (Vo) equals a voltage applied to reference voltage terminal (Vee) at a lower end of a desired temperature range. The gain of VPTAT is then set by trimming first resistor (RPTAT).



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INTEGRATED CIRCUIT TEMPERATURE SENSOR WITH A PROGRAMMABLE OFFSET

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to integrated circuit (IC) proportional to absolute temperature (PTAT) temperature sensors, and more specifically to an IC temperature sensor with a programmable offset.

Description of the Related Art

The base-emitter voltage V_{be} of a forward biased transistor is a linear function of absolute temperature T in degrees Kelvin (°K), and is known to provide a stable and relatively linear temperature sensor.

$$V_{be}=\frac{kT_k}{q}\ln\left(\frac{I_c}{A_eJ_s}\right) \qquad (1)$$

where k is Boltzmann's constant, T_k is the absolute temperature (°K), q is the electron charge ($k/q=86.17\mu V/°K$), I_c is the collector current, A_e is the emitter area, and J_s is the saturation-current density. PTAT sensors eliminate the dependence on collector current by using the difference ΔV_{be} between the base-emitter voltages V_{be1} and V_{be2} of two transistors that are operated at a constant ratio between their emitter-current densities to form the PTAT voltage. The emitter-current density is conventionally defined as the ratio of the collector current to the emitter size (this

ignores the second order base current).

The basic PTAT voltage ΔV_{be} is given by:

$$\Delta V_{be} = V_{be1} - V_{be2} \qquad (2)$$

$$\Delta V_{be} = \left(\frac{kT_k}{q}\right) \ln\left(\frac{I_{c1}A_{e2}}{I_{c2}A_{e1}}\right) \qquad (3)$$

The basic PTAT voltage is amplified so that its gain, i.e. its sensitivity to changes in absolute temperature, can be calibrated to a desired value, suitably 10mV/°K, and buffered so that a PTAT voltage can be read out without corrupting the basic PTAT voltage.

A drawback of standard PTAT sensors is that at ordinary operating temperatures for most ICs there is a large offset voltage signal. For example, if the desired operating range for an IC is 0 to 125°C (273 to 398°K) and the sensor has a gain of 10mV/°K, the PTAT sensor will have an offset voltage of 2.73V at 0°C. If the gain of the PTAT sensor is not perfectly stable, a relatively small change in the offset voltage may shift the output temperature by several degrees. To read out a temperature from 0 to 125° C, a reference voltage of precisely 2.73V must be subtracted from the output of the PTAT sensor. Providing a reference voltage with adequate precision and stability is difficult and costly. Furthermore, PTAT sensors require relatively large supply voltages to supply the offset voltage in addition to the voltage needed to respond over the desired operating range and any head voltage needed to operate the sensor. Thus, products such as lap top computers which run off approximately 3V supplies cannot use PTAT sensors.

Pease, "A New Fahrenheit Temperature Sensor," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, Dec.

1984, pages 971-977, discloses a temperature sensor that provides an output voltage scaled proportional to the Fahrenheit temperature without subtracting a large constant offset voltage at the output. Pease generates a PTAT voltage using a conventional transistor pair and internally subtracts two base-emitter voltages to shift the PTAT voltage by a constant offset voltage. A non-inverting amplifier is used to multiply the shifted PTAT voltage by a fixed gain, e.g. 1.86, to simultaneously set the sensor's desired offset voltage, e.g. 770mV at 77°F, and gain, e.g. 10mV/°F. The gain is inherently calibrated by simply trimming the offset error at room temperature. In this manner, Pease effectively subtracts the offset voltage so that the sensor's output voltage is zero at 0°F.

Pease's circuit topology has several drawbacks. The shifted output voltage is produced in two separate stages: a constant offset is first subtracted from the basic PTAT voltage and then the result is multiplied by the amplifier to achieve the desired output. This increases the sensor's complexity. Because the amplifier is used to buffer the output voltage in addition to providing gain, any errors in the amplifier such as offset voltage or offset voltage drift are reflected into the output voltage signal and may cause a temperature shift. For the Fahrenheit sensor to measure 0°F, the inverting input of the amplifier must be able to go to ground potential. This type of amplifier is complex and difficult to design.

National Semiconductor Corporation produces an LM35 series of Precision Centigrade Temperature Sensors which are disclosed in their Data Acquisition Data Book, 1993, pages 5-12 to 5-15 and are the centigrade equivalent of Pease's Fahrenheit sensor. The centigrade sensors exhibit the same problems and require a minimum 4V supply voltage.

SUMMARY OF THE INVENTION

The present invention provides a temperature sensor with a an accurate programmable offset that generates an output voltage V_o over a desired temperature range that is a PTAT voltage V_{PTAT} shifted by an offset voltage V_{off}, but with a simpler design than prior temperature sensors.

This is accomplished with a band gap cell that generates a basic PTAT voltage across a first resistor to produce a PTAT current I_{PTAT}. A second resistor is connected from the first resistor to a reference voltage terminal to provide voltage gain. A transistor has a base that is connected between the first and second resistors, a collector that is tied to a supply voltage, and an emitter that is connected to an output terminal at which V_o is generated. The transistor's base-emitter voltage provides a portion of offset voltage V_{off}. A third resistor is connected across the transistor's base-emitter junction, which reduces the portion of I_{PTAT} that flows through the second resistor and provides the remaining portion of V_{off}. A current source is positioned between the transistor's emitter and the reference voltage terminal to supply its emitter current and the current for the third resistor.

The offset voltage V_{off} is set by trimming the third resistor until V_o equals a voltage applied to the reference voltage terminal at a lower end of the desired temperature range. The desired gain of V_{PTAT} is then set by trimming the first resistor.

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plot of the output voltage for the sensor of the present invention versus absolute temperature;

FIG. 2 is a simplified schematic diagram of a band gap temperature sensor with a programmable offset voltage in accordance with the present invention;

FIG. 3 is a more detailed schematic diagram of a preferred embodiment of the band gap temperature sensor shown in FIG. 2; and

FIG. 4 is a simplified schematic diagram that illustrates the programmable offset capability of the present invention for a general PTAT voltage source.

DETAILED DESCRIPTION OF THE INVENTION

As shown in FIG. 1, the present invention provides a temperature sensor that generates an output voltage V_o that is a PTAT voltage V_{PTAT} shifted by a desired offset voltage V_{off} so that V_o goes to the sensor's low supply, typically ground, when the temperature is at the lower end of a desired temperature range. The 0V temperature intercept is set by programming the sensor's offset voltage and gain. This increases the sensor's accuracy, removes the need to generate and subtract a reference voltage from the output voltage, and allows the temperature sensor to operate from 0 to 125°C with a gain of 10mV/°C off a single-sided supply voltage of approximately 2.7V. This approach allows the sensor's offset voltage and gain to be adjusted to accommodate both Centigrade and Fahrenheit sensors with a wide range of operating temperatures and gains. Pease's sensor is capable of generating the same graph, but requires more complicated circuitry and at least a 4V supply.

A programmable offset is provided by adding a single offset resistor to a conventional band gap temperature cell and by generating V_o at a different point in the cell. The desired offset is programmed by trimming the offset resistor until V_o equals 0V at the desired offset temperature. The sensor's gain is programmed independently by trimming another resistor in the band gap cell. An output amplifier

is preferably connected to the cell to buffer V_o so that it is not effected by external loading.

This approach is simple and accurate. The offset voltage is programmed in a single stage by trimming a single resistor while the gain is controlled independently by trimming a second resistor. The output amplifier is used only to buffer V_o, and hence errors in the amplifier are not reflected into the output voltage. Furthermore, the amplifier is a simple one whose input does not have to be capable of going to ground potential.

As shown in FIG. 2, a temperature sensor 10 that has a programmable offset in accordance with the invention includes a band gap cell 12 that provides a basic PTAT voltage ΔV_{be}, and an offset resistor R_{off} that selects an offset voltage so that sensor 10 produces output voltage Vo, where V_o substantially equals the voltage at the low supply V_{ee}, preferably ground potential, at a lower end of a desired temperature range. Band gap cell 12 includes a pair of npn transistors Q1 and Q2 that conduct different current densities to establish the basic PTAT voltage. The ratio of their current densities is preferably set by substantially equating their collector currents I_{Q1} and I_{Q2}, suitably 3 μA, and providing transistor Q1 with an emitter area A_{e1} that is A, suitably 10, times larger than the emitter area A_{e2} of transistor Q2.

The emitters 16 and 18 of transistors Q1 and Q2, respectively, are tied together at an output terminal 20. A current source IS1 is connected between output terminal 20 and ground, and supplies tail current for both transistors. Their bases 22 and 24 are connected across a resistor R_{PTAT} and establish the basic PTAT voltage ΔV_{be}, as described in equations 2 and 3, across a resistor R_{PTAT}. The PTAT voltage causes a PTAT current I_{PTAT} to flow through resistor R_{PTAT}. A resistor R_{gain} is connected from the base 22 of transistor Q1 to ground to provide gain for the basic PTAT voltage.

Without the invention and ignoring the base currents of transistors Q1 and Q2, I_{PTAT} would flow through resistor R_{gain}.

The collector currents I_{Q1} and I_{Q2} that flow through the collectors 26 and 28 of transistors Q1 and Q2, respectively, are input to a differential current amplifier A1 which has a current gain of suitably one hundred. The amplifier's output 32 is connected between a high voltage supply V_{cc} and the base 24 of transistor Q2, and supplies I_{PTAT} (ignoring the second order effects of Q2's base current) to maintain the basic PTAT voltage across resistor R_{PTAT}. The purpose of amplifier A1 is to make the band gap cell insensitive to changes in supply voltage V_{cc}. Alternately, a differential voltage amplifier could be used with pull resistors connecting its differential input and output 32 to the high supply.

In the absence of R_{off}, the output voltage would be taken from the top of resistor R_{PTAT} and would be given by:

$$V_o = (1+\frac{R_{gain}}{R_{PTAT}})\frac{kT_k}{q}\ln(A) \qquad (4)$$

The ratio of R_{gain} to R_{PTAT} would be set to select the desired gain for the temperature sensor, and the conventional output voltage V_o would be PTAT, and thus would incorporate a large offset voltage.

In accordance with the invention, resistor R_{off} is connected across transistor Q1's base 22 and emitter 16, and output voltage Vo is read out at output terminal 20. The effect of taking the output voltage at output terminal 20 is twofold. First, the base-emitter voltage of transistor Q1 is subtracted from the PTAT voltage across resistor R_{gain} and provides a portion of the desired offset V_{off}. Second, the output voltage V_o can be reduced to 0V at a desired temperature by collapsing the voltage across current source IS1.

The effect of connecting resistor R_{off} across transistor Q1's base-emitter junction is to provide a current source that sinks a portion of IPTAT from resistor R_{PTAT}, thereby reducing the portion of I_{PTAT} that flows through resistor R_{gain}. This reduces the voltage across resistor R_{gain} by the remaining portion of the desired offset V_{off}, which reduces V_o by the same amount.

Because the base-emitter voltage of transistor Q1 is a function of temperature, connecting resistor R_{off} across its base-emitter junction and moving the output has the additional effect of increasing the gain of output voltage Vo. This reduces the amount of gain that must be provided by the basic PTAT voltage and resistor R_{gain}, which in turn reduces the supply voltage V_{cc} required to drive the sensor.

The characteristic equation for output voltage V_o is given by the following derivation. First, the voltage across resistor R_{gain} is described by:

$$V_{R_{gain}} = (I_{PTAT} - I_{Roff}) R_{gain} \qquad (5)$$

where $I_{PTAT} = \frac{\Delta V_{be}}{R_{PTAT}}$ and $I_{off} = \frac{V_{be1}}{R_{off}}$. Substituting these relationships into equation 5 gives:

$$V_{Rgain} = \left(\frac{kT}{q}\frac{\ln(A)}{R_{PTAT}} - \frac{V_{be1}}{R_{off}}\right) R_{gain} \qquad (6)$$

Thus, the output voltage, which is V_{Rgain} shifted down by a base-emitter voltage, is given by:

$$V_o = \left(\frac{kT}{q}\frac{\ln(A)}{R_{PTAT}} - \frac{V_{be1}}{R_{OFF}}\right) R_{gain} - V_{be1} \qquad (7)$$

The base-emitter voltage for a transistor is given by:

$$V_{be} = E_g - BT_k \qquad (8)$$

where E_g is the band gap voltage and B is a constant. E_g is independent of processing parameters, bias-current levels, and transistor geometry, and thus provides a constant reference value of approximately 1.17V for silicon. The constant B depends on bias current and processing, and has a typical value of 2mV/°K.

Substituting the relation for V_{be} from equation 8 into equation 7 and rearranging to separate the voltage component that is PTAT from the constant voltage offset gives:

$$V_o = \left[\frac{R_{gain}}{R_{PTAT}}\frac{k}{q}\ln(A) + B\left(1+\frac{R_{gain}}{R_{off}}\right)\right]T_k - \left(1+\frac{R_{gain}}{R_{off}}\right)E_g \qquad (9)$$

Therefore, the desired offset voltage V_{off} is given by:

$$V_{off} = -\left(1+\frac{R_{gain}}{R_{off}}\right)E_g \qquad (10)$$

and the PTAT voltage V_{PTAT} generated at output terminal 20 is:

$$V_{PTAT} = \left[\frac{R_{gain}}{R_{PTAT}}\frac{k}{q}\ln(A) + B\left(1+\frac{R_{gain}}{R_{off}}\right)\right]T_k \qquad (11)$$

Thus, offset voltage V_{off} is set by selecting the ratio of R_{gain}/R_{off}, and the gain of VPTAT is calibrated by selecting the resistance of R_{PTAT}. In practice E_g does not vary appreciably, and hence R_{gain}/R_{off} can be set without trimming. The slope of V_{be} does vary so that R_{PTAT} can be trimmed until V_{out} equals a desired value, for example V_{out}=0.25V at 25°C.

This configuration has the additional benefit of re-

ducing the amount of supply voltage V_{cc} that is required to drive the temperature sensor. The supply voltage has to provide approximately the voltage at base 24 of transistor Q2 for the maximum desired temperature plus a V_{be} for amplifier A1. Simply providing an offset voltage at the output would not reduce this amount. However, the invention reduces the gain of the basic PTAT voltage and offsets the voltage across resistor R_{gain}. This reduces the voltage at base 24, and thus reduces the required supply voltage.

A good approximation is that the voltage at base 24 is a V_{be} above the output voltage, and hence the supply voltage V_{cc} must be at least two V_{be}'s above the maximum output voltage. For example, a temperature sensor with a temperature range of 0-125°C and a gain of 10mV/°K has a maximum V_o of 1.25V. A V_{be} is approximately 0.414V at 125°C. Thus, the minimum supply voltage V_{cc} would be approximately 2.1V. Therefore, a centigrade temperature sensor with a 10mV/°C gain and a range of 0-125°C would run comfortably off a 2.7V supply.

FIG. 3 shows a preferred temperature sensor that 10 includes the band gap cell 12 from FIG. 2 with preferred implementations of current source IS1 and differential amplifier A1, and an output amplifier A2 for buffering V_o. Current source IS1 is implemented with a current source IS2 that provides current I_{s2}, suitably 3μA, which flows from the positive supply V_{cc} through a diode D1 to ground. Diode D1 is implemented as a diode-connected npn transistor having an emitter 34 that is connected to ground and a base-collector 36. Another npn transistor Q3 has an emitter 38 that is connected to ground, a base 40 that is connected to base-collector 36 of diode D1, and a collector 42 that mirrors I_{s2} to output terminal 20 with a fixed amount of gain. This supplies the emitter currents of transistors Q1 and Q2 and the offset current I_{off} flowing through resistor R_{off}.

Differential current amplifier A1 includes a current

mirror M1 that drives a difference current equal to IQ1-I_{Q2} into the base 44 of a pnp output stage transistor Q4 that amplifies the difference current to supply I_{PTAT}. One side of current mirror M1 includes a diode D2 that is implemented as a diode connected pnp transistor having an emitter 46 that is connected to V_{cc} and a base-collector 48 that is connected to transistor Q1's collector 26. The other side of mirror M1 includes a pnp transistor Q5 having a base 50 that is connected to base-collector 48 of diode D2, an emitter 52 that is tied to V_{cc}, and a collector 54 that is connected to transistor Q2's collector 28 and base 44 of output stage transistor Q4. The emitter 56 of transistor Q4 is connected to V_{cc} and its collector, which provides amplifier A1's output 32, is connected to the base 24 of transistor Q2.

Current mirror M1 and output stage transistor Q4 together provide a negative feedback path that stabilizes band gap cell 12 and makes it insensitive to fluctuations in the supply voltage V_{cc}. For example, an increase in the difference current causes an increase in I_{PTAT}. This in turn increases the voltage at the base 24 of transistor Q2, which increases its collector current I_{Q2} and consequently reduces the difference current.

Output amplifier A2 is connected between band gap cell 12 and a load 57 such as a read out circuit, and supplies load current I_L to drive load 57 in accordance with output voltage V_o. Without amplifier A2, transistors Q1 and Q2 would have to drive the load. Although Q1 and Q2 are capable of providing some current without affecting V_o, it is preferable to use amplifier A2 to provide a buffer that maintains the integrity of V_o over a wide range of load conditions.

Amplifier A2 includes a current mirror M2 that mirrors collector current I_{Q1} to a current node 58. Current mirror M2 shares diode D2 with mirror M1 and includes a pnp tran-

sistor Q6 having a base 60 that is connected to D2's base-collector 48, an emitter 62 that is tied to V_{cc}, and a collector 64 that is connected to node 58. An npn transistor Q7 having a base 66 that is connected to the base-collector 36 of diode D1, an emitter 68 tied to ground, and a collector 70, sinks a reference current I_{ref} from current node 58 so that a difference current of I_{Q1}-I_{ref} is supplied from node 58 to the base 72 of an output transistor Q8. This transistor has a collector 74 that is tied to V_{cc}, and an emitter 76 that is connected to output terminal 20. Output transistor Q8 amplifies the difference current I_{Q1}-I_{ref} by its current gain β, suitably 100, to supply most of the load current I_L at output terminal 20. Transistors Q1 and Q2 supply a small second order portion of the total load current I_L, approximately I_L/β, which is not appreciable and does not significantly effect V_o.

In the preferred embodiments of temperature sensor 10 shown in FIGs. 2 and 3, transistor Q1 served a dual purpose. First, it forms part of the transistor pair Q1/Q2 that sets the basic PTAT voltage. Second, transistor Q1 together with offset resistor R_{off} provides the programmable offset voltage. However, many different circuit topologies might be used to generate the basic PTAT voltage ΔV_{be}. The generalized situation is shown in FIG. 4, in which a PTAT voltage source 80, such as band gap cell 12 in FIGs. 2 and 3, generates the basic PTAT voltage across resistor R_{PTAT}, which causes I_{PTAT} to flow through resistor R_{gain}. The combination of transistor Q1 and resistor R_{off} reduces the portion of I_{PTAT} that flows through resistor R_{gain} so that the output voltage V_o at output terminal 20 is shifted by the desired offset.

While several illustrative embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art. Such variations and alternate embodiments are contem-

plated, and can be made without departing from the spirit and scope of the invention as defined in the appended claims.

I CLAIM:

1. A band gap temperature sensor, comprising:

a first resistor R_{PTAT};

first and second transistors (Q1,Q2) having respective bases that are connected across said first resistor, collectors, and emitters that are connected together, said transistors conducting respective collector currents with different current densities which establishes a basic voltage proportional to absolute temperature (PTAT) across resistor R_{PTAT} causing a PTAT current I_{PTAT} to flow through resistor R_{PTAT};

a reference voltage terminal (V_{ee});

a second resistor R_{gain} that is connected between the base of the first transistor and said reference voltage terminal and conducts a first portion of I_{PTAT};

a biasing current source (IS1) that is connected from the emitters of said transistors to said reference voltage terminal and supplies emitter current for said transistors; and

an offset current source (R_{off}) that sinks a second portion of I_{PTAT} to set the first portion of I_{PTAT} that flows through resistor R_{gain},

said temperature sensor responding to I_{PTAT} by producing an output voltage V_o at said emitters that is a PTAT voltage V_{PTAT} shifted by an offset voltage V_{off}, resistor R_{gain} being selected to set V_{off} so that V_o is substantially the same as a voltage applied to said reference voltage terminal at a desired temperature.

2. The temperature sensor of claim 1, wherein said offset current source comprises a third resistor R_{off} that is connected across the first transistor's base and emitter and conducts said second portion of I_{PTAT}, the ratio of R_{gain} to R_{off} being selected to set V_{off}.

3. The temperature sensor of claims 1 or 2, further comprising:

a supply voltage terminal for receiving a supply voltage (V_{cc}); and

a differential amplifier (A1) that is connected to the supply voltage terminal, and has a differential input that is connected to the transistors' collectors and an output that is coupled to the base of the second transistor, said differential amplifier stabilizing the temperature sensor so that the basic PTAT voltage is insensitive to changes in said supply voltage.

4. The temperature sensor of claims 1,2 or 3, wherein said output voltage V_o responds to centigrade temperatures from approximately zero degrees centigrade to approximately 125 degrees centigrade with a sensitivity of approximately 10mV/°C, said reference and supply voltages differing by less than 3 volts.

5. The temperature sensor of claims 1,2,3 or 4, wherein said reference voltage is ground reference potential.

6. The temperature sensor of claims 3,4 or 5, wherein said differential amplifier comprises:

a current mirror (M1) having a current input that is connected to said supply voltage terminal, said differential input, and a current output;

an output stage transistor (Q4) having a base that is connected to said current output and a current circuit that supplies current to resistor R_{PTAT}.

7. The temperature sensor of claims 3,4 or 5, further comprising:

a reference current source (IS1) that generates a reference current;

an output amplifier (A2) having a differential input that is connected to said reference current source and the collector of said first transistor, and having a current output that is connected to said first transistor's emitter, said output amplifier comparing said first transistor's collector current to said reference current to supply a drive current at said current output.

8. The temperature sensor of claim 7, wherein said first and second transistors' emitters are connected at an output node (20), said differential and output amplifiers comprising:

a current mirror (M1,M2) having a reference input that is connected to said first transistor's collector and supplies its collector current, first and second inputs that are connected to said second transistor's collector and said reference current source, respectively, and which conduct said first transistor's collector current, and first and second current outputs that supply the difference between the first and second transistors' collector currents and the difference between the first transistor's collector current and said reference current, respectively;

an output stage transistor (Q4) having a base that is connected to said first current output and a current circuit that supplies current to resistor R_{PTAT}; and

a drive transistor (Q8) having a base that is connected to said second current output and a current circuit that supplies current at said output node.

9. The temperature sensor of claim 8, wherein said output voltage V_o responds to centigrade temperatures from approximate zero degrees centigrade to approximately 125 degrees centigrade with a sensitivity of approximately

10mV/°C, said reference voltage is ground potential and said supply voltage is less than 3 volts.

AMENDED CLAIMS

[received by the International Bureau on 29 November 1995 (29.11.95);
original claims 3-6 amended;
remaining claims unchanged (3 pages)].

1. A band gap temperature sensor, comprising:

a first resistor R_{PTAT};

first and second transistors (Q1,Q2) having respective bases that are connected across said first resistor, collectors, and emitters that are connected together, said transistors conducting respective collector currents with different current densities which establishes a basic voltage proportional to absolute temperature (PTAT) across resistor R_{PTAT} causing a PTAT current I_{PTAT} to flow through resistor R_{PTAT};

a reference voltage terminal (V_{ee});

a second resistor R_{gain} that is connected between the base of the first transistor and said reference voltage terminal and conducts a first portion of I_{PTAT};

a biasing current source (IS1) that is connected from the emitters of said transistors to said reference voltage terminal and supplies emitter current for said transistors; and

an offset current source (R_{off}) that sinks a second portion of I_{PTAT} to set the first portion of I_{PTAT} that flows through resistor R_{gain},

said temperature sensor responding to I_{PTAT} by producing an output voltage V_o at said emitters that is a PTAT voltage V_{PTAT} shifted by an offset voltage V_{off}, resistor R_{gain} being selected to set V_{off} so that V_o is substantially the same as a voltage applied to said reference voltage terminal at a desired temperature.

2. The temperature sensor of claim 1, wherein said offset current source comprises a third resistor R_{off} that is connected across the first transistor's base and emitter and conducts said second portion of I_{PTAT}, the ratio of R_{gain}

to R_{off} being selected to set V_{off}.

3. The temperature sensor of claim 1, further comprising:

a supply voltage terminal for receiving a supply voltage (V_{cc}); and

a differential amplifier (A1) that is connected to the supply voltage terminal, and has a differential input that is connected to the transistors' collectors and an output that is coupled to the base of the second transistor, said differential amplifier stabilizing the temperature sensor so that the basic PTAT voltage is insensitive to changes in said supply voltage.

4. The temperature sensor of claim 1, wherein said output voltage V_o responds to centigrade temperatures from approximately zero degrees centigrade to approximately 125 degrees centigrade with a sensitivity of approximately 10mV/°C, said reference and supply voltages differing by less than 3 volts.

5. The temperature sensor of claim 1, wherein said reference voltage is ground reference potential.

6. The temperature sensor of claim 3, wherein said differential amplifier comprises:

a current mirror (M1) having a current input that is connected to said supply voltage terminal, said differential input, and a current output;

an output stage transistor (Q4) having a base that is connected to said current output and a current circuit that supplies current to resistor R_{PTAT}.

7. The temperature sensor of claims 3,4 or 5, further comprising:

a reference current source (IS1) that generates a

reference current;

an output amplifier (A2) having a differential input that is connected to said reference current source and the collector of said first transistor, and having a current output that is connected to said first transistor's emitter, said output amplifier comparing said first transistor's collector current to said reference current to supply a drive current at said current output.

8. The temperature sensor of claim 7, wherein said first and second transistors' emitters are connected at an output node (20), said differential and output amplifiers comprising:

a current mirror (M1,M2) having a reference input that is connected to said first transistor's collector and supplies its collector current, first and second inputs that are connected to said second transistor's collector and said reference current source, respectively, and which conduct said first transistor's collector current, and first and second current outputs that supply the difference between the first and second transistors' collector currents and the difference between the first transistor's collector current and said reference current, respectively;

an output stage transistor (Q4) having a base that is connected to said first current output and a current circuit that supplies current to resistor R_{PTAT}; and

a drive transistor (Q8) having a base that is connected to said second current output and a current circuit that supplies current at said output node.

9. The temperature sensor of claim 8, wherein said output voltage V_o responds to centigrade temperatures from approximate zero degrees centigrade to approximately 125 degrees centigrade with a sensitivity of approximately 10mV/°C, said reference voltage is ground potential and said supply voltage is less than 3 volts.

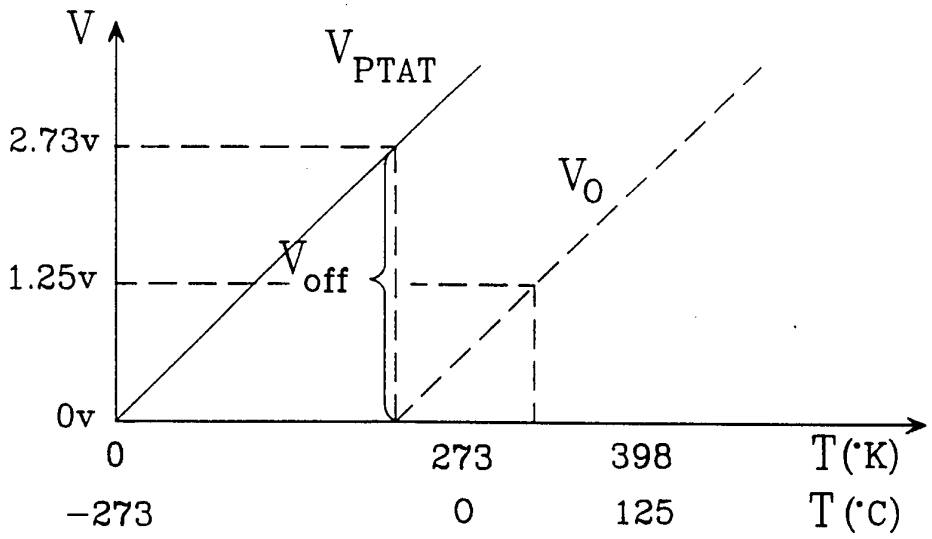

FIG.1

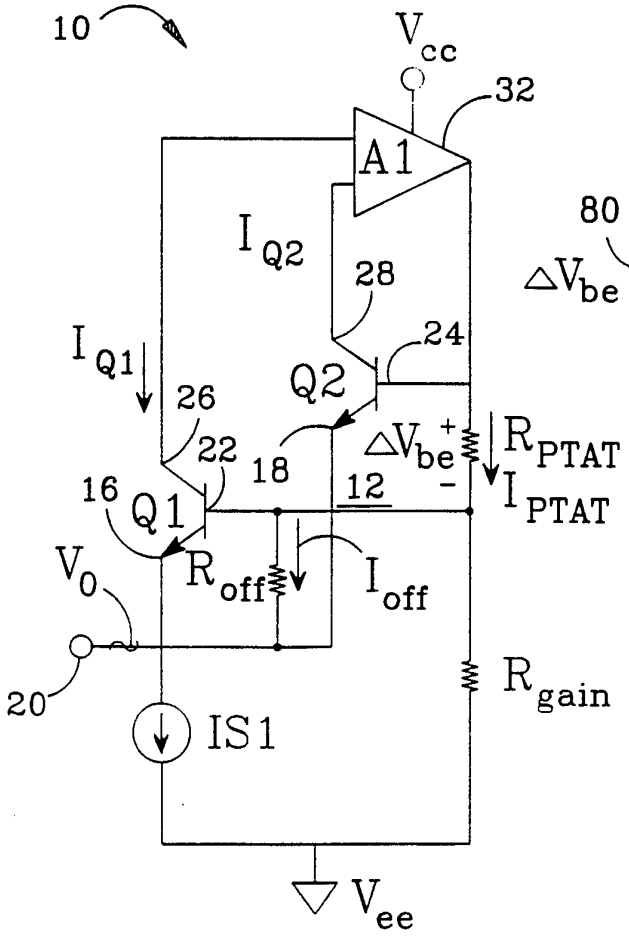

FIG.2

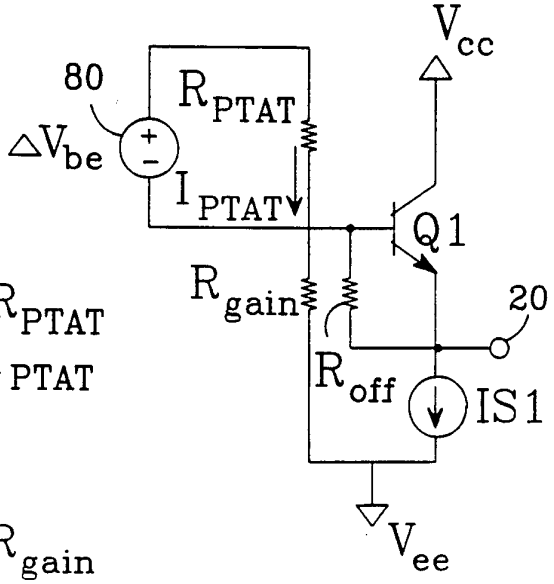

FIG.4

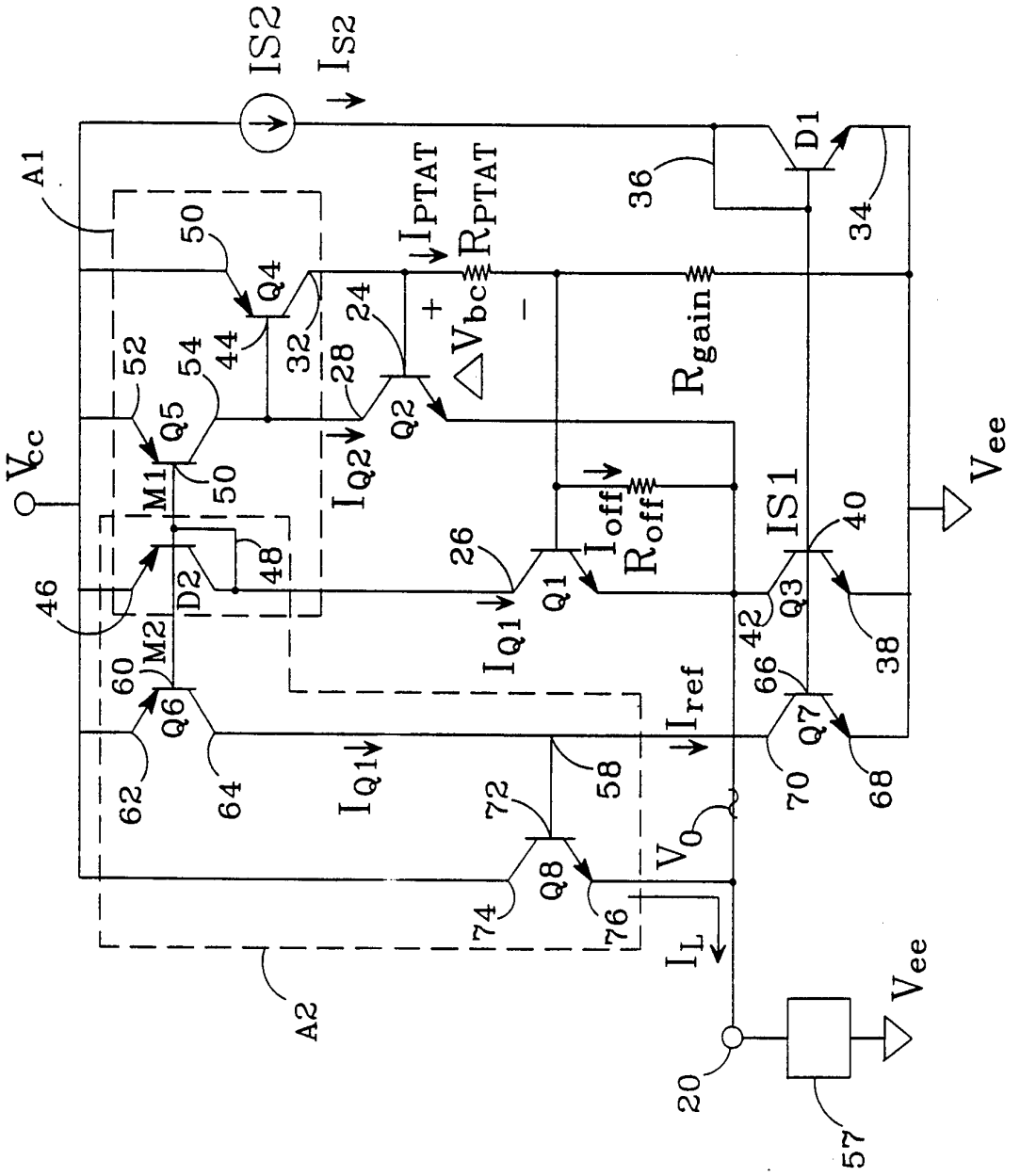
IS2
Is2
A1
50
Q4
44
32
24
28
Q2
IPTAT
RPTAT
+
ΔVbc
−
36
D1
34
Rgain
52
54
Q5
M1
50
IQ2
Vcc
46
D2
48
26
Q1
Ioff
Roff
IS1
40
Vee
M2
60
Q6
IQ1
42
Q3
66
38
62
64
IQ1
72
58
Iref
Q7
70
68
Q8
74
76
V0
IL
A2
20
Vee
57

FIG.3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/11320

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G05F 3/30, 1/567
US CL : 327/513, 512, 539; 307/651; 374/178; 323/313
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 327/513, 512, 539; 307/651; 374/178, 163, 180, 183; 323/313

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A, P	US, A, 5,430,395 (ICHIMARU) 04 July 1995, Fig. 1	NONE
A	US, A, 4,797,577 (HING) 10 January 1989, Fig. 1	NONE
A	US, A, 4,683,416 (BYNUM) 28 July 1987, Fig. 2	NONE
A	US, A, 4,652,144 (GUNTHER ET AL.) 24 March 1987, Fig. 2	NONE
A	US, A, 4,497,586 (NELSON) 05 February 1985, Fig. 5	NONE

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 01 NOVEMBER 1995	Date of mailing of the international search report 13 NOV 1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer TERRY L. ENGLUND Telephone No. (703)308-4817

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/11320

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 4 - 9
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

APS
search terms: temperature sensor, offset, proportional to absolute temperature, PTAT, bandgap, bipolar, offset resistor, offset voltage, programmable offset