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(54) **Title**: MEMORIES UTILIZING HYBRID ERROR CORRECTING CODE TECHNIQUES

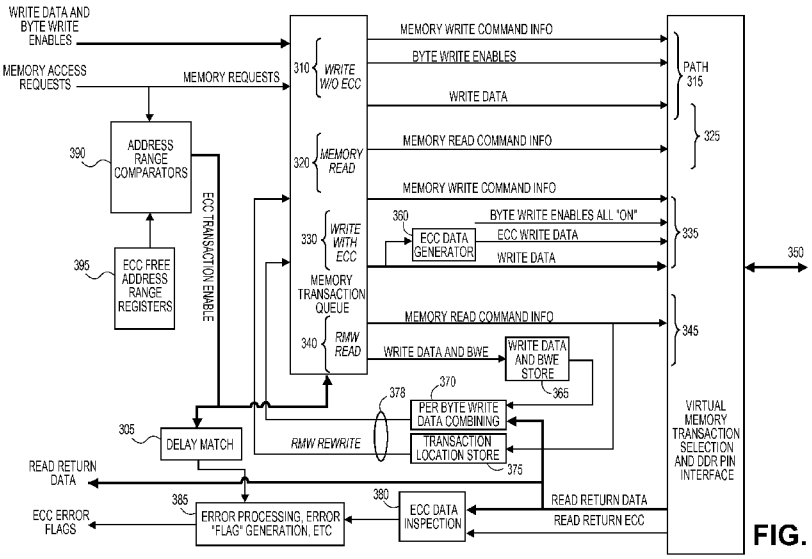


FIG. 3

(57) **Abstract**: Use of hybrid error correcting code (ECC) techniques. A memory access request having an associated address is received. A memory controller determines whether the address corresponds to a first region of a memory for which ECC techniques are applied or a second region of the memory for which ECC techniques are not applied. The memory access is processed utilizing ECC techniques if the address corresponds to the first region of the memory and processed without utilizing the ECC techniques if the address corresponds to the second region of the memory.

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MEMORIES UTILIZING HYBRID ERROR CORRECTING CODE TECHNIQUES

TECHNICAL FIELD

[0001] Embodiments of the invention relate to memory systems. More particularly, embodiments of the invention relate to utilization of hybrid error correcting code techniques to provide more efficient memories.

BACKGROUND

[0002] Error correcting code (ECC) techniques are utilized to detect and/or correct errors in memory, and may be used, for example, in mission-critical applications. Memory errors with ECC do not cause a system failure, but allow a system to detect and correct the error and continue operating. Use of ECC techniques is expanding and is desirable in other applications as well. However, ECC overhead may excessive for some applications where ECC is desirable.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is a conceptual illustration of an example memory map including both ECC protected regions and non-ECC protected regions.

Figure 2 is a block diagram of one embodiment of an electronic system.

Figure 3 is a block diagram of one embodiment of a memory subsystem with selectable ECC processing.

Figure 4 is a flow diagram of a technique for selective use of ECC techniques.

DETAILED DESCRIPTION

[0003] In the following description, numerous specific details are set forth. However, embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the understanding of this description.

[0004] Partial write memory throughput performance as part of ECC protection can experience up to a 70% degradation due to a Read/Modify/Write process for the checksum calculation required by ECC techniques. This performance degradation in partial writes can be a severe problem, for example, for integrated graphics performance because integrated graphics frequently update the frame buffer stored in system memory with numerous partial writes. Thus, applying ECC to integrated graphics results in performance degradation that may outweigh the benefits of ECC protection. This may be applicable to other situations as well.

[0005] Techniques described herein provide a "non-ECC" window or area in a memory map. This is an area in the memory map where ECC operations (e.g., Read/Modify/Write, compute checksum) do not apply. In one embodiment, this area is specified by a starting address and size or range; however, other techniques for specifying the non-ECC window can also be utilized.

[0006] Returning to the integrated graphics example, the area of system memory reserved for integrated graphics would be assigned to a non-ECC window. The same may also apply to video encode and video decode blocks that also share system memory normally protected by ECC. These regions for integrated graphics as well as video encode and decode do not require the protection that ECC affords because, if a pixel has an error and appears as the wrong color, it will be on the screen for 1/24 or 1/60 of a second, for example, depending on the refresh rate. This may not be noticeable to a user.

[0007] Various embodiments of the techniques described herein utilize one or more registers (or other storage mechanisms) to define one or more non-ECC windows in a memory protected by ECC techniques, as well as logic that checks incoming addresses for reads and writes in the memory controller against the window. For addresses that fall within the non-ECC window, the partial writes will not incur the read-merge-checksum-compute-write penalty, but rather be written

directly with the checksum value being a "don't care." For reads, the checksum may be ignored and checksum errors suppressed.

[0008] Currently, a system designer must choose between higher-level graphics performance protection and ECC protection. Some systems address this problem by adding a shared cache to a graphics core. This causes the memory controller to see a full cache line instead of a partial cache line, thus not needing the Read/Modify/Write operation. This is a costly addition to a graphics core that is not applicable, for example, to embedded systems, where power and cost must be kept as low as possible.

[0009] **Figure 1** is a conceptual illustration of an example memory map including both ECC protected regions and non-ECC protected regions. The example of Figure 1 illustrates only one ECC-free region; however, any number of ECC-free regions can be supported in a similar manner. The example of Figure 1 illustrates the ECC-free region near the "top" of the memory region; however, the ECC-free region(s) can be placed in other locations as well.

[0010] In the example of Figure 1, ECC-Protected region 130 includes conventional memory space (e.g., 0 to 640 kb), upper memory space (e.g., 640 kb to 1 Mb) and a portion of extended memory space (e.g., 1 Mb and higher). In one embodiment, ECC-free region 120 is within the extended memory space. In one embodiment, there is also ECC-protected region 110 above ECC-free area 120. In alternate embodiments, multiple ECC- free areas may be created within the extended memory space.

[0011] **Figure 2** is a block diagram of one embodiment of an electronic system. The electronic system illustrated in Figure 2 is intended to represent a range of electronic systems (either wired or wireless) including, for example, desktop computer systems, laptop computer systems, cellular telephones, personal digital assistants (PDAs) including cellular-enabled PDAs, set top boxes. Alternative electronic systems may include more, fewer and/or different components. The electronic system of Figure 2 may represent any of the electronic systems of Figure 1.

[0012] Electronic system 200 includes bus 205 or other communication device to communicate information, and processor 210 coupled to bus 205 that may process information. While electronic system 200 is illustrated with a single processor,

electronic system 200 may include multiple processors and/or co-processors. Electronic system 200 further may include random access memory (RAM) or other dynamic storage device 220 (referred to as main memory), coupled to bus 205 and may store information and instructions that may be executed by processor 210. Memory 220 may also be used to store temporary variables or other intermediate information during execution of instructions by processor 210. In one embodiment, memory 220 may be a memory system organized as described above with respect to Figure 1.

[0013] Electronic system 200 may also include read only memory (ROM) and/or other static storage device 230 coupled to bus 205 that may store static information and instructions for processor 210. Data storage device 240 may be coupled to bus 205 to store information and instructions. Data storage device 240 such as a magnetic disk or optical disc and corresponding drive may be coupled to electronic system 200.

[0014] Electronic system 200 may also be coupled via bus 205 to display device 250, such as a cathode ray tube (CRT) or liquid crystal display (LCD), to display information to a user. Alphanumeric input device 260, including alphanumeric and other keys, may be coupled to bus 205 to communicate information and command selections to processor 210. Another type of user input device is cursor control 270, such as a mouse, a trackball, or cursor direction keys to communicate direction information and command selections to processor 210 and to control cursor movement on display 250.

[0015] Electronic system 200 further may include network interface(s) 280 to provide access to a network, such as a local area network. Network interface(s) 280 may include, for example, a wireless network interface having antenna 285, which may represent one or more antenna(e). Network interface(s) 280 may also include, for example, a wired network interface to communicate with remote devices via network cable 287, which may be, for example, an Ethernet cable, a coaxial cable, a fiber optic cable, a serial cable, or a parallel cable.

[0016] In one embodiment, network interface(s) 280 may provide access to a local area network, for example, by conforming to IEEE 802.11b and/or IEEE 802.11g standards, and/or the wireless network interface may provide access to a personal area

network, for example, by conforming to Bluetooth standards. Other wireless network interfaces and/or protocols can also be supported.

[0017] IEEE 802.11b corresponds to IEEE Std. 802.11b-1999 entitled "Local and Metropolitan Area Networks, Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: Higher-Speed Physical Layer Extension in the 2.4 GHz Band," approved September 16, 1999 as well as related documents. IEEE 802.11g corresponds to IEEE Std. 802.11g-2003 entitled "Local and Metropolitan Area Networks, Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, Amendment 4: Further Higher Rate Extension in the 2.4 GHz Band," approved June 27, 2003 as well as related documents. Bluetooth protocols are described in "Specification of the Bluetooth System: Core, Version 1.1," published February 22, 2001 by the Bluetooth Special Interest Group, Inc. Associated as well as previous or subsequent versions of the Bluetooth standard may also be supported.

[0018] In addition to, or instead of, communication via wireless LAN standards, network interface(s) 280 may provide wireless communications using, for example, Time Division, Multiple Access (TDMA) protocols, Global System for Mobile Communications (GSM) protocols, Code Division, Multiple Access (CDMA) protocols, and/or any other type of wireless communications protocol.

[0019] **Figure 3** is a block diagram of one embodiment of a memory subsystem with selectable ECC processing. In one embodiment, the memory subsystem supports four main types of memory transactions: 1) writes with ECC disabled, 2) reads with or without ECC enabled, 3) writes with ECC enabled, and 4) prefetch reads associated with read/write/modify (RMW) cycles needed for partial writes with ECC.

[0020] When ECC is enabled, for example, through software selection, all writes (at least al partial writes) are completed via two memory accesses: a read of the memory location to prefetch the data already present (via path 340-345), an internal merging of the read data with the new write data on a byte-by-byte basis (via path 378), and a rewrite of the memory location including new ECC values (via path 330-335).

[0021] In one embodiment, path 310-315 includes mechanisms (e.g., bus lines) to transmit memory write command information, byte write enable signals, and the data to be written from a memory transaction queue to a memory interface (e.g., DDR-3, DDR-4). In one embodiment, path 320-325 includes mechanisms (e.g., bus lines) to transmit memory read command information from the memory transaction queue to the memory interface.

[0022] In one embodiment, path 330-335 includes mechanisms (e.g., bus lines) to transmit memory write command information, byte write enable signals, ECC write data as generated by ECC data generator 360 and data to be written. Path 340-345 includes mechanisms (e.g., bus lines) to transmit memory read command information to the memory interface. The memory read command information is also transmitted to transaction location store 375 that utilizes the memory read command information for RMW rewrite operations on path 378.

[0023] In one embodiment, the memory transaction queue provides write data and BWE to write data and BWE store 365, which stores the data and forwards it to transaction location store 375 that utilizes it for RMW rewrite operations on path 378. Path 378 provides the data to the memory transaction queue.

[0024] The memory subsystem of Figure 3 is enhanced by providing a mechanism to identify system memory regions that require no ECC processing and memory regions that do require ECC processing. With this enhanced capability, ECC can be enabled or disabled for each transaction type. In the example above, software-programmable ECC-free address range registers and comparison circuitry (e.g., 390) are provided in the memory subsystem.

[0025] In one embodiment, when a particular transaction address maps to one of the ECC-free ranges, the corresponding memory transaction is performed without ECC processing. In the case of a memory read, the ECC data returning is "ignored" and ECC error processing proceeds as if no CC error is encountered (i.e., no error flags assert, no error processing is done, etc.). In the case of a write, only one memory access is required (via path 310-315), instead of needing to do a RMW (via one or more of paths 330-335, 340-345, 378).

[0026] In one embodiment, address range comparator(s) 390 compare memory access addresses sent to the memory transactions queue to one or more addresses

stored in ECC-Free Address Range Registers 395 that define the boundaries of one or more ECC-free regions in memory. In response to the comparison, address range comparator(s) 390 an ECC transaction enable signal is selectively asserted to the path(s) utilized by the memory transaction queue to send data to the memory interface depending on whether ECC techniques should be applied or not.

[0027] For read operations, ECC data inspection circuitry 380 and error processing circuitry 385 operate to selectively utilize ECC data as described above. In some situations, data read form memory may be combined for rewrite operations through per byte write data combining circuitry 370.

[0028] **Figure 4** is a flow diagram of a technique for selective use of ECC techniques. The technique of Figure 4 may be used to provide a memory mapping similar to the one illustrated in Figure 1 and may be supported, for example, by using the arrangement of Figure 3.

[0029] A memory address corresponding to a memory access is received, 410. This memory address can be received in any manner known in the art. In the example of Figure 3, the memory address is received and compared in the memory subsystem; however, other configurations may also be supported.

[0030] The memory address is compared to one or more ECC-free regions, 420. In one embodiment, the memory subsystem includes two or more registers that are used to define the boundaries of one or more ECC-free regions; however, other configurations can also be supported. In the example of Figure 3, the memory address is received and compared in the memory subsystem; however, other configurations may also be supported.

[0031] If the address corresponds to an ECC-free region, 430, a path through the memory subsystem that does not apply ECC protection is selected, 440. As described above with respect to Figure 3, one or more paths through the memory subsystem may be provided that do not utilize ECC protection. In one embodiment, the comparison circuitry controls an enabling signal to determine whether ECC protection is applied or not.

[0032] The non-ECC protected data is written to memory, 450. The memory can be any type of memory, for example, DDR-3 or DDR-4 compliant memory. Other memory types can be similarly supported.

[0033] If the address does not correspond to an ECC-free region, 430, a path through the memory subsystem that does apply ECC protection is selected, 445. As described above with respect to Figure 3, one or more paths through the memory subsystem may be provided that do utilize ECC protection. In one embodiment, the comparison circuitry controls an enabling signal to determine whether ECC protection is applied or not.

[0034] ECC protection is applied to the data, 455. Any ECC techniques known in the art can be supported. The ECC protected data is written to memory, 465. The memory can be any type of memory, for example, DDR-3 or DDR-4 compliant memory. Other memory types can be similarly supported.

[0035] This has the effect of making more efficient use of existing memory bandwidth, reducing average latency for each memory transaction, and increasing the total memory bandwidth available for each application. Identification of the ECC-free regions can be done by mechanisms other than address range mapping. For example, particular application streams (e.g., video or graphics pixel updates) might be tagged in such a way that the memory subsystem chooses the ECC-free path for transactions originating from these application sources.

[0036] Use of hybrid error correcting code (ECC) techniques. A memory access request having an associated address is received. A memory controller determines whether the address corresponds to a first region of a memory for which ECC techniques are applied or a second region of the memory for which ECC techniques are not applied. The memory access is processed utilizing ECC techniques if the address corresponds to the first region of the memory and processed without utilizing the ECC techniques if the address corresponds to the second region of the memory.

[0037] The memory access request can be a read request. The memory access request comprises a write request. The second portion of the memory addresses can be configurable. The second portion of the memory addresses can be utilized to store graphics data. The second portion of the memory addresses may reside in an expended memory region. The memory devices can be dynamic random access memory (DRAM) devices.

[0038] A system may be utilized, the system can include memory devices to provide data storage corresponding to a range of memory addresses. A first portion of the memory addresses are protected by an error correcting code (ECC) technique and a second portion of the memory addresses are not protected by the ECC technique. A memory control device can be coupled with the memory devices. The memory control device can have a plurality of processing paths. A first set of the processing paths apply the ECC technique to data and a second set of the processing paths cause the data to be stored without applying the ECC technique. The memory control device selectively applies the ECC technique based on an address corresponding to a memory access request.

[0039] The memory access request can be a read request. The memory access request comprises a write request. The second portion of the memory addresses can be configurable. The second portion of the memory addresses can be utilized to store graphics data. The second portion of the memory addresses may reside in an expended memory region. The memory devices can be dynamic random access memory (DRAM) devices.

[0040] A memory control circuit can include a first interface to communicate with processing circuitry and a second interface to communicate with memory devices and control circuitry coupled with the first interface and the second interface. The control circuitry receives a memory access request having an associated address via the first interface, determines whether the address corresponds to a first region of a memory for which error correcting code (ECC) techniques are applied or a second region of the memory for which ECC techniques are not applied, processes the memory access utilizing ECC techniques if the address corresponds to the first region of the memory, and processes the memory access without utilizing the ECC techniques if the address corresponds to the second region of the memory.

[0041] The memory access request can be a read request. The memory access request comprises a write request. The second portion of the memory addresses can be configurable. The second portion of the memory addresses can be utilized to store graphics data. The second portion of the memory addresses may reside in an

expended memory region. The memory devices can be dynamic random access memory (DRAM) devices.

[0042] Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[0043] While the invention has been described in terms of several embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.

CLAIMS

What is claimed is:

1. A system comprising:

memory devices to provide data storage corresponding to a range of memory addresses, a first portion of the memory addresses are protected by an error correcting code (ECC) technique and a second portion of the memory addresses are not protected by the ECC technique;

a memory control device coupled with the memory devices, the memory control device having a plurality of processing paths, wherein a first set of the processing paths operate to apply the ECC technique to data and a second set of the processing paths operate to cause the data to be stored without applying the ECC technique, the memory control device to selectively apply the ECC technique based on an address corresponding to a memory access request.

2. The system of claim 1 wherein the memory access request comprises a read request.

3. The system of claim 1 wherein the memory access request comprises a write request.

4. The system of claim 1 wherein the second portion of the memory addresses is configurable.

5. The system of claim 1 wherein the second portion of the memory addresses is utilized to store graphics data.

6. The system of claim 1 wherein the second portion of the memory addresses reside in an expended memory region.

7. The system of claim 1 wherein the memory devices comprise dynamic random access memory (DRAM) devices.

8. A method comprising:

receiving a memory access request having an associated address;

determining whether the address corresponds to a first region of a memory for which error correcting code (ECC) techniques are applied or a second region of the memory for which ECC techniques are not applied;

processing the memory access utilizing ECC techniques if the address corresponds to the first region of the memory;

processing the memory access without utilizing the ECC techniques if the address corresponds to the second region of the memory.

9. The method of claim 8 wherein the memory access comprises a read operation.

10. The method of claim 8 wherein the memory access comprises a write operation.

11. The method of claim 8 wherein determining whether the address corresponds to a first region of a memory for which error correcting code (ECC) techniques are applied or a second region of the memory for which ECC techniques are not applied comprises comparing the address to at least two addresses stored in registers that correspond to boundaries of the second region of the memory.

12. The method of claim 8 wherein the processing of the memory access request comprises selecting one of a plurality of paths through a memory controller corresponding to whether or not ECC techniques are applied to the memory access.

13. The method of claim 8 wherein the second region of the memory addresses is utilized to store graphics data.

14. The method of claim 8 wherein the second region of the memory addresses reside in an expended memory region.

15. An apparatus comprising:

a first interface to communicate with processing circuitry;

a second interface to communicate with memory devices;

control circuitry coupled with the first interface and the second interface, the control circuitry to receive a memory access request having an associated address via the first interface, to determine whether the address corresponds to a first region of a memory for which error correcting code (ECC) techniques are applied or a second region of the memory for which ECC techniques are not applied, to process the memory access utilizing ECC techniques if the address corresponds to the first region of the memory, and to process the memory access without utilizing the ECC techniques if the address corresponds to the second region of the memory.

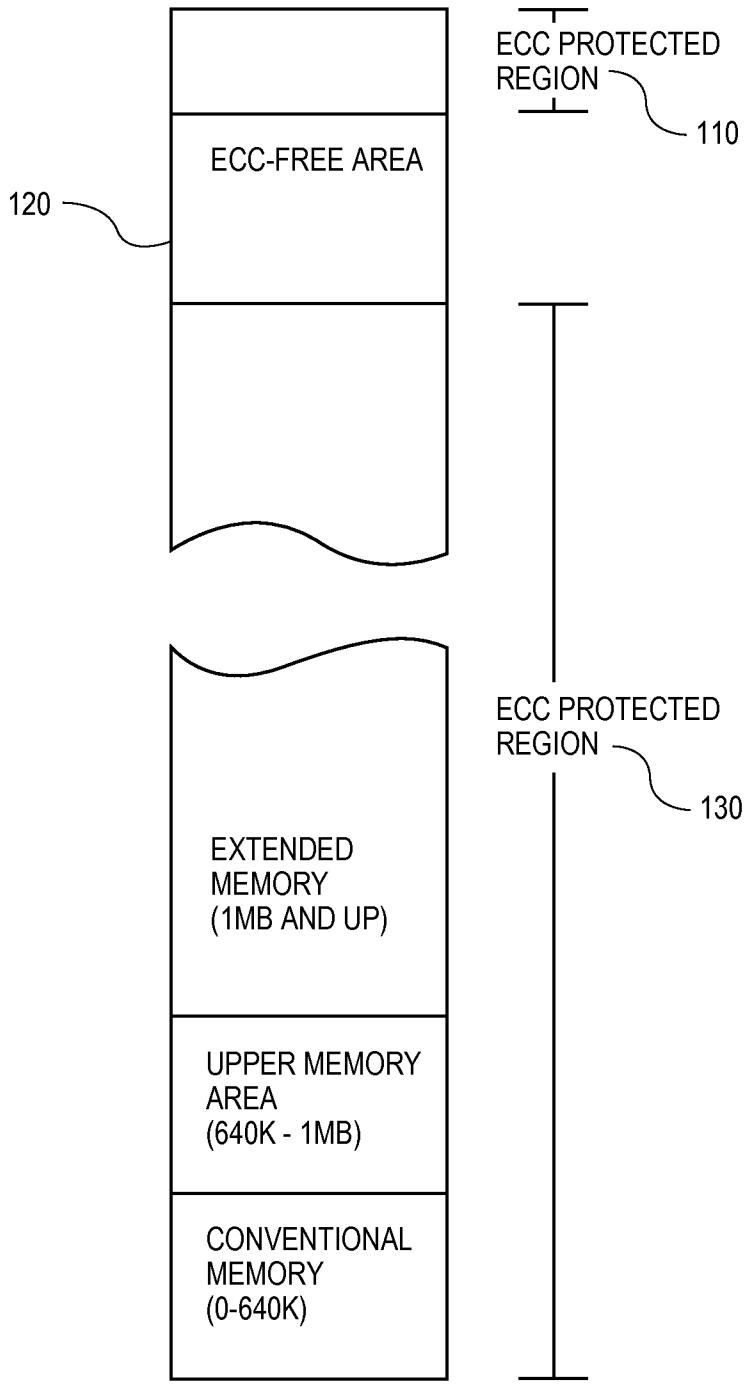
16. The apparatus of claim 15 wherein determining whether the address corresponds to a first region of a memory for which error correcting code (ECC) techniques are applied or a second region of the memory for which ECC techniques are not applied comprises comparing the address to at least two addresses stored in registers that correspond to boundaries of the second region of the memory.

17. The apparatus of claim 15 wherein the processing of the memory access request comprises selecting one of a plurality of paths through a memory controller corresponding to whether or not ECC techniques are applied to the memory access.

18. The apparatus of claim 15 wherein the second region of the memory addresses is utilized to store graphics data.

19. The apparatus of claim 15 wherein the memory devices comprise dynamic random access memory (DRAM) devices.

20. The apparatus of claim 19 wherein the DRAM devices comprise DDR-4 compliant devices.



MEMORY MAP WITH HYBRID-ECC

FIG. 1

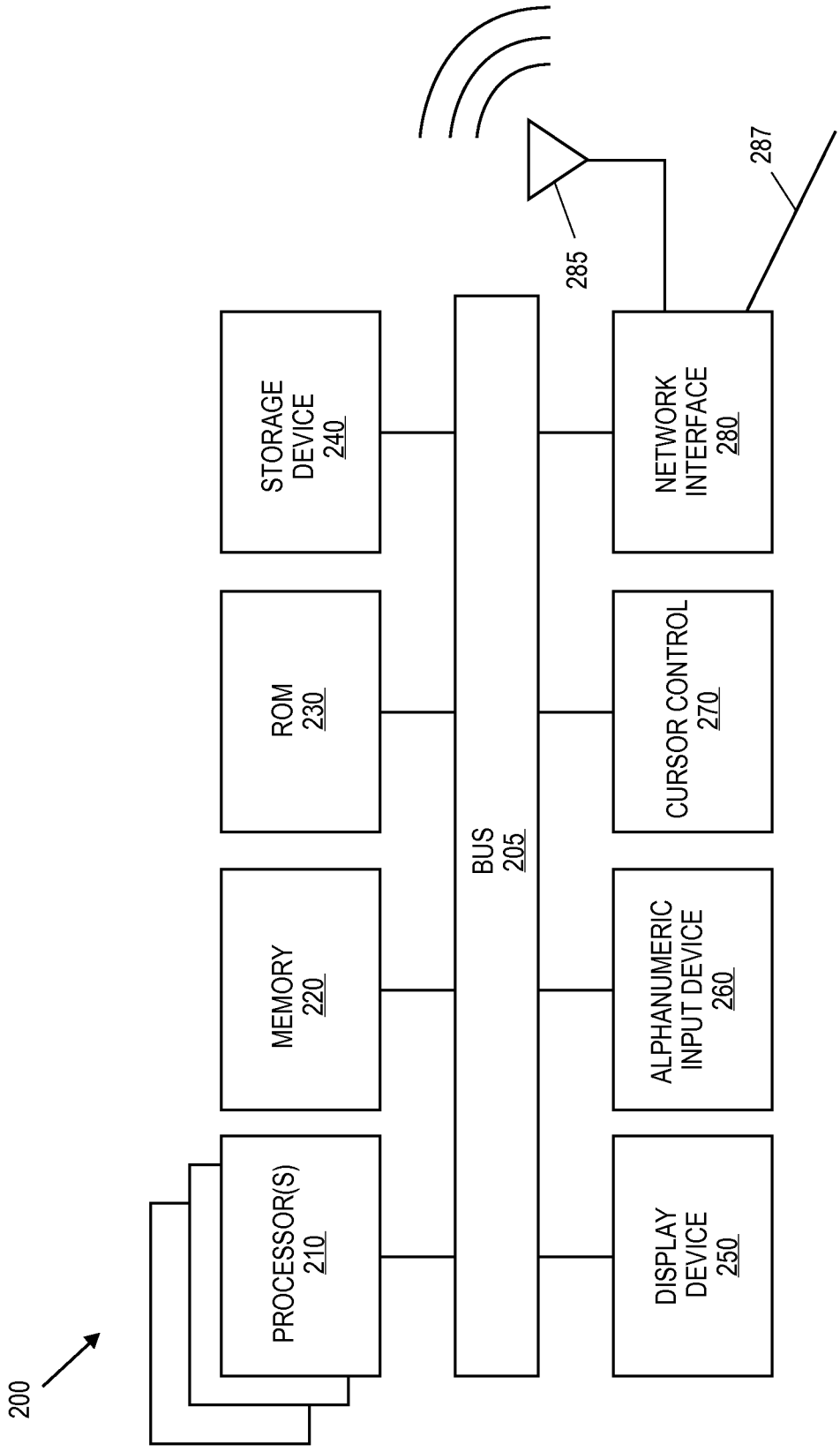

200
PROCESSOR(S)
210
MEMORY
220
ROM
230
STORAGE
DEVICE
240
BUS
205
DISPLAY
DEVICE
250
ALPHANUMERIC
INPUT DEVICE
260
CURSOR CONTROL
270
NETWORK
INTERFACE
280
285
287

FIG. 2

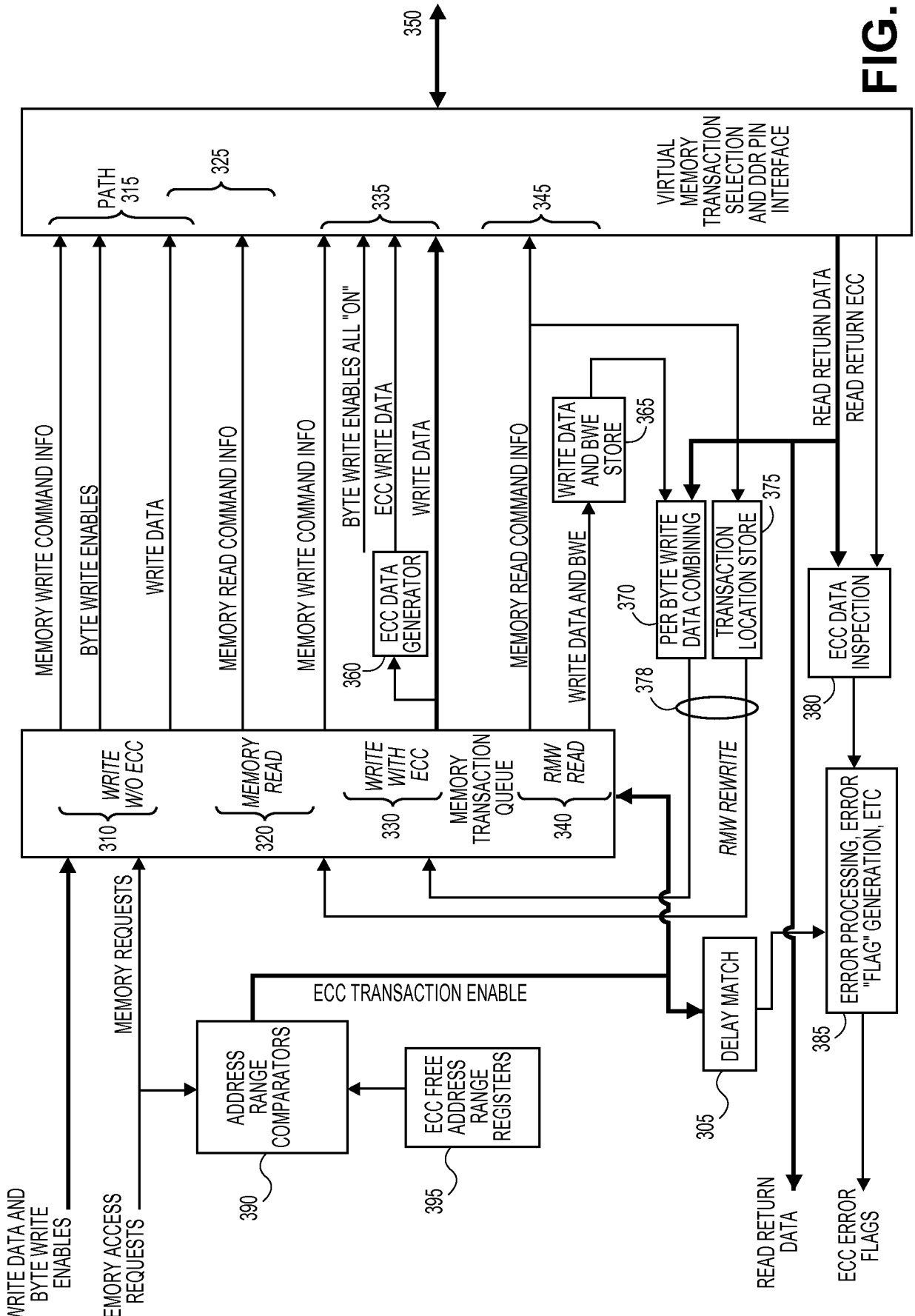

350
VIRTUAL MEMORY TRANSACTION SELECTION AND DDR PIN INTERFACE
PATH 315
325
335
345
MEMORY WRITE COMMAND INFO
BYTE WRITE ENABLES
WRITE DATA
MEMORY READ COMMAND INFO
MEMORY WRITE COMMAND INFO
BYTE WRITE ENABLES ALL "ON"
ECC WRITE DATA
WRITE DATA
MEMORY READ COMMAND INFO
WRITE DATA AND BWE
READ RETURN DATA
READ RETURN ECC
ECC DATA GENERATOR
360
WRITE DATA AND BWE STORE
365
PER BYTE WRITE DATA COMBINING
370
TRANSACTION LOCATION STORE
375
378
ECC DATA INSPECTION
380
WRITE W/O ECC
310
MEMORY READ
320
WRITE WITH ECC
330
MEMORY TRANSACTION QUEUE
RMW READ
340
RMW REWRITE
ERROR PROCESSING, ERROR "FLAG" GENERATION, ETC
385
ECC TRANSACTION ENABLE
DELAY MATCH
305
ADDRESS RANGE COMPARATORS
390
ECC FREE ADDRESS RANGE REGISTERS
395
WRITE DATA AND BYTE WRITE ENABLES
MEMORY ACCESS REQUESTS
MEMORY REQUESTS
READ RETURN DATA
ECC ERROR FLAGS

FIG. 3

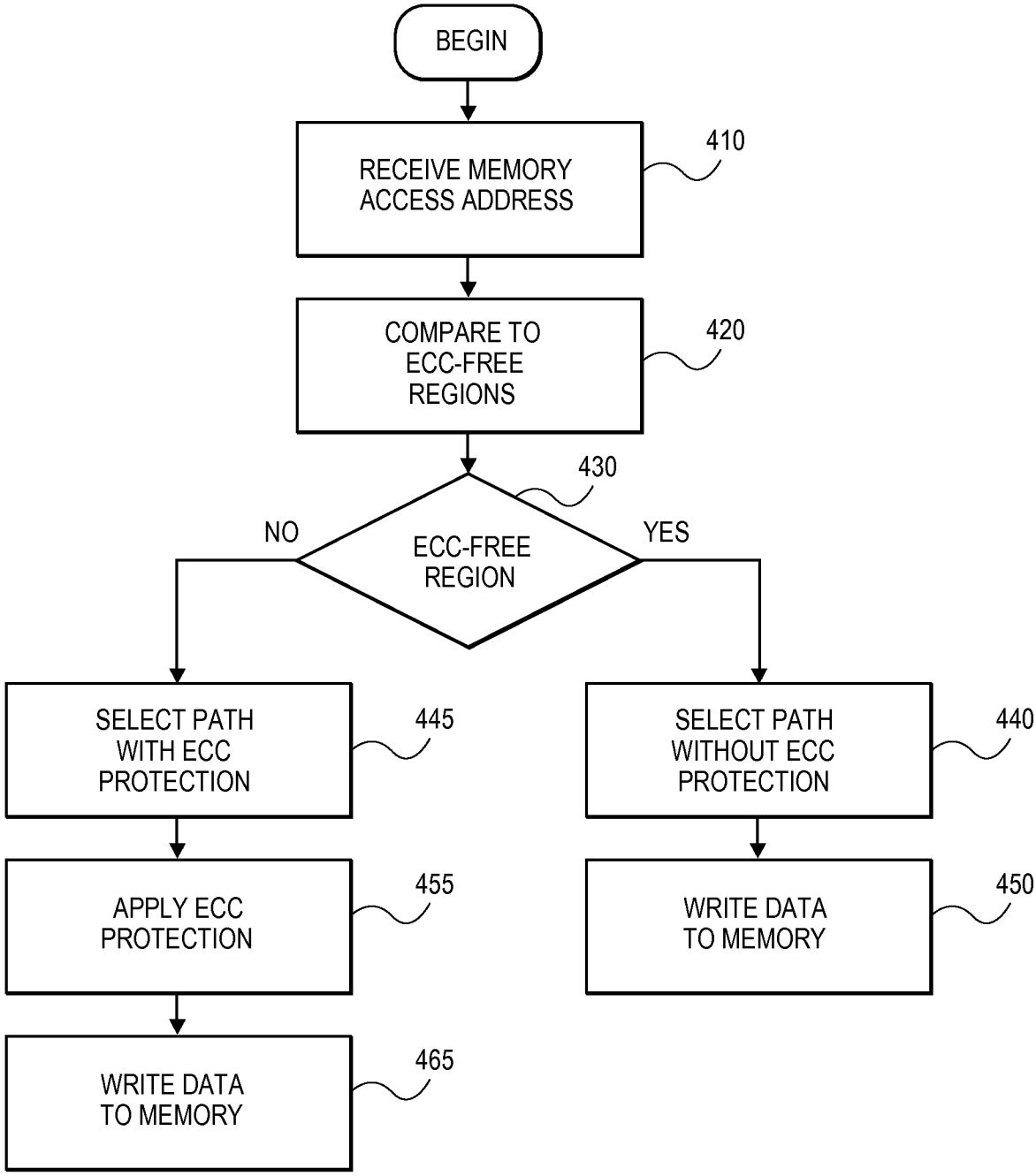

BEGIN
RECEIVE MEMORY ACCESS ADDRESS
410
COMPARE TO ECC-FREE REGIONS
420
430
ECC-FREE REGION
NO
YES
SELECT PATH WITH ECC PROTECTION
445
APPLY ECC PROTECTION
455
WRITE DATA TO MEMORY
465
SELECT PATH WITHOUT ECC PROTECTION
440
WRITE DATA TO MEMORY
450

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/031683

A. CLASSIFICATION OF SUBJECT MATTER

G06F 12/16(2006.01)i, G06F 11/10(2006.01)i, G11C 29/42(2006.01)i, G06F 13/14(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 12/16; G11C 29/42; G08C 15/00; H04Q 7/00; H03M 13/00; G06F 12/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: hybrid, error correcting code, address, path.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-0866970 B1 (SAMSUNG ELECTRONICS) 05 November 2008 See abstract, paragraphs [0028],[0035]-[0046], claims 1,3,7 and figures 1,3.	1-20
A	US 7904786 B2 (HILTON RICHARD L. et al.) 08 March 2011 See abstract, column 4 line 6 - column 5 line 4, claim 18 and figure 2.	1-20
A	US 2008-0235485 A1 (HAERTEL MICHAEL JOHN et al.) 25 September 2008 See abstract, paragraphs [0035],[0040], claim 1 and figures 3,6.	1-20
A	US 2007-0014292 A1 (HITOSHI OBATA) 18 January 2007 See abstract, paragraphs [0026],[0027],[0032], claims 7,12 and figures 3,7.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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Information on patent family members

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