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(54) Title: HYBRID SWITCHED MODE AMPLIFIER

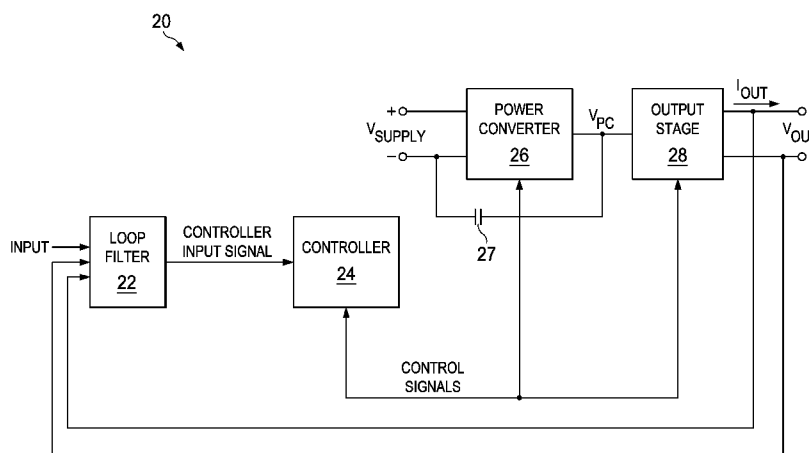


FIG. 3

(57) Abstract: A switching power stage for producing a load voltage may include a first processing path having a first output, a second processing path having a second output, a first plurality of switches comprising at least a first switch coupled between the first output and a first load terminal and a second switch coupled between the first output and the second load terminal, a second plurality of switches comprising at least a third switch coupled between the second output and the first load terminal and a fourth switch coupled between the second output and the second load terminal, and a controller configured to control switches in order to generate the load voltage as a function of an input signal such that one of the first switch and the second switch operates in a linear region of operation and one of the third switch and the fourth switch operates in a saturated region of operation for a predominance of a dynamic range of the load voltage.



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HYBRID SWITCHED MODE AMPLIFIER

RELATED APPLICATIONS

The present disclosure claims priority to United States Patent Application Serial
5 No. 15/270,631, which is a continuation-in-part of United States Patent Application Serial
No. 15/168,680, filed May 31, 2016, which claims priority to United States Provisional
Patent Application Serial No. 62/279,956, filed January 18, 2016, all of which are
incorporated by reference herein in their entirety.

FIELD OF DISCLOSURE

10 The present disclosure relates in general to circuits for audio devices, including
without limitation personal audio devices such as wireless telephones and media players,
and more specifically, to a switched mode amplifier including a switched mode converter
for driving an audio transducer of an audio device.

BACKGROUND

15 Personal audio devices, including wireless telephones, such as mobile/cellular
telephones, cordless telephones, mp3 players, and other consumer audio devices, are in
widespread use. Such personal audio devices may include circuitry for driving a pair of
20 headphones or one or more speakers. Such circuitry often includes a speaker driver
including a power amplifier for driving an audio output signal to headphones or speakers.

SUMMARY

25 In accordance with the teachings of the present disclosure, one or more
disadvantages and problems associated with existing approaches to driving an audio
output signal to an audio transducer may be reduced or eliminated.

In accordance with embodiments of the present disclosure, a switching power
stage for producing a load voltage at a load output of the switching power stage, wherein
the load output comprising a first load terminal having a first load voltage and a second
30 load terminal having a second load voltage such that the load voltage comprises a
difference between the first load voltage and the second load voltage, may include a
power converter comprising a power inductor and a first plurality of switches, wherein

the power converter is configured to drive a power converter output terminal coupled to the first load terminal in order to drive the first load terminal, a linear amplifier configured to drive a linear amplifier output terminal coupled to the second load terminal in order to drive the second load terminal, a second plurality of switches comprising at least a first switch coupled between the power converter output terminal and the first load terminal and a second switch coupled between the power converter output terminal and the second load terminal such that the power converter output terminal and the first load terminal are coupled via the first switch and the power converter output terminal and the second load terminal are coupled via the second switch, and a third plurality of switches comprising at least a third switch coupled between the linear amplifier output terminal and the first load terminal and a fourth switch coupled between the linear amplifier output terminal and the second load terminal such that the linear amplifier output terminal and the first load terminal are coupled via the third switch and the linear amplifier output terminal and the second load terminal are coupled via the fourth switch. The switching power stage may also comprise a controller configured to control the first plurality of switches, the second plurality of switches, the third plurality of switches, and the linear amplifier in order to generate the load voltage as a function of an input signal to the controller such that energy delivered to the load output is supplied predominantly by the power converter, and such that one of the first switch and the second switch operates in a linear region of operation and one of the third switch and the fourth switch operates in a saturated region of operation for a predominance of a dynamic range of the load voltage.

In accordance with these and other embodiments of the present disclosure, a method may be provided for producing a load voltage at a load output of the switching power stage, the load output comprising a first load terminal having a first load voltage and a second load terminal having a second load voltage such that the load voltage comprises a difference between the first load voltage and the second load voltage, wherein the switching power stage comprises a power converter comprising a power inductor and a first plurality of switches, wherein the power converter is configured to drive a power converter output terminal coupled to the first load terminal in order to drive the first load terminal, a linear amplifier configured to drive a linear amplifier output terminal coupled to the second load terminal in order to drive the second load terminal, a second plurality of switches comprising at least a first switch coupled between the power

converter output terminal and the first load terminal and a second switch coupled between the power converter output terminal and the second load terminal such that the power converter output terminal and the first load terminal are coupled via the first switch and the power converter output terminal and the second load terminal are coupled via the second switch, and a third plurality of switches comprising at least a third switch coupled between the linear amplifier output terminal and the first load terminal and a fourth switch coupled between the linear amplifier output terminal and the second load terminal such that the linear amplifier output terminal and the first load terminal are coupled via the third switch and the linear amplifier output terminal and the second load terminal are coupled via the fourth switch. The method may include controlling the first plurality of switches, the second plurality of switches, the third plurality of switches, and the linear amplifier in order to generate the load voltage as a function of an input signal to the controller such that energy delivered to the load output is supplied predominantly by the power converter, and such that one of the first switch and the second switch operates in a linear region of operation and one of the third switch and the fourth switch operates in a saturated region of operation for a predominance of a dynamic range of the load voltage.

In accordance with these and other embodiments of the present disclosure, a switching power stage for producing a load voltage at a load output of the switching power stage, wherein the load output comprises a first load terminal having a first load voltage and a second load terminal having a second load voltage such that the load voltage comprises a difference between the first load voltage and the second load voltage, may include a first processing path configured to process a first signal derived from an input signal to generate a first path voltage at a first processing path output, a second processing path configured to process a second signal derived from the input signal to generate a second path voltage at a second processing path output, a first plurality of switches comprising at least a first switch coupled between the first processing path output and the first load terminal and a second switch coupled between the first processing path output and the second load terminal, a second plurality of switches comprising at least a third switch coupled between the second processing path output and the first load terminal and a fourth switch coupled between the second processing path output and the second load terminal, and a controller configured to control the first plurality of switches and the second plurality of switches in order to generate the load

voltage as a function of the input signal such that one of the first switch and the second switch operates in a linear region of operation and one of the third switch and the fourth switch operates in a saturated region of operation for a predominance of a dynamic range of the load voltage.

5 In accordance with these and other embodiments of the present disclosure, a method may be provided for producing a load voltage at a load output of a switching power stage, the load output comprising a first load terminal having a first load voltage and a second load terminal having a second load voltage such that the load voltage comprises a difference between the first load voltage and the second load voltage,
10 wherein the switching power stage comprises a first processing path configured to process a first signal derived from an input signal to generate a first path voltage at a first processing path output, a second processing path configured to process a second signal derived from the input signal to generate a second path voltage at a second processing path output, a first plurality of switches comprising at least a first switch coupled between
15 the first processing path output and the first load terminal and a second switch coupled between the first processing path output and the second load terminal, and a second plurality of switches comprising at least a third switch coupled between the second processing path output and the first load terminal and a fourth switch coupled between the second processing path output and the second load terminal. The method may include
20 controlling the first plurality of switches and the second plurality of switches in order to generate the load voltage as a function of the input signal such that one of the first switch and the second switch operates in a linear region of operation and one of the third switch and the fourth switch operates in a saturated region of operation for a predominance of a dynamic range of the load voltage.

25 Technical advantages of the present disclosure may be readily apparent to one skilled in the art from the figures, description and claims included herein. The objects and advantages of the embodiments will be realized and achieved at least by the elements, features, and combinations particularly pointed out in the claims.

30 It is to be understood that both the foregoing general description and the following detailed description are examples and explanatory and are not restrictive of the claims set forth in this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

FIGURE 1 illustrates an example personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 2 illustrates a block diagram of selected components of an example audio integrated circuit of a personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 3 illustrates a block and circuit diagram of selected components of an example switched mode amplifier, in accordance with embodiments of the present disclosure;

FIGURE 4 illustrates a circuit diagram of selected components of an example boost converter that may be used to implement the power converter depicted in FIGURE 3, in accordance with embodiments of the present disclosure;

FIGURE 5 illustrates a circuit diagram of selected components of an example output stage that may be used to implement the output stage depicted in FIGURE 3, in accordance with embodiments of the present disclosure;

FIGURE 6 illustrates a graph depicting the relationship of a voltage driven by the power converter depicted in FIGURE 3 and a voltage driven by a linear amplifier of the output stage depicted in FIGURE 3 as a function of a desired output voltage, in accordance with embodiments of the present disclosure;

FIGURE 7 illustrates a circuit diagram of selected components of an example linear amplifier that may be used to implement the linear amplifier depicted in FIGURE 5, in accordance with embodiments of the present disclosure;

FIGURE 8 illustrates a circuit diagram of selected components of another example output stage that may be used to implement the second control loop depicted in FIGURE 3, in accordance with embodiments of the present disclosure; and

FIGURE 9 illustrates a circuit diagram of selected components of an example linear amplifier that may be used to implement the linear amplifier depicted in FIGURE 8, in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

FIGURE 1 illustrates an example personal audio device 1, in accordance with embodiments of the present disclosure. FIGURE 1 depicts personal audio device 1 coupled to a headset 3 in the form of a pair of earbud speakers 8A and 8B. Headset 3 depicted in FIGURE 1 is merely an example, and it is understood that personal audio device 1 may be used in connection with a variety of audio transducers, including without limitation, headphones, earbuds, in-ear earphones, and external speakers. A plug 4 may provide for connection of headset 3 to an electrical terminal of personal audio device 1. Personal audio device 1 may provide a display to a user and receive user input using a touch screen 2, or alternatively, a standard liquid crystal display (LCD) may be combined with various buttons, sliders, and/or dials disposed on the face and/or sides of personal audio device 1. As also shown in FIGURE 1, personal audio device 1 may include an audio integrated circuit (IC) 9 for generating an analog audio signal for transmission to headset 3 and/or another audio transducer.

FIGURE 2 illustrates a block diagram of selected components of an example audio IC 9 of a personal audio device, in accordance with embodiments of the present disclosure. As shown in FIGURE 2, a microcontroller core 18 may supply a digital audio input signal DIG_IN to a digital-to-analog converter (DAC) 14, which may convert the digital audio input signal to an analog signal V_{IN} . DAC 14 may supply analog signal V_{IN} to an amplifier 16 which may amplify or attenuate audio input signal V_{IN} to provide a differential audio output signal V_{OUT} , which may operate a speaker, a headphone transducer, a line level signal output, and/or other suitable output. In some embodiments, DAC 14 may be an integral component of amplifier 16. A power supply 10 may provide the power supply rail inputs of amplifier 16. In some embodiments, power supply 10 may comprise a battery. Although FIGURES 1 and 2 contemplate that audio IC 9 resides in a personal audio device, systems and methods described herein may also be applied to electrical and electronic systems and devices other than a personal audio device, including audio systems for use in a computing device larger than a personal audio device, an automobile, a building, or other structure.

FIGURE 3 illustrates a block and circuit diagram of selected components of an example switched mode amplifier 20, in accordance with embodiments of the present disclosure. In some embodiments, switched mode amplifier 20 may implement all or a

portion of amplifier 16 described with respect to FIGURE 2. As shown in FIGURE 3, switched mode amplifier 20 may comprise a loop filter 22, a controller 24, a power converter 26, and a second control loop 28.

Loop filter 22 may comprise any system, device, or apparatus configured to
5 receive an input signal (e.g., audio input signal V_{IN} or a derivative thereof) and a feedback signal (e.g., audio output signal V_{OUT} , a derivative thereof, or other signal indicative of audio output signal V_{OUT}) and based on such input signal and feedback signal, generate a controller input signal to be communicated to controller 24. In some embodiments, such controller input signal may comprise a signal indicative of an integrated error between the
10 input signal and the feedback signal. In other embodiments, such controller input signal may comprise a signal indicative of a target current signal to be driven as an output current I_{OUT} or a target voltage signal to be driven as an output voltage V_{OUT} to a load coupled to the output terminals of second control loop 28.

Controller 24 may comprise any system, device, or apparatus configured to, based
15 on an input signal (e.g., input signal INPUT), output signal V_{OUT} , and/or other characteristics of switched mode amplifier 20, control switching of switches integral to power converter 26, switches integral to second control loop 28, and/or one or more linear amplifiers integral to second control loop 28, in order to transfer electrical energy from a power supply V_{SUPPLY} to the load of switched-mode amplifier 20 in accordance with the
20 input signal.

Power converter 26 may receive at its input a voltage V_{SUPPLY} (e.g., provided by power supply 10), and may generate at its output a voltage V_{PC} . In some embodiments, voltage V_{SUPPLY} may be received via input terminals including a positive input terminal and a negative input terminal which may be coupled to a ground voltage. As described in
25 greater detail in this disclosure (including, without limitation, in reference to FIGURE 4, below), power converter 26 may comprise a power inductor and a plurality of switches that are controlled by control signals received from controller 24 in order to convert voltage V_{SUPPLY} to voltage V_{PC} , such that audio output signal V_{OUT} generated from voltage V_{PC} is a function of the input signal to loop filter 22. Also as shown in FIGURE
30 3, a capacitor 27 may be coupled between a second supply terminal (which may in some embodiments be coupled to ground) and the power converter output terminal. However,

in other embodiments, capacitor 27 may be coupled between a first supply terminal and the power converter output terminal.

Turning briefly to FIGURE 4, a non-limiting example of a single-ended switching mode power supply which may be used to implement power converter 26 is described. FIGURE 4 illustrates a circuit diagram of selected components of an example buck converter 40 that may be used to implement power converter 26 depicted in FIGURE 3, in accordance with embodiments of the present disclosure. As shown in FIGURE 4, buck converter 40 may include a power inductor 42, switches 44, 46, 47, and 49 and capacitor 27 arranged as shown. In operation, controller 24 may be configured to, when non-inverting buck-boost converter 40 is used to implement power converter 26, control switches 44, 46, 47, and 49 such that power converter output voltage V_{PC} is a function of the controller input signal provided to controller 24.

Turning again to FIGURE 3, second control loop 28 may receive at its input the power converter output voltage V_{PC} , and may generate at its output audio output signal V_{OUT} . As described in greater detail in this disclosure (including, without limitation, in reference to FIGURES 5A and 5B, below), second control loop 28 may comprise at least one linear amplifier and, in some embodiments, a plurality of switches, wherein the at least one linear amplifier and the plurality of switches, if present, are controlled by control signals received from controller 24 in order to convert power converter output voltage V_{PC} to audio output signal V_{OUT} , such that audio output signal V_{OUT} is a function of the input signal to loop filter 22.

FIGURE 5 illustrates a circuit diagram of selected components of an example output stage 28A that may be used to implement second control loop 28 depicted in FIGURE 3, in accordance with embodiments of the present disclosure. As shown in FIGURE 5, power converter 26 may drive power converter output voltage V_{PC} . Output stage 28A may comprise a plurality of switches including switch 64 coupled between the power converter output and a first output terminal of output stage 28A and switch 66 coupled between the power converter output and a second output terminal of output stage 28A. In addition, second control loop 28 may include a linear amplifier 60 (an example of which is depicted in FIGURE 7) configured to drive a linear amplifier output voltage V_{AMP} . Output stage 28A may also include a plurality of switches including switch 68 coupled between the output of linear amplifier 60 and a first output terminal of output

stage 28A and switch 70 coupled between the output of linear amplifier 60 and a second output terminal of output stage 28A.

In operation of output stage 28A, controller 24 may activate switches 64 and 70 and deactivate switches 66 and 68 for positive values of audio output signal V_{OUT} and
 5 activate switches 66 and 68 and deactivate switches 64 and 70 for negative values of audio output signal V_{OUT} . Controller 24 may, as power converter output voltage V_{PC} approaches the lower saturation limit, cause linear amplifier 60 to drive a non-zero linear amplifier output voltage V_{AMP} in order to increase a common mode voltage between the first output terminal and the second output terminal, allowing audio output signal V_{OUT} to
 10 approach and cross zero. Above the lower saturation limit of power converter output voltage V_{PC} , controller 24 may cause linear amplifier 60 to drive an approximately zero linear amplifier output voltage V_{AMP} such that a magnitude of audio output signal V_{OUT} is equal to power converter output voltage V_{PC} .

In other words, controller 24 may control power converter 26 and linear amplifier
 15 60 to generate voltages in accordance with the following functions, which are graphically depicted in FIGURE 6, and wherein voltage V_{TGT} represents a target or desired voltage to be output as audio output signal V_{OUT} as indicated by the input signal to controller 24:

$$\begin{aligned} V_{PC} &= V_{TGT}; \text{ for } |V_{TGT}| > V_{SAT} \\ V_{PC} &= V_{SAT}; \text{ for } |V_{TGT}| \leq V_{SAT} \\ V_{AMP} &= 0; \text{ for } |V_{TGT}| > V_{SAT} \\ V_{AMP} &= V_{SAT} - V_{TGT}; \text{ for } |V_{TGT}| \leq V_{SAT} \end{aligned}$$

20 In some embodiments, an offset voltage may be added to each of the output of power converter 26 and the output of linear amplifier 60, to ensure that the voltage $V_{AMP} > 0$ at all times.

Accordingly, presence of linear amplifier 60 and its ability to increase the common mode voltage of the output terminals in response to low magnitudes of the
 25 output signal V_{OUT} may minimize non-linearities of output signal V_{OUT} as a function of the input signal received by controller 24, and permit crossing a magnitude of zero by audio output signal V_{OUT} .

FIGURE 7 illustrates a circuit diagram of selected components of an example linear amplifier 71A that may be used to implement linear amplifier 60 depicted in
 30 FIGURE 5, in accordance with embodiments of the present disclosure. As shown in

FIGURE 7, linear amplifier 71A may include a first stage 74 and a second stage 76. First stage 74 may comprise a gain stage 78 having a transconductance gain G_m to convert a voltage signal INPUT received from controller 24 to a current I_E .

Second stage 76 may comprise a totem-pole topology with an input at a gate terminal of n-type field effect transistor (NFET) 80 and an output node shared by the drain terminal of NFET 82 of source terminal of NFET 80 at which linear amplifier 71A drives linear amplifier output voltage V_{AMP} . In such topology, NFET 80 may source current into a load coupled to the output node and NFET 82 may sink current from such load. A local current feedback loop may be arranged with respect to NFET 82 in order to regulate a minimum level of quiescent current through NFET 80. Thus, second stage 76 may be viewed as a source follower having a unity gain from its input node (e.g. gate terminal of NFET 80) to its output node.

Within the current feedback loop of second stage 76, a current-sensing amplifier 84 may sense a current associated with NFET 80 generating a scaled current to be compared with a reference current I_{REF} , resulting in an error current equal to the difference between the scaled current and reference current I_{REF} . A gain booster stage 86 may receive the error current and operate as a current mirror to compensate for loss of loop gain due to the current sensing scheme of current-sensing amplifier 84. At the output of gain booster stage 86, a conventional Miller-compensated common-source output scheme may be applied for stability as long as NFET 82 remains in its saturation region, which may be maintained by keeping its drain-to-source voltage V_{DS} being greater than a saturation voltage V_{d_sat} . For example, when drain-to-source voltage V_{ds} becomes less than V_{d_sat} for a given drain-to-source voltage I_{ds} of NFET 82, an output drain impedance of NFET 82 may decrease, and a voltage gain of NFET 82 will decrease accordingly. Consequently, the current loop gain and unity-gain bandwidth of the local current feedback loop may decrease. When such an amplifier is integral to a high-order feedback loop, reduction of unity-gain bandwidth may lead to system instability and must be avoided. Therefore, gain-compensator 88 may be present and may include a variable current gain as a function of drain-to-source voltage of NFET 82, which in the first order can be translated to an output impedance of NFET 82.

FIGURE 8 illustrates a circuit diagram of selected components of another example output stage 28B that may be used to implement second control loop 28 depicted

in FIGURE 3, in accordance with embodiments of the present disclosure. Output stage 28B of FIGURE 8 may be similar in many respects to output stage 28A of FIGURE 5, and thus, only the main differences between output stage 28B and output stage 28A are discussed in detail. One main difference between output stage 28B and output stage 28A is that in output stage 28B, linear amplifier 60, switch 64, switch 66, switch 68, and/or switch 70 may be integral to a final output stage of a differential amplifier 72.

To further illustrate, FIGURE 9 illustrates a circuit diagram of an example linear amplifier 71B which may be used to implement portions of the example output stage 28B depicted in FIGURE 8, in accordance with embodiments of the present disclosure. As one of skill in the relevant art may recognize, linear amplifier 71B may comprise the differential-output analog to the single-ended topology of linear amplifier 71A depicted in FIGURE 7, and analogous components of linear amplifier 71B have the same reference numerals as that of linear amplifier 71A with an additional letter "A" or "B" added to the reference numerals. In some embodiments, one or more of NFETs 80A, 80B, 82A, and 82B may be equivalent to switches 64, 66, 68, and 70, respectively, of output stage 28B of FIGURE 8.

In these and other embodiments, additional circuitry may be present to cause the gate-to-source voltage of switch 66 and/or 64 to be at or greater than supply voltage(s) in order to operate as a switch (e.g., activate and deactivate). In these and other embodiments, switch 70 and/or 68 may operate in the linear region of such devices, wherein the gate-to-source voltage of such devices is less than the supply voltage.

In light of the foregoing, in operation, switches 68 and 70 of example output stage 28B may be viewed as ground-referenced devices in a first differential amplifier and switches 64 and 66 may be viewed as supply voltage-referenced devices of a second differential amplifier example output stage 28B. When viewed in such manner, the behavior of the amplifier described herein operates to control polarity and magnitude of output voltage V_{OUT} by operating such first and second differential amplifiers such that, when implemented as transistors (e.g., n-type metal-oxide-semiconductor field-effect transistors), one switch in each of the differential amplifiers may operate in its saturation region while the remaining switch in each of the differential amplifiers may operate in its linear region. For example, when switch 64 operates in its saturated region, switch 66 may operate in its linear region, and vice versa. When switch 68 operates in its saturated

region, switch 70 may operate in its linear region, and vice versa. Because of this behavior, non-idealities (such as high-frequency switching ripple) may be divided between such differential amplifiers such that the predominance of ripple is seen by one switch in each such differential amplifier.

5 In the foregoing discussion, embodiments are disclosed in which a capacitor 27 is coupled between the power converter output terminal and one of a first supply terminal having a first voltage and a second supply terminal having a second voltage, and embodiments are disclosed in which a capacitor 62 is coupled between the first load terminal and the second load terminal of switched mode amplifier 20. However, in these
10 and other embodiments, a capacitor may be coupled between the first load terminal of switched mode amplifier 20 and one of the first supply terminal and the second supply terminal. In addition, in these and other embodiments, a capacitor may be coupled between the second load terminal of switched mode amplifier 20 and one of the first supply terminal and the second supply terminal.

15 As used herein, a “switch” may comprise any suitable device, system, or apparatus for making a connection in an electric circuit when the switch is enabled (e.g., activated, closed, or on) and breaking the connection when the switch is disabled (e.g., deactivated, open, or off) in response to a control signal received by the switch. For purposes of clarity and exposition, control signals for switches described herein are not
20 depicted although such control signals would be present to selectively enable and disable such switches. In some embodiments, a switch may comprise a metal-oxide-semiconductor field-effect transistor (e.g., an n-type metal-oxide-semiconductor field-effect transistor).

As used herein, when two or more elements are referred to as “coupled” to one
25 another, such term indicates that such two or more elements are in electronic communication or mechanical communication, as applicable, whether connected indirectly or directly, with or without intervening elements.

This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in
30 the art would comprehend. Similarly, where appropriate, the appended claims encompass all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in the art would comprehend.

Moreover, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative.

All examples and conditional language recited herein are intended for pedagogical objects to aid the reader in understanding the invention and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present inventions have been described in detail, it should be understood that various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the disclosure.

WHAT IS CLAIMED IS:

1. A switching power stage for producing a load voltage at a load output of the switching power stage, the load output comprising a first load terminal having a first
5 load voltage and a second load terminal having a second load voltage such that the load voltage comprises a difference between the first load voltage and the second load voltage, the switching power stage comprising:

10 a power converter comprising a power inductor and a first plurality of switches, wherein the power converter is configured to drive a power converter output terminal coupled to the first load terminal in order to drive the first load terminal;

a linear amplifier configured to drive a linear amplifier output terminal coupled to the second load terminal in order to drive the second load terminal;

15 a second plurality of switches, comprising at least a first switch coupled between the power converter output terminal and the first load terminal and a second switch coupled between the power converter output terminal and the second load terminal such that the power converter output terminal and the first load terminal are coupled via the first switch and the power converter output terminal and the second load terminal are coupled via the second switch;

20 a third plurality of switches, comprising at least a third switch coupled between the linear amplifier output terminal and the first load terminal and a fourth switch coupled between the linear amplifier output terminal and the second load terminal such that the linear amplifier output terminal and the first load terminal are coupled via the third switch and the linear amplifier output terminal and the second load terminal are coupled via the fourth switch; and

25 a controller configured to control the first plurality of switches, the second plurality of switches, the third plurality of switches, and the linear amplifier in order to generate the load voltage as a function of an input signal to the controller such that energy delivered to the load output is supplied predominantly by the power converter, and such that one of the first switch and the second switch
30 operates in a linear region of operation and one of the third switch and the fourth

switch operates in a saturated region of operation for a predominance of a dynamic range of the load voltage.

2. The switching power stage of Claim 1, further comprising a capacitor
5 coupled between the first load terminal and the second load terminal.

3. The switching power stage of Claim 1, further comprising a capacitor
coupled between the first load terminal and one of a first supply terminal having a first
voltage and a second supply terminal having a second voltage.
10

4. The switching power stage of Claim 3, wherein a second terminal of the
power inductor is coupled to the power converter output terminal.

5. The switching power stage of Claim 3, wherein the first plurality of
15 switches comprises:

a first switch coupled between a second terminal of the power inductor and the
power converter output terminal; and

a second switch coupled between the second terminal of the power inductor and
the second supply terminal.
20

6. The switching power stage of Claim 1, further comprising:
a first capacitor coupled between the power converter output terminal and one of a
first supply terminal having a first voltage and a second supply terminal having a second
voltage; and

25 a second capacitor coupled between the second load terminal and one of the first
supply terminal and the second supply terminal.

7. The switching power stage of Claim 1, wherein the first plurality of switches comprises:

a fifth switch coupled between a first terminal of the power inductor and a first supply terminal having a first voltage; and

5 a sixth switch coupled between the first terminal of the power inductor and a second supply terminal having a second voltage.

8. The switching power stage of Claim 7, wherein the first plurality of switches further comprises:

10 a seventh switch coupled between a second terminal of the power inductor and the power converter output terminal; and

an eighth switch coupled between the second terminal of the power inductor and the second supply terminal.

15 9. The switching power stage of Claim 1, wherein the controller further controls the first plurality of switches to drive the first load voltage as a function of a target output voltage which is a function of the input signal.

20 10. The switching power stage of Claim 9, wherein the function of the target output voltage includes a magnitude of the target output voltage.

11. The switching power stage of Claim 9, wherein the function of the target output voltage includes a lower saturation limit of the power converter output terminal.

25 12. The switching power stage of Claim 11, wherein the controller further controls the linear amplifier to drive a non-zero voltage as the second load voltage in order to increase a common mode voltage of the first load terminal and the second load terminal when the power converter output terminal is driven to the lower saturation limit in order to produce the output voltage as a function of an input signal to the controller
30 while minimizing non-linearities of the output voltage as a function of the input signal.

13. The switching power stage of Claim 1, wherein the controller further controls the linear amplifier to drive the second load voltage as a function of a target output voltage which is a function of the input signal.

5 14. A method for producing a load voltage at a load output of the switching power stage, the load output comprising a first load terminal having a first load voltage and a second load terminal having a second load voltage such that the load voltage comprises a difference between the first load voltage and the second load voltage, wherein the switching power stage comprises:

10 a power converter comprising a power inductor and a first plurality of switches, wherein the power converter is configured to drive a power converter output terminal coupled to the first load terminal in order to drive the first load terminal;

a linear amplifier configured to drive a linear amplifier output terminal
15 coupled to the second load terminal in order to drive the second load terminal;

a second plurality of switches, comprising at least a first switch coupled between the power converter output terminal and the first load terminal and a second switch coupled between the power converter output terminal and the second load terminal such that the power converter output terminal and the first
20 load terminal are coupled via the first switch and the power converter output terminal and the second load terminal are coupled via the second switch; and

a third plurality of switches, comprising at least a third switch coupled between the linear amplifier output terminal and the first load terminal and a fourth switch coupled between the linear amplifier output terminal and the second
25 load terminal such that the linear amplifier output terminal and the first load terminal are coupled via the third switch and the linear amplifier output terminal and the second load terminal are coupled via the fourth switch;

wherein the method comprises controlling the first plurality of switches, the second plurality of switches, the third plurality of switches, and the linear amplifier in
30 order to generate the load voltage as a function of an input signal to the controller such that energy delivered to the load output is supplied predominantly by the power converter, and such that one of the first switch and the second switch operates in a linear region of

operation and one of the third switch and the fourth switch operates in a saturated region of operation for a predominance of a dynamic range of the load voltage.

15 15. The method of Claim 14, further comprising a capacitor coupled between the first load terminal and the second load terminal.

10 16. The method of Claim 14, further comprising a capacitor coupled between the first load terminal and one of a first supply terminal having a first voltage and a second supply terminal having a second voltage.

17. The method of Claim 16, wherein a second terminal of the power inductor is coupled to the power converter output terminal.

15 18. The method of Claim 16, wherein the first plurality of switches comprises:
a first switch coupled between a second terminal of the power inductor and the power converter output terminal; and
a second switch coupled between the second terminal of the power inductor and the second supply terminal.

20 19. The method of Claim 14, further comprising:
a first capacitor coupled between the power converter output terminal and one of a first supply terminal having a first voltage and a second supply terminal having a second voltage; and
a second capacitor coupled between the second load terminal and one of the first
25 supply terminal and the second supply terminal.

20. The method of Claim 14, wherein the first plurality of switches comprises:
a fifth switch coupled between a first terminal of the power inductor and a first supply terminal having a first voltage; and
30 a sixth switch coupled between the first terminal of the power inductor and a second supply terminal having a second voltage.

21. The method of Claim 20, wherein the first plurality of switches further comprises:

a seventh switch coupled between a second terminal of the power inductor and the power converter output terminal; and

5 an eighth switch coupled between the second terminal of the power inductor and the second supply terminal.

22. The method of Claim 14, wherein the controller further controls the first plurality of switches to drive the first load voltage as a function of a target output voltage
10 which is a function of the input signal.

23. The method of Claim 22, wherein the function of the target output voltage includes a magnitude of the target output voltage.

15 24. The method of Claim 23, wherein the function of the target output voltage includes a lower saturation limit of the power converter output terminal.

25. The method of Claim 24, wherein the controller further controls the linear amplifier to drive a non-zero voltage as the second load voltage in order to increase a
20 common mode voltage of the first load terminal and the second load terminal when the power converter output terminal is driven to the lower saturation limit in order to produce the output voltage as a function of an input signal to the controller while minimizing non-linearities of the output voltage as a function of the input signal.

25 26. The method of Claim 14, wherein the controller further controls the linear amplifier to drive the second load voltage as a function of a target output voltage which is a function of the input signal.

27. A switching power stage for producing a load voltage at a load output of the switching power stage, the load output comprising a first load terminal having a first load voltage and a second load terminal having a second load voltage such that the load voltage comprises a difference between the first load voltage and the second load voltage,
5 the switching power stage comprising:

a first processing path configured to process a first signal derived from an input signal to generate a first path voltage at a first processing path output;

a second processing path configured to process a second signal derived from the input signal to generate a second path voltage at a second processing path output;

10 a first plurality of switches, comprising at least a first switch coupled between the first processing path output and the first load terminal and a second switch coupled between the first processing path output and the second load terminal;

a second plurality of switches, comprising at least a third switch coupled between the second processing path output and the first load terminal and a fourth switch coupled
15 between the second processing path output and the second load terminal; and

a controller configured to control the first plurality of switches and the second plurality of switches in order to generate the load voltage as a function of the input signal such that one of the first switch and the second switch operates in a linear region of operation and one of the third switch and the fourth switch operates in a saturated region
20 of operation for a predominance of a dynamic range of the load voltage.

28. A method for producing a load voltage at a load output of a switching power stage, the load output comprising a first load terminal having a first load voltage and a second load terminal having a second load voltage such that the load voltage
25 comprises a difference between the first load voltage and the second load voltage, wherein the switching power stage comprises a first processing path configured to process a first signal derived from an input signal to generate a first path voltage at a first processing path output, a second processing path configured to process a second signal derived from the input signal to generate a second path voltage at a second processing
30 path output, a first plurality of switches, comprising at least a first switch coupled between the first processing path output and the first load terminal and a second switch coupled between the first processing path output and the second load terminal, and a

second plurality of switches, comprising at least a third switch coupled between the second processing path output and the first load terminal and a fourth switch coupled between the second processing path output and the second load terminal, the method comprising:

- 5 controlling the first plurality of switches and the second plurality of switches in order to generate the load voltage as a function of the input signal such that one of the first switch and the second switch operates in a linear region of operation and one of the third switch and the fourth switch operates in a saturated region of operation for a predominance of a dynamic range of the load voltage.

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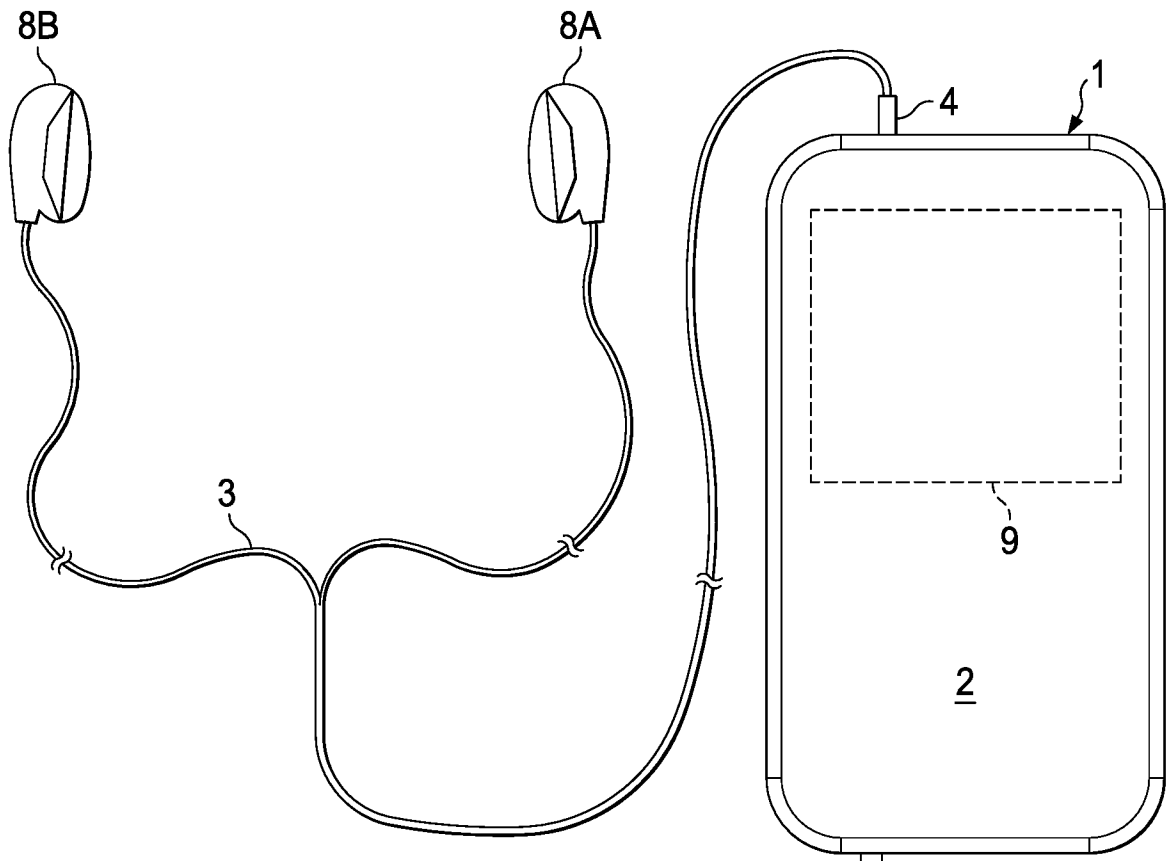


FIG. 1

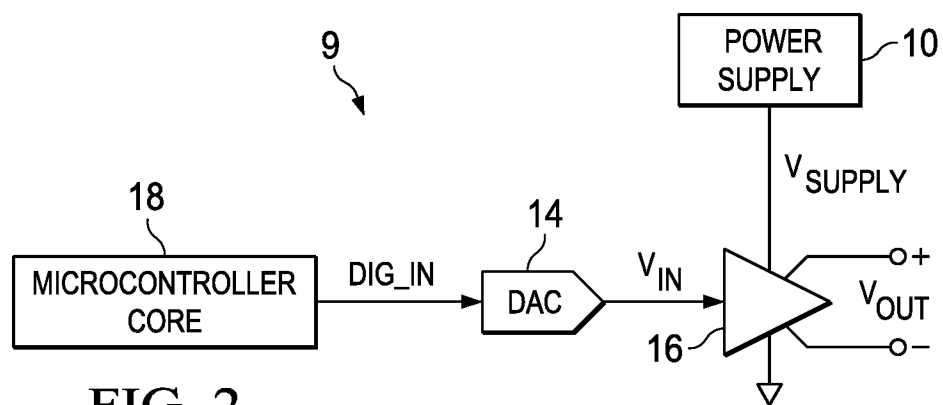


FIG. 2

20 ↗

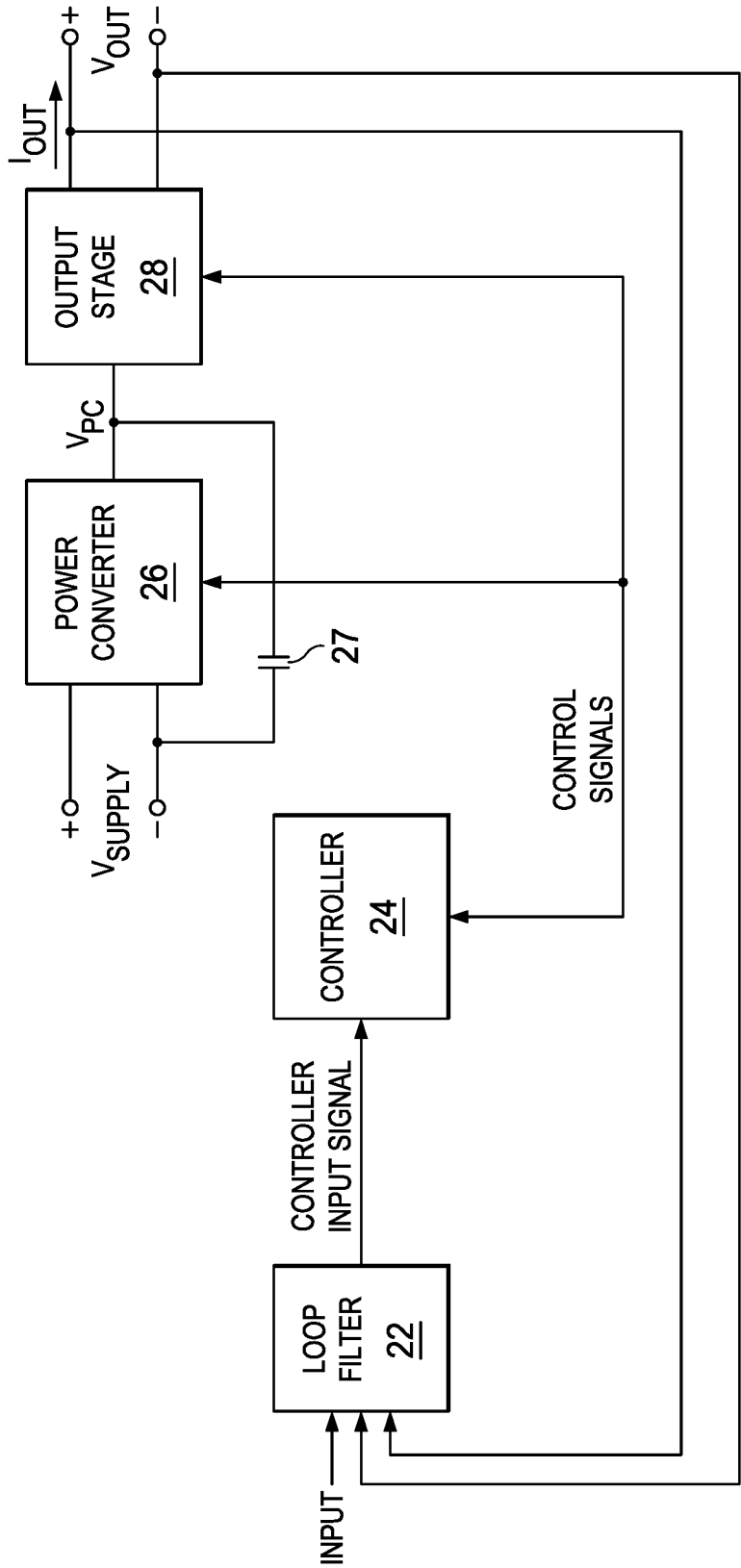


FIG. 3

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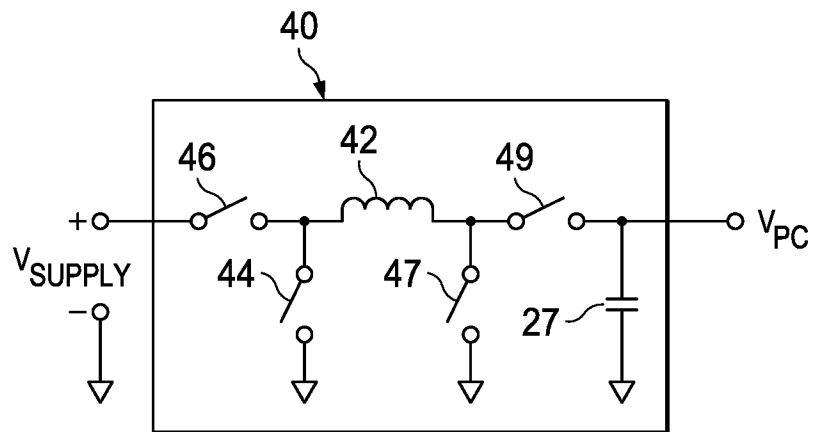


FIG. 4

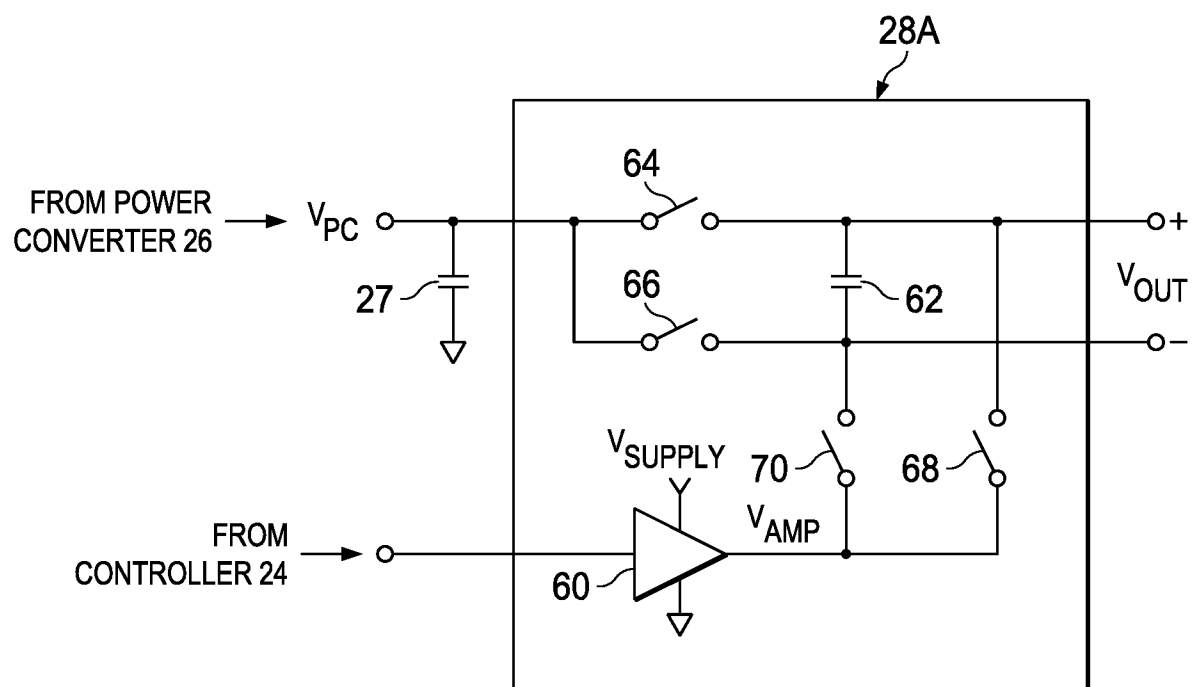


FIG. 5

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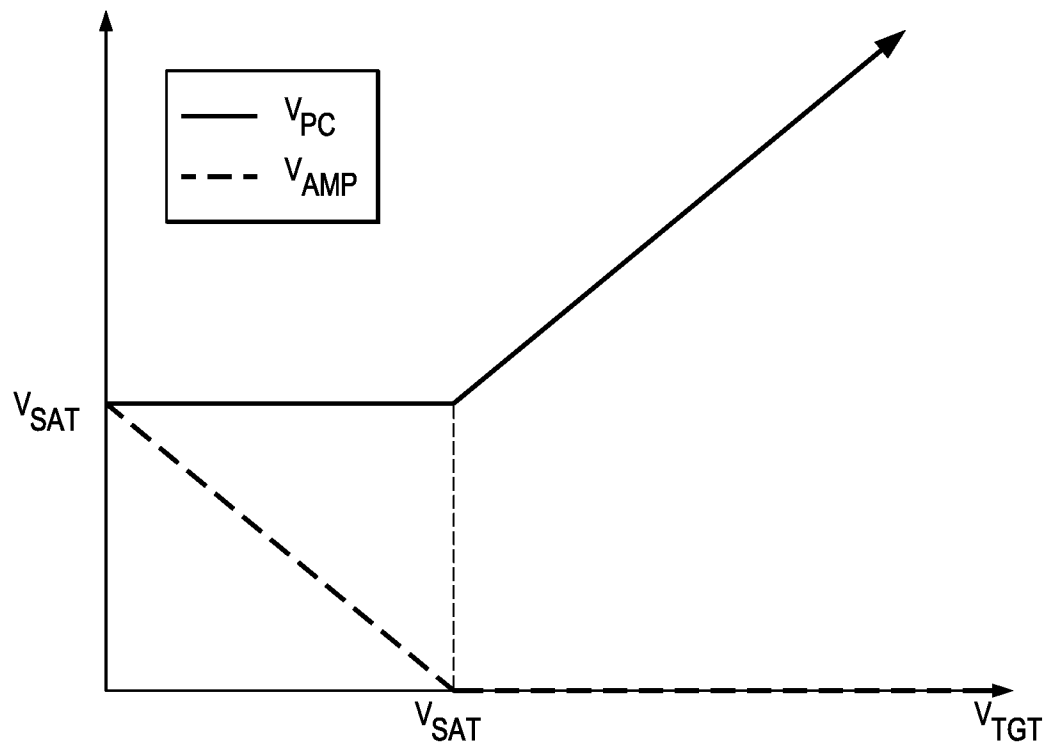


FIG. 6

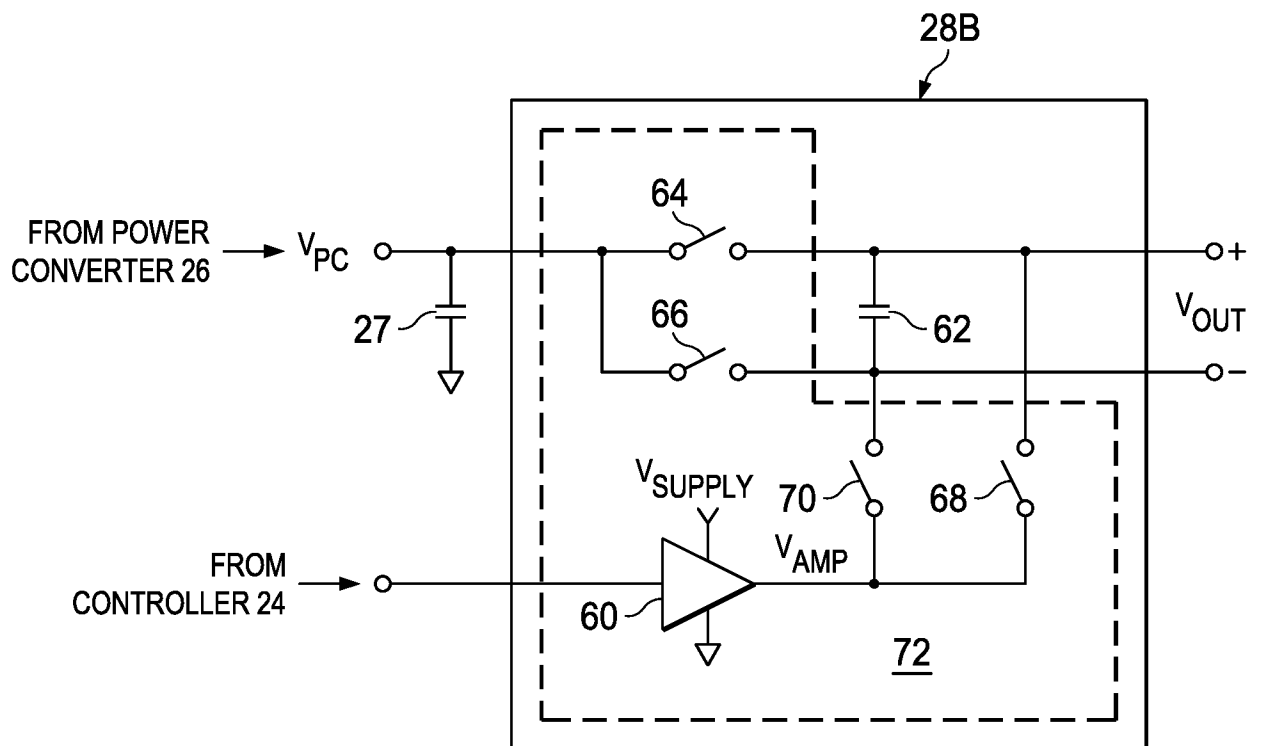


FIG. 8

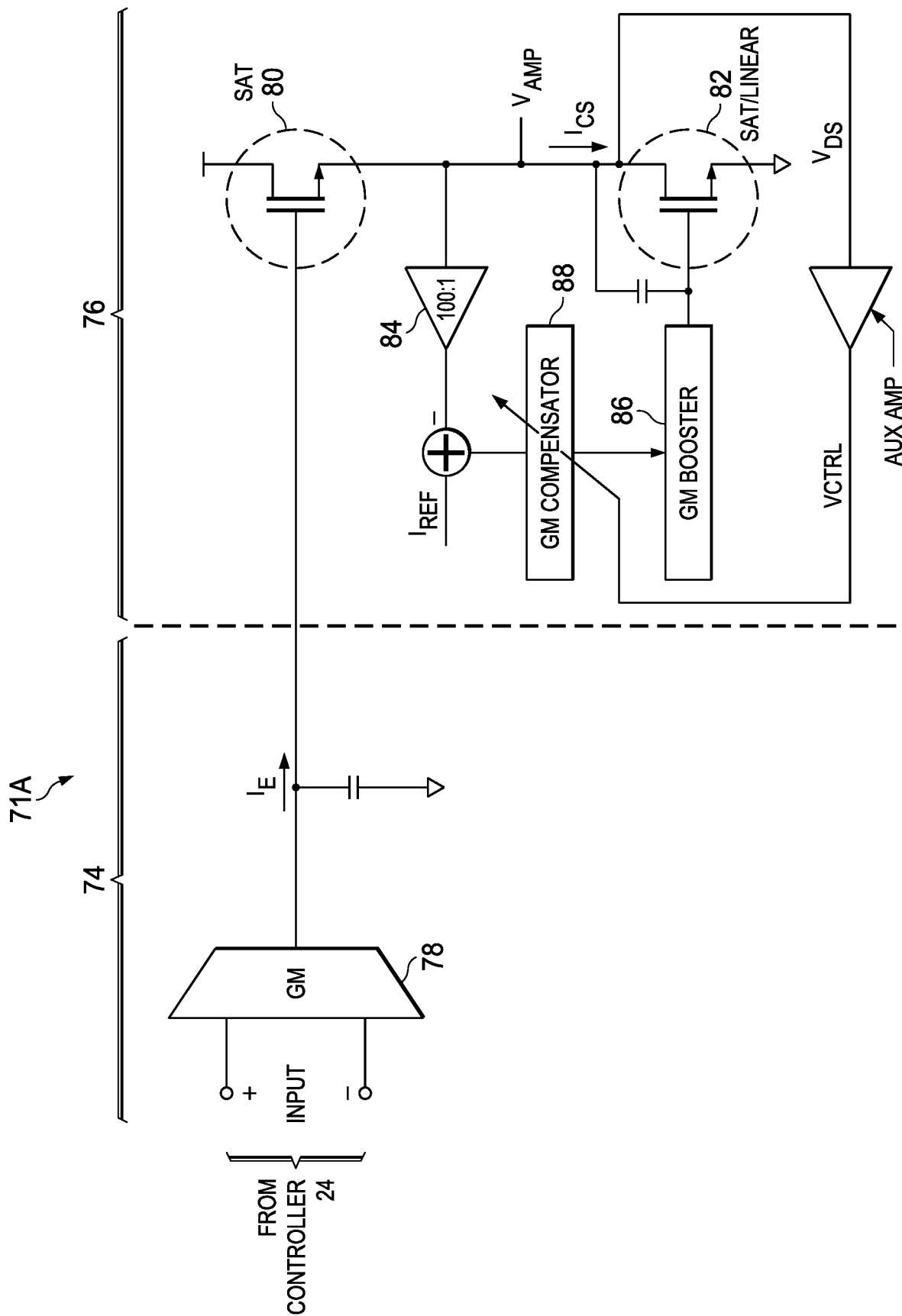
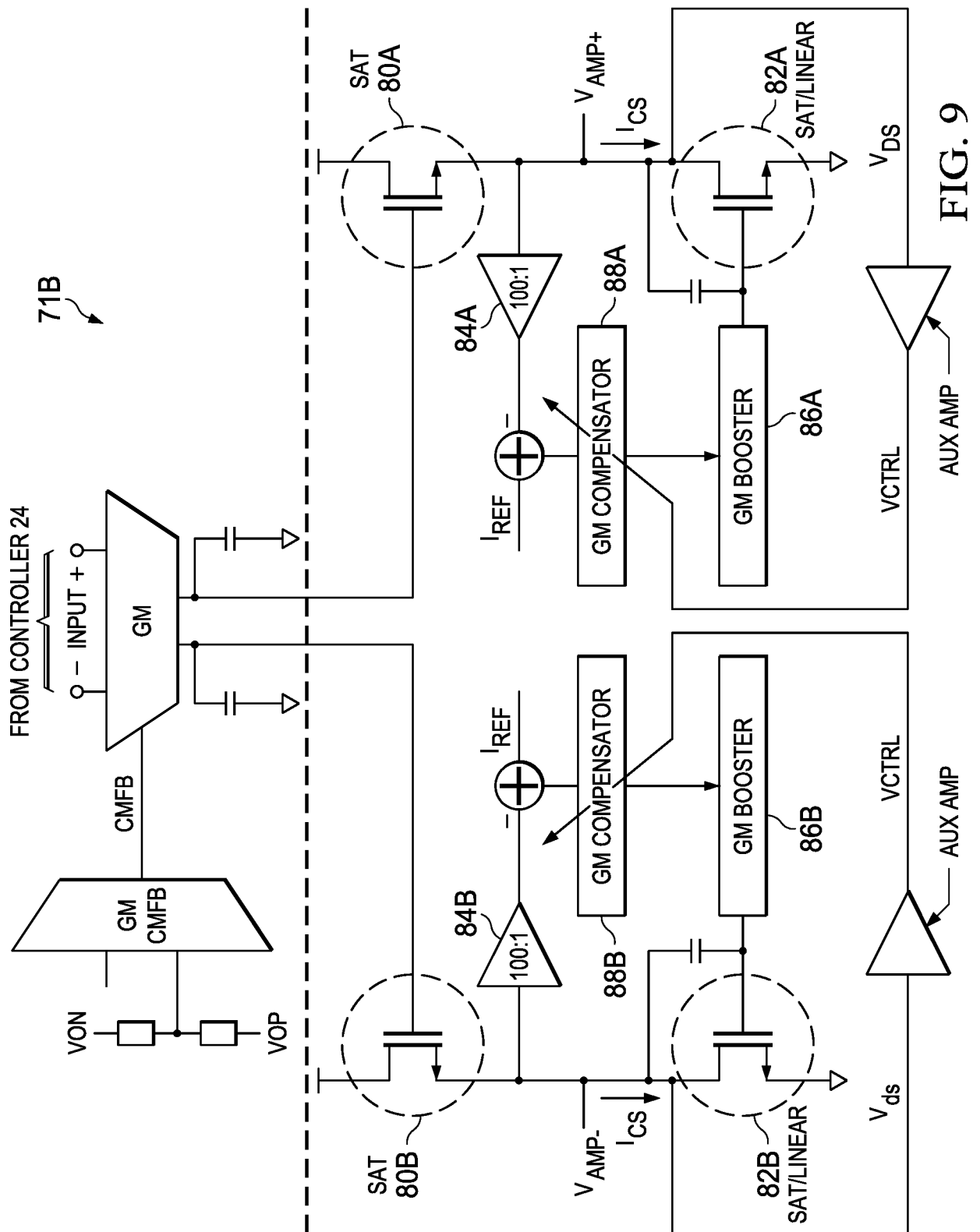


FIG. 7



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/013756

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/217
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	----- WO 2007/136800 A2 (CIRRAS LOGIC INC [US]; MAZDA BABAK [US]; SHINKRE RAHUL [US]; SAHANDIES) 29 November 2007 (2007-11-29) paragraph [0010] - paragraph [0015]; figure 1	1-28
A	----- US 2015/222184 A1 (MELANSON JOHN L [US] ET AL) 6 August 2015 (2015-08-06) paragraph [0064] - paragraph [0069]; figure 12	1-28



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

18 May 2017

Date of mailing of the international search report

30/05/2017

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Lorenzo, Carlos

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2017/013756

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