



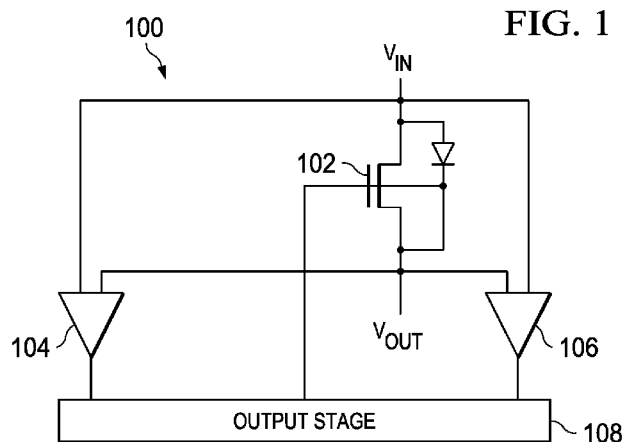
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Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) Title: A LOW POWER IDEAL DIODE CONTROL CIRCUIT



(57) Abstract: In described examples of a circuit (100) that operates as a low-power ideal diode, the circuit (100) includes a p-channel transistor (102) connected to receive an input voltage (V_{IN}) on a first terminal and to provide an output voltage (V_{OUT}) on a second terminal, a first amplifier (106) connected to receive the input voltage and the output voltage and to provide a first signal that dynamically biases a gate of the p-channel transistor (102) as a function of the voltage across the p-channel transistor, and a second amplifier (104) connected to receive the input voltage and the output voltage and to provide a second signal that operates to turn off the gate of the p-channel transistor (102) responsive to the input voltage (V_{IN}) being less than the output voltage (V_{OUT}).

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A LOW POWER IDEAL DIODE CONTROL CIRCUIT

[0001] This relates generally to the field of circuit design, and more particularly to a circuit, chip and method that controls a transistor to provide the functionality of an ideal diode having both fast forward recovery and fast reverse recovery.

BACKGROUND

[0002] In low power applications that require a diode, the forward voltage drop of the diode can create either supply headroom issues or excessive power dissipation. A Schottky diode can reduce this voltage drop, but Schottky diodes are unavailable in many semiconductor processes. To avoid these issues, a single transistor can be used in place of the diode, with the gate voltage of the transistor controlled to operate as an ideal diode. A so-called “ideal diode” circuit has a fast forward drop recovery and a fast reverse recovery with low voltage headroom for very low power applications.

SUMMARY

[0003] In described examples, an ideal diode circuit may include low power, low voltage operation, fast reverse recovery speed, and fast forward recovery speed.

[0004] In one example of a circuit that operates as a low-power ideal diode, the circuit includes: a p-channel transistor connected to receive an input voltage on a first terminal and to provide an output voltage on a second terminal; a first amplifier connected to receive the input voltage at a first input and the output voltage at a second input and to provide a first signal that dynamically biases a gate of the p-channel transistor as a function of the voltage across the p-channel transistor; and a second amplifier connected to receive the input voltage at a first input and the output voltage at a second input and to provide a second signal that operates to turn off the gate of the p-channel transistor responsive to the input voltage being less than the output voltage.

[0005] In another example, a power management chip includes: a first connection for a first power supply having a first voltage; a second connection for a second power supply having a second voltage higher than the first voltage; and an internal power rail for the chip. The first power supply and the second power supply are each connected to the internal power rail through

a circuit including: a p-channel transistor connected to receive an input voltage on a first terminal and to provide an output voltage on a second terminal; a first amplifier connected to receive the input voltage at a first input and the output voltage at a second input and to provide a first signal that dynamically biases a gate of the p-channel transistor as a function of the voltage across the p-channel transistor; and a second amplifier connected to receive the input voltage at a first input and the output voltage at a second input and to provide a second signal that operates to turn off the gate of the p-channel transistor responsive to the input voltage being less than the output voltage.

[0006] Advantages of the disclosed circuit may include one or more of the following: low power, low voltage operation, quick recovery in the forward direction, quick recovery the reverse direction, and small area. At least one example of the disclosed circuit is in an all complementary metal-oxide semiconductor (CMOS) design.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 illustrates an example of a circuit that operates as a low-power ideal diode according to an embodiment.

[0008] FIG. 2 illustrates a specific implementation of the circuit of FIG. 1 according to an embodiment.

[0009] FIG. 3 depicts the diode characteristics of the circuit of FIG. 2 in terms of voltage and current.

[0010] FIG. 4 depicts the transient diode characteristics of the circuit of FIG. 2.

[0011] FIG. 5 depicts overlapping regions of operation of the circuit of FIG. 1.

[0012] FIG. 6 depicts a chip that incorporates the circuit of FIG. 1 according to an embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0013] A diode's primary purpose is to allow current in a single direction. Ideally, this means zero forward biased voltage drop, zero reverse current, and zero equivalent series resistance when forward biased. The closest approximation of these ideals can be achieved by using a single transistor as a switch, and controlling the gate voltage as a function of the voltage across it. Several timing issues are also important in the optimal operation of an ideal diode. For example, if a diode is conducting in a forward condition and is immediately switched to a reverse condition, the diode will conduct in a reverse direction for a short time as the forward voltage

bleeds off. The current through the diode will be fairly large in a reverse direction during this small recovery time, known as reverse recovery time. After the carriers have been flushed and the diode is operating as a normal blocking device in the reversed condition, the current flow should drop to leakage levels. Similarly, forward recovery time is the time required for the voltage to reach a specified value after a large change in forward biasing. Preferably, both the reverse recovery time and the forward recovery time are minimized.

[0014] FIG. 1 shows a circuit 100 that operates as a low-power ideal diode according to an embodiment. A transistor 102 receives an input voltage V_{IN} on a first terminal and provides an output voltage V_{OUT} on a second terminal. The body of transistor 102, as created, contains two parasitic diodes facing in opposite directions. However, in the example of FIG. 1, the gate of transistor 102 has been connected to the body to short circuit one of the parasitic diodes, so only one diode is shown. Transistor 102 is the main pass transistor, and its gate is controlled to operate as a diode. Amplifier 104 is connected to receive V_{IN} and V_{OUT} as inputs and to provide an output to output stage 108. Similarly, amplifier 106 is also connected to receive V_{IN} and V_{OUT} as inputs and to provide an output to output stage 108. An output of stage 108 is then connected to control the gate of transistor 102. In at least one embodiment, output stage 108 is simply a node that combines the outputs of amplifiers 104 and 106. In one example, output stage 108 is a circuit that receives the outputs of amplifiers 104 and 106 in a manner that smooths the operation of transistor 102. To achieve the goal of an ideal amplifier, amplifier 104 is configured to provide a shortened turn-off time for transistor 102 whenever V_{OUT} becomes greater than V_{IN} , and amplifier 106 is configured to dynamically bias the gate of transistor 102 as a function of the voltage across transistor 102. Accordingly, if V_{OUT} drops (e.g., due to a change in load), amplifier 106 will adjust the gate of transistor 106 to follow the changing needs.

[0015] Referring to FIG. 2, circuit 200 is a specific implementation of circuit 100. In at least one embodiment, circuit 200 is implemented in CMOS technology. However, it can also be realized in other technologies, such as bipolar junction transistors. Reference to CMOS technology or to component elements (such as n-channel MOS (NMOS) and p-channel MOS (PMOS) technology) is often a misnomer, because the “metal” in CMOS circuits can be replaced with doped polysilicon, and the “oxide” can be replaced with other passivation layers. Accordingly, any reference to CMOS, NMOS and PMOS in this disclosure refers more generally to any related type of transistor technology, such as insulated-gate field-effect (IGFET) or

metal-insulator–semiconductor FET (MISFET). In circuit 200, transistor M5 is a PMOS transistor that is controlled to operate as a diode. Like transistor 102, M5 receives V_{IN} at a first terminal and provides V_{OUT} at a second terminal. As shown in FIG. 2, the source of M5 is connected to V_{OUT} , and its drain is connected to V_{IN} . The transistor is shown this way, because V_{OUT} can sometimes be greater than V_{IN} , which is the reason that M5 is to operate as a diode for preventing the backflow of current. The source and drain of M5 can be viewed as interchangeable, depending on whether V_{IN} or V_{OUT} is higher. The gate of M5 is connected to the source of M5 (as shown) through resistor R1 and is also connected to the source of PMOS transistor M6. As in FIG. 1, the gate of M5 is connected to the body of M5 to short circuit one parasitic diode, so that only the parasitic diode shown is active. In at least one embodiment, the threshold voltage of the parasitic diode of M5 is approximately 0.7 volts. This threshold is too high for use in low-power situations, such as on portable devices, which typically operate on 3-5 volts. Thus, M5 is controlled to have a much lower threshold voltage.

[0016] M0 is a diode-connected PMOS transistor having a source connected to V_{IN} and a drain connected through current source CS1 to a lower rail, herein referred to as ground. The gate of M0 is tied to the gates of PMOS transistors M1 and M2 to form a common-gate amplifier. M1 has a source connected to V_{OUT} and a drain connected between the source of M6 and the gate of M5. M2 also has a source connected to V_{OUT} . The drain of M2 is connected to the gate of M6. Transistor M6 has a source connected to M5, a drain connected to ground, and a gate that receives input from M2, M8 and R0, where R0 is connected between V_{OUT} and the drain of NMOS transistor M8. The source of M8 is connected to ground. Diode-connected PMOS transistor M3 has a source connected to V_{OUT} and has a drain connected through current source CS2 to ground. PMOS transistor M4 has a source connected to V_{IN} and has a drain connected to the drain of diode-connected NMOS transistor M9. The source of M9 is connected to ground. The gates of M3 and M4 are connected together to form an operational transconductance amplifier (OTA). The gates of M8 and M9 are connected to mirror the current output from M4 and provide a voltage to M6.

[0017] In the disclosed embodiment, M0, M1 and M2 together form amplifier 204, which (like amplifier 104 of FIG. 1) operates to speed up the turn-off of transistor M5 when V_{OUT} becomes greater than V_{IN} . Likewise, M3, M4 and M9 form amplifier 206, which (like amplifier 106 of FIG. 1) operates to dynamically bias the gate of M5 as a function of the voltage across M5.

Transistors M6 and M8 together with resistors R0 and R1 form output stage 208, which combines the outputs of amplifiers 204, 206 to provide a smooth operation for M5. In one example, M3, M4, M9, M8, R0 and M6 are defined as part of a forward regulating loop, while M0, M1 and M2 form a reverse blocking speed-up loop that aids in the shut-off speed of M5.

[0018] In operation of circuit 200, referring to output stage 208, the gate of M5 is controlled by: (a) M6, which can pull the gate of M5 towards ground when M6 is on; and (B) M1, which can pull the gate of M5 upwards towards V_{OUT} when M1 is on. The degree to which M6 is turned on is determined by three elements, namely: (a) R0 will always pull the gate of M6 towards V_{OUT} ; (b) M8, when turned on, will pull the gate of M6 towards ground; and (c) M2, when turned on, will assist in pulling the gate of M6 towards V_{OUT} .

[0019] When V_{IN} is greater than V_{OUT} and current is flowing in a forward direction through M5, amplifier 206 operates as follows to ensure quick forward recovery. M3 operates as a floating reference voltage for amplifier 206, such that M4 essentially sees the voltage across M5. If V_{OUT} goes low suddenly, the gate of M3 is pulled downward and will pull down on the gate of M4. M4 will then have a large gate/source voltage V_{GS} , and will quickly allow increased current to M9, which also increases the voltage on the gate of M9. The gate of M9 will mirror the increased voltage on the gate of M8, so that M8 will turn on more fully. Turning on M8 will pull downward on the gate of M5, thereby turning M6 on more strongly, which ultimately turns on M5 more strongly, providing the additional power needed. When V_{OUT} becomes greater than V_{IN} , the reverse will happen, with M4 being shut off, which in turn shuts off M9 and M8. With M8 turned off, R0 will eventually pull the gate of M6 to V_{OUT} and turn off both M6 and M5, although by itself R0 operates more slowly than desired. This is the time when the action of amplifier 204 becomes useful.

[0020] In amplifier 204, M0 operates as a floating reference voltage, so that M1 and M2 both see the voltage across M5. If V_{OUT} is greater than V_{IN} , the source of both M1 and M2 goes high, while their respective gates remain low because of the connection to the gate of M0. The low gate voltages and high source voltages turn both M1 and M2 on strongly, allowing more current to flow. M1 pulls the source of M6 towards V_{OUT} , and M2 helps to pull the gate of M6 towards V_{OUT} , which operates to turn off M6 and M5. Because of the action of amplifier 204, M5 is able to turn off much more quickly than would happen with only R0 pulling up on the gate.

[0021] In this embodiment, the forward regulating loop is controlled by the differential pair

M3/M4, and the load is R0. This loop can be made output pole dominant with low impedance at the source of M6 and with R0 reducing effective impedance at the drain of M8, and a large decoupling capacitor on V_{OUT}. In this circuit, one characteristic of the forward loop is the fast forward recovery to heavy load steps. The reverse recovery speed-up loop in this circuit is not activated under normal forward bias conditions, but only when the voltage on V_{OUT} increases above V_{IN}. No current flows from V_{OUT} to ground when V_{OUT} is greater than V_{IN}.

[0022] FIG. 3 illustrates the DC current-voltage (I-V) curve characteristics of the embodiment of FIG. 2. The current through M5 is zero for all negative voltages in region D of the curve, which is when V_{OUT} is greater than V_{IN}. As V_{IN} becomes greater than V_{OUT}, the current remains zero in region A until the threshold voltage, V_{TH} is reached at approximately 30 millivolts. By comparison, the threshold voltage of a regular diode in this technology would be approximately 700 millivolts. Thus, the disclosed circuit is useful in situations where voltage headroom is a concern or where power loss due to current flowing through a real diode is a concern. V_{TH} is determined by the transconductance of differential pair M3, M4 times the resistance of R0. Above V_{TH}, the current rises at a first rate in region B until the transistor is fully turned on. After the transistor is fully turned on (e.g., in region C), the slope of the I-V curve is a second value that is equal to the inverse of the drain/source resistance (i.e., 1/RDS_{on}). The current to run the disclosed circuit is taken from either the input current or the output current and can be very low power. In at least one implementation, the quiescent current supply (I_{DDQ}) for the circuit is approximately 1.25 μA. Thus, in at least some implementations, the quiescent current supply is in the micro-amp range. The circuitry can be pushed even lower if needed, depending on design requirements (e.g., into the nano-amp range).

[0023] FIG. 4 illustrates the transient characteristics of the ideal diode that is enabled by the disclosed embodiments. As shown in the lower graph, the output voltage V_{OUT} of the embodiment of FIG. 2 was switched from approximately 3.265 V to 3.33 V while the input voltage V_{IN} was held at 3.3 V (not shown). After 0.5 milliseconds, the output voltage was dropped back to its former level. The current response through ideal diode M5 is shown in the upper graph. As the reverse voltage was applied, a reverse current appeared, peaking at around 42 mA, but within 0.020 ms, the reverse current fell to zero. When the reverse voltage condition was removed, the current returned to previous levels. No undershooting occurred in the voltage during recovery, even though this is a common problem in ideal diode circuits.

[0024] FIG. 5 illustrates the region of operation 500 of both amplifiers 204 and 206 in one embodiment and plots the I-V graph for each of those amplifiers, where the voltage is measured as $V_{IN} - V_{OUT}$. FIG. 5 is not drawn to scale and is offered simply to illustrate that operation of these two amplifier circuits will overlap. The dotted line represents the curve for amplifier 204, and the solid line represents the curve for amplifier 206. As shown in FIG. 5, when the difference in voltages is in the negative region (i.e., V_{OUT} is greater than V_{IN}), only amplifier 204 operates. As the voltage difference becomes more positive, the current from amplifier 204 drops, and the current from amplifier 206 starts to grow, such that both amplifiers are operating at the same time. Finally, a point is reached where amplifier 204 is completely turned off and only amplifier 206 is active. This handoff between amplifier 204 and amplifier 206 provides a smooth operation of the circuit as a whole. The actual curve for each amplifier circuit is determined by the threshold voltages of the transistors in each circuit and the transconductance of the devices.

[0025] In example embodiments, the control circuitry has many applications, such as: (a) zero reverse current switch; (b) ideal diode OR-ing of multiple power sources with very little power loss (important in many low power battery operated devices); and (c) inside a low dropout (LDO) feedback loop to block any reverse current into the supply of the LDO.

[0026] FIG. 6 illustrates the use of the disclosed ideal diode circuit in a larger circuit within an integrated circuit (IC) chip 600. The circuit shown in IC chip 600 uses PMOS based ideal diodes 602A, 602B to create a single, diode-ORed internal power rail 604 from either: (a) VBUS, which connects to a cable (in the case of dead battery); or (b) VIN, the system power supply at 3.3 V, with priority given to VIN. Notably, all low voltage elements can be used in ideal diode 602B, because this diode appears on the low voltage side of LDO regulator 606. FIG. 6 discloses two diode-ORed inputs. However, this is not a limitation, because this approach can be scaled to an unlimited number of input supplies.

[0027] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit comprising:
 - a p-channel transistor connected to receive an input voltage on a first terminal and to provide an output voltage on a second terminal;
 - a first amplifier connected to receive the input voltage at a first input and the output voltage at a second input and to provide a first signal that dynamically biases a gate of the p-channel transistor as a function of the voltage across the p-channel transistor; and
 - a second amplifier connected to receive the input voltage at a first input and the output voltage at a second input and to provide a second signal that operates to turn off the gate of the p-channel transistor responsive to the input voltage being less than the output voltage.
2. The circuit of claim 1 wherein a region of operation of the first amplifier overlaps a region of operation of the second amplifier.
3. The circuit of claim 2 further comprising a shared output stage connected to receive the first signal and the second signal and to control the gate of the p-channel transistor.
4. The circuit of claim 3, wherein the p-channel transistor is a first p-channel transistor, and wherein the shared output stage includes a second p-channel transistor connected to pull the gate of the first p-channel transistor towards a lower rail when the second p-channel transistor is turned on, the gate of the second p-channel transistor receiving input from the first amplifier and the second amplifier.
5. The circuit of claim 4 wherein the first amplifier includes a third p-channel transistor having a source connected to the output voltage and a fourth p-channel transistor having a source connected to the input voltage, the third and fourth p-channel transistors forming an operational transconductance amplifier (OTA) that provides an output to a first n-channel transistor that mirrors a gate voltage of the first n-channel transistor to the output stage.
6. The circuit of claim 5 wherein the third p-channel transistor is a floating DC voltage reference.
7. The circuit of claim 5 wherein the second amplifier includes a fifth, a sixth and a seventh p-channel transistor forming a common-gate amplifier, the fifth p-channel transistor having a source connected to the input voltage and the sixth and seventh p-channel transistors each having a source connected to the output voltage.

8. The circuit of claim 7 wherein the fifth p-channel transistors is a floating DC voltage reference.
9. The circuit of claim 8 wherein the sixth p-channel transistor has a drain connected to pull the gate of the first p-channel transistor towards the output voltage when on and the seventh p-channel transistor has a drain connected to pull the gate of the second p-channel transistor towards the output voltage when on.
10. The circuit of claim 9 wherein the shared output stage further includes a first resistor coupled between the output voltage and a drain of a first n-channel transistor, the source of the first n-channel transistor being tied to the lower rail, wherein the gate of the second p-channel transistor is connected to a point between the first resistor and the first n-channel transistor.
11. The circuit of claim 10 wherein the shared output stage further includes a second resistor connected between the gate and the second terminal of the first p-channel transistor.
12. The circuit of claim 2 wherein the circuit is embodied in complementary metal-oxide semiconductor (CMOS) technology.
13. The circuit of claim 2 wherein the quiescent current in the circuit is less than approximately 1.25 μA .
14. The circuit of claim 2 wherein no current flows from V_{OUT} to the lower rail when V_{OUT} is greater than V_{IN} .
15. The circuit of claim 1 wherein the circuit is configured to operate as a low-power ideal diode.
16. A power management chip comprising:
 - a first connection for a first power supply having a first voltage;
 - a second connection for a second power supply having a second voltage different than the first voltage; and
 - an internal power rail for the chip, wherein the first power supply and the second power supply are each connected to the internal power rail through a circuit including: a p-channel transistor connected to receive an input voltage on a first terminal and to provide an output voltage on a second terminal; a first amplifier connected to receive the input voltage at a first input and the output voltage at a second input and to provide a first signal that dynamically biases a gate of the p-channel transistor as a function of the voltage across the p-channel transistor; and a second amplifier connected to receive the input voltage at a first input and the

output voltage at a second input and to provide a second signal that operates to turn off the gate of the p-channel transistor responsive to the input voltage being less than the output voltage.

17. The power management chip of claim 16 wherein the power management chip is a USB Type-C and USB-PD port power management chip.

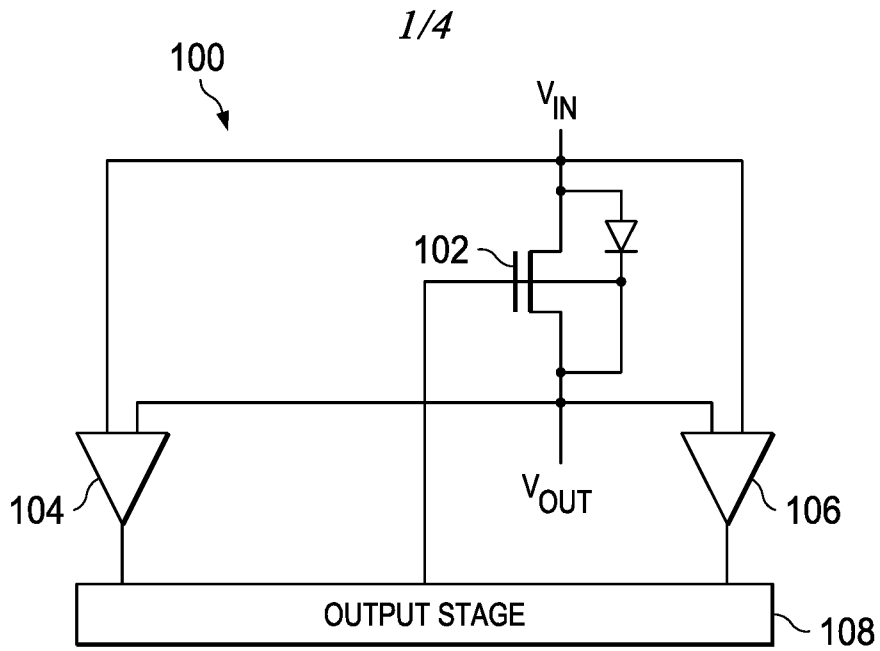


FIG. 1

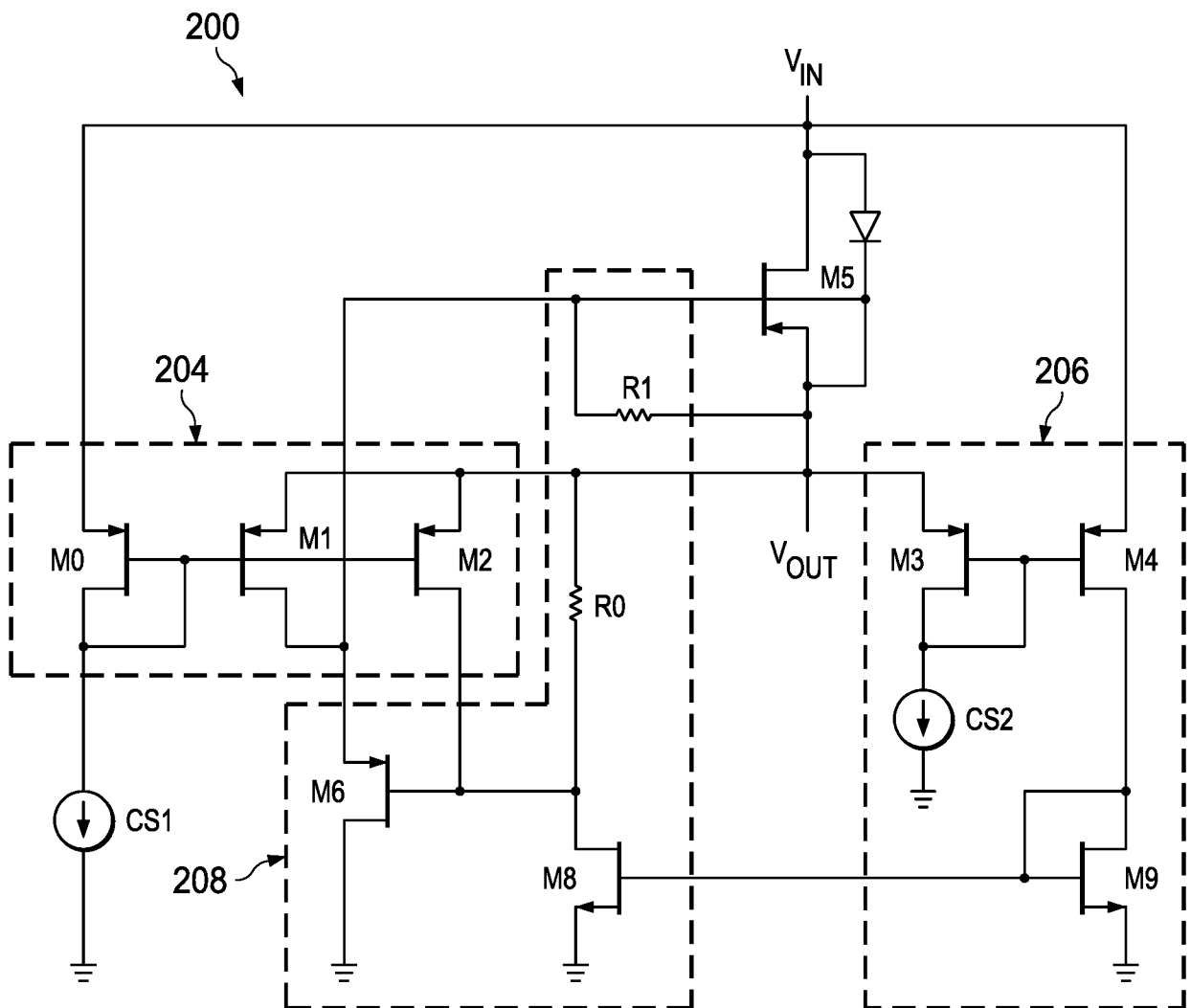


FIG. 2

FIG. 3

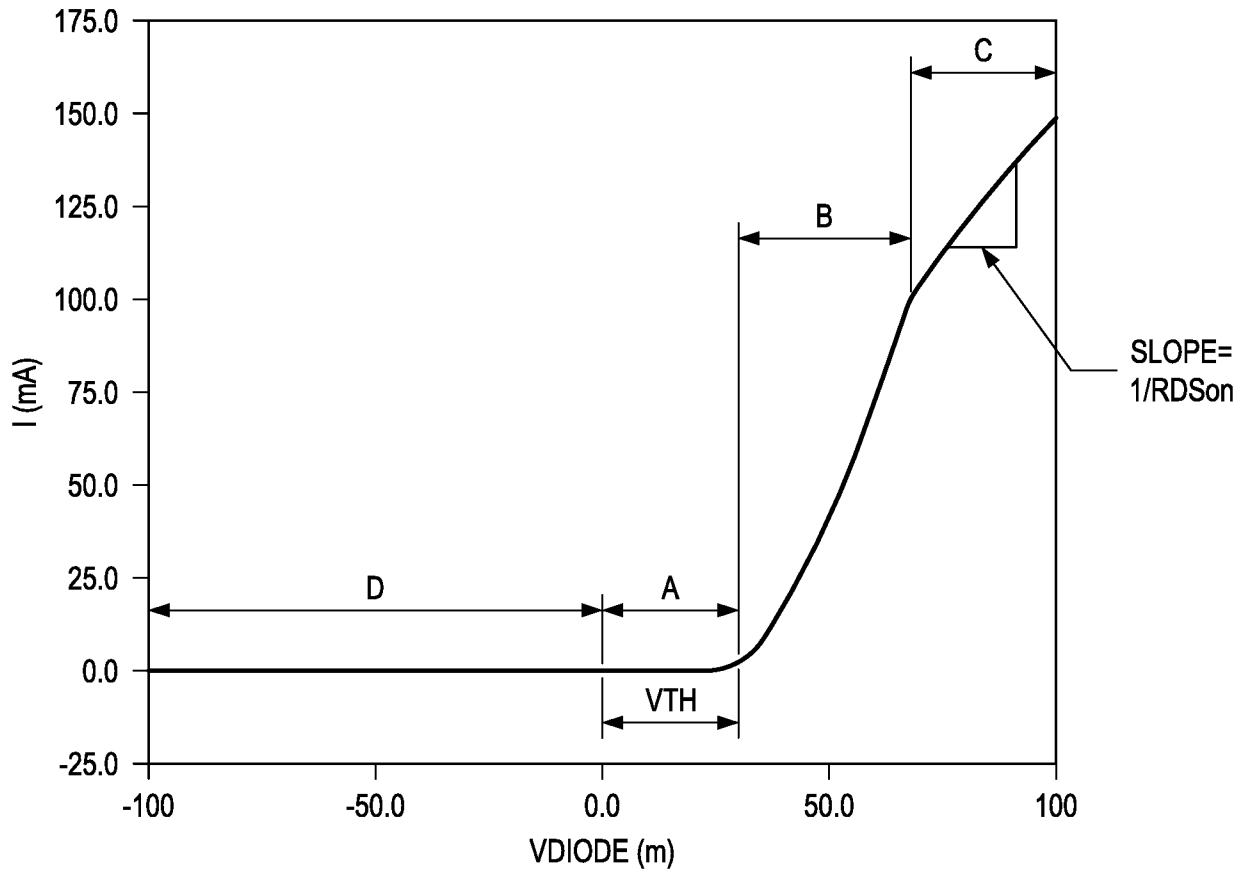


FIG. 5

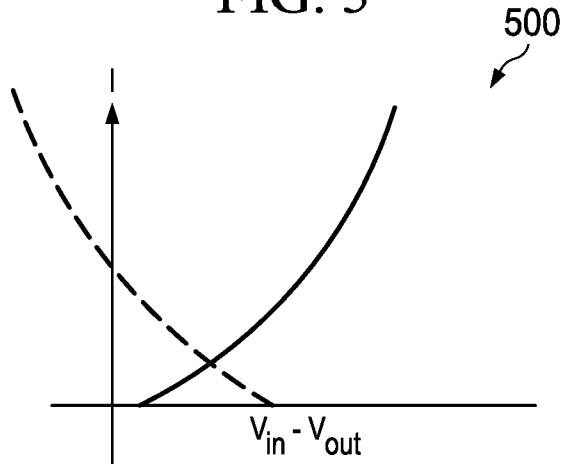
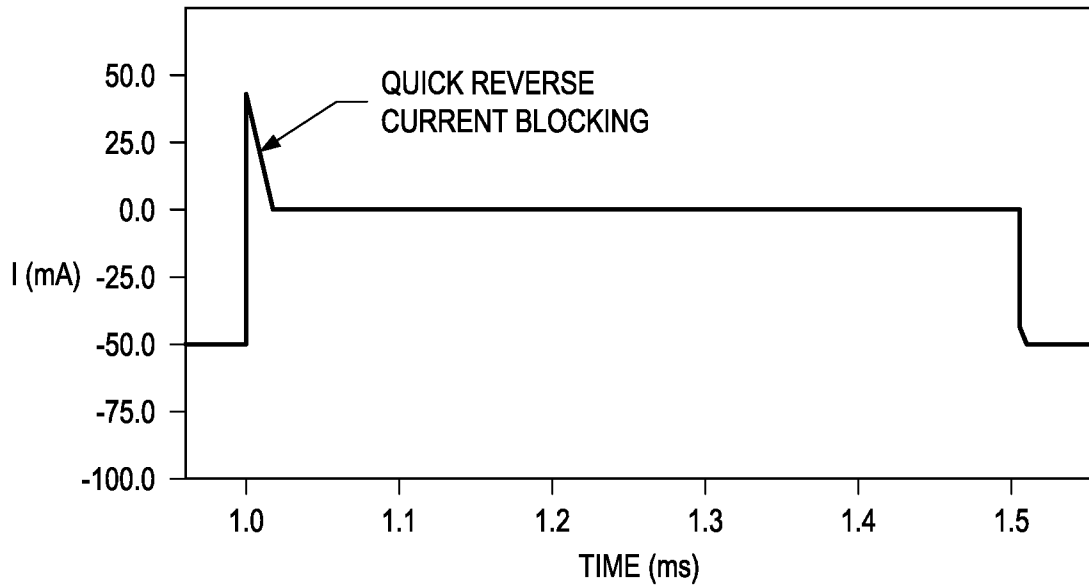
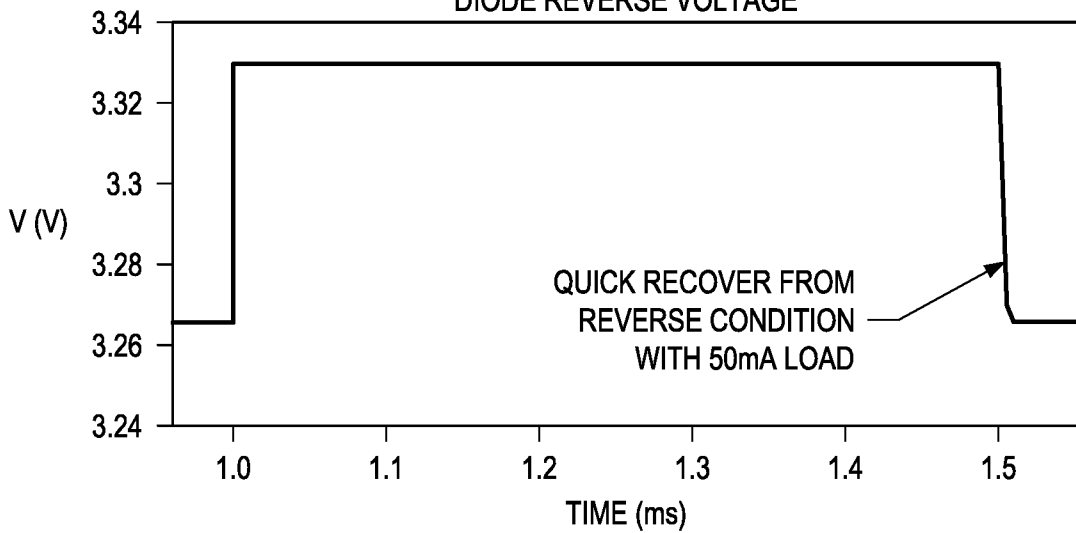


FIG. 4

DIODE REVERSE CURRENT



DIODE REVERSE VOLTAGE



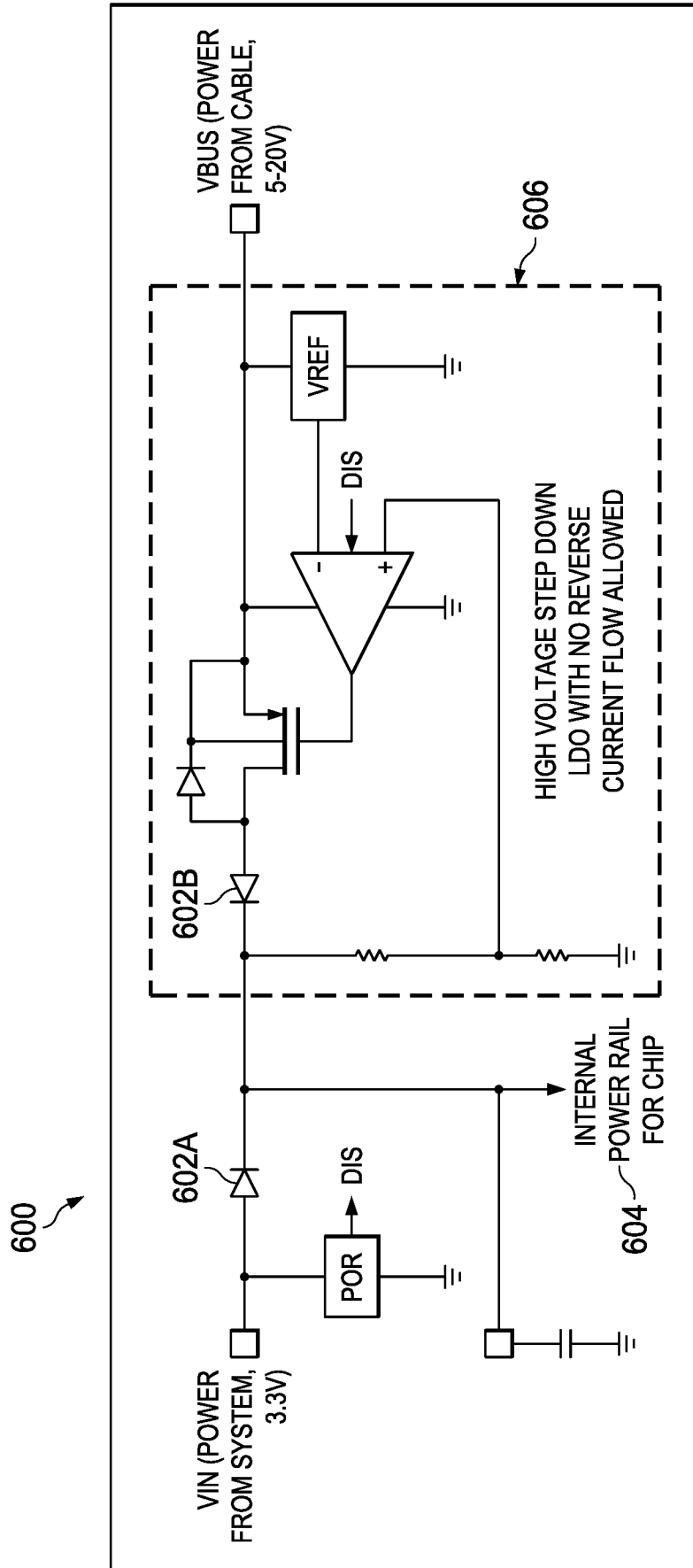


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2015/067747

| A. CLASSIFICATION OF SUBJECT MATTER | | |
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| <i>H02M 7/217 (2006.01)</i> | | |
| According to International Patent Classification (IPC) or to both national classification and IPC | | |
| B. FIELDS SEARCHED | | |
| Minimum documentation searched (classification system followed by classification symbols) | | |
| H02M 7/217, H03K 17/06 | | |
| Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched | | |
| Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) | | |
| PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE | | |
| C. DOCUMENTS CONSIDERED TO BE RELEVANT | | |
| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
| A | US 2011/0304360 A1 (NAOYUKI NAKAMURA et al.) 15.12.2011 | 1-17 |
| A | JP 2013042193 A (PANASONIC CORP) 28.02.2013 | 1-17 |
| A | RU 2451385 C1 (OTKRYTOE AKTSIONERNOE OBSHESTVO "RAKETNO-KOSMICHESKAYA KORPORATSIYA "ENERGIYA" IMENI S. P. KOROLEVA") 20.05.2012 | 1-17 |
| <input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex. | | |
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| Date of the actual completion of the international search | | Date of mailing of the international search report |
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