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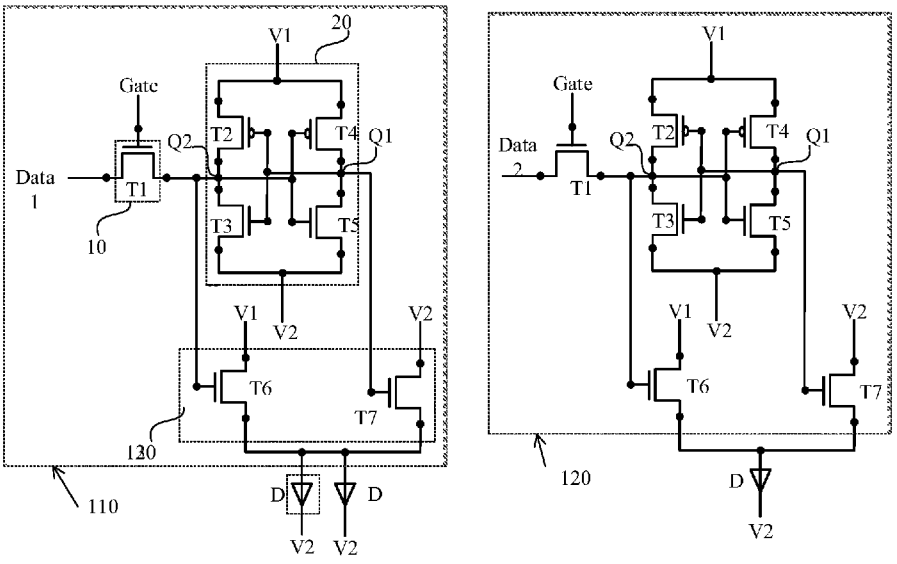


Fig. 2

(57) Abstract: A pixel circuit may include at least one light emitting circuit (100). One of the at least one light emitting circuit (100) may include an input sub-circuit (10), a latch sub-circuit (20), and an output sub-circuit (30). The input sub-circuit (10) may be configured to transmit a signal at a data voltage terminal (DATA) to the latch sub-circuit (20). The latch sub-circuit (20) may be configured to generate a control signal in accordance with the signal at the data voltage terminal (DATA) and store the control signal. The output sub-circuit (30) may be configured to transmit one of a signal at a first voltage terminal (V1) and a signal at a second voltage terminal (V2) to a light emitting unit (101) under control of the control signal.

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PIXEL CIRCUIT, DRIVING METHOD THEREOF, AND DISPLAY APPARATUS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of the filing date of Chinese Patent Application No. 201810681407.3 filed on July 27, 2018, the disclosure of which is hereby incorporated in its entirety by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to a field of display technology, and particularly, to a pixel circuit, a driving method thereof and a display apparatus.

BACKGROUND

[0003] The micro light-emitting diode (uLED) technology utilizes an array of high-density micro-scaled LEDs integrated on a substrate to achieve thin film formation, miniaturization and matrixing of the LEDs. The distance between pixels can reach a micrometer scale, and each pixel is addressable and can be individually driven to emit light.

[0004] The signals of the LEDs in the uLED apparatus are directly supplied by an integrated circuit (IC). That is, the IC and LED are transferred onto a silicon-based substrate, and the IC provides the signals to each of the LEDs. In order to ensure normal display during the process of driving the LEDs, it is necessary to continuously provide the signals to the LED by the IC, thereby increasing power consumption of the IC.

BRIEF SUMMARY

[0005] An example of the present disclosure provides a pixel circuit. The pixel circuit may include at least one light emitting circuit. One of the at least one light emitting circuit may include an input sub-circuit, a latch sub-circuit, and an output sub-circuit. The input sub-circuit may be configured to transmit a signal at a data voltage terminal to the latch sub-circuit. The latch sub-circuit may be configured to generate a control signal in accordance with the signal at the data voltage terminal and store the control signal. The output sub-circuit may be configured

to transmit one of a signal at a first voltage terminal and a signal at a second voltage terminal to a light emitting unit under control of the control signal.

[0006] The input sub-circuit may be coupled to the data voltage terminal and the latch sub-circuit respectively, and the output sub-circuit may be coupled to the input sub-circuit, the latch sub-circuit, the at least one light emitting unit, the first voltage terminal, and the second voltage terminal respectively.

[0007] The input sub-circuit may include a first transistor. A gate of the first transistor may be coupled to a scan signal terminal, a first electrode of the first transistor may be coupled to the data voltage terminal, and a second electrode of the first transistor may be coupled to the latch sub-circuit.

[0008] The latch sub-circuit may include a second transistor, a third transistor, a fourth transistor, and a fifth transistor. A gate of the second transistor may be coupled to a first node, a first electrode of the second transistor may be coupled to the first voltage terminal, and a second electrode of the second transistor may be coupled to a second node. A gate of the third transistor may be coupled to the first node, a first electrode of the third transistor may be coupled to the second voltage terminal, and a second electrode of the third transistor may be coupled to the second node. A gate of the fourth transistor may be coupled to the second node, a first electrode of the fourth transistor may be coupled to the first voltage terminal, and a second electrode of the fourth transistor may be coupled to the first node. A gate of the fifth transistor may be coupled to the second node, a first electrode of the fifth transistor may be coupled to the second node, and a second electrode of the fifth transistor may be coupled to the first node. The first node may be coupled to the output sub-circuit, and the second node may be coupled to the input sub-circuit and the output sub-circuit.

[0009] The second transistor and the fourth transistor may be P-type transistors, and the third transistor and the fifth transistor may be N-type transistors.

[0010] The output sub-circuit may include a sixth transistor and a seventh transistor. A gate of the sixth transistor may be coupled to the latch sub-circuit, a first electrode of the sixth

transistor may be coupled to the first voltage terminal, and a second electrode of the sixth transistor may be coupled to the at least one light emitting unit. A gate of the seventh transistor may be coupled to the latch sub-circuit, a first electrode of the seventh transistor may be coupled to the second voltage terminal, and a second electrode of the seventh transistor may be coupled to the at least one light emitting unit. The sixth transistor and the seventh transistor may be a same type of transistor.

[0011] In one embodiment, the input sub-circuit includes a first transistor, and a gate of the first transistor is coupled to a scan signal terminal, a first electrode of the first transistor is coupled to the data voltage terminal, and a second electrode of the first transistor is coupled to the latch sub-circuit. The latch sub-circuit includes a second transistor, a third transistor, a fourth transistor, and a fifth transistor, a gate of the second transistor is coupled to a first node, a first electrode of the second transistor is coupled to the first voltage terminal, and a second electrode of the second transistor is coupled to a second node; a gate of the third transistor is coupled to the first node, a first electrode of the third transistor is coupled to the second voltage terminal, and a second electrode of the third transistor is coupled to the second node, a gate of the fourth transistor is coupled to the second node, a first electrode of the fourth transistor is coupled to the first voltage terminal, and a second electrode of the fourth transistor is coupled to the first node, a gate of the fifth transistor is coupled to the second node, a first electrode of the fifth transistor is coupled to the second node, and a second electrode of the fifth transistor is coupled to the first node, and the first node is coupled to the output sub-circuit, and the second node is coupled to the input sub-circuit and the output sub-circuit. The output sub-circuit includes a sixth transistor and a seventh transistor; a gate of the sixth transistor is coupled to the latch sub-circuit, a first electrode of the sixth transistor is coupled to the first voltage terminal, and a second electrode of the sixth transistor is coupled to the at least one light emitting unit; and a gate of the seventh transistor is coupled to the latch sub-circuit, a first electrode of the seventh transistor is coupled to the second voltage terminal, and a second electrode of the seventh transistor is coupled to the at least one light emitting unit.

[0012] The at least one light emitting circuit may include a plurality of light emitting circuits; and each of the light emitting circuits may be coupled to a different data voltage terminal. At least two of the light emitting circuits may be coupled to a different first voltage terminal respectively, or at least two of the light emitting circuits may be coupled to a different second voltage terminal respectively.

[0013] The plurality of light emitting circuits may include a first light emitting circuit and a second light emitting circuit; a light emitting unit coupled to the first light emitting circuit may include a first light emitting unit and a second light emitting unit, and a light emitting unit coupled to the second light emitting circuit may include a third light emitting unit. The first light emitting unit, the second light emitting unit and the third light emitting unit may be capable of emitting a same wavelength of light.

[0014] The first light emitting circuit and the second light emitting circuit may be coupled to the same first voltage terminal and the same second voltage terminal. The first light emitting unit may be coupled to the first voltage terminal and the second light emitting unit may be coupled to the second voltage terminal; the third light emitting unit may be coupled to both the first voltage terminal and the second voltage terminal. The light emitting unit may be a light emitting diode.

[0015] Another example of the present disclosure is a display apparatus. The display apparatus may include a plurality of sub-pixels. Each of the plurality of sub-pixels may include the pixel circuit according to one embodiment of the present disclosure. Each of the plurality of sub-pixels may include a plurality of light emitting units.

[0016] In one embodiment, the pixel circuit includes a plurality of light emitting circuits, and the plurality of the light emitting circuits is sequentially arranged along an extending direction of a gate line of the display apparatus.

[0017] In one embodiment, the pixel circuit includes a plurality of light emitting circuits, and the plurality of the light emitting circuits are sequentially arranged along an extending direction of a data line of the display apparatus.

[0018] Another example of the present disclosure is a driving method for a pixel circuit. The pixel circuit may include at least one light emitting circuit. One of the at least one light emitting circuit may include an input sub-circuit, a latch sub-circuit, and an output sub-circuit. The input sub-circuit may be configured to transmit a signal at a data voltage terminal to a latch sub-circuit. The latch sub-circuit may be configured to generate a control signal in accordance with the signal at the data voltage terminal and store the control signal. An output sub-circuit may be configured to transmit one of a signal at a first voltage terminal and a signal at a second voltage terminal to a light emitting unit under control of the control signal. The driving method may include providing a signal from the data voltage terminal through the input sub-circuit to the latch sub-circuit, generating and storing a control signal by the latch sub-circuit, and transmitting one of the signal at the first voltage terminal and the signal at the second voltage terminal through a output sub-circuit to a light emitting unit under control of the control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The subject matter which is regarded as the disclosure is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the present disclosure are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0020] Fig 1 is a schematic block diagram of a pixel circuit according to one embodiment of the present disclosure;

[0021] Fig. 2 is a schematic structural diagram of a pixel circuit according to one embodiment of the present disclosure;

[0022] Fig. 3 is a schematic diagram of a driving process of a pixel circuit according to one embodiment of the present disclosure;

[0023] Fig. 4 is a schematic diagram of light emitting units in a pixel circuit according to one embodiment of the present disclosure;

[0024] Fig. 5 is a schematic structural diagram of a pixel circuit according to one embodiment of the present disclosure;

[0025] Fig. 6 is a schematic diagram of sub-pixels in a display apparatus according to one embodiment of the present disclosure;

[0026] Fig. 7 is a schematic diagram of an arrangement of light emitting circuits in a display apparatus according to one embodiment of the present disclosure; and

[0027] Fig. 8 is a schematic diagram of an arrangement of light emitting circuits in a display apparatus according to one embodiment of the present disclosure.

DETAILED DESCRIPTION

[0028] The present disclosure will be described in further detail with reference to the accompanying drawings and embodiments in order to provide a better understanding by those skilled in the art of the technical solutions of the present disclosure. Throughout the description of the disclosure, reference is made to Figs. 1-8. When referring to the figures, like structures and elements shown throughout are indicated with like reference numerals.

[0029] One embodiment of the present disclosure provides a pixel circuit. As shown in Fig 1, the pixel circuit includes at least one light emitting circuit 100 such as two light emitting circuits 100 as shown in Fig. 1. The light emitting circuit 100 includes an input sub-circuit 10, a latch sub-circuit 20, an output sub-circuit 30. In one embodiment, as illustrated in Fig. 1, one light emitting unit 101 includes two light emitting units D, and the other light emitting unit 101 includes one light emitting unit D.

[0030] In addition, that the light emitting unit 101 may include at least one light emitting unit D indicates that each light emitting unit 101 may include one or a plurality of light emitting units D. The plurality of light emitting units D may be coupled in series, or may be coupled in parallel as shown in Fig. 1. In one embodiment, as shown in Fig. 1, the pixel circuit includes a plurality of light emitting units 100. Each of the light emitting circuits 100 may include a plurality of light emitting units D. In addition, in the case where the pixel circuit includes a plurality of light emitting units D, areas of the light emitting regions of the plurality of light emitting units D may be the same or different.

[0031] In one embodiment, as shown in Fig. 1, the input sub-circuit 10 is coupled to the latch sub-circuit 20 and a data voltage terminal DATA respectively for transmitting the signal at the data voltage terminal DATA to the latch sub-circuit 20.

[0032] The latch sub-circuit 20 may be configured to generate and store a control signal based on the signal inputted at the data voltage terminal DATA. In one embodiment, the latch sub-circuit 20 may be a latch.

[0033] In one embodiment, the output sub-circuit 30 is coupled to the input sub-circuit 10, the latch sub-circuit 20, the light emitting units D, a first voltage terminal V1, and a second voltage terminal V2 for outputting the signal of the first voltage terminal V1 or the signal of the second voltage terminal V2 based on the control signal.

[0034] Here, in the following embodiments of the present disclosure, the signal at the first voltage terminal V1 is a high-level signal in comparison with the signal at the second voltage terminal V2. In one embodiment, the signal at the first voltage terminal V1 is a high level voltage (VDD), and the signal at the second voltage terminal V2 is a low level voltage (VSS).

[0035] In one embodiment, the at least one light emitting unit D is also coupled to the second voltage terminal V2. The at least one light emitting unit D is controlled to be at a light state under control of the signal of the first voltage terminal V outputted from the output sub-circuit 30, and to be at a dark state under control of the signal of the second voltage terminal V2 outputted from the output sub-circuit 30.

[0036] In one embodiment, as shown in Fig. 1, the pixel circuit includes a plurality of light emitting circuits 100. Different light emitting circuits 100 may be coupled to different data voltage terminals DATA respectively. In other words, the light emitting circuits 100 can transmit signals at different data voltage terminals DATA so that the plurality of light emitting circuits 100 can be driven asynchronously. As a result, the light and dark states of each of the respective light emitting units D located in the plurality of light emitting circuits 100 are not synchronized so that multi-gray scale display can be realized.

[0037] One embodiment of the present disclosure provides a pixel circuit. The pixel circuit includes a latch sub-circuit 20 that generates a control signal in response to the signal of the input sub-circuit 10 to control the at least one light emitting unit D to be at a light state or a dark state and stores the control signal in order to maintain the current state of the at least one light emitting unit D. In this way, during the display process, the integrated circuit (IC) inputs a signal to the data voltage terminal DATA of the pixel circuit to display an image. When there is no change to the displayed image, IC does not need to continuously input a signal to the data voltage terminal DATA of the pixel circuit. Instead, the latch sub-circuit 20 maintains the output of the control signal to maintain the currently displayed image, thereby greatly reducing the power consumption of the IC.

[0038] In some embodiments, the pixel circuit includes a plurality of light emitting circuits 100. The luminance of each of the light emitting circuits 100 is different when the light emitting units D are in the light state.

[0039] That is, taking the pixel circuit shown in Fig. 1 as an example, from the perspective of the figure, when the light emitting units D coupled to the light emitting circuit 100 (including two light emitting units D) as shown in the left and the light emitting unit D coupled to the light emitting circuit 100 (including one light emitting unit D) as shown in the right are at the “light” state, the luminance of the light emitting circuit 100 on the left is different from that of the light emitting circuit 100 on the right.

[0040] In one embodiment, area of the light emitting region of each of the light emitting units D in the pixel circuit is the same, but the number of the light emitting units D in each of the light emitting circuits 100 is different. In one embodiment, the number of the light emitting units D in each of the light emitting circuits 100 is the same, but the area of the light emitting region of each of the light emitting units D is not the same. Alternatively, other ways may be used to achieve different luminance of each of the light emitting circuits 100.

[0041] In one embodiment, the pixel circuit includes a first light emitting circuit, a second light emitting circuit, and a third light emitting circuit, and the three light emitting circuits have different luminance. As such, the pixel circuit can display eight gray scales.

Therefore, in the embodiments of the present disclosure, by making the luminance of each of the light emitting circuits 100 to be different, a maximum number of gray scales can be displayed under the premise of the same number of light emitting circuits 100.

[0042] In some embodiments, as shown in Fig. 2, the pixel circuit includes a first light emitting circuit 110 and a second light emitting circuit 120.

[0043] In some embodiments, as shown in Fig. 2, the input sub-circuit 10 includes a first transistor T1. A gate of the first transistor is coupled to a scan signal terminal GATE. A first electrode of the first transistor is coupled to the data voltage terminal DATA. A second electrode of the first transistor T1 is coupled to the latch sub-circuit 20.

[0044] In some embodiments, as shown in Fig. 2, the input sub-circuit 10 includes a first transistor T1. A gate of the first transistor is coupled to a scan signal terminal GATE. A first electrode of the first transistor is coupled to the data voltage terminal DATA. A second electrode of the first transistor T1 is coupled to a second node Q2.

[0045] It should be noted that the input sub-circuit 10 may further include a plurality of switching transistors connected in parallel with the first transistor T1. The above is only an example of the input sub-circuit 10. Other structures having the same function as the input sub-circuit 10 will not be further described herein, but all should belong to the protection scope of the present disclosure.

[0046] In some embodiments, in order to simplify the structure of the pixel circuit, as shown in Fig. 2, the latch sub-circuit 20 includes a second transistor T2, a third transistor T3, a fourth transistor T4, and a fifth transistor T5. The second transistor T2 and the fourth transistor T4 are P-type transistors. The third transistor T3 and the fifth transistor T5 are N-type transistors.

[0047] In one embodiment, a gate of the second transistor T2 is coupled to the first node Q1. A first electrode of the second transistor T2 is coupled to the first voltage terminal V1. A second electrode of the second transistor T2 is coupled to the second node Q2.

[0048] In one embodiment, a gate of the third transistor T3 is coupled to the first node Q1. A first electrode of the third transistor T3 is coupled to the second voltage terminal V2. A second electrode of the third transistor T3 is coupled to the second node Q2.

[0049] In one embodiment, a gate of the fourth transistor T4 is coupled to the second node Q2. A first electrode of the fourth transistor T4 is coupled to the first voltage terminal V1. A second electrode of the fourth transistor T4 is coupled to the first node Q1.

[0050] In one embodiment, a gate of the fifth transistor is coupled to the second node Q2. A first electrode of the fifth transistor T5 is coupled to the second voltage V2. A second electrode of the fifth transistor T5 is coupled to the first node Q1.

[0051] In one embodiment, the first node is coupled to the output sub-circuit 30. The second node Q2 is coupled to the input sub-circuit 10 and the output sub-circuit 30. In other words, the second node Q2 serves both as an input port of the latch sub-circuit 20 and as an output port of the latch sub-circuit 20.

[0052] In some embodiments, as shown in Fig. 2, the output sub-circuit 30 includes a sixth transistor T6 and a seventh transistor T7. The sixth transistor T6 and the seventh transistor T7 are transistors of the same type.

[0053] In one embodiment, a gate of the sixth transistor T6 is coupled to the latch sub-circuit 20. A first electrode of the sixth transistor T6 is coupled to the first voltage V1. A second electrode of the sixth transistor T6 is coupled to the at least one light emitting unit D.

[0054] In one embodiment, as shown in Fig. 2, the gate of the sixth transistor is coupled to the second node Q2, the first electrode of the sixth transistor T6 is coupled to the first voltage V1. The second electrode of the sixth transistor T6 is coupled to the at least one light emitting unit D.

[0055] In one embodiment, a gate of the seventh transistor T7 is coupled to the latch sub-circuit 20. A first electrode of the seventh transistor T7 is coupled to the second voltage terminal V2. A second electrode of the seventh transistor T7 is coupled to the at least one light emitting unit D.

[0056] In one embodiment, as shown in Fig. 2, the gate of the seventh transistor T7 is coupled to the first node Q1. The first electrode of the seventh transistor T7 is coupled to the second voltage terminal V2. The second electrode of the seventh transistor T7 is coupled to the at least one light emitting unit D.

[0057] It should be noted that the output sub-circuit 30 may include a plurality of switching transistor coupled in parallel with the sixth transistor T6 or a plurality of switching transistor coupled in parallel with the seventh transistor T7. The above is only an example of the output sub-circuit 30. Other structures having the same function as the output sub-circuit 30 will not be further described herein, but all should belong to the protection scope of the present disclosure.

[0058] In one embodiment, as can be seen from Fig. 2, the plurality of light emitting circuits 100 included in the pixel circuit are coupled to different data voltage terminals DATA, but are coupled to the same scan signal terminal GATE.

[0059] Based on the above description of the sub-circuits, some embodiments of the driving method of the above mentioned pixel circuit will be described in detail below.

[0060] It should be noted that, first, in the embodiments of the present disclosure, if the respective transistors in the pixel circuit are not clearly defined, the transistors may be an N-type transistor or a P-type transistor. In one embodiment, the first transistor T1, the sixth transistor T6, and the seventh transistor T7 are N-type transistors. The following embodiments of the present disclosure are all described by taking the above transistors as N-type transistors as example.

[0061] Here, the first electrode of the above-mentioned transistor may be the drain and the second electrode may be the source. Alternatively, the first electrode may be the source, and the second electrode may be the drain, which are not limited in the embodiments of the present disclosure.

[0062] Further, based on the various electrically conductive manner of the transistor, the transistors in the above pixel circuit can be classified as enhancement transistors and depletion transistors. The embodiment of the present disclosure is not limited to these.

[0063] Second, in the embodiments of the present disclosure, that a high-level VDD is inputted to the first voltage terminal V1 and a low-level VSS is inputted into the second voltage terminal V2 is taken as an example. The second voltage terminal can also be grounded. The high and low values only indicate the relative magnitude relationship between the input voltages.

[0064] In one embodiment, as shown in Fig. 3, in the case where it is required to control the first light emitting unit D1 and the second light emitting unit D2 to be in a light state, and the third light emitting unit D3 to be in a dark state:

[0065] In the light emitting circuit on the left, the scan signal terminal GATE is inputted a high level "on" signal, and the first data voltage terminal DATA 1 is inputted a high level signal. The fourth transistor T4 is controlled to be turned off, and at the same time, the fifth transistor T5 is controlled to be turned on. As such, the low level signal of the second voltage terminal V2 is transmitted to the first node Q1, which controls the third transistor T3 to be turned off, and, at the same time, controls the second transistor T2 to be turned on. As a result, the high level signal of the first voltage terminal V1 is transmitted to the second node Q2. The seventh transistor T7 is turned off under the control of the low level signal of the first node Q1. The sixth transistor T6 is turned on under the control of the high level signal of the second node Q2 and transmits the high level signal of the first voltage terminal V1 to the first light emitting unit D1 and the second light emitting unit D2. Accordingly, the first light emitting unit D1 and the second light emitting unit D2 are driven to be at a light state. Here, the transistors in the off state are indicated by "X."

[0066] At the same time in the light emitting circuit on the right, the scan signal terminal GATE is inputted a high level "on" signal, and the data voltage terminal is inputted a low level signal. The fifth transistor is controlled to be turned off and the fourth transistor to be turned on. As such, the high level signal of the first voltage terminal V1 is transmitted to the first node Q1, which controls the second transistor to be turned off and the third transistor to be turned on. As a

result, the low level signal of the second voltage terminal V2 is transmitted to the second node Q2. The sixth transistor T6 is turned off under the control of the second node Q2. The seventh transistor T7 is turned on under the control of the high level signal of the first node and transmits the low level signal of the second voltage terminal to the third light emitting unit D3. Accordingly, the third light emitting unit D3 is driven to be at a dark state.

[0067] Based on this, in some embodiments, as shown in Figs. 4 and 5, the pixel circuit includes two light emitting circuits 100. One of the light emitting circuits 100 coupled to two light emitting units D (the first light emitting unit D1 and the second light emitting unit D2), and the other light emitting circuit 100coupled to one light emitting unit D (the third light emitting unit D3).

[0068] In some embodiments, the two light emitting units D in the light emitting circuit 100 may be coupled in series or in parallel. The light emitting unit D may be, for example, a light emitting diode. The light emitting units D of a sub-pixel can be arranged as shown in Fig. 4. The box with the dotted line indicates a connecting member of the first light emitting unit D1 and the second light emitting unit D2. The first light emitting unit D1 and the second light second emitting unit D2 may be coupled in parallel through the connecting member. It can be understood that the connecting member can connect the two light emitting units D1 and D2 in parallel by using a bridge or a through hole.

[0069] Based on this, in some embodiments, the plurality of light emitting circuits 100 in the same pixel circuit emits light having the same wavelength. That is, regardless of the number of light emitting circuits included in the pixel circuit, the light emitting circuits 100 located in the same pixel circuit emits light of the same wavelength. That is, the light emitting units D located in the same pixel circuit emits light of the same color. Each of the pixel circuits emits a monochromatic light or emits white light. In one embodiment, the light emitting unit D emitting white light can be formed by a combination of a blue light emitting diode and a phosphor.

[0070] For the convenience of explanation, the transistors in the two light emitting circuits 100 as shown in Fig. 5 are distinguished by adding " ' " after the label. For example, the

first node in the left light emitting circuit 100 is Q1, and the first node in the right light emitting circuit 100 is Q1'.

[0071] Based on the above description, the driving state of the pixel circuit can be divided into the following:

[0072] In one embodiment, the scan signal terminal GATE is inputted a high level "on" signal, the first data voltage terminal Data1 is inputted a high level signal, the first node Q1 stores a digital signal "1" (high level), and the second node Q2 stores a digital signal "0" (low level). The sixth transistor is controlled to be turned on, and the first light emitting unit D1 and the second light emitting unit D2 emit light. The second data voltage terminal Data 2 is inputted a high level signal, the first node Q1' stores a digital signal "1," the second node Q2' stores a digital signal "0," the sixth transistor T6' is controlled to be turned on, and the third light emitting unit D3 emits light. This state is defined as L3 grayscale.

[0073] In one embodiment, the scan digital terminal GATE is inputted a high level "on" signal, the first data voltage terminal Data 1 is inputted a high level signal, the first node Q1 stores a digital signal "1," and the second node Q2 stores a digital signal "0." The sixth transistor T6 is controlled to be turned on, and the first light emitting unit D1 and the second light emitting unit D2 emit light. The second data voltage terminal Data 2 is inputted a low level signal, the first node Q1' stores the digital signal "0," and the second node Q2' store a digital signal "1." The seventh transistor T7' is controlled to be turned on, and the third light emitting unit D3 does not emit light. This state is defined as L2 grayscale.

[0074] In one embodiment, the scan digital terminal GATE is inputted a high level "on" signal, the first data voltage terminal Data1 is inputted a low level signal, the first node Q1 stores a digital signal "0," and the second node Q2 stores a digital signal "1." The seventh transistor T7 is controlled to be turned on, and the first light emitting unit D1 and the second light emitting unit D2 do not emit light. The second node Q2' stores a digital signal "0" and controls the sixth transistor T6' to be turned on. The third light emitting unit D3 emits light. The state is defined as L1 grayscale.

[0075] In one embodiment, the scan digital terminal GATE is inputted a high level "on" signal, the first data voltage terminal Data1 is inputted a low level signal, the first node Q1 stores a digital signal "0," and the second node Q2 stores a digital signal "1." The seventh transistor T7 is controlled to be turned on, and the first light emitting unit D1 and the second light emitting unit D2 do not emit light. The second data voltage terminal Data2 is inputted a low level signal, the first node Q1' stores a digital signal "0," the second node Q2' stores a digital signal "1" and controls the seventh transistor T7' to be turned on. The third light emitting unit D3 does not emit light. This state is defined as L0 grayscale.

[0076] Therefore, the pixel circuit can realize four grayscales of L3-L0. When the pixel circuit is applied to a combination of red sub-pixel, green sub-pixel, and blue sub-pixel, a 4X4X4=64 grayscales can be realized, which is enough for everyday display devices such as watches. Further, when the image being displayed is unchanged, the IC does not need to provide signals to the data voltage terminal DATA and the scan signal terminal GATE. Therefore, the power consumption of the IC can be greatly reduced.

[0077] Here, when a higher grayscale is to be displayed, it can be realized by increasing the number of the light emitting circuits 100 in the pixel circuit. Here only using the pixel circuit including two light emitting circuits 100 for illustration.

[0078] Everyday display panels and watches today, in consideration of the leakage current, supports frequencies of 60Hz and 30Hz, and it is difficult to support lower frequencies. However, the present disclosure adopts a digital circuit control mode and uses a latch sub-circuit 20 to store signal "1" and "0" to control whether the light emitting diode emits light or does not emit light. Therefore, frequencies below 30Hz or even 1Hz can be supported.

[0079] One embodiment of the present disclosure provides a driving method of the above-mentioned pixel circuit. The driving method includes the following:

[0080] The data voltage terminal DATA provides a signal to the latch sub-circuit 20 through the input sub-circuit 10, causes the latch sub-circuit 20 to generate a control signal. The

latch sub-circuit 20 transmits the control signal to the output sub-circuit and stores the control signal.

[0081] Under the control of the control signal, the output sub-circuit 30 outputs a signal at the first voltage terminal V1 or a signal at the second voltage terminal V2 to the at least one light emitting unit D.

[0082] Here, the output sub-circuit 30 outputs the signal at the first voltage terminal V1 or the signal at the second voltage terminal V2 under the control of the control signal. In other words, the output sub-circuit 30 outputs a different signal depending on the control signal. Therefore, the control signal generated by the latch sub-circuit 20 includes a first control signal and a second control signal.

[0083] Under the control of the first control signal, the output sub-circuit 30 outputs the signal of the first voltage terminal V1 to control the at least one light emitting unit to be at a light state. Under the second control signal, the output sub-circuit 30 outputs the signal of the second voltage terminal V2 to control the at least one light emitting unit to be at a dark state.

[0084] The beneficial effects of the driving method of the pixel circuit provided by the embodiments of the present disclosure are the same as those of the pixel circuit and are not described herein again.

[0085] In some embodiments, as shown in Fig. 2, the input sub-circuit 10 includes a first transistor T1. The latch sub-circuit 20 includes a second transistor T2, a third transistor T3, a fourth transistor T4 and a fifth transistor T5. The output sub-circuit 30 includes a sixth transistor T6 and a seventh transistor T7.

[0086] The driving method of the pixel circuit includes the following: under the control of the scan signal terminal Gate, the first transistor T1 transmits the first signal (high level signal) of the data voltage terminal to the second node Q2. Under the control of the second node Q2, the fifth transistor T5 transmits the signal of the second voltage terminal V2 to the first node, and the fourth transistor T4 is turned off. The seventh transistor T7 and the third transistor T3 are turned off under the control of the first node Q1, and the second transistor T2 transmits the first voltage

terminal V1 signal to the second node Q2. Under the control of the second node Q2, the sixth transistor T6 transits the signal of the first voltage terminal V1 to the at least one light emitting unit D to control the at least one light emitting unit D to be in a light state.

[0087] Under the control of the scan terminal GATE, the first transistor T1 transits the signal (low level signal) of the data voltage terminal DATA to the second node Q2. Under the control of the second node Q2, the fourth transistor T4 transmits the signal of the first voltage terminal V1 to the first node Q1, and the fifth transistor T5 is turned off. Under the control of the first node Q1, the seventh transistor T7 transmits the signal of the second voltage terminal V2 to the at lease one light emitting unit D to control the at least one light emitting unit D to be in a dark state, the second transistor T2 is turned off, and the third transistor T3 transmits the second voltage terminal V2 signal to the second node Q2. Under the control of the second node Q2, the sixth transistor T6 is turned off.

[0088] Here, the first signal inputted at the data voltage terminal DATA is a high level signal relative to the second signal inputted at the data voltage terminal DATA.

[0089] One embodiment of the present disclosure also provides a display apparatus. The display apparatus includes a plurality of sub-pixels. Each of the sub-pixels includes the above pixel circuit.

[0090] Here, the above display apparatus may be a display panel, or an apparatus including a display panel and may specifically be a projector, components with any display function such as monitors, digital photo frames, mobile phones, tablets, navigators, and watches, etc.

[0091] One embodiment of the present disclosure provides a display apparatus. The pixel circuit of the display apparatus includes a latch sub-circuit 20. The latch sub-circuit 20 transmits the control signal generated in accordance with the signal of the input sub-circuit 10 to control the at least one light emitting unit D to be either in a light state or a dark state, and the control signal is stored in the latch sub-circuit 20 in order to maintain the current state of the at least one light emitting unit D. In this way, during the display process, the IC inputs a signal to

the data voltage terminal to display the to-be-displayed image. When the displayed image does not change, the IC does not need to continuously input a signal to the data voltage terminal. The latch sub-circuit 20 maintains the output of the control signal to maintain the currently displayed image, thereby greatly reducing the power consumption of the IC.

[0092] On the basis of this, the pixel circuit of the display apparatus provided by some embodiments of the present disclosure can be directly formed on the glass substrate, and the process thereof is mature and the cost is low.

[0093] The display apparatus provided by the embodiments of the present disclosure includes the above pixel circuit, and the beneficial effects are the same as those of the above pixel circuit, and therefore, are not described herein again.

[0094] In some embodiments, as shown in Fig. 6, each of the sub-pixels includes a plurality of light emitting units D, and area of the light emitting region of each of the light emitting units of the same sub-pixel is the same.

[0095] As shown in Fig. 6, three sub-pixels are illustrated. Each of the sub-pixels includes three light emitting units D, and the area of the light emitting region of each of the three light emitting units D in the same sub-pixel is the same. However, the areas of the light emitting regions of the light emitting units D of different sub-pixels are not the same. Of course, the number of light emitting units D in each of the sub-pixel pixels can be different.

[0096] In this way, since the size of each of the light emitting units D is the same, the process of making the light emitting units D can be simplified.

[0097] In some embodiments, as shown in Fig. 7, the pixel circuit includes a plurality of light emitting circuits 100. The plurality of light emitting circuits 100 are sequentially arranged along extending direction of the gate lines of the display apparatus.

[0098] During the process of display, the plurality of light emitting circuits 100 in one sub-pixel need to be simultaneously driven. Therefore, sequentially arranging the plurality of the light emitting circuits 100 along the extending direction of the gate lines of the display apparatus

can reduce the number of gate lines. A single gate line can drive all the light emitting circuits 100 in a row of sub-pixels.

[0099] Here, the light emitting circuits 100 are sequentially arranged along the extending direction of the gale lines of the display apparatus, and the light emitting units D in the light emitting circuit 100 can also be sequentially arranged along the extending direction of the gate lines. As such, the light emitting units D in the entire display apparatus are arranged in an array.

[00100] In some embodiments, as shown in Fig. 8, the pixel circuit includes a plurality of light emitting circuits 100. The plurality of light emitting circuits 100 are sequentially arranged along the extending direction of the data lines of the display apparatus.

[00101] In addition, since the plurality of light emitting circuits 100 in one sub-pixel need to be driven at the same time during the process of displaying, each of the light emitting circuits 100 needs to input a gate driven signal. A gate line can drive a group of light emitting circuits 100. The three gate lines for the same sub-pixel can be coupled to a same signal terminal, or can be respectively coupled to a signal terminal. Of course, it is also possible to reduce the number of gate lines by rationally planning the path of the gate lines.

[00102] Here, the light emitting circuits 100 are sequentially arranged along the extending direction of the data lines of the display device. The light emitting units D in the light emitting circuit 100 can also be sequentially arranged along the extending direction of the data lines. As such, the light emitting units D in the entire display device are arranged in an array.

[00103] In this way, the pixel circuits in the same row are simultaneously driven by one gate line, and the pixel circuits in the same column are driven by one data line in a time division manner which can reduce the IC power consumption and at the same time, greatly reduce the number of IC. This is suitable for display apparatuses that perform long display time such as a watch.

[00104] The principle and the embodiment of the present disclosures are set forth in the specification. The description of the embodiments of the present disclosure is only used to help understand the method of the present disclosure and the core idea thereof. Meanwhile, for a

person of ordinary skill in the art, the disclosure relates to the scope of the disclosure, and the technical scheme is not limited to the specific combination of the technical features, and also should covered other technical schemes which are formed by combining the technical features or the equivalent features of the technical features without departing from the inventive concept. For example, technical scheme may be obtained by replacing the features described above as disclosed in this disclosure (but not limited to) with similar features.

[00105] Reference numbers in the figures:

[00106] lighting circuit 100; input sub-circuit 10; latch sub-circuit 20; output sub-circuit 30; light emitting unit D; data voltage terminal DATA; scanning signal terminal GATE; first voltage terminal V1; second voltage terminal V2; first node Q1; second node Q2; first transistor T1; second transistor T2; third transistor T3; fourth transistor T4; fifth transistor T5; sixth transistor T6; seventh transistor T7.

CLAIMS

What is claimed is:

1. A pixel circuit, comprising:

at least one light emitting circuit, one of the at least one light emitting circuit comprising,

an input sub-circuit, configured to transmit a signal at a data voltage terminal to a latch sub-circuit;

the latch sub-circuit, configured to generate a control signal in accordance with the signal at the data voltage terminal and store the control signal; and

an output sub-circuit, configured to transmit one of a signal at a first voltage terminal and a signal at a second voltage terminal to a light emitting unit under control of the control signal.

2. The pixel circuit according to claim 1, wherein the input sub-circuit is coupled to the data voltage terminal and the latch sub-circuit respectively, and the output sub-circuit is coupled to the input sub-circuit, the latch sub-circuit, the at least one light emitting unit, the first voltage terminal, and the second voltage terminal respectively.

3. The pixel circuit according to claims 1 or 2, wherein the input sub-circuit comprises a first transistor, and

wherein a gate of the first transistor is coupled to a scan signal terminal, a first electrode of the first transistor is coupled to the data voltage terminal, and a second electrode of the first transistor is coupled to the latch sub-circuit.

4. The pixel circuit according to any one of claims 1-3, wherein the latch sub-circuit comprises a second transistor, a third transistor, a fourth transistor, and a fifth transistor,

wherein a gate of the second transistor is coupled to a first node, a first electrode of the second transistor is coupled to the first voltage terminal, and a second electrode of the second transistor is coupled to a second node;

a gate of the third transistor is coupled to the first node, a first electrode of the third transistor is coupled to the second voltage terminal, and a second electrode of the third transistor is coupled to the second node,

a gate of the fourth transistor is coupled to the second node, a first electrode of the fourth transistor is coupled to the first voltage terminal, and a second electrode of the fourth transistor is coupled to the first node,

a gate of the fifth transistor is coupled to the second node, a first electrode of the fifth transistor is coupled to the second node, and a second electrode of the fifth transistor is coupled to the first node, and

the first node is coupled to the output sub-circuit, and the second node is coupled to the input sub-circuit and the output sub-circuit.

5. The pixel circuit according to claim 4, wherein the second transistor and the fourth transistor are P-type transistors, and the third transistor and the fifth transistor are N-type transistors.

6. The pixel circuit according to any one of claims 1-5, wherein the output sub-circuit comprises a sixth transistor and a seventh transistor;

wherein a gate of the sixth transistor is coupled to the latch sub-circuit, a first electrode of the sixth transistor is coupled to the first voltage terminal, and a second electrode of the sixth transistor is coupled to the at least one light emitting unit; and

a gate of the seventh transistor is coupled to the latch sub-circuit, a first electrode of the seventh transistor is coupled to the second voltage terminal, and a second electrode of the seventh transistor is coupled to the at least one light emitting unit.

7. The pixel circuit according to claim 6, where the sixth transistor and the seventh transistor are a same type of transistor.

8. The pixel circuit according to claim 1, wherein:

the input sub-circuit comprises a first transistor, and a gate of the first transistor is coupled to a scan signal terminal, a first electrode of the first transistor is coupled to the data voltage terminal, and a second electrode of the first transistor is coupled to the latch sub-circuit;

the latch sub-circuit comprises a second transistor, a third transistor, a fourth transistor, and a fifth transistor, a gate of the second transistor is coupled to a first node, a first electrode of the second transistor is coupled to the first voltage terminal, and a second electrode of the second transistor is coupled to a second node; a gate of the third transistor is coupled to the first node, a first electrode of the third transistor is coupled to the second voltage terminal, and a second electrode of the third transistor is coupled to the second node, a gate of the fourth transistor is coupled to the second node, a first electrode of the fourth transistor is coupled to the first voltage terminal, and a second electrode of the fourth transistor is coupled to the first node, a gate of the fifth transistor is coupled to the second node, a first electrode of the fifth transistor is coupled to the second node, and a second electrode of the fifth transistor is coupled to the first node, and the first node is coupled to the output sub-circuit, and the second node is coupled to the input sub-circuit and the output sub-circuit;

the output sub-circuit comprises a sixth transistor and a seventh transistor; a gate of the sixth transistor is coupled to the latch sub-circuit, a first electrode of the sixth transistor is coupled to the first voltage terminal, and a second electrode of the sixth transistor is coupled to the at least one light emitting unit; and a gate of the seventh transistor is coupled to the latch sub-circuit, a first electrode of the seventh transistor is coupled to the second voltage terminal, and a second electrode of the seventh transistor is coupled to the at least one light emitting unit.

9. The pixel circuit according to any one of claims 1-8, wherein the at least one light emitting circuit comprises a plurality of light emitting circuits; and each of the light emitting circuits is coupled to a different data voltage terminal.

10. The pixel circuit according to claim 9, wherein at least two of the light emitting circuits are coupled to a different first voltage terminal respectively, or at least two of the light emitting circuits is coupled to a different second voltage terminal respectively.

11. The pixel circuit according to claim 9, wherein the plurality of light emitting circuits comprise a first light emitting circuit and a second light emitting circuit; a light emitting unit coupled to the first light emitting circuit comprises a first light emitting unit and a second light emitting unit, and a light emitting unit coupled to the second light emitting circuit comprises a third light emitting unit.

12. The pixel circuit according to claim 11, wherein the first light emitting unit, the second light emitting unit and the third light emitting unit are capable of emitting a same wavelength of light.

13. The pixel circuit according to claims 11 or 12, wherein the first light emitting circuit and the second light emitting circuit are coupled to the same first voltage terminal and the same second voltage terminal.

14. The pixel circuit according to claim 13, wherein the first light emitting unit is coupled to the first voltage terminal and the second light emitting unit is coupled to the second voltage terminal; the third light emitting unit is coupled to both the first voltage terminal and the second voltage terminal.

15. The pixel circuit according to any one of claims 1-14, wherein the light emitting unit is a light emitting diode.

16. A display apparatus, comprising:

a plurality of sub-pixels,

wherein each of the plurality of sub-pixels comprises the pixel circuit of any one of claims 1-14.

17. The display apparatus according to claim 16, wherein each of the plurality of sub-pixels comprises a plurality of light emitting units.

18. The display apparatus according to claim 17, wherein the pixel circuit comprises a plurality of light emitting circuits, and the plurality of the light emitting circuits are sequentially arranged along an extending direction of a gate line of the display apparatus.

19. The display apparatus according to claim 18, wherein the pixel circuit comprises a plurality of light emitting circuits, and the plurality of the light emitting circuits are sequentially arranged along an extending direction of a data line of the display apparatus.

20. A driving method for a pixel circuit, the pixel circuit comprises at least one light emitting circuit, one of the at least one light emitting circuit comprising, an input sub-circuit, configured to transmit a signal at a data voltage terminal to a latch sub-circuit; the latch sub-circuit, configured to generate a control signal in accordance with the signal at the data voltage terminal and store the control signal; and an output sub-circuit, configured to transmit one of a signal at a first voltage terminal and a signal at a second voltage terminal to a light emitting unit under control of the control signal, wherein, the driving method comprising:

providing a signal from the data voltage terminal through the input sub-circuit to the latch sub-circuit,

generating and storing a control signal by the latch sub-circuit,

transmitting one of the signal at the first voltage terminal and the signal at the second voltage terminal through a output sub-circuit to a light emitting unit under control of the control signal.

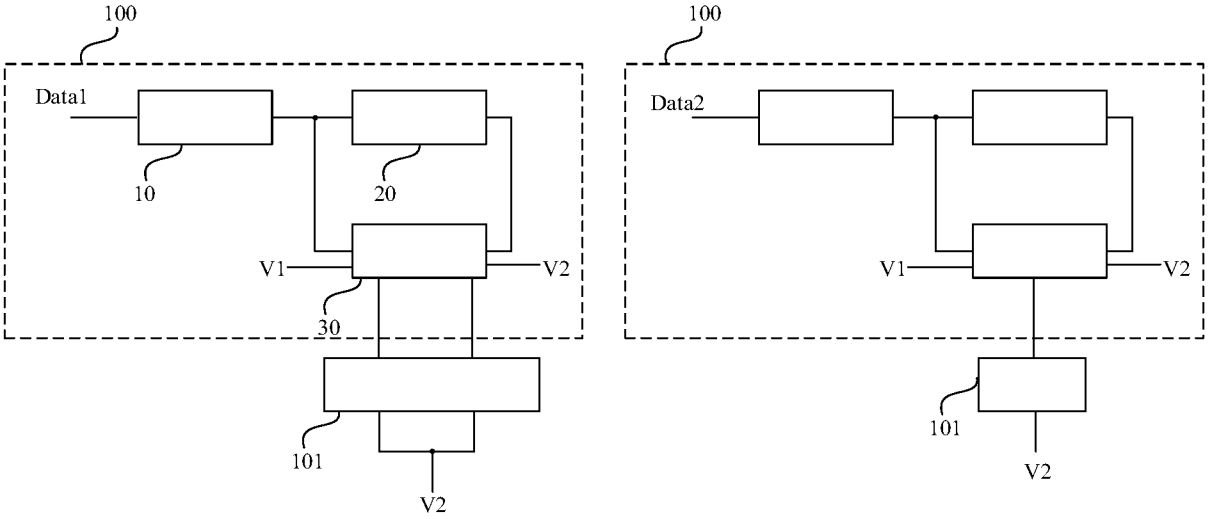


Fig. 1

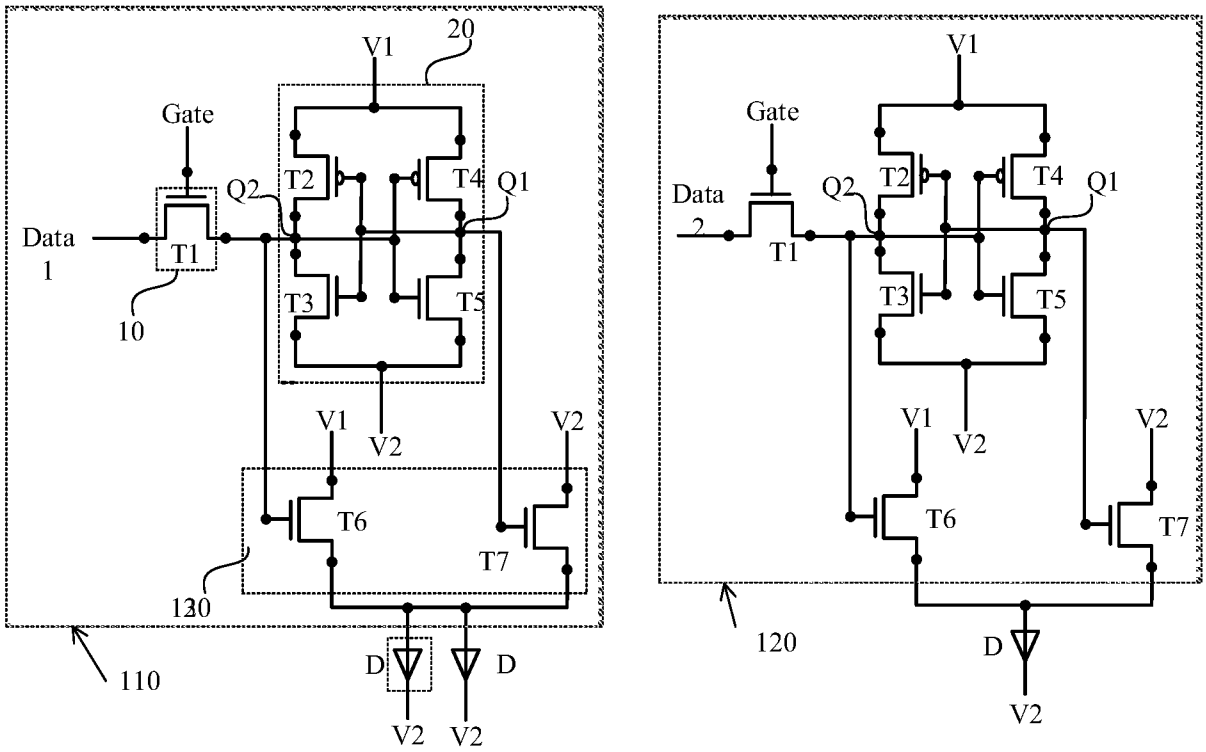

V1
20
Gate
Q2
T2
T4
Q1
Data
1
T1
10
T3
T5
V1
V2
V2
T6
T7
120
110
D
D
V2
V2
V1
Gate
Data
2
Q2
T2
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T6
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D
V2

Fig. 2

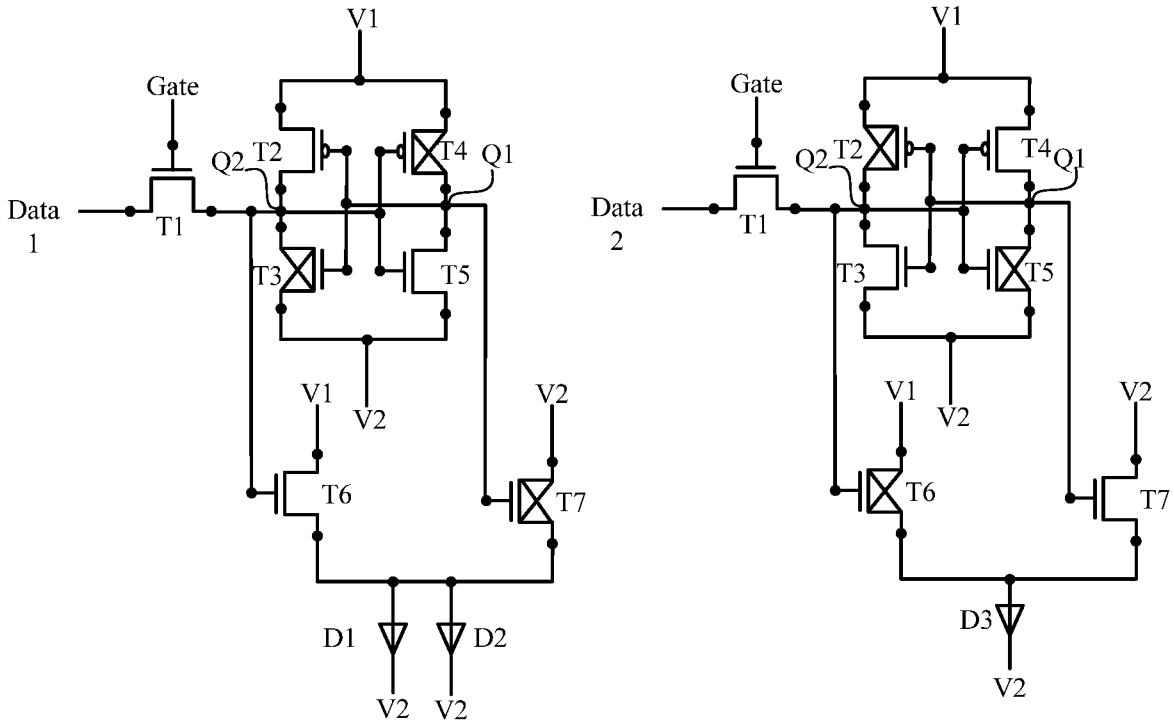

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D1
D2
V2
V2
V1
Gate
Q2
T2
T4
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Data
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T1
T3
T5
V1
V2
V2
T6
T7
D3
V2

Fig. 3

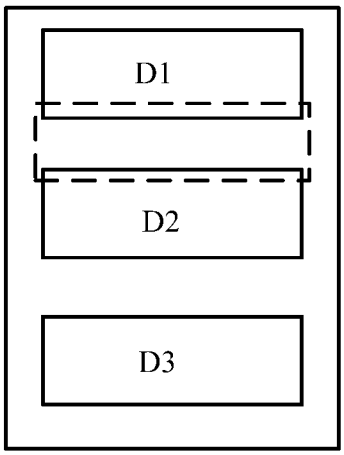


Fig. 4

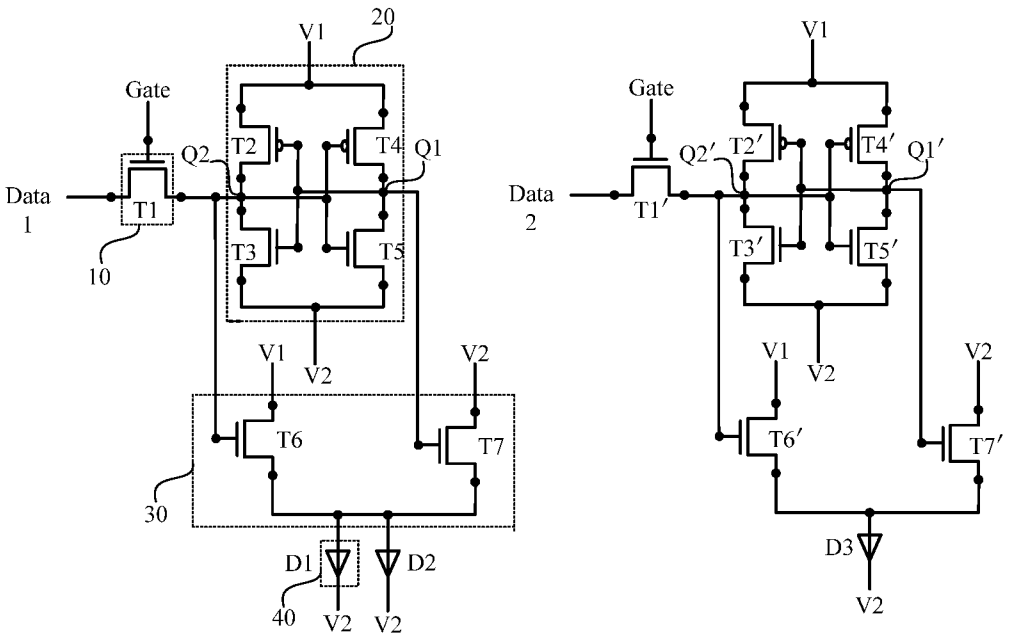

V1
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Q1
Data
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T3
T5
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V1
V2
V2
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D2
40
V2
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V1
Gate
Q2′
T2′
T4′
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T7′
D3
V2

Fig. 5

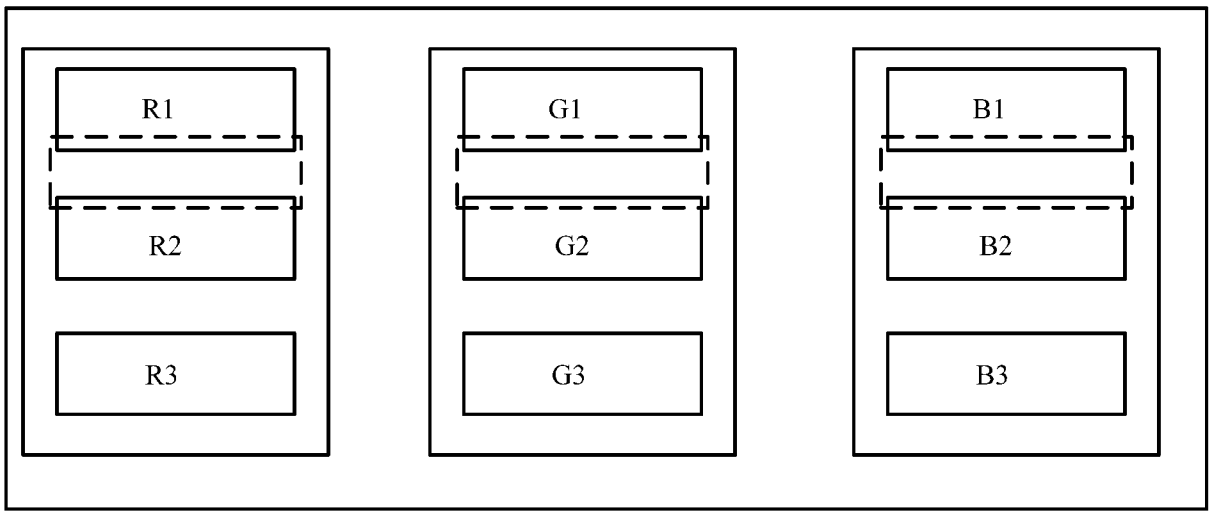


Fig. 6

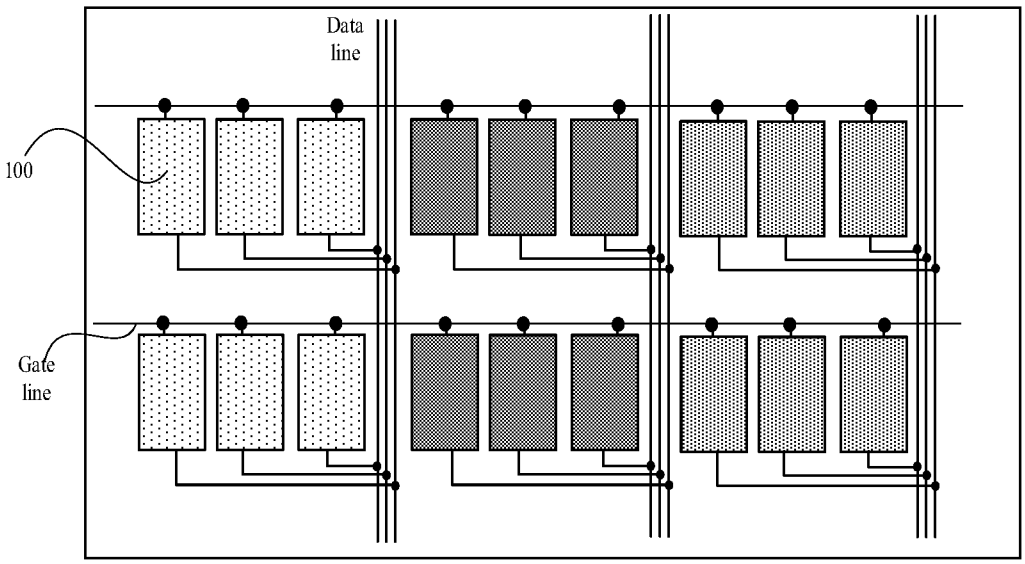


Fig. 7

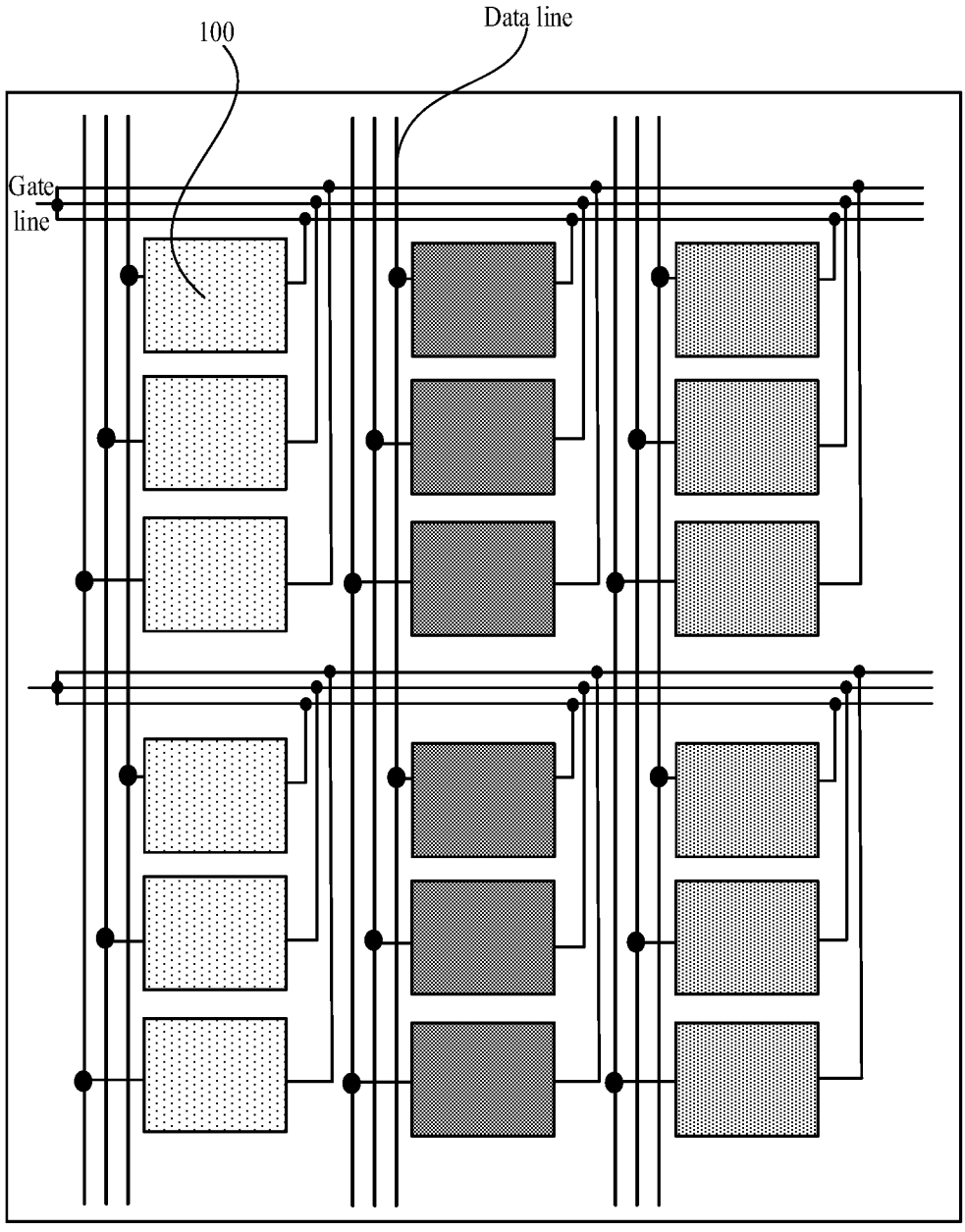


Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/120523

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/32(2016.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,EPODOC,WPI:pixel?,latch,memory,circuit?,cell?,module?,light,emit+,transistor?,OLED,input+,output+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 107025889 A (JAPAN DISPLAY INC.) 08 August 2017 (2017-08-08) description, paragraphs [0023], [0040] to [0049] and figures 2, 3	1-20
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A	CN 101317211 A (SONY CORPORATION) 03 December 2008 (2008-12-03) the whole document	1-20
A	CN 101281737 A (SONY CORPORATION) 08 October 2008 (2008-10-08) the whole document	1-20
A	US 2002130828 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 19 September 2002 (2002-09-19) the whole document	1-20
A	US 2017124968 A1 (JAPAN DISPLAY INC.) 04 May 2017 (2017-05-04) the whole document	1-20
A	WO 0217289 A1 (EMAGIN CORPORATION) 28 February 2002 (2002-02-28) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 February 2019	**01 April 2019**

Name and mailing address of the ISA/CN	Authorized officer
National Intellectual Property Administration, PRC **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing** **100088** **China**	**LI,Wenfei**
Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53962508**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2018/120523

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