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(54) Title: AN ANALOGUE TO DIGITAL CONVERTER

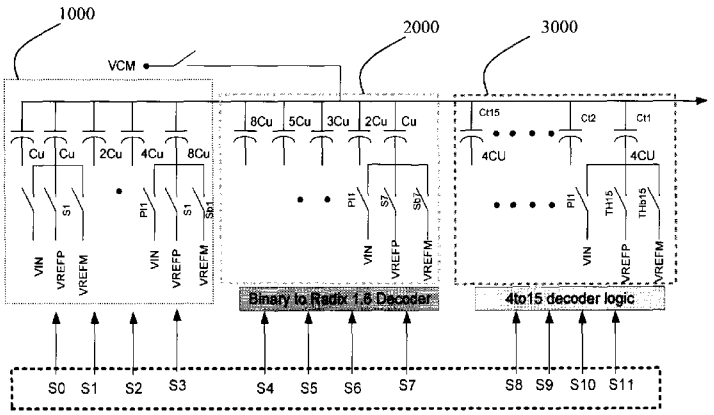


Figure 2

(57) Abstract: The present invention relates to a small area multi segment DAC that is used within a successive approximation analog to digital converter. The present invention comprising: a comparator (100) for comparing input signal with a reference signal; a successive approximation logic (200) that takes input from the comparator (100); and a digital to analogue converter block (300) including a plurality of capacitors that receives input from the successive approximation logic (200) block and generates reference signal that is applied to the comparator (100). The present invention not only combines the thermometer coded (3000) and binary coded segments (1000) but also a segment that has sub-radix 2 (radix < 2) weights (2000). A sub-radix 2 weights (2000) is in between binary (1000) and unitary weights (3000), hence its area and decoder size is also in between the two while its differential non-linearity DNL parameter (measure of linearity) is in between the two as well.

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Description

Title of Invention: AN ANALOGUE TO DIGITAL CONVERTER

[1] **FIELD OF INVENTION**

[2] The present invention relates to an analogue to digital converter (ADC) which converts the analogue signal to digital signal.

[3] **BACKGROUND OF THE INVENTION**

[4] The performance of analog to digital converters is generally limited by the matching accuracy of components. Improving the matching accuracy, while possible, is expensive or requires extra chip area. The Binary Weighted DAC contains binary weighted resistor, capacitor or current source segment for each possible value of DAC output. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision resistors, capacitors or current sources are sophisticated, so this type of converter is usually limited to 8-bit resolution or less.

[5] The thermometer coded DAC contains an equal resistor, capacitor or current source segment for each possible value of DAC output. An 8-bitthermometer weighted DAC would have 255 segments, and a 16-bit thermometer weighted DAC would have 65,535 segments. This is perhaps the highest precision DAC architecture but a large area incurred thus hindering the balance of performance between the accuracy and speed.

[6] Therefore it is a need for an invention that can tackle those drawbacks.

[7] **SUMMARY OF THE INVENTION**

[8] According to an aspect of the present invention, the present invention providesan analogue to digital converter comprising: a comparator (100) for comparing input signal with a reference signal; a successive approximation logic (200) that takes input from the comparator (100) for determining the digital output code; and a digital to analogue converter block (300) including a plurality of capacitors that receives input from the successive approximation logic (200) block and generates reference signal that is applied to the comparator (100); characterised in that the digital to analogue converter block (300) further comprising a plurality of a binary weight (radix = 2) segment (1000), a (radix < 2) weight segment (2000) and a unitary weight (radix = 1) segment (3000) elements. The segment elements including: a binary to thermometer/ unitary decoder for unitary weight segment (3000); and a binary to radix < 2 decoder for (radix < 2) weight segment (2000) wherein the input signal is compared with the signal charged on capacitors from plurality of digital to analogue converter block (300) capacitor beginning from the most significant bit down to the least significant bit.

[9] The above provision is advantageous as the present invention combines the

thermometer coded principle for the most significant bits and the binary weighted principle for the least significant bits. In this way, a compromise is obtained between precision (by the use of the thermometer coded principle) and number of resistors, capacitors or current sources (by the use of the binary weighted principle).

[10] The present invention not only combines the thermometer coded and binary coded segments but also a segment that has sub-radix 2 (radix < 2) weights. A sub-radix 2 weights is in between binary and unitary weights, hence its area and decoder size is also in between the two (for example for radix = 1.6, 6-bit sub-radix 2 DAC would have 7 segments) while its differential non-linearity DNL parameter (measure of linearity) is also in between the two.

[11] The present invention provides the optimal compromise between complexity and accuracy.

[12] **BRIEF DESCRIPTION OF THE DRAWINGS**

[13] **Figure 1**illustrates Successive Approximation Analog Digital Converter (SA-ADC) block diagram.

[14] **Figure 2**illustrates block diagram of an example 12 bit multi segmentdigital to analogue converter block (300)with 4 bit radix 1.6 weighted (2000) + 4 bit unitary/ thermometer weighted (3000) + 4 bit binary weighted (1000) capacitor array.

[15] **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

[16] As illustrated in **Figure 1**, generally, the present invention relates to an analogue to digital converter comprising: a comparator (100) for comparing input signal with a reference signal; a successive approximation logic (200) that takes input from the comparator (100) for determining the digital output code; and a digital to analogue converter block (300) including a plurality of capacitors that receives input from the successive approximation logic (200) block and generates reference signal that is applied to the comparator (100); characterised in that the digital to analogue converter block (300) further comprising a plurality of a binary weight (radix = 2) segment (1000), a (radix < 2) weight segment (2000) and a unitary weight (radix = 1) segment (3000) elements. The segment elements including: a binary to thermometer/unitary decoder for unitary weight segment (3000); and a binary to radix < 2 decoder for (radix < 2) weight segment (2000) wherein the input signal is compared with the signal charged on capacitors from plurality of digital to analogue converter block (300) capacitor beginning from the most significant bit down to the least significant bit.

[17] As illustrated in **Figure 2**,it illustrates block diagram of an example of 12 bit multi segmentdigital to analogue converter block (300)with 4 bit radix 1.6 weighted (2000) + 4 bit unitary/thermometer weighted (3000) + 4 bit binary weighted (1000) capacitor array.The specialdigital to analogue converter block (300)combination gives the best trade-off in terms of area, performance (DNL as measurement of static linearity) and

complexity as there is no need to use attenuation or split capacitor especially for higher resolutiondigital to analogue converter blocksuch as 10 - 12 bits. The unitary/ thermometer weighted capacitor array uses largest area but gives best linearity (as measured by this metric DNL, Differential Non-linearity) whereas binary weighted capacitor array uses the least area but gives the worst linearity (as measured by this metric DNL, Differential Non-linearity) and radix < 2 weighted capacitor array uses an area in between binary and unitary and gives linearity as well in between binary and unitary weighted DNL.

[18] Although the invention has been described with reference to particular embodiment, it is to be understood that the embodiment is merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiment that other arrangements may be devised without departing from the scope of the present invention as defined by the appended claims.

Claims

[Claim 1] An analogue to digital converter comprising:
a comparator (100) for comparing input signal with a reference signal;
a successive approximation logic (200) that takes input from the comparator (100) for determining the digital output code; and
a digital to analogue converter block (300) including a plurality of capacitors that receives input from the successive approximation logic (200) block and generates reference signal that is applied to the comparator (100);
characterised in that
the digital to analogue converter block (300) further comprising a plurality of a binary weight (radix = 2) segment (1000), a (radix < 2) weight segment (2000) and a unitary weight (radix = 1) segment (3000) elements.

[Claim 2] An analogue to digital converter as claimed in Claim 1, wherein the segment elements further comprising: a binary to thermometer/unitary decoder for unitary weight segment (3000); and a binary to radix < 2 decoder for (radix < 2) weight segment (2000), wherein the input signal is compared with the signal charged on capacitors from plurality of digital to analogue converter block (300) capacitor beginning from the most significant bit down to the least significant bit.

[Claim 3] An analogue to digital converter as claimed in Claim 1, wherein the digital to analogue converter block (300) further comprising12 bit multi segmentdigital to analogue converter block(300) with 4 bit radix 1.6 weighted (2000), 4 bit unitary/thermometer weighted (3000), and 4 bit binary weighted (1000) capacitor array.

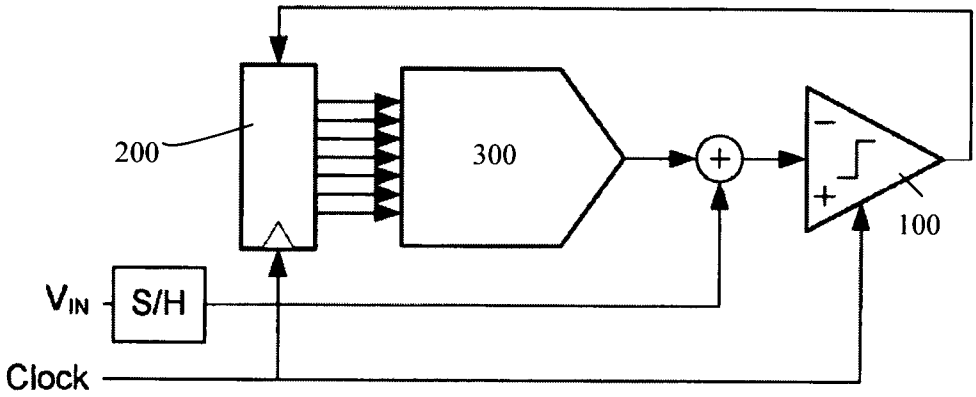


Figure 1

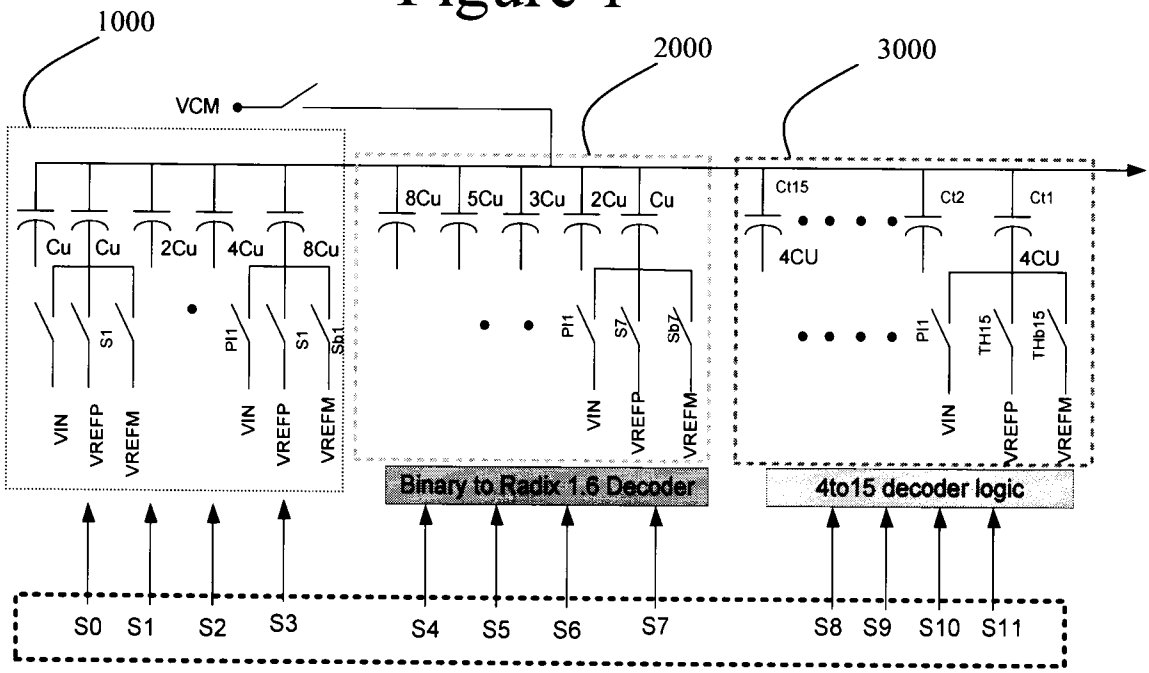


Figure 2

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2014/000097

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/06
ADD. H03M1/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7 812 757 B1 (WONG YAT TO WILLIAM [HK] ET AL) 12 October 2010 (2010-10-12) column 9, lines 19-34; figures 7,8 column 6, line 65 - column 7, line 6 -----	1-3
A	US 2012/200442 A1 (LI YUANFANG [US] ET AL) 9 August 2012 (2012-08-09) the whole document -----	2

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
30 October 2014	07/11/2014

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7812757 B1	12-10-2010	CN 101807923 A	18-08-2010
		US 7812757 B1	12-10-2010
US 2012200442 A1	09-08-2012	NONE	