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(54) **Code division multiple access communication system**

Kodeverteilvielfachzugriffsnachrichtenübertragungssystem

Système de communication par accés multiple par division de code

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Description

BACKGROUND OF THE INVENTION

[0001] The present invention generally pertains to Code Division Multiple Access (CDMA) communications, also known as spread-spectrum communications. More particularly, the present invention pertains to a system and method for providing a high capacity, CDMA communications system which provides for one or more simultaneous user bearer channels over a given radio frequency, allowing dynamic allocation of bearer channel rate while rejecting multipath interference.

DESCRIPTION OF THE RELEVANT ART

[0002] Providing quality telecommunication services to user groups which are classified as remote, such as rural telephone systems and telephone systems in underdeveloped countries, has proved to be a challenge in recent years. These needs have been partially satisfied by wireless radio services, such as fixed or mobile frequency division multiplex (FDM), frequency division multiple access (FDMA), time division multiplex (TDM), time division multiple access (TDMA) systems, combination frequency and time division systems (FD/TDMA), and other land mobile radio systems. Usually, these remote services are faced with more potential users than can be supported simultaneously by their frequency or spectral bandwidth capacity.

[0003] Recognizing these limitations, recent advances in wireless communications have used spread spectrum modulation techniques to provide simultaneous communication by multiple users. Spread spectrum modulation refers to modulating a information signal with a spreading code signal; the spreading code signal being generated by a code generator where the period Tc of the spreading code is substantially less than the period of the information data bit or symbol signal. The code may modulate the carrier frequency upon which the information has been sent, called frequency-hopped spreading, or may directly modulate the signal by multiplying the spreading code with the information data signal, called direct-sequence spreading (DS). Spread-spectrum modulation produces a signal with bandwidth substantially greater than that required to transmit the information signal. Synchronous reception and despreading of the signal at the receiver recovers the original information. A synchronous demodulator in the receiver uses a reference signal to synchronize the despreading circuits to the input spread-spectrum modulated signal to recover the carrier and information signals. The reference signal can be a spreading code which is not modulated by an information signal.

[0004] Spread-spectrum modulation in wireless networks offers many advantages because multiple users may use the same frequency band with minimal interference to each user's receiver. Spread-spectrum modulation also reduces effects from other sources of interference. In addition, synchronous spread-spectrum modulation and demodulation techniques may be expanded by providing multiple message channels for a single user, each spread with a different spreading code, while still transmitting only a single reference signal to the user.

[0005] One area in which spread-spectrum techniques are used is in the field of mobile cellular communications to provide personal communication services (PCS). Such systems desirably support large numbers of users, control Doppler shift and fade, and provide high speed digital data signals with low bit error rates. These systems employ a family of orthogonal or quasi-orthogonal spreading codes, with a pilot spreading code sequence synchronized to the family of codes. Each user is assigned one of the spreading codes as a spreading function. Related problems of such a system are: supporting a large number of users with the orthogonal codes, handling reduced power available to remote units, and handling multipath fading effects. Solutions to such problems include using phased-array antennas to generate multiple steerable beams, using very long orthogonal or quasi-orthogonal code sequences. These sequences may be reused by cyclic shifting of the code synchronized to a central reference, and diversity combining of multipath signals.

[0006] The problems associated with the prior art systems focus around reliable reception and synchronization of the receiver despreading circuits to the received signal. The presence of multipath fading introduces a particular problem with spread spectrum receivers in that a receiver must somehow track the multipath components to maintain code-phase lock of the receiver's despreading means with the input signal. Prior art receivers generally track only one or two of the multipath signals, but this method is not satisfactory because the combined group of low power multipath signal components may actually contain far more power than the one or two strongest multipath components. The prior art receivers track and combine the strongest components to maintain a predetermined Bit Error Rate (BER) of the receiver. Such a receiver is described, for example, in U.S. Patent 5,109,390 entitled DIVERSITY RECEIVER IN A CDMA CELLULAR TELEPHONE SYSTEM by Gilhousen et al. A receiver that combines all multipath components, however, is able to maintain the desired BER with a signal power that is lower than that of prior art systems because more signal power is available to the receiver. Consequently, there is a need for a spread spectrum communication system employing a receiver that tracks substantially all of the multipath signal components, so that substantially all multipath signals may be combined in the receiver, and hence the required transmit power of the signal for a given

BER may be reduced.

[0007] Another problem associated with multiple access, spread-spectrum communication systems is the need to reduce the total transmitted power of users in the system, since users may have limited available power. An associated problem requiring power control in spread-spectrum systems is related to the inherent characteristic of spread-spectrum systems that one user's spread-spectrum signal is received by another user's receiver as noise with a certain power level. Consequently, users transmitting with high levels of signal power may interfere with other users' reception. Also, if a user moves relative to another user's geographic location, signal fading and distortion require that the users adjust their transmit power level to maintain a particular signal quality. At the same time, the system should keep the power that the base station receives from all users relatively constant. Finally, because it is possible for the spread-spectrum system to have more remote users than can be supported simultaneously, the power control system should also employ a capacity management method which rejects additional users when the maximum system power level is reached.

[0008] Prior spread-spectrum systems have employed a base station that measures a received signal and sends an adaptive power control (APC) signal to the remote users. Remote users include a transmitter with an automatic gain control (AGC) circuit which responds to the APC signal. In such systems the base station monitors the overall system power or the power received from each user, and sets the APC signal accordingly. This open loop system performance may be improved by including a measurement of the signal power received by the remote user from the base station, and transmitting an APC signal back to the base station to effectuate a closed loop power control method.

[0009] These power control systems, however, exhibit several disadvantages. First, the base station must perform complex power control algorithms, increasing the amount of processing in the base station. Second, the system actually experiences several types of power variation: variation in the noise power caused by the variation in the number of users and variations in the received signal power of a particular bearer channel. These variations occur with different frequency, so simple power control algorithms can be optimized to compensate for only one of the two types of variation. Finally, these power algorithms tend to drive the overall system power to a relatively high level. Consequently, there is a need for a spread-spectrum power control method that rapidly responds to changes in bearer channel power levels, while simultaneously making adjustments to all users' transmit power in response to changes in the number of users. Also, there is a need for an improved spread-spectrum communication system employing a closed loop power control system which minimizes the system's overall power requirements while maintaining a sufficient BER at the individual remote receivers. In addition, such a system should control the initial transmit power level of a remote user and manage total system capacity.

[0010] Spread-spectrum communication systems desirably should support large numbers of users, each of which has at least one communication channel. In addition, such a system should provide multiple generic information channels to broadcast information to all users and to enable users to gain access to the system. Using prior art spread-spectrum systems this could only be accomplished by generating large numbers of spreading code sequences.

[0011] Further, spread-spectrum systems should use sequences that are orthogonal or nearly orthogonal to reduce the probability that a receiver locks to the wrong spreading code sequence or phase. However, generating such large families of code sequences with such properties is difficult. Also, generating large code families requires generating sequences which have a long period before repetition. Consequently, the time a receiver takes to achieve synchronization with such a long sequence is increased. Prior art spreading code generators often combine shorter sequences to make longer sequences, but such sequences may no longer be sufficiently orthogonal. Therefore, there is a need for an improved method for reliably generating large families of code sequences that exhibit nearly orthogonal characteristics and have a long period before repetition, but also include the benefit of a short code sequence that reduces the time to acquire and lock the receiver to the correct code phase. In addition, the code generation method should allow generation of codes with any period, since the spreading code period is often determined by parameters used such as data rate or frame size.

[0012] Another desirable characteristic of spreading code sequences is that the transition of the user data value occur at a transition of the code sequence values. Since data typically has a period which is divisible by 2^N, such a characteristic usually requires the code-sequence to be an even length of 2^N. However, code generators, as is well known in the art, generally use linear feedback shift registers which generate codes of length $2^N - 1$. Consequently, the spread-spectrum communication system should also generate spreading code sequences of even length.

[0013] Finally, the spread-spectrum communication system should be able to handle many different types of data, such as FAX, voiceband data, and ISDN, in addition to traditional voice traffic. To increase the number of users supported, many systems employ encoding techniques such as ADPCM to achieve "compression" of the digital telephone signal. FAX, ISDN and other data, however, require the channel to be a clear channel. Consequently, there is a need for a spread spectrum communication system that supports compression techniques that also dynamically modify the spread spectrum bearer channel between an encoded channel and a clear channel in response to the type of information contained in the user's signal.

[0014] US 5,022,049 describes apparatus for generating a complex composite code for fast acquisition by multiple users. Component codes of an in-phase composite code are derived from code generators in a quadrature channel.

When a first component code is correlated with an incoming signal, a code detect signal is generated at a code detector to provide an acquisition signal.

SUMMARY OF THE INVENTION

[0015] The present invention provides a fast acquisition apparatus for quickly synchronizing a spread code phase of a spread spectrum communication system according to claim 1. Further preferred aspects of the invention are provided according to the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016]

Figure 1 is a block diagram of a code division multiple access communication system according to the present invention.

Figure 2a is a block diagram of a 36 stage linear shift register suitable for use with long spreadingcode of the code generator of the present invention.

Figure 2b is a block diagram of circuitry which illustrates the feed-forward operation of the code generator.

Figure 2c is a block diagram of an exemplary code generator of the present invention including circuitry for generating spreading code sequences from the long spreading codes and the short spreading codes.

Figure 2d is an alternate embodiment of the code generator circuit including delay elements to compensate for electrical circuit delays.

Figure 3a is a graph of the constellation points of the pilot spreading code QPSK signal.

Figure 3b is a graph of the constellation points of the message channel QPSK signal.

Figure 3c is a block diagram of exemplary circuitry which implements the method of tracking the received spreading code phase of the present invention.

Figure 4 is a block diagram of the tracking circuit that tracks the median of the received multipath signal components.

Figure 5a is a block diagram of the tracking circuit that tracks the centroid of the received multipath signal components.

Figure 5b is a block diagram of the Adaptive Vector Correlator.

Figure 6 is a block diagram of exemplary circuitry which implements the acquisition decision method of the correct spreading code phase of the received pilot code of the present invention.

Figure 7 is a block diagram of an exemplary pilot rake filter which includes the tracking circuit and digital phase locked loop for despreading the pilot spreading code, and generator of the weighting factors of the present invention.

Figure 8a is a block diagram of an exemplary adaptive vector correlator and matched filter for despreading and combining the multipath components of the present invention.

Figure 8b is a block diagram of an alternative implementation of the adaptive vector correlator and adaptive matched filter for despreading and combining the multipath components of the present invention.

Figure 8c is a block diagram of an alternative embodiment of the adaptive vector correlator and adaptive matched filter for despreading and combining the multipath components of the present invention.

Figure 8d is a block diagram of the Adaptive Matched Filter of one embodiment of the present invention.

Figure 9 is a block diagram of the elements of an exemplary radio carrier station (RCS) of the present invention.

Figure 10 is a block diagram of the elements of an exemplary multiplexer suitable for use in the RCS shown in Figure 9.

Figure 11 is a block diagram of the elements of an exemplary wireless access controller (WAC) of the RCS shown in Figure 9.

Figure 12 is a block diagram of the elements of an exemplary modem interface unit (MIU) of the RCS shown in Figure 9.

Figure 13 is a high level block diagram showing the transmit, receive, control, and code generation circuitry of the CDMA modem.

Figure 14 is a block diagram of the transmit section of the CDMA modem.

Figure 15 is a block diagram of an exemplary modem input signal receiver.

Figure 16 is a block diagram of an exemplary convolutional encoder as used in the present invention.

Figure 17 is a block diagram of the receive section of the CDMA modem.

Figure 18 is a block diagram of an exemplary adaptive matched filter as used in the CDMA modem receive section.

Figure 19 is a block diagram of an exemplary pilot rake as used in the CDMA modem receive section.

Figure 20 is a block diagram of an exemplary auxiliary pilot rake as used in the CDMA modem receive section.

Figure 21 is a block diagram of an exemplary video distribution circuit (VDC) of the RCS shown in Figure 9.

Figure 22 is a block diagram of an exemplary RF transmitter/receiver and exemplary power amplifiers of the RCS shown in Figure 9.

Figure 23 is a block diagram of an exemplary subscriber unit (SU) of the present invention.

Figure 24 is a flow-chart diagram of an exemplary call establishment algorithm for an incoming call request used by the present invention for establishing a bearer channel between an RCS and an SU.

Figure 25 is a flow-chart diagram of an exemplary call establishment algorithm for an outgoing call request used by the present invention for establishing a bearer channel between an RCS and an SU.

Figure 26 is a flow-chart diagram of an exemplary maintenance power control algorithm of the present invention.

Figure 27 is a flow-chart diagram of an exemplary automatic forward power control algorithm of the present invention.

Figure 28 is a flow-cbart diagram of an exemplary automatic reverse power control algorithm of the present invention.

Figure 29 is a block diagram of an exemplary closed loop power control system of the present invention when the bearer channel is established.

Figure 30 is a block diagram of an exemplary closed loop power control system of the present invention during the process of establishing the bearer channel.

GLOSSARY OF ACRONYMS	
Acronym	Definition
AC	Assigned Channels
A/D	Analog-to-Digital
ADPCM	Adaptive Differential Pulse Code Modulation
AFPC	Automatic Forward Power Control
AGC	Automatic Gain Control
AMF	Adaptive Matched Filter
APC	Automatic Power Control
ARPC	Automatic Reverse Power Control
ASPT	Assigned Pilot
AVC	Adaptive Vector Correlator
AXCH	Access Channel
B-CDMA	Broadband Code Division Multiple Access
BCM	Bearer Channel Modification
BER	Bit Error Rate
BS	Base Station
CC	Call Control
CDM	Code Division Multiplex
CDMA	Code Division Multiple Access
CLK	Clock Signal Generator
CO	Central Office
CTCH	Control Channel
CUCH	Check-Up Channel
dB	Decibels
DCC	Data Combiner Circuitry
DI	Distribution Interface
DLL	Delay Locked Loop
DM	Delta Modulator
DS	Direct Sequence
EPIC	Extended PCM Interface Controller
FBCH	Fast Broadcast Channel
FDM	Frequency Division Multiplex
FD/TDMA	Frequency & Time Division Systems
FDMA	Frequency Division Multiple Access
FEC	Forward Error Correction
FSK	Frequency Shift Keying
FSU	Fixed Subscriber Unit
GC	Global Channel
GLPT	Global Pilot
GPC	Global Pilot Code
GPSK	Gaussian Phase Shift Keying
GPS	Global Positioning System
HPPC	High Power Passive Components
HSB	High Speed Bus
I	In-Phase
IC	Interface Controller
ISDN	Integrated Services Digital Network
ISST	Initial System Signal Threshold
LAXPT	Long Access Pilot

(continued)

GLOSSARY OF ACRONYMS	
Acronym	Definition
LAPD	Link Access Protocol
LCT	Local Craft Terminal
LE	Local Exchange
LFSR	Linear Feedback Shift Register'
LI	Line Interface
LMS	Least Mean Square
LOL	Loss of Code Lock
LPF	Low Pass Filter
LSR	Linear Shift Register
MISR	Modem Input Signal Receiver
MIU	Modem Interface Unit
MM	Mobility Management
MOI	Modem Output Interface
MPC	Maintenance Power Control
MPSK	M-ary Phase Shift Keying
MSK	Minimum Shift Keying
MSU	Mobile Subscriber Unit
NE	Network Element
OMS	Operation and Maintenance System
OS	Operations System
OQPSK	Offset Quadrature Phase Shift Keying
OW	Order Wire
PARK	Portable Access Rights Key
PBX	Private Branch Exchange
PCM	Pulse Coded Modulation
PCS	Personal Communication Services
PG	Pilot Generator
PLL	Phase Locked Loop
PLT	Pilot
PN	Pseudonoise
POTS	Plain Old Telephone Service
PSTN	Public Switched Telephone Network
Q	Quadrature
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RCS	Radio Carrier Station
RDI	Receiver Data Input Circuit
RDU	Radio Distribution Unit
RF	Radio Frequency
RLL	Radio Local Loop
SAXPT	Short Access Channel Pilots
SBCH	Slow Broadcast Channel
SHF	Super High Frequency
SIR	Signal Power to Interface Noise Power Ratio
SLIC	Subscriber Line Interface Circuit
SNR	Signal-to-Noise Ratio
SPC	Service PC
SPRT	Sequential Probability Ratio Test

(continued)

GLOSSARY OF ACRONYMS	
Acronym	Definition
STCH	Status Channel
SU	Subscriber Unit
TDM	Time Division Multiplexing
TMN	Telecommunication Management Network
TRCH	Traffic Channels
TSI	Time-Slot Interchanger
TX	Transmit
TXIDAT	I-Modem Transmit Data Signal
TXQDAT	Q-Modem Transmit Data Signal
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator
VDC	Video Distribution Circuit
VGA	Variable Gain Amplifier
VHF	Very High Frequency
WAC	Wireless Access Controller

DESCRIPTION OF THE EXEMPLARY EMBODIMENT

General System Description

[0017] The system of the present invention provides local-loop telephone service using radio links between one or more base stations and multiple remote subscriber units. In the exemplary embodiment, a radio link is described for a base station communicating with a fixed subscriber unit (FSU), but the system is equally applicable to systems including multiple base stations with radio links to both FSUs and Mobile Subscriber Units (MSUs). Consequently, the remote subscriber units are referred to herein as Subscriber Units (SUs).

[0018] Referring to Figure 1, Base Station (BS) 101 provides call connection to a local exchange (LE) 103 or any other telephone network switching interface, such as a private branch exchange (PBX) and includes a Radio Carrier Station (RCS) 104. One or more RCSs 104, 105, 110 connect to a Radio Distribution Unit (RDU) 102 through links 131, 132, 137, 138, 139, and RDU 102 interfaces with LE 103 by transmitting and receiving call set-up, control, and information signals through telco links 141, 142, 150. SUs 116, 119 communicate with the RCS 104 through radio links 161, 162, 163, 164, 165. Alternatively, another embodiment of the invention includes several SUs and a "master" SU with functionality similar to the RCS. Such an embodiment may or may not have connection to a local telephone network.

[0019] The radio links 161 to 165 operate within the frequency bands of the DCS 1800 standard (1.71 - 1.785 Ghz and 1.805 - 1.880 GHz); the US-PCS standard (1.85 - 1.99 Ghz); and the CEPT standard (2.0 -2.7 GHz). Although these bands are used in described embodiment, the invention is equally applicable to the entire UHF to SHF bands, including bands from 2.7 GHz to 5 GHz. The transmit and receive bandwidths are multiples of 3.5 MHz starting at 7 MHz, and multiples of 5 MHz starting at 10 MHz, respectively. The described system includes bandwidths of 7, 10, 10.5, 14 and 15 MHz. In the exemplary embodiment of the invention, the minimum guard band between the Uplink and Downlink is 20 MHz, and is desirably at least three times the signal bandwidth. The duplex separation is between 50 to 175 MHz, with the described invention using 50, 75, 80, 95, and 175 MHz. Other frequencies may also be used.

[0020] Although the described embodiment uses different spread-spectrum bandwidths centered around a carrier for the transmit and receive spread-spectrum channels, the present method is readily extended to systems using multiple spread-spectrum bandwidths for the transmit channels and multiple spread-spectrum bandwidths for the receive channels. Alternatively, because spread-spectrum communication systems have the inherent feature that one user's transmission appears as noise to another user's despreading receiver, an embodiment may employ the same spread-spectrum channel for both the transmit and receive path channels. In other words, Uplink and Downlink transmissions can occupy the same frequency band. Furthermore, the present method may be readily extended to multiple CDMA frequency bands, each conveying a respectively different set of messages, uplink, downlink or uplink and downlink.

[0021] The spread binary symbol information is transmitted over the radio links 161 to 165 using Quadrature Phase Shift Keying (QPSK) modulation with Nyquist Pulse Shaping in the present embodiment, although other modulation techniques may be used, including, but not limited to, Offset QPSK (OQPSK) and Minimum Shift Keying (MSK). Gaus-

sian Phase Shift Keying (GPSK) and M-ary Phase Shift Keying (MPSK)

[0022] The radio links 161 to 165 incorporate Broadband Code Division Multiple Access (B-CDMA™) as the mode of transmission in both the Uplink and Downlink directions. CDMA (also known as Spread Spectrum) communication techniques used in multiple access systems are well-known, and are described in U.S. Patent 5,228,056 entitled SYNCHRONOUS SPREAD-SPECTRUM COMMUNICATION SYSTEM AND METHOD by Donald T Schilling. The system described utilizes the Direct Sequence (DS) spreading technique. The CDMA modulator performs the spread-spectrum spreading code sequence generation, which can be a pseudonoise (PN) sequence; and complex DS modulation of the QPSK signals with spreading code sequences for the In-phase (I) and Quadrature (Q) channels. Pilot signals are generated and transmitted with the modulated signals, and pilot signals of the present embodiment are spreading codes not modulated by data. The pilot signals are used for synchronization, carrier phase recovery, and for estimating the impulse response of the radio channel. Each SU includes a single pilot generator and at least one CDMA modulator and demodulator, together known as a CDMA modem. Each RCS 104, 105, 110 has a single pilot generator plus sufficient CDMA modulators and demodulators for all of the logical channels in use by all SUs.

[0023] The CDMA demodulator despreads the signal with appropriate processing to combat or exploit multipath propagation effects. Parameters concerning the received power level are used to generate the Automatic Power Control (APC) information which, in turn, is transmitted to the other end of the communication link. The APC information is used to control transmit power of the automatic forward power control (AFPC) and automatic reverse power control (ARPC) links. In addition, each RCS 104, 105 and 110 can perform Maintenance Power Control (MPC), in a manner similar to APC, to adjust the initial transmit power of each SU 111, 112, 115, 117 and 118. Demodulation is coherent where the pilot signal provides the phase reference.

[0024] The described radio links support multiple traffic channels with data rates of 8, 16, 32, 64, 128, and 144 kb/s. The physical channel to which a traffic channel is connected operates with a 64k symbol/sec rate. Other data rates may be supported, and Forward Error Correction (FEC) coding can be employed. For the described embodiment, FEC with coding rate of 1/2 and constraint length 7 is used. Other rates and constraint lengths can be used consistent with the code generation techniques employed.

[0025] Diversity combining at the radio antennas of RCS 104, 105 and 110 is not necessary because CDMA has inherent frequency diversity due to the spread bandwidth. Receivers include Adaptive Matched Filters (AMFs) (not shown in Figure 1) which combine the multipath signals. In the present embodiment, the exemplary AMFs perform Maximal Ratio Combining.

[0026] Referring to Figure 1, RCS 104 interfaces to RDU 102 through links 131, 132, 137 with, for example, 1.544 Mb/s DS1, 2.048 Mb/s E1; or HDSL Formats to receive and send digital data signals. While these are typical telephone company standardized interfaces, the present invention is not limited to these digital data formats only. The exemplary RCS line interface (not shown in Figure 1) translates the line coding (such as HDB3, B8ZS, AMI) and extracts or produces framing information, performs Alarms and Facility signaling functions, as well as channel specific loop-back and parity check functions. The interfaces for this description provide 64 kb/s PCM encoded or 32 kb/s ADPCM encoded telephone traffic channels or ISDN channels to the RCS for processing. Other ADPCM encoding techniques can be used consistent with the sequence generation techniques.

[0027] The system of the present invention also supports bearer rate modification between the RCS 104 and each SU 111, 112, 115, 117 and 118 communicating with RCS 104 in which a CDMA message channel supporting 64 kb/s may be assigned to voiceband data or FAX when rates above 4.8 kb/s are present. Such 64 kb/s bearer channel is considered an unencoded channel. For ISDN, bearer rate modification may be done dynamically, based upon the D channel messages.

[0028] In Figure 1, each SU 111, 112, 115, 117 and 118 either includes or interfaces with a telephone unit 170, or interfaces with a local switch (PBX) 171. The input from the telephone unit may include voice, voiceband data and signaling. The SU translates the analog signals into digital sequences, and may also include a Data terminal 172 or an ISDN interface 173. The SU can differentiate voice input, voiceband data or FAX and digital data. The SU encodes voice data with techniques such as ADPCM at 32 kb/s or lower rates, and detects voiceband data or FAX with rates above 4.8 kb/s to modify the traffic channel (bearer rate modification) for unencoded transmission. Also, A-law, u-law, or no companding of the signal may be performed before transmission. For digital data, data compression techniques, such as idle flag removal, may also be used to conserve capacity and minimize interference.

[0029] The transmit power levels of the radio interface between RCS 104 and SUs 111, 112, 115, 117 and 118 are controlled using two different closed loop power control methods. The Automatic Forward Power Control (AFPC) method determines the Downlink transmit power level, and the Automatic Reverse Power Control (ARPC) method determines the Uplink transmit power level. The logical control channel by which SU 111 and RCS 104, for example, transfer power control information operates at least a 16 kHz update rate. Other embodiments may use a faster or slower update rate for example 64 kHz. These algorithms ensure that the transmit power of a user maintains an acceptable Bit-Error Rate (BER), maintains the system power at a minimum to conserve power, and maintains the power level of all SUs 111, 112, 115, 117 and 118 received by RCS 104 at a nearly equal level.

[0030] In addition, the system uses an optional maintenance power control method during the inactive mode of a SU. When SU 111 is inactive or powered-down to conserve power, the unit occasionally activates to adjust its initial transmit power level setting in response to a maintenance power control signal from RCS 104. The maintenance power signal is determined by the RCS 104 by measuring the received power level of SU 111 and present system power level and, from this, calculates the necessary initial transmit power. The method shortens the channel acquisition time of SU 111 to begin a communication. The method also prevents the transmit power level of SU 111 from becoming too high and interfering with other channels during the initial transmission before the closed loop power control reduces the transmit power.

[0031] RCS 104 obtains synchronization of its clock from an interface line such as, but not limited to, E1, T1, or HDSL interfaces. RCS 104 can also generate its own internal clock signal from an oscillator which may be regulated by a Global Positioning System (GPS) receiver. RCS 104 generates a Global Pilot Code, a channel with a spreading code but no data modulation, which can be acquired by remote SUs 111 through 118. All transmission channels of the RCS are synchronized to the Pilot channel, and spreading code phases of code generators (not shown) used for Logical communication channels within RCS 104 are also synchronized to the Pilot channel's spreading code phase. Similarly, SUs 111 through 118 which receive the Global Pilot Code ofRCS 104 synchronize the spreading and de-spreading code phases of the code generators (not shown) of the SUs to the Global Pilot Code.

[0032] RCS 104, SU 111, and RDU 102 may incorporate system redundancy of system elements and automatic switching between internal functional system elements upon a failure event to prevent loss or drop-out of a radio link, power supply, traffic channel, or group of traffic channels.

Logical Communication Channels

[0033] A 'channel' of the prior art is usually regarded as a communications path which is part of an interface and which can be distinguished from other paths of that interface without regard to its content. However, in the case of CDMA, separate communications paths are distinguished only by their content. The term 'logical channel' is used to distinguish the separate data streams, which are logically equivalent to channels in the conventional sense. All logical channels and sub-channels of the present invention are mapped to a common 64 kilo-symbols per second (ksym/s) QPSK stream. Some channels are synchronized to associated pilot codes which are generated from, and perform a similar function to the system Global Pilot Code (GPC). The system pilot signals are not, however, considered logical channels.

[0034] Several logical communication channels are used over the RF communication link between the RCS and SU. Each logical communication channel either has a fixed, pre-determined spreading code or a dynamically assigned spreading code. For both pre-determined and assigned codes, the code phase is synchronized with the Pilot Code. Logical communication channels are divided into two groups: the Global Channel (GC) group includes channels which are either transmitted from the base station RCS to all remote SUs or from any SU to the RCS of the base station regardless of the SU's identity. The channels in the GC group may contain information of a given type for all users including those channels used by SUs to gain system access. Channels in the Assigned Channels (AC) group are those channels dedicated to communication between the RCS and a particular SU.

[0035] The Global Channels (GC) group provides for 1) Broadcast Control logical channels, which provide point to multipoint services for broadcasting messages to all SUs and paging messages to SUs; and 2) Access Control logical channels which provide point-to-point services on global channels for SUs to access the system and obtain assigned channels.

[0036] The RCS of the present invention has multiple Access Control logical channels, and one Broadcast Control group. An SU of the present invention has at least one Access Control channel and at least one Broadcast Control logical channel.

[0037] The Global logical channels controlled by the RCS are the Fast Broadcast Channel (FBCH) which broadcasts fast changing information concerning which services and which access channels are currently available, and the Slow Broadcast Channel (SBCH) which broadcasts slow changing system information and paging messages. The Access Channel (AXCH) is used by the SUs to access an RCS and gain access to assigned channels. Each AXCH is paired with a Control Channel (CTCH). The CTCH is used by the RCS to acknowledge and reply to access attempts by SUs. The Long Access Pilot (LAXPT) is transmitted synchronously with AXCH to provide the RCS with a time and phase reference.

[0038] An Assigned Channel (AC) group contains the logical channels that control a single telecommunication connection between the RCS and an SU. The functions developed when an AC group is formed include a pair of power control logical message channels for each of the Uplink and Downlink connections, and depending on the type of connection, one or more pairs of traffic channels. The Bearer Control function performs the required forward error control, bearer rate modification, and encryption functions.

[0039] Each SU 111, 112, 115, 117 and 118 has at least one AC group formed when a telecommunication connection

exists, and each RCS 104, 105 and 110 has multiple AC groups formed, one for each connection in progress. An AC group of logical channels is created for a connection upon successful establishment of the connection. The AC group includes encryption, FEC coding, and multiplexing on transmission, and FEC decoding, decryption and demultiplexing on reception.

[0040] Each AC group provides a set of connection oriented point-to-point services and operates in both directions between a specific RCS, for example, RCS 104 and a specific SU, for example, SU 111. An AC group formed for a connection can control more than one bearer over the RF communication channel associated with a single connection. Multiple bearers are used to carry distributed data such as, but not limited to, ISDN. An AC group can provide for the duplication of traffic channels to facilitate switch over to 64 kb/s PCM for high speed facsimile and modem services for the bearer rate modification function.

[0041] The assigned logical channels formed upon a successful call connection and included in the AC group are a dedicated signaling channel [order wire (OW)], an APC channel, and one or more Traffic channels (TRCH) which are bearers of 8, 16, 32, pr 64 kb/s depending on the service supported. For voice traffic, moderate rate coded speech, ADPCM, or PCM can be supported on the Traffic channels. For ISDN service types, two 64 kb/s TRCHs form the B channels and a 16 kb/s TRCH forms the D channel. Alternatively, the APC subchannel may either be separately modulated on its own CDMA channel, or may be time division multiplexed with a traffic channel or OW channel.

[0042] Each SU 111, 112, 115, 117 and 118 of the present invention supports up to three simultaneous traffic channels. The mapping of the three logical channels for TRCHs to the user data is shown below in Table 1:

Table 1:

Mapping of service types to the three available TRCH channels			
Service	**TRCH(0)**	**TRCH(1)**	**TRCH(2)**
16 kb/s POTS	TRCH /16	not used	not used
32 + 64 kb/s POTS (during BCM)	TRCH /32	TRCH /64	not used
32 kb/s POTS	TRCH /32	not used	not used
64 kb/s POTS	not used	TRCH /64	not used
ISDN D	not used	not used	TRCH /16
ISDN B+D	TRCH /64	not used	TRCH /16
ISDN 2B + D	TRCH /64	TRCH /64	TRCH /16
Digital LL @ 64 kb/s	TRCH /64	not used	not used
Digital LL @ 2 x 64 kb/s	TRCH /64	TRCH /64	not used
Analog LL @ 64 kb/s	TRCH/64	not used	not used

[0043] The APC data rate is sent at 64 kb/s. The APC logical channel is not FEC coded to avoid delay and is transmitted at a relatively low power level to minimize capacity used for APC. Alternatively, the APC and OW may be separately modulated using complex spreading code sequences, or they may be time division multiplexed.

[0044] The OW logical channel is FEC coded with a rate 1/2 convolutional code. This logical channel is transmitted in bursts when signaling data is present to reduce interference. After an idle period, the OW signal begins with at least 35 symbols prior to the start of the data frame. For silent maintenance call data, the OW is transmitted continuously between frames of data. Table 2 summarizes the logical channels used in the exemplary embodiment:

Table 2:

Logical Channels and sub-channels of the B-CDMA Air Interface							
Channel name	Abbr.	Brief Description	Direction (forward or reverse)	Bit rate	Max BER	Power level	Pilot
Global Channels							
Fast Broadcast Channel	FBCH	Broadcasts fast-changing system information	F	16 kb/s	1e-4	Fixed	GLPT
Slow Broadcast Channel	SBCH	Broadcasts paging messages to FSUs and slow-changing system information	F	16 kb/s	1e-7	Fixed	GLPT
Access Channels	AXCH(i)	For initial access attempts by FSUs	R	32 kh/s	1e-7	Controlled by APC	LAXPT(i)
Control Channels	CTCH(i)	For granting access	F	32 kb/s	1e-7	Fixed	GLPT
Assigned Channels							
16 kb/s POTS	TRCH /16	General POTS use	F/R	16 kb/s	1e-4	Controlled by APC	F-GLPT R-ASPT
32 kb/s POTS	TRCH /32	General POTS use	F/R	32 kb/s	1e-4	Controlled by APC	F-GLPT R-ASPT
64 kb/s POTS	TRCH /64	POTS use for in-band modems/ fax	F/R	64 kb/s	1e-4	Controlled by APC	F-GLPT R-ASPT
Channel name	Abbr.	Brief Description	Direction (forward or reverse)	Bit rate	Max BER	Power level	Pilot
D channel	TRCH /16	ISDN D channel	F/R	16 kb/s	1e-7	Controlled by APC	F-GLPT R-ASPT
Order wire channel	OW	assigned signaling channel	FIR	32 kb/s	1e-7	Controlled by APC	F-GLPT R-ASPT
APC channel	APC	carries APC commands	F/R	64 kb/s	2e-1	Controlled by APC	F-GLPT R-ASPT

The Spreading Codes

[0045] The CDMA code generators used to encode the logical channels of the present invention employ Linear Shift Registers (LSRs) with feedback logic which is a method well known in the art. The code generators of the present embodiment of the invention generate 64 synchronous unique sequences. Each RF communication channel uses a

pair of these sequences for complex spreading (in-phase and quadrature) of the logical channels, so the generator gives 32 complex spreading sequences. The sequences are generated by a single seed which is initially loaded into a shift register circuit.

The Generation of Spreading Code Sequences and Seed Selection

[0046] The spreading code period of the present invention is defined as an integer multiple of the symbol duration, and the beginning of the code period is also the beginning of the symbol. The relation between bandwidths and the symbol lengths chosen for the exemplary embodiment of the present invention is:

BW (MHZ)	L(chips/ symbol)
7	91
10	130
10.5	133
14	182
15	195

[0047] The spreading code length is also a multiple of 64 and of 96 for ISDN frame support. The spreading code is a sequence of symbols, called chips or chip values. The general methods of generating pseudorandom sequences using Galois Field mathematics is known to those skilled in the art; however, a unique set, or family, of code sequences has been derived for the present invention. First, the length of the linear feedback shift register to generate a code sequence is chosen, and the initial value of the register is called a "seed". Second, the constraint is imposed that no code sequence generated by a code seed may be a cyclic shift of another code sequence generated by the same code seed. Finally, no code sequence generated from one seed may be a cyclic shift of a code sequence generated by another seed.

[0048] It has been determined that the spreading code length of chip values of the present invention is:

$$128 \times 233415 = 29877120 \quad (1)$$

The spreading codes are generated by combining a linear sequence of period 233415 and a nonlinear sequence of period 128

[0049] The FBCH channel of the exemplary embodiment is an exception because it is not coded with the 128 length sequence, so the FBCH channel spreading code has period 233415.

[0050] The nonlinear sequence of length 128 is implemented as a fixed sequence loaded into a shift register with a feed-back connection. The fixed sequence can be generated by an m-sequence of length 127 padded with an extra logic 0, 1, or random value as is well known in the art.

[0051] The linear sequence of length L=233415 is generated using a linear feedback shift register (LFSR) circuit with 36 stages. The feedback connections correspond to a irreducible polynomial h(n) of degree 36. The polynomial h(x) chosen for the exemplary embodiment of the present invention is

$$h(x)=x^{36}+x^{35}+x^{30}+x^{28}+x^{26}+x^{25}+x^{22}+x^{20}+x^{19}+x^{17}$$
$$+x^{16}+x^{15}+x^{14}+x^{12}+x^{11}+x^{9}+x^{8}+x^{4}+x^{3}+x^{2}+1$$

or, in binary notation

$$h(x)=(1100001010110010110111101101100011101) \quad (2)$$

[0052] A group of "seed" values for a LFSR representing the polynomial h(x) of equation (2) which generates code sequences that are nearly orthogonal with each other is determined. The first requirement of the seed values is that the seed values do not generate two code sequences which are simply cyclic shifts of each other.

[0053] The seeds are represented as elements of $GF(2^{36})$ which is the field of residue classes modulo h(x). This

field has a primitive element $\delta = x^2 + x + 1$. The binary representation of δ is

$$\delta = 00000000000000000000000000000111 \quad (3)$$

[0054] Every element of $GF(2^{36})$ can also be written as a power of δ reduced modulo h(x). Consequently, the seeds are represented as powers of δ, the primitive element.

[0055] The solution for the order of an element does not require a search of all values; the order of an element divides the order of the field ($GF(2^{36})$). When δ is any element of $GF(2^{36})$ with

$$x^e \equiv 1 \quad (4)$$

for some e, then $e | 2^{36}-1$. Therefore, the order of any element in $GF(2^{36})$ divides $2^{36}-1$.

[0056] Using these constraints, it has been determined that a numerical search generates a group of seed values, n, which are powers of δ, the primitive element of h(x).

[0057] The present invention includes a method to increase the number of available seeds for use in a CDMA communication system by recognizing that certain cyclic shifts of the previously determined code sequences may be used simultaneously. The round trip delay for the cell sizes and bandwidths of the present invention are less than 3000 chips. In one embodiment of the present invention, sufficiently separated cyclic shifts of a sequence can be used within the same cell without causing ambiguity for a receiver attempting to determine the code sequence. This method enlarges the set of sequences available for use.

[0058] By implementing the tests previously described, a total of 3879 primary seeds were determined through numerical computation. These seeds are given mathematically as

$$\delta^n \text{ modulo } h(x) \quad (5)$$

where 3879 values of n are listed in the Appendix A, with δ = (00,...00111) as before in (3).

[0059] When all primary seeds are known, all secondary seeds of the present invention are derived from the primary seeds by shifting them multiples of 4095 chips modulo h(x). Once a family of seed values is determined, these values are stored in memory and assigned to logical channels as necessary. Once assigned, the initial seed value is simply loaded into LFSR to produce the required spreadingcode sequence associated with the seed value.

Rapid Acquisition Feature of Long and Short codes.

[0060] Rapid acquisition of the correct code phase by a spread-spectrum receiver is improved by designing spreading codes which are faster to detect. The present embodiment of the invention includes a new method of generating code sequences that have rapid acquisition properties by using one or more of the following methods. First, a long code may be constructed from two or more short codes. The new implementation uses many code sequences, one or more of which are rapid acquisition sequences of length L that have average acquisition phase searches r=log2L. Sequences with such properties are well known to those practiced in the art. The average number of acquisition test phases of the resulting long sequence is a multiple of r=log2L rather than half of the number of phases of the long sequence.

[0061] Second, a method of transmitting complex valued spreading code sequences (In-phase (I) and Quadrature (Q) sequences) in a pilot spreading code signal may be used rather than transmitting real valued sequences. Two or more separate code sequences may be transmitted over the complex channels. If the sequences have different phases, an acquisition may be done by acquisition circuits in parallel over the different code sequences when the relative phase shift between the two or more code channels is known. For example, for two sequences, one can be sent on an In phase (I) channel and one on the Quadrature (Q) channel. To search the code sequences, the acquisition detection means searches the two channels, but begins the (Q) channel with an offset equal to one-half of the spreading code sequence length. With code sequence length of N, the acquisition means starts the search at N/2 on the (Q) channel. The average number of tests to find acquisition is N/2 for a single code search, but searching the (I) and phase delayed (Q) channel in parallel reduces the average number of tests to N/4. The codes sent on each channel could be the same code, the same code with one channel's code phase delayed, or different code sequences.

Epoch and Sub-epoch Structures

[0062] The long complex spreading codes used for the exemplary system of the present invention have a number of chips after which the code repeats. The repetition period of the spreading sequence is called an epoch. To map the logical channels to CDMA spreading codes, the present invention uses an Epoch and Sub-epoch structure. The code period for the CDMA spreading code to modulate logical channels is 29877120 chips/code period which is the same number of chips for all bandwidths. The code period is the epoch of the present invention, and Table 3 below defines the epoch duration for the supported chip rates. In addition, two sub-epochs are defined over the spreading code epoch and are 233415 chips and 128 chips long.

[0063] The 233415 chip sub-epoch is referred to as a long sub-epoch, and is used for synchronizing events on the RF communication interface such as encryption key switching and changing from global to assigned codes. The 128 chip short epoch is defined for use as an additional timing reference. The highest symbol rate used with a single CDMA code is 64 ksym/s. There is always an integer number of chips in a symbol duration for the supported symbol rates 64, 32, 16, and 8 ksym/s.

Table 3

Bandwidths, Chip Rates, and Epochs					
Bandwidth (MHz)	Chip Rate, Complex (Mchip/sec)	number of chips in a 64 kbit/sec symbol	128 chip sub-epoch duration* (μs)	233415 chip sub-epoch duration* (ms)	Epoch duration (sec)
7	5.824	91	21.978	40.078	5.130
10	8.320	130	15.385	28.055	3.591
10.5	8.512	133	15.038	27.422	3.510
14	11.648	182	10.989	20.039	2.565
15	12.480	195	10.256	18.703	2.394

* numbers in these columns are rounded to 5 digits.

Mapping of the Logical Channels to Epochs and Sub-epochs

[0064] The complex spreading codes are designed such that the beginning of the sequence epoch coincides with the beginning of a symbol for all of the bandwidths supported. The present invention supports bandwidths of 7, 10, 10.5, 14, and 15 MHz. Assuming nominal 20% roll-off, these bandwidths correspond to the following chip rates in Table 4.

Table 4:

Supported Bandwidths and Chip Rates for CDMA.				
BW (MHz)	R_c (Complex Mchips/sec)	Excess BW, %	L:(R_c/L)=64k	Factorization of *L*
7	5.824	20.19	91	7X13
10	8.320	20.19	130	2X5X13
10.5	8.512	23.36	133	7X19
14	11.648	20.19	182	2X7X13
15	12.480	20.19	195	3X5X13

The number of chips in an epoch is:

$$N = 29877120 = 2^7 x 3^3 x 5 x 7 x 13 x 19 \quad (6)$$

[0065] If interleaving is used, the beginning of an interleaver period coincides with the beginning of the sequence epoch. The spreading sequences generated using the method of the present invention can support interleaver periods that are multiples of 1.5 ms for various bandwidths.

[0066] Cyclic sequences of the prior art are generated using linear feedback shift register (LFSR) circuits. However, this method does not generate sequences of even length. One embodiment of the spreading code sequence generator using the code seeds generated previously is shown in Figure 2a, Figure 2b, and Figure 2c. The present invention uses a 36 stage LFSR 201 to generate a sequence of period $N'=233415=3^3x5x7x13x19$, which is C_o in Figure 2a. In Figures 2a, 2b, and 2c, the symbol ⊕ represents a binary addition (EXCLUSIVE-OR). A sequence generator designed as above generates the in-phase and quadrature parts of a set of complex sequences. The tap connections and initial state of the 36 stage LFSR determine the sequence generated by this circuit. The tap coefficients of the 36 stage LFSR are determined such that the resulting sequences have the period 233415. Note that the tap connections shown in Figure 2a correspond to the polynomial given in equation (2). Each resulting sequence is then overlaid by binary addition with the 128 length sequence C• to obtain the epoch period 29877120.

[0067] Figure 2b shows a Feed Forward (FF) circuit 202 which is used in the code generator. The signal X[n-1] is output of the chip delay 211, and the input of the chip delay 211 is X[n]. The code chip C[n] is formed by the logical adder 212 from the input X[n] and X[n-1]. Figure 2c shows the complete spreadingcode generator. From the LFSR 201, output signals go through a chain of up to 63 single stage FFs 203 cascaded as shown. The output of each FF is overlaid with the short, even code sequence C • period $128=2^7$ which is stored in code memory 222 and which exhibits spectral characteristics of a pseudorandom sequence to obtain the epoch N=29877120. This sequence of 128 is determined by using an m-sequence (PN sequence) of length $127=2^7$ -1 and adding a bit-value, such as logic 0, to the sequence to increase the length to 128 chips. The even code sequence C • is input to the even code shift register 221, which is a cyclic register, that continually outputs the sequence. The short sequence is then combined with the long sequence using an EXCLUSIVE-OR operation 213, 214, 220.

[0068] As shown in Figure 2c, up to 63 spreadingcode sequences C_o through C_{63} are generated by tapping the output signals of FFs 203 and logically adding the short sequence C• in binary adders 213, 214, and 220, for example. One skilled in the art would realize that the implementation of FF 203 will create a cumulative delay effect for the code sequences produced at each FF stage in the chain. This delay is due to the nonzero electrical delay in the electronic components of the implementation. The timing problems associated with the delay can be mitigated by inserting additional delay elements into the FF chain in one version of the embodiment of the invention. The FF chain of Figure 2c with additional delay elements is shown in Figure 2d.

[0069] The code-generators in the exemplary embodiment of the present invention are configured to generate either global codes, or assigned codes. Global codes are CDMA codes that can be received or transmitted by all users of the system. Assigned codes are CDMA codes that are allocated for a particular connection. When a set of sequences are generated from the same generator as described, only the seed of the 36 stage LFSR is specified to generate a family of sequences. Sequences for all the global codes, are generated using the same LFSR circuit. Therefore, once an SU has synchronized to the Global pilot signal from an RCS and knows the seed for the LFSR circuit for the Global Channel codes, it can generate not only the pilot sequence but also all other global codes used by the RCS.

[0070] The signal-that is upconverted to RF is generated as follows. The output signals of the above shift register circuits are converted to an antipodal sequence (0 maps into +1, 1 maps into -1). The Logical channels are initially converted to QPSK signals, which are mapped as constellation points as is well known in the art. The In-phase and Quadrature channels of each QPSK signal form the real and imaginary parts of the complex data value. Similarly, two spreading codes are used to form complex spreading chip values. The complex data are spread by being multiplied by the complex spreading code. Similarly, the received complex data is correlated with the conjugate of the complex spreading code to recover despread data.

Short Codes

[0071] Short codes are used for the initial ramp-up process when an SU accesses an RCS. The period of the short codes is equal to the symbol duration and the start of each period is aligned with a symbol boundary. Both SU and RCS derive the real and imaginary parts of the short codes from the last eight feed-forward sections of the sequence generator producing the global codes for that cell.

[0072] The short codes that are in use in the exemplary embodiment of the invention are updated every 3 ms. Other update times that are consistent with the symbol rate may be used. Therefore, a change-over occurs every 3 ms starting from the epoch boundary. At a change-over, the next symbol length portion of the corresponding feed-forward output becomes the short code. When the SU needs to use a particular short code, it waits until the first 3 ms boundary of the next epoch and stores the next symbol length portion output from the corresponding FF section. This shall be used as the short code until the next change-over, which occurs 3 ms later.

[0073] The signals represented by these short codes are known as Short Access Channel pilots (SAXPTs).

Mapping of Logical Channels to Spreading Codes

[0074] The exact relationship between the spreading code sequences and the CDMA logical channels and pilot signals is documented in Table 5a and Table 5b. Those signal names ending in '-CH' correspond to logical channels. Those signal names ending in '-PT' correspond to pilot signals, which are described in detail below.

Table 5a:

Spreading code sequences and global CDMA codes			
Sequence	Quadrature	Logical Channel or Pilot Signal	Direction
C_0	I	FBCH	Forward (F)
C_1	Q	FBCH	F
$C_2 \oplus C^*$	I	GLPT	F
$C_3 \oplus C^*$	Q	GLPT	F
$C_4 \oplus C^*$	I	SBCH	F
$C_5 \oplus C^*$	Q	SBCH	F
$C_6 \oplus C^*$	I	CTCH (0)	F
$C_7 \oplus C^*$	Q	CTCH (0)	F
$C_8 \oplus C^*$	I	APCH (1)	F
$C_9 \oplus C^*$	Q	APCH (1)	F
$C_{10} \oplus C\bullet$	I	CTCH (1)	F
$C_{11} \oplus C\bullet$	Q	CTCH (1)	F
$C_{12} \oplus C\bullet$	I	APCH (1)	F
$C_{13} \oplus C\bullet$	Q	APCH (1)	F
$C_{14} \oplus C\bullet$	I	CTCH (2)	F
$C_{15} \oplus C\bullet$	Q	CTCH (2)	F
$C_{16} \oplus C\bullet$	I	APCH (2)	F
$C_{17} \oplus C\bullet$	Q	APCH (2)	F
$C_{18} \oplus C\bullet$	I	CTCH (3)	F
$C_{19} \oplus C\bullet$	Q	CTCH (3)	F
$C_{20} \oplus C\bullet$	I	APCH (3)	F
$C_{21} \oplus C\bullet$	Q	APCH (3)	F
$C_{22} \oplus C\bullet$	I	reserved	-
$C_{23} \oplus C\bullet$	Q	reserved	-
. . . .	. . . .	. . . .	. . . .
. . . .	. . . .	. . . .	. . . .
$C_{40} \oplus C\bullet$	I	reserved	-
$C_{41} \oplus C\bullet$	Q	reserved	-
$C_{42} \oplus C\bullet$	I	AXCH(3)	Reverse (R)
$C_{43} \oplus C\bullet$	Q	AXCH(3)	R
$C_{44} \oplus C\bullet$	I	LAXPT(3) SAXPT(3) seed	R
$C_{45} \oplus C\bullet$	Q	LAXPT(3) SAXPT(3) seed	R
$C_{46} \oplus C\bullet$	I	AXCH(2)	R

Table 5a: (continued)

Spreading code sequences and global CDMA codes			
Sequence	Quadrature	Logical Channel or Pilot Signal	Direction
$C_{47}\oplus C\bullet$	Q	AXCH(2)	R
$C_{48}\oplus C\bullet$	I	LAXPT(2) SAXPT(2) seed	R
$C_{49}\oplus C\bullet$	Q	LAXPT(2) SAXPT(2) seed	R
$C_{50}\oplus C\bullet$	I	AXCH(1)	R
$C_{51}\oplus C\bullet$	Q	AXCH(1)	R
$C_{52}\oplus C\bullet$	I	LAXPT(1) SAXPT(1) seed	R
$C_{53}\oplus C\bullet$	Q	LAXPT(1) SAXPT(1) seed	R
$C_{54}\oplus C\bullet$	I	AXCH(0)	R
$C_{55}\oplus C\bullet$	Q	AXCH(0)	R

Table 5b:

Spreading code sequences and assigned CDMA codes.			
Sequence	Quadrature	Logical Channel or Pilot Signal	Direction
$C_0\oplus C\bullet$	I	ASPT	Reverse (R)
$C_1\oplus C\bullet$	Q	ASPT	R
$C_2\oplus C\bullet$	I	APCH	R
$C_3\oplus C\bullet$	Q	APCH	R
$C_4\oplus C\bullet$	I	OWCH	R
$C_5\oplus C\bullet$	Q	OWCH	R
$C_6\oplus C\bullet$	I	TRCH(0)	R
$C_7\oplus C\bullet$	Q	TRCH(0)	R
$C_8\oplus C\bullet$	I	TRCH(1)	R
$C_9\oplus C$	Q	TRCH(1)	R
$C_{10}\oplus C\bullet$	I	TRCH(2)	R
$C_{11}\oplus C\bullet$	Q	TRCH(2)	R
$C_{12}\oplus C\bullet$	I	TRCH(3)	R
$C_{13}\oplus C\bullet$	Q	TRCH(3)	R
$C_{14}\oplus C\bullet$	I	reserved	-
$C_{15}\oplus C\bullet$	Q	reserved	-
. . . .	. . . .	. . . .	. . . .
. . . .	. . . .	. . . .	. . . .
$C_{44}\oplus C\bullet$	I	reserved	-
$C_{45}\oplus C\bullet$	Q	reserved	-
$C_{46}\oplus C\bullet$	I	TRCH(3)	Forward (F)
$C_{47}\oplus C\bullet$	Q	TRCH(3)	F
$C_{48}\oplus C\bullet$	I	TRCH(2)	F
$C_{49}\oplus C\bullet$	Q	TRCH(2)	F

Table 5b: (continued)

Spreading code sequences and assigned CDMA codes.			
Sequence	Quadrature	Logical Channel or Pilot Signal	Direction
$C_{50}\oplus C\bullet$	I	TRCH(1)	F
$C_{51}\oplus C\bullet$	Q	TRCH(1)	F
$C_{52}\oplus C\bullet$	I	TRCH(0)	F
$C_{53}\oplus C\bullet$	Q	TRCH(0)	F
$C_{54}\oplus C\bullet$	I	OWCH	F
$C_{55}\oplus C\bullet$	Q	OWCH	F
$C_{56}\oplus C\bullet$	I	APCH	F
$C_{57}\oplus C\bullet$	Q	APCH	F
$C_{58}\oplus C\bullet$	I	IDLE	-
$C_{59}\oplus C\bullet$	Q	IDLE	-
$C_{60}\oplus C\bullet$	I	reserved	-
$C_{61}\oplus C\bullet$	Q	reserved	-
$C_{62}\oplus C\bullet$	I	reserved	-
$C_{63}\oplus C\bullet$	Q	reserved	-

[0075] For global codes, the seed values for the 36 bit shift register are chosen to avoid using the same code, or any cyclic shift of the same code, within the same geographical area to prevent ambiguity or harmful interference. No assigned code is equal to, or a cyclic shift of a global code.

Pilot Signals

[0076] The pilot signals are used for synchronization, carrier phase recovery, and for estimating the impulse response of the radio channel.

[0077] The RCS 104 transmits a forward link pilot carrier reference as a complex pilot code sequence to provide time and phase reference for all SUs 111, 112, 115, 117 and 118 in its service area. The power level of the Global Pilot (GLPT) signal is set to provide adequate coverage over the whole RCS service area, which area depends on the cell size. With only one pilot signal in the forward link, the reduction in system capacity due to the pilot energy is negligible.

[0078] The SUs 111, 112, 115, 117 and 118 each transmits a pilot carrier reference as a quadrature modulated (complex-valued) pilot spreading code sequence to provide a time and phase reference to the RCS for the reverse link. The pilot signal transmitted by the SU of one embodiment of the invention is 6 dB lower than the power of the 32 kb/s POTS traffic channel. The reverse pilot channel is subject to APC. The reverse link pilot associated with a particular connection is called the Assigned Pilot (ASPT). In addition, there are pilot signals associated with access channels. These are called the Long Access Channel Pilots (LAXPTs). Short access channel pilots (SAXPTs) are also associated with the access channels and used for spreading code acquisition and initial power ramp-up

[0079] All pilot signals are formed from complex codes, as defined below:

$$\text{GLPT (forward)} = \{C_2\oplus C\bullet) + j.(C_3\oplus C\bullet)\} \,.\, \{(1) + j.(0)\}$$

$$\{\text{ Complex Code }\}.\{\text{ Carrier }\}$$

[0080] The complex pilot signals are de-spread by multiplication with conjugate spreading codes: $\{(C_2\oplus C\bullet) - j.(C_3\oplus C\bullet)\}$. By contrast, traffic channels are of the form:

$$TRCH_n\text{(forward/reverse)} = \{(C_k\oplus C\bullet) + j.(C_l\oplus C\bullet)\} \,.\, \{(\pm 1) + j(\pm 1)\}$$

{ Complex Codes } . { Data Symbol}

which thus form a constellation set at $\frac{\pi}{4}$ radians with respect to the pilot signal constellations.

[0081] The GLPT constellation is shown in Figure 3a, and the $TRCH_n$ traffic channel constellation is shown in Figure 3b.

Logical Channel Assignment of the FBCH, SBCH, and Traffic Channels

[0082] The FBCH is a global forward link channel used to broadcast dynamic information about the availability of services and AXCHs. Messages are sent continuously over this channel, and each message lasts approximately 1 ms. The FBCH message is 16 bits long, repeated continuously, and is epoch aligned. The FBCH is formatted as defined in Table 6.

Table 6:

FBCH format	
Bit	Definition
0	Traffic Light 0
1	Traffic Light 1
2	Traffic Light 2
3	Traffic Light 3
4-7	service indicator bits
8	Traffic Light 0
9	Traffic Light 1
10	Traffic Light 2
11	Traffic Light 3
12-15	service indicator bits

[0083] For the FBCH, bit 0 is transmitted first. As used in Table 6, a traffic light corresponds to an Access Channel (AXCH) and indicates whether the particular access channel is currently in use (a red) or not in use (a green). A logic '1' indicates that the traffic light is green, and a logic '0' indicates the traffic light is red. The values of the traffic light bits may change from octet to octet, and each 16 bit message contains distinct service indicator bits which describe the types of services that are available for the AXCHs.

[0084] One embodiment of the present invention uses service indicator bits as follows to indicate the availability of services or AXCHs. The service indicator bits {4,5,6,7,12,13,14,15} taken together may be an unsigned binary number, with bit 4 as the MSB and bit 15 as the LSB. Each service type increment has an associated nominal measure of the capacity required, and the FBCH continuously broadcasts the available capacity. This is scaled to have a maximum value equivalent to the largest single service increment possible. When an SU requires a new service or an increase in the number of bearers, it compares the capacity required to that indicated by the FBCH, and then considers itself blocked if the capacity is not available. The FBCH and the traffic channels are aligned to the epoch.

[0085] Slow Broadcast Information frames contain system or other general information that is available to all SUs and Paging Information frames contain information about call requests for particular SUs. Slow Broadcast Information frames and Paging Information frames are multiplexed together on a single logical channel which forms the Slow Broadcast Channel (SBCH). As previously defined, the code epoch is a sequence of 29 877 20 chips having an epoch duration which is a function of the chip rate defined in Table 7 below. In order to facilitate power saving, the channel is divided into N "Sleep" Cycles, and each Cycle is subdivided into M Slots, which are 19 ms long, except for 10.5 Mhz bandwidth which has slots of 18 ms.

Table 7:

SBCH Channel Format Outline						
Bandwidth (MHz)	Spreading Code Rate (MHz)	Epoch Length (ms)	Cycles/ Epoch N	Cycle Length (ms)	Slots/Cycle M	Slot Length (ms)
7.0	5.824	5130	5	1026	54	19
10.0	8.320	3591	3	1197	63	19
10.5	8.512	3510	3	1170	65	18
14.0	11.648	2565	3	855	45	19
15.0	12.480	2394	2	1197	63	19

[0086] Sleep Cycle Slot #1 is always used for slow broadcast information. Slots #2 to #M-1 are used for paging groups unless extended slow broadcast information is inserted. The pattern of cycles and slots in one embodiment of the present invention run continuously at 16 kb/s.

[0087] Within each Sleep Cycle the SU powers-up the receiver and re-acquires the pilot code. It then achieves carrier lock to a sufficient precision for satisfactory demodulation and Viterbi decoding. The settling time to achieve carrier lock may be up to 3 Slots in duration. For example, an SU assigned to Slot #7 powers up the Receiver at the start of Slot #4. Having monitored its Slot the SU will have either recognized its Paging Address and initiated an access request, or failed to recognize its Paging Address in which case it reverts to the Sleep mode. Table 8 shows duty cycles for the different bandwidths, assuming a wake-up duration of 3 Slots.

Table 8:

Steep-Cycle Power Saving		
Bandwidth (MHz)	Slots/Cycle	Duty Cycle
7.0	54	7.4%
10.0	63	6.3%
10 5	65	6.2%
14.0	45	8.9%
15.0	63	6.3%

Spreading code Tracking and AMF Detection in Multipath Channels

Spreading code Tracking

[0088] Three CDMA spreading code tracking methods in multipath fading environments are described which track the code phase of a received multipath spread-spectrum signal. The first is the prior art tracking circuit which simply tracks the spreading code phase with the highest detector output signal value, the second is a tracking circuit that tracks the median value of the code phase of the group of multipath signals, and the third is the centroid tracking circuit which tracks the code-phase of an optimized, least mean squared weighted average of the multipath signal components. The following describes the algorithms by which the spreading code phase of the received CDMA signal is tracked.

[0089] A tracking circuit has operating characteristics that reveal the relationship between the time error and the control voltage that drives a Voltage Controlled Oscillator (VCO) of a spreading code phase tracking circuit. When there is a positive timing error, the tracking circuit generates a negative control voltage to offset the timing error. When there is a negative timing error, the tracking circuit generates a positive control voltage to offset the timing error. When the tracking circuit generates a zero value, this value corresponds to the perfect time alignment called the 'lock-point'. Figure 3 shows the basic tracking circuit. Received signal r(t) is applied to matched filter 301, which correlates r(t) with a local code-sequence c(t) generated by Code Generator 303. The output signal of the matched filter x(t) is sampled at the sampler 302 to produce samples x[nT] and x[nT + T/2]. The samples x[nT] and x[nT + T/2] are used by a tracking circuit 304 to determine if the phase of the spreading code c(t) of the code generator 303 is correct. The tracking circuit

304 produces an error signal e(t) as an input to the code generator 303. The code generator 303 uses this signal e(t) as an input signal to adjust the code-phase it generates.

[0090] In a CDMA system, the signal transmitted by the reference user is written in the lowpass representation as

$$s(t) = \sum_{k=-\infty}^{\infty} c_k P_{Tc}(t - kT_c) \qquad (7)$$

where c_k represents the spreading code coefficients, $P_{Tc}(t)$ represents the spreading code chip waveform, and T_c is the chip duration. Assuming that the reference user is not transmitting data so that only the spreading code modulates the carrier. Referring to Figure 3c, the received signal is

$$r(t) = \sum_{i=1}^{M} a_i s(t - \tau_i) \qquad (8)$$

[0091] Here, a_i is due to fading effect of the multipath channel on the i-th path and τ_i is the random time delay associated with the same path. The receiver passes the received signal through a matched filter, which is implemented as a correlation receiver and is described below. This operation is done in two steps: first the signal is passed through a chip matched filter and sampled to recover the spreading code chip values, then this chip sequence is correlated with the locally generated code sequence.

[0092] Figure 3c shows the chip matched filter 301, matched to the chip waveform $P_{Tc}(t)$, and the sampler 302. Ideally, the signal $x(t)$ at the output terminal of the chip matched filter is

$$x(t) = \sum_{i=k}^{M} \sum_{k=-\infty}^{\infty} a_i c_k g(t - \tau_i - kT_c) \qquad (9)$$

where

$$g(t) = P_{Tc}(t) * h_R(t) \qquad (10)$$

Here, $h_R(t)$ is the impulse response of the chip matched filter and '*' denotes convolution. The order of the summations can be rewritten as

$$x(t) = \sum_{k=-\infty}^{\infty} c_k f(t - kT_c) \qquad (11)$$

where

$$f(t) = \sum_{i=1}^{M} a_i g(t - \tau_i) \qquad (12)$$

[0093] In the multipath channel described above, the sampler samples the output signal of the matched filter to produce x(nT) at the maximum power level points of $g(t)$. In practice, however, the waveform $g(t)$ is severely distorted because of the effect of the multipath signal reception, and a perfect time alignment of the signals is not available.

[0094] When the multipath distortion in the channel is negligible and a perfect estimate of the timing is available, i.

e., a_1=1, τ_1=0, and a_i=0, i=2,...,M, the received signal is *r(t) = s(t)*. Then, with this ideal channel model, the output of the chip matched filter becomes

$$x(t) = \sum_{k=-\infty}^{\infty} c_k g(t - kT_c) \qquad (13)$$

[0095] When there is multipath fading, however, the received spreading code chip value waveform is distorted, and has a number of local maxima that can change from one sampling interval to another depending on the channel characteristics.

[0096] For multipath fading channels with quickly changing channel characteristics, it is not practical to try to locate the maximum of the waveform *f(t)* in every chip period interval. Instead, a time reference may be obtained from the characteristics of *f(t)* that may not change as quickly. Three tracking methods are described based on different characteristics of *f(t)*.

Prior Art Spreading Code Tracking Method:

[0097] Prior art tracking methods include a code tracking circuit in which the receiver attempts to determine the timing of the maximum matched filter output value of the chip waveform occurs and sample the signal accordingly. However, in multipath fading channels, the receiver despread code waveform can have a number of local maxima, especially in a mobile environment. In the following, f(t) represents the received signal waveform of the spreading code chip convolved with the channel impulse response. The frequency response characteristic of *f(t)* and the maximum of this characteristic can change rather quickly making it impractical to track the maximum of *f(t)*.

[0098] Define τ to be the time estimate that the tracking circuit calculates during a particular sampling interval. Also, define the following error function

$$\varepsilon = \begin{cases} \int_{|\tau - t| > \delta} f(t)dt, & |\tau - t| > \delta \\ 0, & |\tau - t| < \delta \end{cases} \qquad (14)$$

The tracking circuits of the prior art calculate a value of the input signal that minimizes the error ε. One can write

$$\min \varepsilon = 1 - \max_{\tau} \int_{\tau-\delta}^{\tau+\delta} f(t)dt \qquad (15)$$

[0099] Assuming *f(τ)* has a smooth shape in the values given, the value of τ for which *f(τ)* is maximum minimizes the error ε, so the tracking circuit tracks the maximum point of *f(t)*.

Median Weighted Value Tracking Method:

[0100] The Median Weighted Tracking Method of one embodiment of the present invention, minimizes the absolute weighted error, defined as

$$\varepsilon = \int_{-\infty}^{\infty} |t - \tau| f(t)dt \qquad (16)$$

[0101] This tracking method calculates the 'median' signal value of *f(t)* by collecting information from all paths, where *f(τ)* is as in equation 12. In a multipath fading environment, the waveform *f(t)* can have multiple local maxima, but only

one median.

[0102] To minimize ε, take the derivative of equation (16) is taken with respect to τ and the result is equated to zero, which gives

$$\int_{-\infty}^{\tau} f(t)dt = \int_{\tau}^{\infty} f(t)dt \qquad (17)$$

[0103] The value of τ that satisfies (17) is called the 'median' of *f(t)*. Therefore, the Median Tracking Method of the present embodiment tracks the median of *f(t)*. Figure 4 shows an implementation of the tracking circuit based on minimizing the absolute weighted error defined above: The signal *x(t)* and its one-half chip offset version *x(t+T/2)* are sampled by the A/D 401 at a rate *I/T*. The following equation determines the operating characteristic of the circuit in Figure 4:

$$\varepsilon(\tau) = \sum_{n=1}^{2L} \left| f(\tau - nT/2) \right| - \left| f(\tau + nT/2) \right| \qquad (18)$$

[0104] Tracking the median of a group of multipath signals keeps the received energy of the multipath signal components substantially equal on the early and late sides of the median point of the correct locally generated spreading code phase c_n. The tracking circuit consists of an A/D 401 which samples an input signal x(t) to form the half-chip offset samples. The half chip offset samples are alternatively grouped into even samples called an early set of samples x (nT+τ) and odd samples called a late set of samples x(nT+(T/2)+τ). The first correlation bank adaptive matched filter 402 multiplies each early sample by the spreading code phases c(n+1), c(n+2), ..., c(n+L), where L is small compared to the code length and approximately equal to number of chips of delay between the earliest and latest multipath signal. The output of each correlator is applied to a respective first sum-and-dump bank 404. The magnitudes of the output values of the L sum-and-dumps are calculated in the calculator 406 and then summed in summer 408 to give an output value proportional to the signal energy in the early multipath signals. Similarly, a second correlation bank adaptive matched filter 403 operates on the late samples, using code phases c(n-1), c(n-2), ..., c(n-L), and each output signal is applied to a respective sum-and-dump circuit in an integrator 405. The magnitudes of the L sum-and-dump output signals are calculated in calculator 407 and then summed in summer 409 to give a value for the late multipath signal energy. Finally, the subtractor 410 calculates the difference and produces error signal ε(t) of the early and late signal energy values.

[0105] The tracking circuit adjusts by means of error signal ε(τ) the locally generated code phases c(t) to cause the difference between the early and late values to tend toward 0.

Centroid Tracking Method

[0106] The optimal spreading code tracking circuit of one embodiment of the present invention is called the squared weighted tracking (or centroid) circuit. Defining τ to denote the time estimate that the tracking circuit calculates, based on some characteristic of *f(t)*, the centroid tracking circuit minimizes the squared weighted error defined as

$$\varepsilon = \int_{-\infty}^{\infty} |t - \tau|^2 f(t)dt \qquad (19)$$

[0107] This function inside the integral has a quadratic form, which has a unique minimum. The value of τ that minimizes ε can be found by taking the derivative of the above equation with respect to τ and equating to zero, which gives

$$\int_{-\infty}^{\infty} (-2t + 2\tau) f(t)dt = 0 \qquad (20)$$

Therefore, the value of τ that satisfies equation (21)

$$\tau - \frac{1}{\beta}\int_{-\infty}^{\infty} tf(t)dt = 0 \qquad (21)$$

is the timing estimate that the tracking circuit calculates, where β is a constant value.

[0108] Based on these observations, a realization of an exemplary tracking circuit which minimizes the squared weighted error is shown in Figure 5a. The following equation determines the error signal ε(τ) of the centroid tracking circuit:

$$\varepsilon(\tau) = \sum_{n=1}^{2L} n\left[\left|f(\tau - nT/2)\right| - \left|f(\tau + nT/2)\right|\right] = 0 \qquad (22)$$

The value that satisfies ε(τ)=0 is the perfect estimate of the timing.

[0109] The early and late multipath signal energy on each side of the centroid point are equal. The centroid tracking circuit shown in Figure 5a consists of an A/D converter 501 which samples an input signal x(t) to form the half-chip offset samples. The half chip offset samples are alternatively grouped as an early set of samples x(nT+τ) and a late set of samples x(nT+(T/2)+ τ). The first correlation bank adaptive matched filter 502 multiplies each early sample and each late sample by the positive spreading code phases c(n+1), c(n+2), ..., c(n+L), where L is small compared to the code length and approximately equal to number of chips of delay between the earliest and latest multipath signal. The output signal of each correlator is applied to a respective one ofL sum-and-dump circuits of the first sum and dump bank 504. The magnitude value of each sum-and-dump circuit of the sum and dump bank 504 is calculated by the respective calculator in the calculator bank 506 and applied to a corresponding weighting amplifier of the first weighting bank 508. The output signal of each weighting amplifier represents the weighted signal energy in a multipath component signal.

[0110] The weighted early multipath signal energy values are summed in sample adder 510 to give an output value proportional to the signal energy in the group of multipath signals corresponding to positive code phases which are the early multipath signals. Similarly, a second correlation bank adaptive matched filter 503 operates on the early and late samples, using the negative spreading code phases c(n-1), c(n-2), ..., c(n-L); each output signal is provided to a respective sum-and-dump circuit of discrete integrator 505. The magnitude value of the L sum-and-dump output signals are calculated by the respective calculator of calculator bank 507 and then weighted in weighting bank 509. The weighted late multipath signal energy values are summed in sample adder 511 to give an energy value for the group of multipath signals corresponding to the negative code phases which are the late multipath signals. Finally, the adder 512 calculates the difference of the early and late signal energy values to produce error sample value ε τ).

[0111] The tracking circuit of Figure 5a produces error signal ε(τ) which is used to adjust the locally generated code phase c(nT) to keep the weighted average energy in the early and late multipath signal groups equal. The embodiment shown uses weighting values that increase as the distance from the centroid increases. The signal energy in the earliest and latest multipath signals is probably less than the multipath signal values near the centroid. Consequently, the difference calculated by the adder 510 is more sensitive to variations in delay of the earliest and latest multipath signals.

Quadratic Detector for Tracking

[0112] In the new embodiment of the tracking method, the tracking circuit adjusts sampling phase to be "optimal" and robust to multipath. Let f(t) represent the received signal waveform as in equation 12 above. The particular method of optimizing starts with a delay locked loop with an error signal ε(τ) that drives the loop. The function ε(τ) must have only one zero at $\tau=\tau_0$ where τ_0 is optimal. The optimal form for ε(τ) has the canonical form:

$$\varepsilon(\tau) = \int_{-\infty}^{\infty} w(t, \tau)\, |f(t)|^2\, dt \qquad (23)$$

where w(t, τ) is a weighting function relating f(t) to the error ε(τ), and the relationship indicated by equation (24) also holds

$$\varepsilon(\tau+\tau_0) = \int_{-\infty}^{\infty} w(t, \tau+\tau_0) \, |f(t)|^2 \, dt \qquad (24)$$

[0113] It follows from equation (24) that w(t, τ) is equivalent to w(t-τ). Considering the slope M of the error signal in the neighborhood of a lock point τ_0:

$$M = \frac{d\varepsilon(\tau)}{d\tau}\Big|_{\tau_0} = -\int_{-\infty}^{\infty} w'(t-\tau_0)\, g(t)\, dt \qquad (25)$$

where w' (t, τ) is the derivative of w(t, τ) with respect to τ, and g(t) is the average of $|f(t)|^2$.

[0114] The error ε(τ) has a deterministic part and a noise part. Let z denote the noise component in ε(τ), then $|z|^2$ is the average noise power in the error function ε(τ). Consequently, the optimal tracking circuit maximizes the ratio

$$F = \frac{M^2}{|z|^2} \qquad (26)$$

[0115] The implementation of the Quadratic Detector is now described. The discrete error value e of an error signal ε(τ) is generated by performing the operation

$$e = y^T B y \qquad (27)$$

where the vector y represents the received signal components yi, i = 0, 1, ... L-1, as shown in Figure 5b. The matrix B is an L by L matrix and the elements are determined by calculating values such that the ratio F of equation (26) is maximized.

[0116] The Quadratic Detector described above may be used to implement the centroid tracking system described above with reference to Figure 5a. For this implementation, the vector y is the output signal of the sum and dump circuits 504: y={f(τ-LT), f(τ-LT+T/2), f(τ-(L-1)T),⋯ f(τ), f(τ+T/2), f(τ+T),⋯ f(τ+LT)} and the matrix B is set forth in table 9.

Table 9 B matrix for quadratic form of Centroid Tracking System

L	0	0	0	0	0	0	0	0	0	0
0	L-1/2	0	0	0	0	0	0	0	0	0
0	0	L-1	0	0	0	0	0	0	0	0
⋮	⋮	⋮	⋱	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	0	0	1/2	0	0	0	0	0	0

0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	-1/2	0	0	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋱	⋮	⋮	⋮
0	0	0	0	0	0	0	0	-L+1	0	0
0	0	0	0	0	0	0	0	0	-L+1/2	0
0	0	0	0	0	0	0	0	0	0	-L

Determining the Minimum Value of *L* needed:

[0117] The value of *L* in the previous section determines the minimum number of correlators and sum-and-dump elements. *L* is chosen as small as possible without compromising the functionality of the tracking circuit.

[0118] The multipath characteristic of the channel is such that the received chip waveform *f(t)* is spread over QT_c seconds, or the multipath components occupy a time period of *Q* chips duration. The value of L chosen is *L*=*Q*. Q is found by measuring the particular RF channel transmission characteristics to determine the earliest and latest multipath component signal propagation delay. QT_c is the difference between the earliest and latest multipath component arrival time at a receiver.

Adaptive Vector Correlator

[0119] An embodiment of the present invention uses an adaptive vector correlator (AVC) to estimate the channel impulse response and to obtain a reference value for coherent combining of received multipath signal components. The described embodiment employs an array of correlators to estimate the complex channel response affecting each multipath component. The receiver compensates for the channel response and coherently combines the received multipath signal components. This approach is referred to as maximal ratio combining.

[0120] Referring to Figure 6, the input signal x(t) to the system includes interference noise of other message channels, multipath signals of the message channels, thermal noise, and multipath signals of the pilot signal. The signal is provided to AVC 601 which, in the exemplary embodiment, includes a despreading means 602, channel estimation means for estimating the channel response 604, correction means for correcting a signal for effects of the channel response 603, and adder 605. The AVC despreading means 602 is composed of multiple code correlators, with each correlator using a different phase of the pilot code c(t) provided by the pilot code generator 608. The output signal of this despreading means corresponds to a noise power level if the local pilot code of the despreading means is not in phase with the input code signal. Alternatively, it corresponds to a received pilot signal power level plus noise power level if the phases of the input pilot code and locally generated pilot code are the same. The output signals of the correlators of the despreading means are corrected for the channel response by the correction means 603 and are applied to the adder 605 which collects all multipath pilot signal power. The channel response estimation means 604 receives the combined pilot signal and the output signals of the despreading means 602, and provides a channel response estimate signal, w(t), to the correction means 603 of the AVC, and the estimate signal w(t) is also available to the adaptive matched filter (AMF) described below. The output signal of the despreading means 602 is also provided to the acquisition decision means 606 which decides, based on a particular algorithm such as a sequential probability ratio test (SPRT), if the present output levels of the despreading circuits correspond to synchronization of the locally generated code to the desired input code phase. If the detector finds no synchronization, then the acquisition decision means sends a control signal a(t) to the local pilot code generator 608 to offset its phase by one or more chip period. When synchronization is found, the acquisition decision means informs tracking circuit 607, which achieves and maintains a close synchronization between the received and locally generated code sequences.

[0121] An exemplary implementation of the Pilot AVC used to despread the pilot spreading code is shown in Figure 7. The described embodiment assumes that the input signal x(t) has been sampled with sampling period T to form samples $x(nT+\tau)$, and is composed of interference noise of other message channels, multipath signals of message channels, thermal noise, and multipath signals of the pilot code. The signal $x(nT+\tau)$ is applied to L correlators, where

L is the number of code phases over which the uncertainty within the multipath signals exists. Each correlator 701, 702, 703 comprises a multiplier 704, 705, 706, which multiples the input signal with a particular phase of the Pilot spreading code signal c((n+i)T), and sum-and-dump circuits 708, 709, 710. The output signal of each multiplier 704, 705, 706 is applied to a respective sum-and dump circuit 708, 709, 710 to perform discrete integration. Before summing the signal energy contained in the outputs of the correlators, the AVC compensates for the channel response and the carrier phase rotation of the different multipath signals. Each output of each sum-and-dump 708, 709, 710 is multiplied with a derotation phaser [complex conjugate of ep(nT)] from digital phase lock loop (DPLL) 721 by the respective multiplier 714, 715, 716 to account for the phase and frequency offset of the carrier signal. The Pilot Rake AMF calculates the weighting factors wk, k=1, .., L, for each multipath signal by passing the output of each multiplier 714, 715, 716 through a low pass filter (LPF) 711, 712, 713. Each despread multipath signal is multiplied by its corresponding weighting factor in a respective multiplier 717, 718, 719. The output signals of the multipliers 717, 718, 719 are summed in a master adder 720, and the output signal p(nT) of the accumulator 720 consists of the combined despread multipath pilot signals in noise. The output signal p(nT) is also input to the DPLL 721 to produce the error signal ep(nT) for tracking of the carrier phase.

[0122] Figures 8a and 8b show alternate embodiments of the AVC which can be used for detection and multipath signal component combining. The message signal AVCs of Figures 8a and 8b use the weighting factors produced by the Pilot AVC to correct the message data multipath signals. The spreading code signal, c(nT) is the spreading code spreading sequence used by a particular message channel and is synchronous with the pilot spreading code signal. The value *L* is the number of correlators in the AVC circuit.

[0123] The circuit of Figure 8a calculates the decision variable Z which is given by

$$Z = w_1 \sum_{i=1}^{N} x(iT+\tau)c(iT) + w_2 \sum_{i=1}^{N} x(iT+\tau)c((i+1)T) + \bullet\bullet\bullet + w_L \sum_{i=1}^{L} x(iT+\tau) + c((i+L)T) \quad (28)$$

where *N* is the number of chips in the correlation window. Equivalently, the decision statistic is given by

$$Z = x(T+\tau)\sum_{i=1}^{L} w_1 c(iT) + x(2T+\tau)\sum_{i=1}^{L} w_1 c((i+1)T) + \bullet\bullet\bullet + x(NT+\tau)\sum_{i=1}^{L} w_N c((i+N)T) = \sum_{k=1}^{N} x(kT-\tau)\sum_{i=1}^{L} w_k c((i+k-1)T) \quad (29)$$

[0124] The alternative implementation that results from equation (29) is shown in Figure 8b.

[0125] Referring to Figure 8a, the input signal x(t) is sampled to form x(nT+τ), and is composed of interference noise of other message channels, multipath signals of message channels, thermal noise, and multipath signals of the pilot code. The signal x(nT+τ) is applied to L correlators, where L is the number of code phases over which the uncertainty within the multipath signals exists. Each correlator 801, 802, 803 comprises a multiplier 804, 805, 806, which multiples the input signal by a particular phase of the message channel spreading code signal, and a respective sum-and-dump circuit 808, 809, 810. The output signal of each multiplier 804, 805, 806 is applied to a respective sum-and dump circuit 808, 809, 810 which performs discrete integration. Before summing the signal energy contained in the output signals of the correlators, the AVC compensates for the different multipath signals. Each despread multipath signal and its corresponding weighting factor, which is obtained from the corresponding multipath weighting factor of the pilot AVC, are multiplied in a respective multiplier 817, 818, 819. The output signals of multipliers 817, 818, 819 are summed in a master adder 820, and the output signal z(nT) of the accumulator 820 consists of sampled levels of a despread message signal in noise.

[0126] The alternative embodiment of the invention includes a new implementation of the AVC despreading circuit for the message channels which performs the sum-and-dump for each multipath signal component simultaneously.

The advantage of this circuit is that only one sum-and dump circuit and one adder is necessary. Referring to Figure 8b, the message code sequence generator 830 provides a message code sequence to shift register 831 of length L. The output signal of each register 832, 833, 834, 835 of the shift register 831 corresponds to the message code sequence shifted in phase by one chip. The output value of each register 832, 833, 834, 835 is multiplied in multipliers 836, 837, 838, 839 with the corresponding weighting factor w_k, k=1, .., L obtained from the Pilot AVC. The output signals of the L multipliers 836, 837, 838, 839 are summed by the adding circuit 840. The adding circuit output signal and the receiver input signal $x(nT+\tau)$ are then multiplied in the multiplier 841 and integrated by the sum-and-dump circuit 842 to produce message signal z(nT).

[0127] A third embodiment of the adaptive vector correlator is shown in Figure 8c. The embodiment shown uses the least mean square (LMS) statistic to implement the vector correlator and determines the derotation factors for each multipath component from the received multipath signal. The AVC of Figure 8c is similar to the exemplary implementation of the Pilot AVC used to despread the pilot spreading code shown in Figure 7. The digital phase locked loop 721 is replaced by the phase locked loop 850 having voltage controlled oscillator 851, loop filter 852, limiter 853, and imaginary component separator 854. The difference between the corrected despread output signal dos and an ideal despread output signal is provided by adder 855, and the difference signal is a despread error value ide which is further used by the derotation circuits to compensate for errors in the derotation factors.

[0128] In a multipath signal environment, the signal energy of a transmitted symbol is spread out over the multipath signal components. The advantage of multipath signal addition is that a substantial portion of signal energy is recovered in an output signal from the AVC. Consequently, a detection circuit has an input signal from the AVC with a higher signal-to-noise ratio (SNR), and so can detect the presence of a symbol with a lower bit-error ratio (BER). In addition, measuring the output of the AVC is a good indication of the transmit power of the transmitter, and a good measure of the system's interference noise.

Adaptive Matched Filter

[0129] One embodiment of the current invention includes an Adaptive Matched Filter (AMF) to optimally combine the multipath signal components in a received spread spectrum message signal. The AMF is a tapped delay line which holds shifted values of the sampled message signal and combines these after correcting for the channel response: The correction for the channel response is done using the channel response estimate calculated in the AVC which operates on the Pilot sequence signal. The output signal of the AMF is the combination of the multipath components which are summed to give a maximum value. This combination corrects for the distortion of multipath signal reception. The various message despreading circuits operate on this combined multipath component signal from the AMF.

[0130] Figure 8d shows an exemplary embodiment of the AMF. The sampled signal from the A/D converter 870 is applied to the L-stage delay line 872. Each stage of this delay line 872 holds the signal corresponding to a different multipath signal component. Correction for the channel response is applied to each delayed signal component by multiplying the component in the respective multiplier of multiplier bank 874 with the respective weighting factor w_1, w_2, ..., w_L, from the AVC corresponding to the delayed signal component. All weighted signal components are summed in the adder 876 to give the combined multipath component signal y(t).

[0131] The combined multipath component signal y(t) does not include the correction due to phase and frequency offset of the carrier signal. The correction for the phase and frequency offset of the carrier signal is made to y(t) by multiplying y(t) with carrier phase and frequency correction (derotation phasor) in multiplier 878. The phase and frequency correction is produced by the AVC as described previously. Figure 8d shows the correction as being applied before the despreading circuits 880, but alternate embodiments of the invention can apply the correction after the despreading circuits.

Method to Reduce Re-Acquisition Time with Virtual Location

[0132] One consequence of determining the difference in code phase between the locally generated pilot code sequence and a received spreading code sequence is that an approximate value for the distance between the base station and a subscriber unit can be calculated. If the SU has a relatively fixed position with respect to the RCS of the base station, the uncertainty of received spreading code phase is reduced for subsequent attempts at re-acquisition by the SU or RCS. The time required for the base station to acquire the access signal of a SU that has gone "off-hook" contributes to the delay between the SU going off-hook and the receipt of a dial tone from the PSTN. For systems that require a short delay, such as 150 msec for dial tone after off-hook is detected, a method which reduces the acquisition and bearer channel establishment time is desirable. One embodiment of the present invention uses such a method of reducing re-acquisition by use of virtual locating.

[0133] The RCS acquires the SU CDMA signal by searching only those received code phases corresponding to the largest propagation delay of the particular system. In other words, the RCS assumes that all SUs are at a predetermined,

fixed distance from the RCS. The first time the SU establishes a channel with the RCS, the normal search pattern is performed by the RCS to acquire the access channel. The normal method starts by searching the code phases corresponding to the longest possible delay, and gradually adjusts the search to the code phases with the shortest possible delay. However, after the initial acquisition, the SU can calculate the delay between the RCS and the SU by measuring the time difference between sending a short access message to the RCS and receiving an acknowledgment message, and using the received Global Pilot channel as a timing reference. The SU can also receive the delay value by having the RCS calculate the round trip delay difference from the code phase difference between the Global Pilot code generated at the RCS and the received assigned pilot sequence from the SU, and then sending the SU the value on a predetermined control channel. Once the round trip delay is known to the SU , the SU may adjust the code phase of the locally generated assigned pilot and spreading code sequences by adding the delay required to make the SU appear to the RCS to be at the predetermined fixed distance from the RCS. Although the method is explained for the largest delay, a delay corresponding to any predetermined location in the system can be used.

[0134] A second advantage of the method of reducing re-acquisition by virtual locating is that a conservation in SU power use can be achieved. Note that a SU that is "powered down" or in a sleep mode needs to start the bearer channel acquisition process with a low transmit power level and ramp-up power until the RCS can receive its signal in order to minimize interference with other users. Since the subsequent re-acquisition time is shorter, and because the SU's location is relatively fixed in relation to the RCS, the SU can ramp-up transmit power more quickly because the SU will wait a shorter period of time before increasing transmit power. The SU waits a shorter period because it knows, within a small error range, when it should receive a response from the RCS if the RCS has acquired the SU signal.

The Spread Spectrum Communication System

The Radio Carrier Station (RCS)

[0135] The Radio Carrier Station (RCS) of the present invention acts as a central interface between the SU and the remote processing control network element, such as a Radio Distribution Unit (RDU). The interface to the RDU of the present embodiment follows the G.704 standard and an interface according to a modified version of DECT V5.1, but the present invention can support any interface that can exchange call control and traffic channels. The RCS receives information channels from the RDU including call control data, and traffic channel data such as, but not limited to, 32 kb/s ADPCM, 64 kb/s PCM, and ISDN, as well as system configuration and maintenance data. The RCS also terminates the CDMA radio interface bearer channels with SUs, which channels include both control data, and traffic channel data. In response to the call control data from either the RDU or a SU, the RCS allocates traffic channels to bearer channels on the RF communication link and establishes a communication connection between the SU and the telephone network through an RDU.

[0136] As shown in Figure 9, the RCS receives call control and message information data into the MUXs 905, 906 and 907 through interface lines 901,902 and 903. Although E1 format is shown, other similar telecommunication formats can be supported in the same manner as described below. The MUXs shown in Figure 9 may be implemented using circuits similar to that shown in Figure 10. The MUX shown in Figure 10 includes system clock signal generator 1001 consisting of phase locked oscillators (not shown) which generate clock signals for the Line PCM highway 1002 (which is part of PCM Highway 910), and high speed bus (HSB) 970; and the MUX Controller 1010 which synchronizes the system clock 1001 to interface line 1004. It is contemplated that the phase lock oscillators can provide timing signals for the RCS in the absence of synchronization to a line. The MUX Line Interface 1011 separates the call control data from the message information data. Referring to Figure 9, each MUX provides a connection to the Wireless Access Controller (WAC) 920 through the PCM highway 910. The MUX controller 1010 also monitors the presence of different tones present in the information signal by means of tone detector 1030.

[0137] Additionally, the MUX Controller 1010 provides the ISDN D channel network signaling locally to the RDU. The MUX line interface 1011, such as a FALC 54, includes an E1 interface 1012 which consists of a transmit connection pair (not shown) and a receive connection pair (not shown) of the MUX connected to the RDU or Central Office (CO) ISDN Switch at the data rate of 2.048Mbps. The transmit and receive connection pairs are connected to the E1 interface 1012 which translates differential tri-level transmit/receive encoded pairs into levels for use by the Framer 1015. The line interface 1011 uses internal phase-locked-loops (not shown) to produce E1-derived 2.048 MHz, and 4.096 MHz clocks as well as an 8 KHz frame-sync pulse. The line interface can operate in clock-master or clock-slave mode. While the exemplary embodiment is shown as using an E1 Interface, it is contemplated that other types of telephone lines which convey multiple calls may be used, for example, T1 lines or lines which interface to a Private Branch Exchange (PBX).

[0138] The line interface framer 1015 frames the data streams by recognizing the framing patterns on channel-1 (time-slot 0) of the incoming line, and inserts and extracts service bits, generates/checks line service quality information.

[0139] As long as a valid E1 signal appears at the E1 Interface 1012, the FALC 54, recovers a 2.048 MHz PCM clock

signal from the E1 line. This clock, via System Clock 1001, is used system wide as a PCM Highway Clock signal. If the E1 Line fails, the FALC 54 continues to deliver a PCM Clock derived from an oscillator signal o(t) connected to the sync input (not shown) of the FALC 54. This PCM Clock serves the RCS system until another MUX with an operational E1 line assumes responsibility for generating the system clock signals.

[0140] The framer 1015 generates a Received Frame Sync Pulse, which in turn can be used to trigger the PCM Interface 1016 to transfer data onto the line PCM Highway 1002 and into the RCS System for use by other elements. Since all E1 lines are frame synchronized, all Line PCM Highways are also frame synchronized. From this 8 kHz PCM Sync pulse, the system clock signal generator 1001 of the MUX uses a Phase Locked Loop (not shown) to synthesize the PNx2 clock [e.g., 15.96 MHz)(W_0(t)]. The frequency of this clock signal is different for different transmission bandwidths, as described in Table 7.

[0141] The MUX includes a MUX Controller 1010, such as a 25 MHz Quad Integrated Communications Controller, containing a microprocessor 1020, program memory 1021, and Time Division Multiplexer (TDM) 1022. The TDM 1022 is coupled to receive the signal provided by the Framer 1015, and extracts information placed in time slots 0 and 16. The extracted information governs how the MUX controller 1010 processes the Link Access Protocol - D (LAPD) data link. The call control and bearer modification messages, such as those defined as V5.1 Network layer messages, are either passed to the WAC, or used locally by the MUX controller 1010.

[0142] The RCS Line PCM Highway 1002 is connected to and originates with the Framer 1015 through PCM Interface 1016, and comprises of a 2.048 MHz stream of data in both the transmit and receive direction. The RCS also contains a High Speed Bus (HSB) 970 which is the communication link between the MUX, WAC, and MIUs. The HSB 970 supports a data rate of, for example, 100 Mbit/sec. Each of the MUX, WAC, and MIU access the HSB using arbitration. The RCS of the present invention also can include several MUXs requiring one board to be a "master" and the rest "slaves".

[0143] Referring to Figure 9, the Wireless Access Controller (WAC) 920 is the RCS system controller which manages call control functions and interconnection of data streams between the MUXs 905, 906, 907, Modem Interface Units (MIUs) 931, 932, 933. The WAC 920 also controls and monitors other RCS elements such as the VDC 940, RF 950, and Power Amplifiers 960. The WAC 920 as shown in Figure 11, allocates bearer channels to the modems on each MIU 931, 932, 933 and allocates the message data on line PCM Highway 910 from the MUXs 905, 906, 907 to the modems on the MIUs 931, 932, 933. This allocation is made through the System PCM Highway 911 by means of a time slot interchange on the WAC 920. If more than one WAC is present for redundancy purposes, the WACs determines the Master-Slave relationship with a second WAC. The WAC 920 also generates messages and paging information responsive to call control signals from the MUXs 905, 906, 907 received from a remote processor, such as an RDU; generates Broadcast Data which is transmitted to the MIU master modem 934; and controls the generation by the MIU MM 934 of the Global system Pilot spreading code sequence. The WAC 920 also is connected to an external Network Manager (NM) 980 for craftperson or user access.

[0144] Referring to Figure 11, the WAC includes a time-slot interchanger (TSI) 1101 which transfers information from one time slot in a Line PCM Highway or System PCM Highway to another time slot in either the same or different Line PCM Highway or System PCM Highway. The TSI 1101 is connected to the WAC controller 1111 of Figure 11 which controls the assignment or transfer of information from one time slot to another time slot and stores this information in memory 1120. The exemplary embodiment of the invention has four PCM Highways 1102, 1103, 1104, 1105 connected to the TSI. The WAC also is connected to the HSB 970, through which WAC communicates to a second WAC (not shown), to the MUXs and to the MIUs.

[0145] Referring to Figure 11, the WAC 920 includes a WAC controller 1111 employing, for example, a microprocessor 1112, such as a Motorola MC 68040 and a communications processor 1113, such as the Motorola MC68360 QUICC communications processor, and a clock oscillator 1114 which receives a clock synch signal wo(t) from the system clock generator. The clock generator is located on a MUX (not shown) to provide timing to the WAC controller 1111. The WAC controller 1111 also includes memory 1120 including Flash Prom 1121 and SRAM memory 1122. The Flash Prom 1121 contains the program code for the WAC controller 1111, and is reprogrammable for new software programs downloaded from an external source. The SRAM 1122 is provided to contain the temporary data written to and read from memory 1120 by the WAC controller 1111.

[0146] A low speed bus 912 is connected to the WAC 920 for transferring control and status signals between the RF Transmitter/Receiver 950, VDC 940, RF 950 and Power Amplifier 960 as shown in Figure 9. The control signals are sent from the WAC 920 to enable or disable the RF Transmitters/Receiver 950 or Power amplifier 960, and the status signals are sent from the RF Transmitters/Receiver 950 or Power amplifier 960 to monitor the presence of a fault condition.

[0147] Referring to Figure 9, the exemplary RCS contains at least one MIU 931, which is shown in Figure 12 and now described in detail. The MIU of the exemplary embodiment includes six CDMA modems, but the invention is not limited to this number of modems. The MIU includes a System PCM Highway 1201 connected to each of the CDMA Modems 1210, 1211, 1212, 1215 through a PCM Interface 1220, a Control Channel Bus 1221 connected to MIU con-

troller 1230 and each of the CDMA Modems 1210, 1211, 1212, 1213, an MIU clock signal generator (CLK) 1231, and a modem output combiner 1232. The MIU provides the RCS with the following functions: the MIU controller receives CDMA Channel Assignment Instructions from the WAC and assigns a modem to a user information signal which is applied to the line interface of the MUX and a modem to receive the CDMA channel from the SU; it also combines the CDMA Transmit Modem Data for each of the MIU CDMA modems; multiplexes I and Q transmit message data from the CDMA modems for transmission to the VDC; receives Analog I and Q receive message data from the VDC; distributes the I and Q data to the CDMA modems; transmits and receives digital AGC Data; distributes the AGC data to the CDMA modems; and sends MIU Board Status and Maintenance Information to the WAC 920.

[0148] The MIU controller 1230 of the exemplary embodiment of the present invention contains one communication microprocessor 1240, such as the MC68360 "QUICC" Processor, and includes a memory 1242 having a Flash Prom memory 1243 and a SRAM memory 1244. Flash Prom 1243 is provided to contain the program code for the Microprocessors 1240, and the memory 1243 is downloadable and reprogrammable to support new program versions. SRAM 1244 is provided to contain the temporary data space needed by the MC68360 Microprocessor 1240 when the MIU controller 1230 reads or writes data to memory

[0149] The MIU CLK circuit 1231 provides a timing signal to the MIU controller 1230, and also provides a timing signal to the CDMA modems. The MIU CLK circuit 1231 receives and is synchronized to the system clock signal wo (t). The controller clock signal generator 1213 also receives and synchronizes to the spreading code clock signal pn (t) which is distributed to the CDMA modems 1210, 1211, 1212, 1215 from the MUX.

[0150] The RCS of the present embodiment includes a System Modem 1210 contained on one MIU. The System Modem 1210 includes a Broadcast spreader (not shown) and a Pilot Generator (not shown). The Broadcast Modem provides the broadcast information used by the exemplary system, and the broadcast message data is transferred from the MIU controller 1230 to the System Modem 1210. The System Modem also includes four additional modems (not shown) which are used to transmit the signals CT1 through CT4 and AX1 through AX4. The System Modem 1210 provides unweighted I and Q Broadcast message data signals which are applied to the VDC. The VDC adds the Broadcast message data signal to the MIU CDMA Modem Transmit Data of all CDMA modems 1210, 1211, 1212, 1215, and the Global Pilot signal.

[0151] The Pilot Generator (PG) 1250 provides the Global Pilot signal which is used by the present invention, and the Global Pilot signal is provided to the CDMA modems 1210, 1211, 1212, 1215 by the MIU controller 1230. However, other embodiments of the present invention do not require the MIU controller to generate the Global Pilot signal, but include a Global Pilot signal generated by any form of CDMA Code Sequence generator. In the described embodiment of the invention, the unweighted I and Q Global Pilot signal is also sent to the VDC where it is assigned a weight, and added to the MIU CDMA Modem transmit data and Broadcast message data signal.

[0152] System timing in the RCS is derived from the E1 interface. There are four MUXs in an RCS, three of which (905, 906 and 907) are shown in Figure 9. Two MUXs are located on each chassis. One of the two MUXs on each chassis is designated as the master, and one of the masters is designated as the system master. The MUX which is the system master derives a 2.048 Mhz PCM clock signal from the E1 interface using a phase locked loop (not shown). In turn, the system master MUX divides the 2.048 Mhz PCM clock signal in frequency by 16 to derive a 128 KHz reference clock signal. The 128 KHz reference clock signal is distributed from the MUX that is the system master to all the other MUXs. In turn, each MUX multiplies the 128 KHz reference clock signal in frequency to synthesize the system clock signal which has a frequency that is twice the frequency of the PN-clock signal. The MUX also divides the 128 KHz clock signal in frequency by 16 to generate the 8 KHz frame synch signal which is distributed to the MIUs. The system clock signal for the exemplary embodiment has a frequency of 11.648 Mhz for a 7 MHz bandwidth CDMA channel Each MUX also divides the system clock signal in frequency by 2 to obtain the PN-clock signal and further divides the PN-clock signal in frequency by 29 877 120 (the PN sequence length) to generate the PN-synch signal which indicates the epoch boundaries. The PN-synch signal from the system master MUX is also distributed to all MUXs to maintain phase alignment of the internally generated clock signals for each MUX. The PN-synch signal and the frame synch signal are aligned. The two MUXs that are designated as the master MUXs for each chasis then distribute both the system clock signal and the PN-clock signal to the MIUs and the VDC.

[0153] The PCM Highway Interface 1220 connects the System PCM Highway 911 to each CDMA Modem 1210, 1211, 1212, 1215. The WAC controller transmits Modem Control information, including traffic message control signals for each respective user information signal, to the MIU controller 1230 through the HSB 970. Each CDMA Modem 1210, 1211, 1212, 1215 receives a traffic message control signal, which includes signaling information, from the MIU controller 1111. Traffic message control signals also include call control (CC) information and spreading code and despreading code sequence information.

[0154] The MIU also includes the Transmit Data Combiner 1232 which adds weighted CDMA modem transmit data including In-phase (I) and Quadrature (Q) modem transmit data from the CDMA modems 1210, 1211, 1212, 1215 on the MIU. The I modem transmit data is added separately from the Q modem transmit data. The combined I and Q modem transmit data output signal of the Transmit Data Combiner 1232 is applied to the I and Q multiplexer 1233 that

creates a single CDMA transmit message channel composed of the I and Q modem transmit data multiplexed into a digital data stream.

[0155] The Receiver Data Input Circuit (RDI) 1234 receives the Analog Differential I and Q Data from the Video Distribution Circuit (VDC) 940 shown in Figure 9 and distributes Analog Differential I and Q Data to each of the CDMA Modems 1210, 1211, 1212, 1215 of the MIU. The Automatic Gain Control Distribution Circuit (AGC) 1235 receives the AGC Data signal from the VDC and distributes the AGC Data to each of the CDMA Modems of the MIU. The TRL circuit 1233 receives the Traffic lights information and similarly distributes the Traffic light data to each of the Modems 1210, 1211, 1212, 1215.

The CDMA Modem

[0156] The CDMA modem provides for generation of CDMA spreadingcode sequences and synchronization between transmitter and receiver. It also provides four full duplex channels (TR0, TR1, TR2, TR3) programmable to 64, 32, 16, and 8 ksym/sec. each, for spreading and transmission at a specific power level. The CDMA modem measures the received signal strength to allow Automatic Power Control, it generates and transmits pilot signals, and encodes and decodes using the signal for forward error correction (FEC). The modem in an SU also performs transmitter spreading code pulse shaping using an FIR filter. The CDMA modem is also used by the Subscriber Unit (SU), and in the following discussion those features which are used only by the SU are distinctly pointed out. The operating frequencies of the CDMA modem are given in Table 10.

Table 10

Operating Frequencies			
Bandwidth (MHz)	**Chip Rate (MHz)**	**Symbol Rate (KHz)**	**Gain (Chips/Symbol)**
7	5.824	64	91
10	8.320	64	130
10.5	8.512	64	133
14	11.648	64	182
15	12.480	64	195

[0157] Each CDMA modem 1210, 1211, 1212, 1215 of Figure 12, and as shown in Figure 13, is composed of a transmit section 1301 and a receive section 1302. Also included in the CDMA modem is a control center 1303 which receives control messages CNTRL from the external system. These messages are used, for example, to assign particular spreading codes, activate the spreading or despreading, or to assign transmission rates. In addition, the CDMA modem has a code generator means 1304 used to generate the various spreading and despreading codes used by the CDMA modem. The transmit section 1301 is for transmitting the input information and control signals $m_i(t)$, i=1,2,.. I as spread-spectrum processed user information signals $sc_j(t)$, j=1,2,..J. The transmit section 1301 receives the global pilot code from the code generator 1304 which is controlled by the control means 1303. The spread spectrum processed user information signals are ultimately added to other similar processed signals and transmitted as CDMA channels over the CDMA RF forward message link, for example to the SUs. The receive section 1302 receives CDMA channels as r(t) and despreads and recovers the user information and control signals $rc_k(t)$, k=1,2,..K transmitted over the CDMA RF reverse message link, for example to the RCS from the SUs.

CDMA Modem Transmitter Section

[0158] Referring to Figure 14, the code generator means 1304 includes Transmit Timing Control Logic 1401 and spreadingcode PN-Generator 1402, and the Transmit Section 1301 includes Modem Input Signal Receiver (MISR) 1410, Convolution Encoders 1411, 1412, 1413, 1414, Spreaders 1420, 1421, 1422, 1423, 1424, and Combiner 1430. The Transmit Section 1301 receives the message data channels MESSAGE, convolutionally encodes each message data channel in the respective convolutional encoder 1411, 1412, 1413, 1414, modulates the data with random spreading code sequence in the respective spreader 1420, 1421, 1422, 1423, 1424, and combines modulated data from all channels, including the pilot code received in the described embodiment from the code generator, in the combiner 1430 to generate I and Q components for RF transmission. The Transmitter Section 1301 of the present embodiment supports four (TR0, TR1, TR2, TR3) 64, 32, 16, 8 kb/s programmable channels. The message channel data is a time multiplexed signal received from the PCM highway 1201 through PCM interface 1220 and input to the MISR 1410.

[0159] Figure 15 is a block diagram of an exemplary MISR 1410. For the exemplary embodiment of the present invention, a counter is set by the 8 KHz frame synchronization signal MPCMSYNC and is incremented by 2.048 MHz MPCMCLK from the timing circuit 1401. The counter output is compared by comparator 1502 against TRCFG values corresponding to slot time location for TR0, TR1, TR2, TR3 message channel data; and the TRCFG values are received from the MIU Controller 1230 in MCTRL. The comparator sends count signal to the registers 1505, 1506, 1507 and 1508 which clocks message channel data into buffers 1510, 1511, 1512, 1513 using the TXPCNCLK timing signal derived from the system clock. The message data is provided from the signal MSGDAT from the PCM highway signal MESSAGE when enable signals TR0EN, TR1EN, TR2EN and TR3EN from Timing Control Logic 1401 are active. In further embodiments, MESSAGE may also include signals that enable registers depending upon an encryption rate or data rate. If the counter output is equal to one of the channel location addresses, the specified transmit message data in registers 1510, 1511, 1512, 1513 are input to the convolutional encoders 1411, 1412, 1413, 1414 shown in Figure 14.

[0160] The convolutional encoder enables the use of Forward Error Correction (FEC) techniques, which are well known in the art. FEC techniques depend on introducing redundancy in generation of data in encoded form. Encoded data is transmitted and the redundancy in the data enables the receiver decoder device to detect and correct errors. One embodiment of the present invention employs convolutional encoding. Additional data bits are added to the data in the encoding process and are the coding overhead. The coding rate is expressed as the ratio of data bits transmitted to the total bits (code data + redundant data) transmitted and is called the rate "R" of the code.

[0161] Convolution codes are codes where each code bit is generated by the convolution of each new uncoded bit with a number of previously coded bits. The total number of bits used in the encoding process is referred to as the constraint length, "K", of the code. In convolutional coding, data is clocked into a shift register ofK bits length so that an incoming bit is clocked into the register, and it and the existing K-1 bits are convolutionally encoded to create a new symbol. The convolution process consists of creating a symbol consisting of a module-2 sum of a certain pattern of available bits, always including the first bit and the last bit in at least one of the symbols.

[0162] Figure 16 shows the block diagram of a K=7, R=1/2 convolution encoder suitable for use as the encoder 1411 shown in Figure 14. This circuit encodes the TR0 Channel as used in one embodiment of the present invention. Seven-Bit Register 1601 with stages Q1 through Q7 uses the signal TXPNCLK to clock in TR0 data when the TR0EN signal is asserted. The output value of stages Q1, Q2, Q3, Q4, Q6, and Q7 are each combined using EXCLUSIVE-OR Logic 1602, 1603 to produce respective I and Q channel FEC data for the TR0 channel FECTR0DI and FECTR0DQ.

[0163] Two output symbol streams FECTR0DI and FECTR0DQ are generated. The FECTR0DI symbol stream is generated by EXCLUSIVE OR Logic 1602 of shift register outputs corresponding to bits 6, 5, 4,3, and 0, (Octal 171) and is designed as In phase component "I" of the transmit message channel data. The symbol stream FECTR0DQ is likewise generated by EXCLUSIVE-OR logic 1603 of shift register outputs from bits 6, 43, 1 and 0, (Octal 133) and is designated as Quadrature component "Q" of the transmit message channel data. Two symbols are transmitted to represent a single encoded bit creating the redundancy necessary to enable error correction to take place on the receiving end.

[0164] Referring to Figure 14, the shift enable clock signal for the transmit message channel data is generated by the Control Timing Logic 1401. The convolutionally encoded transmit message channel output data for each channel is applied to the respective spreader 1420, 1421, 1422, 1423, 1424 which multiplies the transmit message channel data by its preassigned spreading code sequence from code generator 1402. This spreading code sequence is generated by control 1303 as previously described, and is called a random pseudonoise signature sequence (PN-code).

[0165] The output signal of each spreader 1420, 1421, 1422, 1423, 1424 is a spread transmit data channel. The operation of the spreader is as follows: the spreading of channel output (I + jQ) multiplied by a random sequence (PNI + jPNQ) yields the In-phase component I of the result being composed of (I xor PNI) and (-Q xor PNQ). Quadrature component Q of the result is (Q xor PNI) and (I xor PNQ). Since there is no channel data input to the pilot channel logic (I=1, Q values are prohibited), the spread output signal for pilot channels yields the respective sequences PNI for I component and PNQ for Q component.

[0166] The combiner 1430 receives the I and Q spread transmit data channels and combines the channels into an I modem transmit data signal (TXIDAT) and a Q modem transmit data signal (TXQDAT). The I-spread transmit data and the Q spread transmit data are added separately.

[0167] For an SU, the CDMA modem Transmit Section 1301 includes the FIR filters to receive the I and Q channels from the combiner to provide pulse shaping, close-in spectral control and x / sin (x) correction for the transmitted signal. Separate but identical FIR filters receive the I and Q spread transmit data streams at the chipping rate, and the output signal of each of the filters is at twice the chipping rate. The exemplary FIR filters are 28 tap even symmetrical filters, which upsample (interpolate) by 2. The upsampling occurs before the filtering, so that 28 taps refers to 28 taps at twice the chipping rate, and the upsampling is accomplished by setting every other sample a zero. Exemplary coefficients are shown in Table 11.

Table 11 -

Coefficient Values														
Coeff.No.:	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Value:	3	-11	-34	-22	19	17	-32	-19	52	24	94	-31	277	468
Coeff.No.	14	15	16	17	18	19	20	21	22	24	25	26	27	
Value	277	-31	-94	24	52	-19	-32	17	19	-22	-34	-11	3	

CDMA Modem Receiver Section

[0168] Referring to Figures 9 and 12, the RF receiver 950 of the present embodiment accepts analog input I and Q CDMA channels, which are transmitted to the CDMA modems 1210, 1211, 1212, 1215 through the MIUs 931, 932, 933 from the VDC 940. These I and Q CMDA channel signals are sampled by the CDMA modem receive section 1302 (shown in Figure 13) and converted to I and Q digital receive message signal using an Analog to Digital (A/D) converter 1730, shown in Figure 17. The sampling rate of the A/D converter of the exemplary embodiment of the present invention is equivalent to the despreading code rate. The I and Q digital receive message signals are then despread with correlators using six different complex spreading code sequences corresponding to the despreading code sequences of the four channels (TR0, TR1, TR2, TR3), APC information and the pilot code.

[0169] Time synchronization of the receiver to the received signal is separated into two phases; there is an initial acquisition phase and then a tracking phase after the signal timing has been acquired. The initial acquisition is done by shining the phase of the locally generated pilot code sequence relative to the received signal and comparing the output of the pilot despreader to a threshold. The method used is called sequential search. Two thresholds (match and dismiss) are calculated from the auxiliary despreader. Once the signal is acquired, the search process is stopped and the tracking process begins. The tracking process maintains the code generator 1304 (shown in Figures 13 and 17) used by the receiver in synchronization with the incoming signal. The tracking loop used is the Delay-Locked Loop (DLL) and is implemented in the acquisition & track 1701 and the IPM 1702 blocks of Figure 17.

[0170] In Figure 13, the modem controller 1303 implements the Phase Lock Loop (PLL) as a software algorithm in SW PLL logic 1724 of Figure 17 that calculates the phase and frequency shift in the received signal relative to the transmitted signal. The calculated phase shifts are used to derotate the phase shifts in rotate and combine blocks 1718, 1719, 1720, 1721 of the multipath data signals for combining to produce output signals corresponding to receive channels TR0', TR1', TR2', TR3'. The data is then Viterbi decoded in Viterbi Decoders 1713, 1714, 1715, 1716 to remove the convolutional encoding in each of the received message channels.

[0171] Figure 17 indicates that the Code Generator 1304 provides the code sequences $Pn_i(t)$, i=1,2, ..I used by the receive channel despreaders 1703, 1704, 1705, 1706, 1707, 1708, 1709. The code sequences generated are timed in response to the SYNK signal of the system clock signal and are determined by the CCNTRL signal from the modem controller 1303 shown in Figure 13. Referring to Figure 17, the CDMA modem receiver section 1302 includes Adaptive Matched Filter (AMF) 1710, Channel despreaders 1703, 1704, 1705, 1706, 1707, 1708, 1709, Pilot AVC 1711, Auxiliary AVC 1712, Viterbi decoders 1713, 1714, 1715, 1716, Modem output interface (MOI) 1717, Rotate and Combine logic 1718, 1719, 1720, 1721, AMF Weight Generator 1722, and Quantile Estimation logic 1723.

[0172] In another embodiment of the invention, the CDMA modem receiver also includes a Bit error Integrator to measure the BER of the channel and idle code insertion logic between the Viterbi decoders 1713, 1714, 1715, 1716 and the MOI 1717 to insert idle codes in the event of loss of the message data.

[0173] The Adaptive Matched Filter (AMF) 1710 resolves multipath interference introduced by the air channel. The exemplary AMF 1710 uses an 11 stage complex FIR filter as shown in Figure 18. The received I and Q digital message signals are received at the register 1820 from the A/D 1730 of Figure 17 and are multiplied in multipliers 1801, 1802, 1803, 1810, 1811 by I and Q channel weights W1 to W11 received from AMF weight generator 1722 of Figure 17. In the exemplary embodiment, the A/D 1730 provides the I and Q digital receive message signal data as 2's complement values, 6 bits for I and 6 bits for Q which are clocked through an 11 stage shift register 1820 responsive to the receive spreading -code clock signal RXPNCLK. The signal RXPNCLK is generated by the timing section 1401 of code generation logic 1304. Each stage of the shift register is tapped and complex multiplied in the multipliers 1801, 1802, 1803, 1810, 1811 by individual (6-bit I and 6-bit Q) weight values to provide 11 tap-weighted products which are summed in adder 1830, and limited to 7-bit I and 7-bit Q values.

[0174] The CDMA modem receive section 1302 (shown in Figure 13) provides independent channel despreaders 1703, 1704, 1705, 1706, 1707, 1708, 1709 (shown in Figure 17) for despreading the message channels. The described embodiment despreads 7 message channels, each despreader accepting a 1-bit I b 1-bit Q despreading code signal to perform a complex correlation of this code against a 8-bit I by 8-bit Q data input. The 7 despreaders correspond to

the 7 channels: Traffic Channel 0 (TR0'), TR1', TR2', TR3', AUX (a spare channel), Automatic Power Control (APC) and pilot (PLT).

[0175] The Pilot AVC 1711 shown in Figure 19 receives the I and Q Pilot Spreadingcode sequence values PCI and PCQ into shift register 1920 responsive to the timing signal RXPNCLK, and includes 11 individual despreaders 1901 through 1911 each correlating the I and Q digital receive message signal data with a one chip delayed version of the same pilot code sequence. Signals OE1, OE2, ..OE11 are used by the modem control 1303 to enable the despreading operation. The output signals of the despreaders are combined in combiner 1920 forming correlation signal DSPRDAT of the Pilot AVC 1711, which is received by the ACQ & Track logic 1701 (shown in Figure 17), and ultimately by modem controller 1303 (shown in Figure 13). The ACQ & Track logic 1701 uses the correlation signal value to determine if the local receiver is synchronized with its remote transmitter.

[0176] The Auxiliary AVC 1712 also receives the I and Q digital receive message signal data and, in the described embodiment, includes four separate despreaders 2001, 2002, 2003, 2004 as shown in Figure 20. Each despreader receives and correlates the I and Q digital receive message data with delayed versions of the same despreading code sequence PARI and PARQ which are provided by code generator 1304 input to and contained in shift register 2020. The output signals of the despreaders 2001, 2002, 2003, 2004 are combined in combiner 2030 which provides noise correlation signal ARDSPRDAT. The auxiliary AVC spreading code sequence does not correspond to any transmit spreading code sequence of the system. Signals OE1, OE2, ..OE4 are used by the modem control 1303 to enable the despreading operation. The Auxiliary AVC 1712 provides a noise correlation signal ARDSPRDAT from which quantile estimates are calculated by the Quantile estimator 1733, and provides a noise level measurement to the ACQ & Track logic 1701 (shown in Figure 17) and modem controller 1303 (shown in Figure 13).

[0177] Each despread channel output signal corresponding to the received message channels TR0', TR1', TR2', and TR3' is input to a corresponding Viterbi decoder 1713, 1714, 1715, 1716 shown in Figure 17 which performs forward error correction on convolutionally encoded data. The Viterbi decoders of the exemplary embodiment have a constraint length of K=7 and a rate of R=1/2. The decoded despread message channel signals are transferred from the CDMA modem to the PCM Highway 1201 through the MOI 1717. The operation of the MOI is essentially the same as the operation of the MISR of the transmit section 1301 (shown in Figure 13) except in reverse.

[0178] The CDMA modem receiver section 1302 implements several different algorithms during different phases of the acquisition, tracking and despreading of the receive CDMA message signal.

[0179] When the received signal is momentarily lost (or severely degraded) the idle code insertion algorithm inserts idle codes in place of the lost or degraded receive message data to prevent the user from hearing loud noise bursts on a voice call. The idle codes are sent to the MOI 1717 (shown in Figure 17) in place of the decoded message channel output signal from the Viterbi decoders 1713, 1714, 1715, 1716. The idle code used for each traffic channel is programmed by the Modem Controller 1303 by writing the appropriate pattern IDLE to the MOI, which in the present embodiment is a 8 bit word for a 64 kb/s stream, 4 bit word for a 32 kb/s stream.

Modem Algorithms for Acquisition and Tracking of Received Pilot Signal

[0180] The acquisition and tracking algorithms are used by the receiver to determine the approximate code phase of a received signal, synchronize the local modem receiver despreaders to the incoming pilot signal, and track the phase of the locally generated pilot code sequence with the received pilot code sequence. Referring to Figures 13 and 17, the algorithms are performed by the Modem controller 1303, which provides clock adjust signals to code generator 1304. These adjust signals cause the code generator for the despreaders to adjust locally generated code sequences in response to measured output values of the Pilot Rake 1711 and Quantile values from quantile estimators 1723B. Quantile values are noise statistics measured from the In-phase and Quadrature channels from the output values of the AUX Vector Correlator 1712 (shown in Figure 17). Synchronization of the receiver to the received signal is separated into two phases; an initial acquisition phase and a tracking phase. The initial acquisition phase is accomplished by clocking the locally generated pilot spreading code sequence at a higher or lower rate than the received signal's spreading code rate, sliding the locally generated pilot spreading code sequence and performing sequential probability ratio test (SPRT) on the output of the Pilot Vector correlator 1711. The tracking phase maintains the locally generated spreading code pilot sequence in synchronization with the incoming pilot signal.

[0181] The SU cold acquisition algorithm is used by the SU CDMA modem when it is first powered up, and therefore has no knowledge of the correct pilot spreading code phase, or when an SU attempts to reacquire synchronization with the incoming pilot signal but has taken an excessive amount of time. The cold acquisition algorithm is divided into two sub-phases. The first subphase consists of a search over the length 233415 code used by the FBCH. Once this sub-code phase is acquired, the pilot's 233415 x 128 length code is known to within an ambiguity of 128 possible phases. The second subphase is a search of these remaining 128 possible phases. In order not to lose synch with the FBCH, in the second phase of the search, it is desirable to switch back and forth between tracking of the FBCH code and attempting acquisition of the pilot code.

[0182] The RCS acquisition of short access pilot (SAXPT) algorithm is used by an RCS CDMA modem to acquire the SAXPT pilot signal of an SU. The algorithm is a fast search algorithm because the SAXPT is a short code sequence of length N, where N = chips/symbol, and ranges from 45 to 195, depending on the system's bandwidth. The search cycles through all possible phases until acquisition is complete.

[0183] The RCS acquisition of the long access pilot (LAXPT) algorithm begins immediately after acquisition of SAXPT. The SU's code phase is known within a multiple of a symbol duration, so in the exemplary embodiment of the invention there may be 7 to 66 phases to search within the round trip delay from the RCS. This bound is a result of the SU pilot signal being synchronized to the RCS Global pilot signal.

[0184] The re-acquisition algorithm begins when loss of code lock (LOL) occurs. A Z-search algorithm is used to speed the process on the assumption that the code phase has not drifted far from where it was the last time the system was locked. The RCS uses a maximum width of the Z-search windows bounded by the maximum round trip propagation delay.

[0185] The Pre-Track period immediately follows the acquisition or re-acquisition algorithms and immediately precedes the tracking algorithm. Pre-track is a fixed duration period during which the receive data provided by the modem is not considered valid. The Pre-Track period allows other modem algorithms, such as those used by the ISW PLL 1724, ACQ & Tracking, AMF Weight GEN 1722, to prepare and adapt to the current channel. The Pre-Track period is two parts. The first part is the delay while the code tracking loop pulls in. The second part is the delay while the AMF tap weight calculations are performed by the AMF Weight Gen 1722 to produce settled weighting coefficients. Also in the second part of the Pre-Track period, the carrier tracking loop is allowed to pull in by the SW PLL 1724, and the scalar quantile estimates are performed in the Quantile estimator 1723A.

[0186] The Tracking Process is entered after the Pre-Track period ends. This process is actually a repetitive cycle and is the only process phase during which receive data provided by the modem may be considered valid. The following operations are performed during this phase: AMF Tap Weight Update, Carrier Tracking, Code Tracking, Vector Quantile Update, Scalar Quantile Update, Code Lock Check, Derotation and Symbol Summing, and Power Control (forward and reverse)

[0187] If LOL is detected, the modem receiver terminates the Track algorithm and automatically enters the reaquisition algorithm. In the SU, a LOL causes the transmitter to be shut down. In the RCS, LOL causes forward power control to be disabled with the transmit power held constant at the level immediately prior to loss of lock. It also causes the return power control information being transmitted to assume a 010101...pattern, causing the SU to hold its transmit power constant. This can be performed using the signal lock check function which generates the reset signal to the acquisition and tracking circuit 1701.

[0188] Two sets of quantile statistics are maintained, one by Quantile estimator 1723B and the. other by the scalar Quantile Estimator 1723A. Both are used by the modem controller 1303. The first set is the "vector" quantile information, so named because it is calculated from the vector of four complex values generated by the AUX AVC receiver 1712. The second set is the scalar quantile information, which is calculated from the single complex value AUX signal that is output from the AUX Despreader 1707. The two sets of information represent different sets of noise statistics used to maintain a pre-determined Probability of False Alarm (P_{fa}). The vector quantile data is used by the acquisition and reaquisition algorithms implemented by the modem controller 1303 to determine the presence of a received signal in noise, and the scalar quantile information is used by the code lock check algorithm.

[0189] For both the vector and scalar cases, quantile information consists of calculated values of lambda0 through lambda2, which are boundary values used to estimate the probability distribution function (p.d.f) of the despread receive signal and determine whether the modem is locked to the PN code. The Aux_Power value used in the following C-subroutine is the magnitude squared of the AUX signal output of the scalar correlator array for the scalar quantiles, and the sum of the magnitudes squared for the vector case. In both cases the quantiles are then calculated using the following C-subroutine:

```
for (n = 0; n < 3; n++) {
    lambda [n] += (lambda [n] < Aux_Power) ? CG[n] : GM[n];
}
```

where CG[n] are positive constants and GM[n] are negative constants (different values are used for scalar and vector quantiles).

[0190] During the acquisition phase, the search of the incoming pilot signal with the locally generated pilot code sequence employs a series of sequential tests to determine if the locally generated pilot code has the correct code

phase relative to the received signal. The search algorithms use the Sequential Probability Ratio Test (SPRT) to determine whether the received and locally generated code sequences are in phase. The speed of acquisition is increased by parallelism resulting from having a multi-fingered receiver. For example, in the described embodiment of the invention the main Pilot Rake 1711 has a total of 11 fingers representing a total phase period of 11 chip periods. For acquisition 8 separate sequential probability ratio tests (SPRTs) are implemented, with each SPRT observing a 4 chip window. Each window is offset from the previous window by one chip, and in a search sequence any given code phase is covered by 4 windows. If all 8 of the SPRT tests are rejected, then the set of windows is moved by 8 chips. If any of the SPRT's is accepted, then the code phase of the locally generated pilot code sequence is adjusted to attempt to center the accepted SPRT's phase within the Pilot AVC. It is likely that more than one SPRT reaches the acceptance threshold at the same time. A table lookup is used cover all 256 possible combinations of accept/reject and the modem controller uses the information to estimate the correct center code phase within the Pilot Rake 1711. Each SPRT is implemented as follows (all operations occur at 64k symbol rate): Denote the fingers' output level values as I_Finger [n] and Q_Finger[n], where n=0..10 (inclusive, 0 is earliest (most advanced) finger), then the power of each window is:

$$\text{Power Window}[i] = \sum_{n} (\text{I\_Finger}^2[n] + \text{Q\_Finger}^2[n])$$

To implement the SPRT's the modem controller then performs for each of the windows the following calculations which are expressed as a pseudo-code subroutine:

```
/* find bin for Power */
tmp = SIGMA[0];
for (k = 0; k< 3; k++) {
  if (Power > lambda [k]) tmp = SIGMA[k+1];
}
test_statistic += tmp; /* update statistic */
if(test_statistic > ACCEPTANCE_THRESHOLD)you've got ACQ;
else if (test_statistic < DISMISSAL_THRESHOLD) {
   forget this code phase;
} else keep trying - get more statistics;
```

where lambda[k] are as defined in the above section on quantile estimation, and SIGMA[k], ACCEPTANCE_THRESHOLD and DISMISSAL_THRESHOLD are predetermined constants. Note that SIGMA[k] is negative for values for low values of k, and positive for right values of k, such that the acceptance and dismissal thresholds can be constants rather than a function of how many symbols worth of data have been accumulated in the statistic.

[0191] The modem controller determines which bin delimited by the values of lambda[k] the Power level falls into which allows the modem controller to develop an approximate statistic.

[0192] For the present algorithm, the control voltage is formed as $\varepsilon = y^T B y$, where y is a vector formed from the complex valued output values of the Pilot Vector correlator 1711, and B is a matrix consisting of the constant values pre-determined to maximize the operating characteristics while minimizing the noise as described previously with reference to the Quadratic Detector.

[0193] To understand the operation of the Quadratic Detector, it is useful to consider the following. A spread spectrum (CDMA) signal, s(t) is passed through a multipath channel with an impulse response $h_c(t)$. The baseband spread signal is described by equation (30).

$$s(t) = \sum_i C_i p(t - iT_c) \quad (30)$$

where C_i is a complex spreading code symbol, p(t) is a predefined chip pulse and T_c is the chip time spacing, where $T_c = 1/R_c$ and R_c is the chip rate.

[0194] The received baseband signal is represented by equation (31)

$$r(t) = \sum_i C_i q(t - iT_c - \tau) + n(t) \quad (31)$$

where $q(t) = p(t)*h_c(t)$, τ is an unknown delay and n(t) is additive noise. The received signal is processed by a filter, $h_R(t)$, so the waveform, x(t), to be processed is given by equation (32).

$$x(t) = \sum_i C_i f(t - iT_c - \tau) + z(t) \quad (32)$$

where $f(t) = q(t)*h_R(t)$ and $z(t) = n(t)*h_R(t)$.

[0195] In the exemplary receiver, samples of the received signal are taken at the chip rate, that is to say, $1/T_c$. These samples, $x(mT_c+\tau')$, are processed by an array of correlators that compute, during the rth correlation period, the quantities given by equation (33)

$$v_k^{(r)} = \sum_{m=rL}^{rL+L-1} x(mT_c + \tau')C_{m+k}^* \quad (33)$$

[0196] These quantities are composed of a noise component $w_k^{(\tau)}$ and a deterministic component $y_k^{(r)}$ given by equation (34).

$$y_k^{(r)} = E[v_k^{(r)}] = Lf(kT_c + \tau' - \tau) \quad (34)$$

In the sequel, the time index r may be suppressed for ease of writing, although it is to be noted that the function f(t) changes slowly with time.

[0197] The samples are processed to adjust the sampling phase, τ', in an optimum fashion for further processing by the receiver, such as matched filtering. This adjustment is described below. To simplify the representation of the process, it is helpful to describe it in terms of the function $f(t+\tau)$, where the time-shift, τ, is to be adjusted. It is noted that the function $f(t+\tau)$ is measured in the presence of noise. Thus, it may be problematical to adjust the phase τ' based on measurements of the signal $f(t+\tau)$. To account for the noise, the function v(t): $v(t)=f(t)+m(t)$ is introduced, where the term m(t) represents a noise process. The system processor may be derived based on considerations of the function v(t).

[0198] The process is non-coherent and therefore is based on the envelope power function $|v(t+\tau)|^2$. The functional $e(\tau')$ given in equation (35) is helpful for describing the process.

$$e(\tau') = \int_{-\infty}^{0} |v(t + \tau' - \tau)|^2 dt - \int_{0}^{\infty} |v(t + \tau' - \tau)|^2 dt \quad (35)$$

The shift parameter is adjusted for $e(\tau')=0$, which occurs when the energy on the interval $(-\infty,\tau'-\tau]$ equals that on the interval $[\tau'-\tau,\infty)$. The error characteristic is monotonic and therefore has a single zero crossing point. This is the desirable quality of the functional. A disadvantage of the functional is that it is ill-defined because the integrals are unbounded when noise is present. Nevertheless, the functional $e(\tau')$ may be cast in the form given by equation (36).

$$e(\tau') = \int_{-\infty}^{\infty} w(t)|v(t+\tau'-\tau)|^2 dt \qquad (36)$$

where the characteristic function w(t) is equal to sgn(t), the signum function.

[0199] To optimize the characteristic function w(t), it is helpful to define a figure of merit, F, as set forth in equation (37).

$$F = \frac{\overline{[e(\tau_0'+T_A)-e(\tau_0'-T_A)]}^2}{VAR\{e(\tau_0')\}} \qquad (37)$$

The numerator of F is the numerical slope of the mean error characteristic on the interval $[-T_A, T_A]$ surrounding the tracked value, τ_0'. The statistical mean is taken with respect to the noise as well as the random channel, $h_c(t)$. It is desirable to specify a statistical characteristic of the channel in order to perform this statistical average. For example, the channel may be modeled as a Wide Sense Stationary Uncorrelated Scattering (WSSUS) channel with impulse response $h_c(t)$ and a white noise process U(t) that has an intensity function g(t) as shown in equation (38).

$$h_c(t) = \sqrt{g(t)U(t)} \qquad (38)$$

[0200] The variance of $e(\tau)$ is computed as the mean square value of the fluctuation

$$e'(\tau) = e(\tau) - \langle e(\tau)\rangle \qquad (39)$$

where $<e(\tau)>$ is the average of $e(\tau)$ with respect to the noise.

[0201] Optimization of the figure of merit F with respect to the function w(t) may be carried out using well-known Variational methods of optimization.

[0202] Once the optimal w(t) is determined, the resulting processor may be approximated accurately by a quadratic sample processor which is derived as follows.

[0203] By the sampling theorem, the signal v(t), bandlimited to a bandwidth W may be expressed in terms of its samples as shown in equation (40).

$$v(t) = \Sigma v(k/W)\mathrm{sinc}[(Wt - k)\pi] \qquad (40)$$

substituting this expansion into equation (z+6) results in an infinite quadratic form in the samples $v(k/W+\tau'-\tau)$. Making the assumption that the signal bandwidth equals the chip rate allows the use of a sampling scheme that is clocked by the chip clock signal to be used to obtain the samples. These samples, v_k are represented by equation (41).

$$v_k = v(kT_c + \tau' - \tau) \qquad (41)$$

This assumption leads to a simplification of the implementation. It is valid if the aliasing error is small.

[0204] In practice, the quadratic form that is derived is truncated. An example normalized B matrix is given below in Table 12. For this example, an exponential delay spread profile $g(t)=\exp(-t/\tau)$ is assumed with τ equal to one chip. An aperture parameter T_A equal to one and one-half chips has also been assumed. The underlying chip pulse has a raised cosine spectrum with a 20% excess bandwidth.

Table 12 -

Example B matrix										
0	0	0	0	0	0	0	0	0	0	0
0	0	-0.1	0	0	0	0	0	0	0	0
0	-0.1	0.22	0.19	-0.19	0	0	0	0	0	0
0	0	0.19	1	0.45	-0.2	0	0	0	0	0
0	0	-0.19	0.45	0.99	0.23	0	0	0	0	0
0	0	0	-0.2	0.23	0	-0.18	0.17	0	0	0
0	0	0	0	0	-0.18	-0.87	-0.42	0.18	0	0
0	0	0	0	0	0.17	-0.42	-0.92	-0.16	0	0
0	0	0	0	0	0	0.18	-0.16	-0.31	0	0
0	0	0	0	0	0	0	0	0	-0.13	0
0	0	0	0	0	0	0	0	0	0	0

[0205] Code tracking is implemented via a loop phase detector that is implemented as follows. The vector y is defined as a column vector which represents the 11 complex output level values of the Pilot AVC 1711, and B denotes an 11 x 11 symmetric real valued coefficient matrix with pre-determined values to optimize performance with the non-coherent Pilot AVC output values y. The output signal ε of the phase detector is given by equation (42):

$$\varepsilon = y^T By \tag{42}$$

The following calculations are then performed to implement a proportional plus integral loop filter and the VCO:

$$x[n] = x[n-1] + \beta\varepsilon$$

$$z[n] = z[n-1] + x[n] + \alpha\varepsilon$$

for β and α which are constants chosen from modeling the system to optimize system performance for the particular transmission channel and application, and where x[n] is the loop filter's integrator output value and z[n] is the VCO output value. The code phase adjustments are made by the modem controller the following C-subroutine:

```
if (z > zmx) {
    delay phase 1/16 chip;
    z -= zmax;
} else if (z < -zmax) {
    advance phase 1/16 chip;
    z += zmax;
}
```

[0206] A different delay phase could be used in the above pseudo-code consistant with the present invention.

[0207] The AMF Tap-Weight Update Algorithm of the AMF Weight Gen 1722 occurs periodically to de-rotate and

scale the phase of each finger value of the Pilot Rake 1711 by performing a complex multiplication of the Pilot AVC finger value with the complex conjugate of the current output value of the carrier tracking loop and applying the product to a low pass filter and form the complex conjugate of the filter values to produce AMF tap-weight values, which are periodically written into the AMF filters of the CDMA modem.

[0208] The lock check algorithm, shown in Figure 17, is implemented by the modem controller 1303 performing SPRT operations on the output signal of the scalar correlator array. The SPRT technique is the same as that for the acquisition algorithms, except that the acceptance and rejection thresholds are changed to increase the probability of detection of lock.

[0209] Carrier tracking is accomplished via a second order loop that operates on the pilot output values of the scalar correlated array. The phase detector output is the hard limited version of the quadrature component of the product of the (complex valued) pilot output signal of the scalar correlated array and the VCO output signal. The loop filter is a proportional plus integral design. The VCO is a pure summation, accumulated phase error ϕ, which is converted to the complex phasor $\cos \phi + j \sin \phi$ using a look-up table in memory.

[0210] The previous description of acquisition and tracking algorithm focuses on a non-coherent method because the acquisition and tracking algorithm described requires non-coherent acquisition following by non-coherent tracking because during acquisition a coherent reference is not available until the AMF, Pilot AVC, Aux AVC, and DPLL are in an equilibrium state. However, it is known in the art that coherent tracking and combining is always optimal because in non-coherent tracking and combining the output phase information of each Pilot AVC finger is lost. Consequently, another embodiment of the invention employs a two step acquisition and tracking system, in which the previously described non-coherent acquisition and tracking algorithm is implemented first, and then the algorithm switches to a coherent tracking method. The coherent combining and tracking method is similar to that described previously, except that the error signal tracked is of the form:

$$\varepsilon = y^T A y \tag{43}$$

where y is defined as a column vector which represents the 11 complex output level values of the Pilot AVC 1711, and A denotes an 11 x 11 symmetric real valued coefficient matrix with pre-determined values to optimize performance with the coherent Pilot AVC outputs y. An exemplary A matrix is shown below.

$$A = \begin{matrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{matrix} \tag{44}$$

$$\begin{matrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{matrix}$$

[0211] Referring to Figure 9, the Video Distribution Controller Board (VDC) 940 of the RCS is connected to each MIU 931, 932, 933 and the RF Transmitters/Receivers 950. The VDC 940 is shown in Figure 21. The Data Combiner Circuitry (DCC) 2150 includes a Data Demultiplexer 2101, Data Summer 2102, FIR Filters 2103, 2104, and a Driver 2111. The DCC 2150 1) receives the weighted CDMA modem I and Q data signal MDAT from each of the MIUs, 931, 932, 933, 2) sums the I and Q data with the digital bearer channel data from each MIU 931, 932, 933, 3) and sums the result with the broadcast data message signal BCAST and the Global Pilot spreading code GPILOT provided by the master MIU modem 1210, 4) band shapes the summed signals for transmission, and 5) produces analog data signal

for transmission to the RF Transmitter/Receiver.

[0212] FIR Filters 2103, 2104 are used to modify the MIU CDMA Transmit I and Q Modem Data before transmission. The WAC transfers FIR Filter Coefficient data through the Serial Port link 912 through the VDC Controller 2120 and to the FIR filters 2103, 2104. Each FIR Filter 2103, 2104 is Configured separately. The FIR Filters 2103, 2104 employ Up-Sampling to operate at twice the chip rate so zero data values are sent after every MIU CDMA Transmit Modem DATI and DATQ value to produce FTXI and FTXQ

[0213] The VDC 940 distributes the AGC signal AGCDATA from the AGC 1750 of the MIUs 931, 932, 933 to the RF Transmitter/Receiver 950 through the Distribution interface (DI) 2110. The VDC DI 2110 receives data RXI and RXQ from the RF Transmitter/Receiver and distributes the signal as VDATAI and VDATAQ to MIUs 931, 932, 933.

[0214] Referring to Figure 21, the VDC 940 also includes a VDC controller 2120 which monitors status and fault information signals MIUSTAT from MIUs and connects to the serial link 912 and HSBS 970 to communicate with WAC 920 shown in Figure 9. The VDC controller 2120 includes a microprocessor, such as an Intel 8032 Microcontroller, an oscillator (not shown) providing timing signals, and memory (not shown). The VDC controller memory includes a Flash Prom (not shown) to contain the controller program code for the 8032 Microprocessor, and an SRAM (not shown) to contain the temporary data written to and read from memory by the microprocessor.

[0215] Referring to Figure 9, the present invention includes a RF Transmitter/Receiver 950 and power amplifier section 960. Referring to Figure 22 , the RF Transmitter/Receiver 950 is divided into three sections: the transmitter module 2201, the receiver module 2202, and the Frequency Synthesizer 2203. Frequency Synthesizer 2203 produces a transmit carrier frequency TFREQ and a receive carrier frequency RFREQ in response to a Frequency control signal FREQCTRL received from the WAC 920 on the serial link 912. In the transmitter module 2201, the input analog I and Q data signals TXI and TXQ from the VDC are applied to the Quadrature modulator 2220, which also receives a transmit carrier frequency signal TFREQ from the Frequency Synthesizer 2203 to produce a quadrature modulated transmit carrier signal TX. The analog transmit carrier modulated signal, an upconverted RF signal, TX is then applied to the Transmit Power Amplifier 2252 of the Power Amplifier 960. The amplified transmit carrier signal is then passed through the High Power Passive Components (HPPC) 2253 to the Antenna 2250, which transmits the upconverted RF signal to the communication channel as a CDMA RF signal. In one embodiment of the invention, the Transmit Power Amplifier 2252 comprises eight amplifiers of approximately 60 watts peak-to-peak each.

[0216] The HPPC 2253 comprises a lightning protector, an output filter, a 10 dB directional coupler, an isolator, and a high power termination attached to the isolator.

[0217] A receive CDMA RF signal is received at the antenna 2250 from the RF channel and passed through the HPPC 2253 to the Receive Power Amplifier 2251. The receive power amplifier 2251 includes, for example, a 30 watt power transistor driven by a 5 watt transistor. The RF receive module 2202 has quadrature modulated receive carrier signal RX from the receive power amplifier. The receive module 2202 includes a Quadrature demodulator 2210 which takes the receive carrier modulated signal RX and the receive carrier frequency signal RFREQ from the Frequency Synthesizer 2203, synchronously demodulates the carrier, and provides analog I and Q channels. These channels are filtered to produce the signals RXI and RXQ, which are transferred to the VDC 940.

The Subscriber Unit

[0218] Figure 23 shows the Subscriber Unit (SU) of one embodiment of the present invention. As shown, the SU includes an RF section 2301 including a RF modulator 2302, RF demodulator 2303, and splitter/isolator 2304 which receive Global and Assigned logical channels including traffic and control messages and Global Pilot signals in the Forward link CDMA RF channel signal, and transmit Assigned Channels and Reverse Pilot signals in the Reverse Link CDMA RF channel. The Forward and Reverse links are received and transmitted respectively through antenna 2305. The RF section employs, in one exemplary embodiment, a conventional dual conversion superheterodyne receiver having a synchronous demodulator responsive to the signal ROSC. Selectivity of such a receiver is provided by a 70 MHz transversal SAW filter (not shown). The RF modulator includes a synchronous modulator (not shown) responsive to the carrier signal TOSC to produce a quadrature modulated carrier signal. This signal is stepped up in frequency by an offset mixing circuit (not shown).

[0219] The SU further includes a Subscriber Line Interface 2310, including the functionality of a control (CC) generator, a Data Interface 2320, an ADPCM encoder 2321, an ADPCM decoder 2322, an SU controller 2330, an SU clock signal generator 2331, memory 2332, and a CDMA modem 2340, which is essentially the same as the CDMA modem 1210 described above wih reference to Figure 13. It is noted that data interface 2320, ADPCM Encoder 2321 and ADPCM Decoder 2322 are typically provided as a standard ADPCM Encoder/Decoder chip.

[0220] The Forward Link CDMA RF Channel signal is applied to the RF demodulator 2303 to produce the Forward link CDMA signal. The Forward Link CDMA signal is provided to the CDMA modem 2340, which acquires synchronization with the Global pilot signal, produces global pilot synchronization signal to the Clock 2331, to generate the system timing signals, and despreads the plurality of logical channels. The CDMA modem 2340 also acquires the traffic

messages RMESS and control messages RCTRL and provides the traffic message signals RMESS to the Data Interface 2320 and receive control message signals RCTRL to the SU Controller 2330.

[0221] The receive control message signals RCTRL include a subscriber identification signal, a coding signal, and bearer modification signals. The RCTRL may also include control and other telecommunication signaling information. The receive control message signal RCTRL is applied to the SU controller 2330, which verifies that the call is for the SU from the Subscriber identification value derived from RCTRL. The SU controller 2330 determines the type of user information contained in the traffic message signal from the coding signal and bearer rate modification signal. If the coding signal indicates the traffic message is ADPCM coded, the traffic message RVMESS is sent to the ADPCM decoder 2322 by sending a select message to the Data Interface 2320. The SU controller 2330 outputs an ADPCM coding signal and bearer rate signal derived from the coding signal to the ADPCM decoder 2322. The traffic message signal RVMESS is the input signal to the ADPCM decoder 2322, where the traffic message signal is converted to a digital information signal RINF in response to the values of the input ADPCM coding signal.

[0222] If the SU controller 2330 determines the type of user information contained in the traffic message signal from the coding signal is not ADPCM coded, then RDMESS passes through the ADPCM encoder transparently. The traffic message RDMESS is transferred from the Data Interface 2320 directly to the Interface Controller (IC) 2312 of the subscriber line interface 2310.

[0223] The digital information signal RINF or RDMESS is applied to the subscriber line interface 2310, including a interface controller (IC) 2312 and Line Interface (LI) 2313. For the exemplary embodiment the IC is an Extended PCM Interface Controller (EPIC) and the LI is a Subscriber Line Interface Circuit (SLIC) for POTS which corresponds to RINF type signals, and a ISDN Interface for ISDN which corresponds to RDMESS type signals. The EPIC and SLIC circuits are well known in the art. The subscriber line interface 2310 converts the digital information signal RINF or RDMESS to the user defined format. The user defined format is provided to the IC 2312 from the SU Controller 2330. The LI 2310 includes circuits for performing such functions as A-law or μ-law conversion, generating dial tone and, and generating or interpreting signaling bits. The line interface also produces the user information signal to the SU User 2350 as defined by the subscriber line interface, for example POTS voice, voiceband data or ISDN data service.

[0224] For a Reverse Link CDMA RF Channel, a user information signal is applied to the LI 2313 of the subscriber line interface 2310, which outputs a service type signal and an information type signal to the SU controller. The IC 2312 of the subscriber line interface 2310 produces a digital information signal TINF which is the input signal to the ADPCM encoder 2321 if the user information signal is to be ADPCM encoded, such as for POTS service. For data or other non-ADPCM encoded user information, the IC 2312 passes the data message TDMESS directly to the Data Interface 2320. The Call control module (CC), including in the subscriber line interface 2310, derives call control information from the User information signal, and passes the call control information CCINF to the SU controller 2330. The ADPCM encoder 2321 also receives coding signal and bearer modification signals from the SU controller 2330 and converts the input digital information signal into the output message traffic signal TVMESS in response to the coding and bearer modification signals. The SU controller 2330 also outputs the reverse control signal which includes the coding signal call control information, and bearer channel modification signal, to the CDMA modem. The output message signal TVMESS is applied to the Data Interface 2320. The Data Interface 2320 sends the user information to the CDMA modem 2340 as transmit message signal TMESS. The CDMA modem 2340 spreads the output message and reverse control channels TCTRL received from the SU controller 2330, and produces the reverse link CDMA Signal. The Reverse Link CDMA signal is provided to the RF transmit section 2301 and modulated by the RF modulator 2302 to produce the output Reverse Link CDMA RF channel signal transmitted from antenna 2305.

Call Connection and Establishment Procedure

[0225] The process of bearer channel establishment consists of two procedures: the call connection process for a call connection incoming from a remote call processing unit such as an RDU (Incoming Call Connection), and the call connection process for a call outgoing from the SU (Outgoing Call Connection). Before any bearer channel can be established between an RCS and a SU, the SU must register its presence in the network with the remote call processor such as the RDU. When the off-hook signal is detected by the SU, the SU not only begins to establish a bearer channel; but also initiates the procedure for an RCS to obtain a terrestrial link between the RCS and the remote processor. The process of establishing the RCS and RDU connection is detailed in the DECT V5.1 standard.

[0226] For the Incoming Call Connection procedure shown in Figure 24, first 2401, the WAC 920 (shown in Figure 9) receives, via one of the MUXs 905, 906 and 907, an incoming call request from a remote call processing unit. This request identifies the target SU and that a call connection to the SU is desired. The WAC periodically outputs the SBCH channel with paging indicators for each SU and periodically outputs the FBCH traffic lights for each access channel. In response to the incoming call request, the WAC, at step 2420, first checks to see if the identified SU is already active with another call. If so, the WAC returns a busy signal for the SU to the remote processing unit through the MUX, otherwise the paging indicator for the channel is set.

[0227] Next, at step 2402, the WAC checks the status of the RCS modems and, at step 2421, determines whether there is an available modem for the call. If a modem is available, the traffic lights on the FBCH indicate that one or more AXCH channels are available. If no channel is available after a certain period of time, then the WAC returns a busy signal for the SU to the remote processing unit through the MUX. If an RCS modem is available and the SU is not active (in Sleep mode), the WAC sets the paging indicator for the identified SU on the SBCH to indicate an incoming call request. Meanwhile, the access channel modems continuously search for the Short Access Pilot signal (SAXPT) of the SU.

[0228] At step 2403, an SU in Sleep mode periodically enters awake mode. In awake mode, the SU modem synchronizes to the Downlink Pilot signal, waits for the SU modem AMF filters and phase locked loop to settle, and reads the paging indicator in the slot assigned to it on the SBCH to determine if there is a call for the SU 2422. If no paging indicator is set, the SU halts the SU modem and returns to sleep mode. If a paging indicator is set for an incoming call connection, the SU modem checks the service type and traffic lights on FBCH for an available AXCH.

[0229] Next, at step 2404, the SU modem selects an available AXCH and starts a fast transmit power ramp-up on the corresponding SAXPT. For a period the SU modem continues fast power ramp-up on SAXPT and the access modems continue to search for the SAXPT.

[0230] At step 2405, the RCS modem acquires the SAXPT of the SU and begins to search for the SU LAXPT. When the SAXPT is acquired, the modem informs the WAC controller, and the WAC controller sets the traffic lights corresponding to the modem to "red" to indicate the modem is now busy. The traffic lights are periodically output while continuing to attempt acquisition of the LAXPT.

[0231] The SU modem monitors, at step 2406, the FBCH AXCH traffic light. When the AXCH traffic light is set to red, the SU assumes the RCS modem has acquired the SAXPT and begins transmitting LAXPT. The SU modem continues to ramp-up power of the LAXPT ar a slower rate until Sync-Ind messages are received on the corresponding CTCH. If the SU is mistaken because the traffic light was actually set in response to another SU acquiring the AXCH, the SU modem times out because no Sync-Ind messages are received. The SU randomly waits a period of time, picks a new AXCH channel, and steps 2404 and 2405 are repeated until the SU modem receives Sync-Ind messages.

[0232] Next, at step 2407, the RCS modem acquires the LAXPT of the SU and begins sending Sync-Ind messages on the corresponding CTCH. The modem waits 10 msec for the Pilot and AUX Vector correlator filters and Phase locked loop to settle, but continues to send Synch-Ind messages on the CTCH. The modem then begins looking for a request message for access to a bearer channel (MAC_ACC_REQ), from the SU modem.

[0233] The SU modem, at step 2408, receives the Sync-Ind message and freezes the LAXPT transmit power level. The SU modem then begins sending repeated request messages for access to a bearer traffic channel (MAC_ACC_REQ) at fixed power levels, and listens for a request confirmation message (MAC_BEARER_CFM) from the RCS modem.

[0234] Next, at step 2409, the RCS modem receives a MAC_ACC_REQ message; the modem then starts measuring the AXCH power level, and starts the APC channel. The RCS modem then sends the MAC_BEARER_CFM message to the SU and begins listening for the acknowledgment MAC_BEARER_CFM_ACK of the MAC_BEARER_CFM message.

[0235] At step 2410, the SU modem receives the MAC_BEARER_CFM message and begins obeying the APC power control messages. The SU stops sending the MAC_ACC_REQ message and sends the RCS modem the MAC_BEARER_CFM_ACK message. The SU begins sending the null data on the AXCH. The SU waits 10 msec for the uplink transmit power level to settle.

[0236] The RCS modem, at step 2411, receives the MAC_BEARER_CFM_ACK message and stops sending the MAC_BEARER_CFM messages. APC power measurements continue.

[0237] Next, at step 2412, both the SU and the RCS modems have synchronized the sub-epochs, obey APC messages, measure receive power levels, and compute and send APC messages. The SU waits 10 msec for downlink power level to settle.

[0238] Finally, at step 2413, Bearer channel is established and initialized between the SU and RCS modems. The WAC receives the bearer establishment signal from the RCS modem, re-allocates the AXCH channel and sets the corresponding traffic light to green.

[0239] For the Outgoing Call Connection shown in Figure 25, the SU is placed in active mode by the off-hook signal at the user interface at step 2501.

[0240] Next, at step 2502, the RCS indicates available AXCH channels by setting the respective traffic lights.

[0241] At step 2503, the SU synchronizes to the Downlink Pilot, waits for the SU modem Vector correlator filters and phase lock loop to settle, and the SU checks service type and traffic lights for an available AXCH.

[0242] Steps 2504 through 2513 are identical to the procedure steps 2404 through 2413 for the Incoming Call Connection procedure of Figure 24, and so are not explained in detail.

[0243] In the previous procedures for Incoming Call Connection and Outgoing Call Connection, the power Ramping-Up process consists of the following events. The SU starts from very low transmit power and increases its power level

while transmitting the short code SAXPT; once the RCS modem detects the short code it turns off the traffic light. Upon detecting the changed traffic light, the SU continues ramping-up at a slower rate this time sending the LAXPT. Once the RCS modem acquires the LAXPT and sends a message on CTCH to indicate this, the SU keeps its transmit (TX) power constant and sends the MAC-Access-Request message. This message is answered with a MAC_BEARER_CFM message on the CTCH. Once the SU receives the MAC_BEAER_CFM message it switches to the traffic channel (TRCH) which is the dial tone for POTS.

[0244] When the SU captures a specific user channel AXCH, the RCS assigns a code seed for the SU through the CTCH. The code seed is used by the spreading code generator in the SU modem to produce the assigned code for the reverse pilot of the subscriber, and the spreading codes for associated channels for traffic, call control, and signaling. The SU reverse pilot spreading code sequence is synchronized in phase to the RCS system Global Pilot spreading code sequence, and the traffic, call control, and signaling spreading codes are synchronized in phase to the SU reverse pilot spreading code sequence.

[0245] If the Subscriber unit is successful in capturing a specific user channel, the RCS establishes a terrestrial link with the remote processing unit to correspond to the specific user channel. For the DECT V5.1 standard, once the complete link from the RDU to the LE is established using the V5.1 ESTABLISHMENT message, a corresponding V5.1 ESTABLISHMENT ACK message is returned from the LE to the RDU, and the Subscriber Unit is sent a CONNECT message indicating that the transmission link is complete.

Support of Special Service Types

[0246] The system of the present invention includes a bearer channel modification feature which allows the transmission rate of the user information to be switched from a lower rate to a maximum of 64 kb/s. The Bearer Channel Modification (BCM) method is used to change a 32 kb/s ADPCM channel to a 64 kb/s PCM channel to support high speed data and fax communications through the spread-spectrum communication system of the present invention.

[0247] First, a bearer channel on the RF interface is established between the RCS and SU, and a corresponding link exists between the RCS terrestrial interface and the remote processing unit, such as an RDU. The digital transmission rate of the link between the RCS and remote processing unit normally corresponds to a data encoded rate, which may be, for example, ADPCM at 32 kb/s. The WAC controller of the RCS monitors the encoded digital data information of the link received by the Line Interface of the MUX. If the WAC controller detects the presence of the 2100 Hz tone in the digital data, the WAC instructs the SU through the assigned logical control channel and causes a second, 64 kb/s duplex link to be established between the RCS modem and the SU. In addition, the WAC controller instructs the remote processing unit to establish a second 64 kb/s duplex link between the remote processing unit and the RCS. Consequently, for a brief period, the remote processing unit and the SU exchange the same data over both the 32 kb/s and the 64 kb/s links through the RCS. Once the second link is established, the remote processing unit causes the WAC controller to switch transmission only to the 64 kb/s link, and the WAC controller instructs the RCS modem and the SU to terminate and tear down the 32 kb/s link. Concurrently, the 32 kb/s terrestrial link is also terminated and torn down.

[0248] Another embodiment of the BCM method incorporates a negotiation between the external remote processing unit, such as the RDU, and the RCS to allow for redundant channels on the terrestrial interface, while only using one bearer channel on the RF interface. The method described is a synchronous switchover from the 32 kb/s link to the 64 kb/s link over the air link which takes advantage of the fact that the spreading code sequence timing is synchronized between the RCS modem and SU. When the WAC controller detects the presence of the 2100 Hz tone in the digital data, the WAC controller instructs the remote processing unit to establish a second 64 kb/s duplex link between the remote processing unit and the RCS. The remote processing unit then sends 32 kb/s encoded data and 64 kb/s data concurrently to the RCS. Once the remote processing unit has established the 64 kb/s link, the RCS is informed and the 32 kb/s link is terminated and torn down. The RCS also informs the SU that the 32 kb/s link is being torn down and to switch processing to receive unencoded 64 kb/s data on the channel. The SU and RCS exchange control messages over the bearer control channel of the assigned channel group to identify and determine the particular subepoch of the bearer channel spreading code sequence within which the RCS will begin transmitting 64 kbit/sec data to the SU. Once the subepoch is identified, the switch occurs synchronously at the identified subepoch boundary. This synchronous switchover method is more economical of bandwidth since the system does not need to maintain capacity for a 64 kb/s link in order to support a switchover.

[0249] The previously described embodiments of the BCM feature, the RCS will tear down the 32 kb/s link first, but one skilled in the art would know that the RCS could tear down the 32 kb/s link after the bearer channel has switched to the 64 kb/s link.

[0250] As another special service type, the system of the present invention includes a method for conserving capacity over the RF interface for ISDN types of traffic. This conservation occurs while a known idle bit pattern is transmitted in the ISDN D-channel when no data information is being transmitted. The CDMA system of the present invention

includes a method to prevent transmission of redundant information carried on the D-channel of ISDN networks for signals transmitted through a wireless communication link. The advantage of such method is that it reduces the amount of information transmitted and consequently the transmit power and channel capacity used by that information. The method is described as it is used in the RCS. In the first step, the controller, such as the WAC of the RCS or the SU controller of the SU, monitors the output D-channel from the subscriber line interface for a pre-determined channel idle pattern. A delay is included between the output of the line interface and the CDMA modem. Once the idle pattern is detected, the controller inhibits the transmission of the spread message channel through a message included in the control signal to the CDMA modem. The controller continues to monitor the output D-channel of the line interface until the presence of data information is detected. When data information is detected, the spread message channel is activated. Because the message channel is synchronized to the associated pilot which is not inhibited, the corresponding CDMA modem of the other end of the communication link does not have to reacquire synchronization to the message channel.

Drop Out Recovery

[0251] The RCS and SU each monitor the CDMA bearer channel signal to evaluate the quality of the CDMA bearer channel connection. Link quality is evaluated using the sequential probability ratio test (SPRT) employing adaptive quantile estimation. The SPRT process uses measurements of the received signal power, and if the SPRT process detects that the local spreading code generator has lost synchronization with the received signal spreading code or if it detects the absence or low level of a received signal, the SPRT declares loss of lock (LOL).

[0252] When the LOL condition is declared, the receiver modem of each RCS and SU begins a Z-search of the input signal with the local spreading code generator. Z-search is well known in the art of CDMA spreading code acquisition and detection. The Z-search algorithm of the present invention tests groups of eight spreading code phases ahead and behind the last known phase in larger and larger spreading code phase increments.

[0253] During the LOL condition detected by the RCS, the RCS continues to transmit to the SU on the Assigned Channels, and continues to transmit power control signals to the SU to maintain SU transmit power level. The method of transmitting power control signals is described below. Successful reacquisition desirably takes place within a specified period of time. If reacquisition is successful, the call connection continues, otherwise the RCS tears down the call connection by deactivating and deallocating the RCS modem assigned by the WAC, and transmits a call termination signal to a remote call processor, such as the RDU, as described previously.

[0254] When the LOL condition is detected by the SU, the SU stops transmission to the RCS on the Assigned Channels which forces the RCS into a LOL condition, and starts the reacquisition algorithm. If reacquisition is successful, the call connection continues, and if not successful, the RCS tears down the call connection by deactivating and deallocating the SU modem as described previously.

POWER CONTROL

General

[0255] The power control feature of the present invention is used to minimize the amount of transmit power used by an RCS and the SUs of the system, and the power control subfeature that updates transmit power during bearer channel connection is defined as automatic power control (APC). APC data is transferred from the RCS to an SU on the forward APC channel and from an SU to the RCS on the reverse APC channel. When there is no active data link between the two, the maintenance power control (MFC) subfeature updates the SU transmit power.

[0256] Transmit power levels of forward and reverse assigned channels and reverse global channels are controlled by the APC algorithm to maintain sufficient signal power to interference noise power ratio (SIR) on those channels, and to stabilize and minimize system output power. The present invention uses a closed loop power control mechanism in which a receiver decides that the transmitter should incrementally raise or lower its transmit power. This decision is conveyed back to the respective transmitter via the power control signal on the APC channel. The receiver makes the decision to increase or decrease the traasmitter's power based on two error signals. One error signal is an indication of the difference between the measured and desired despread signal powers, and the other error signal is an indication of the average received total power.

[0257] As used in the described embodiment of the invention, the term *near-end* power control is used to refer to adjusting the transmitter's output power in accordance with the APC signal received on the APC channel from the other end. This means the reverse power control for the SU and forward power control for the RCS; and the term *far-end* APC is used to refer to forward power control for the SU and reverse power control for the RCS (adjusting the opposite end's transmit power).

[0258] In order to conserve power, the SU modem terminates transmission and powers-down while waiting for a call,

defined as the sleep phase. Sleep phase is terminated by an awaken signal from the SU controller. The SU modem acquisition circuit automatically enters the reacquisition phase, and begins the process of acquiring the downlink pilot, as described previously.

Closed Loop Power Control Algorithms

[0259] The near-end power control consists of two steps: first, the initial transmit power is set; and second, the transmit power is continually adjusted according to information received from the far-end using APC.

[0260] For the SU, initial transmit power is set to a minimum value and then ramped up, for example, at a rate of 1 dB/ms until either a ramp-up timer expires (not shown) or the RCS changes the corresponding traffic light value on the FBCH to "red" indicating that the RCS has locked to the SU's short pilot SAXPT. Expiration of the timer causes the SAXPT transmission to be shut down, unless the traffic light value is set to red first, in which case the SU continues to ramp-up transmit power but at a much lower rate than before the "red" signal was detected.

[0261] For the RCS, initial transmit power is set at a fixed value, corresponding to the minimum value necessary for reliable operation as determined experimentally for the service type and the current number of system users. Global channels, such as Global Pilot or, FBCH, are always transmitted at the fixed initial power, whereas traffic channels are switched to APC.

[0262] The APC bits are transmitted as one bit up or down signals on the APC channel. In the described embodiment, the 64 kb/s APC data stream is not encoded or interleaved.

[0263] Far-end power control consists of the near-end transmitting power control information for the far-end to use in adjusting its transmit power.

[0264] The APC algorithm causes the RCS or the SU to transmit +1 if the following inequality holds, otherwise -1.

$$\alpha_1 e_1 - \alpha_2 e_2 > 0 \tag{45}$$

Here, the error signal e_1 is calculated as

$$e_1 = P_d - (1 + SNR_{REQ})P_N \tag{46}$$

where P_d is the despread signal plus noise power, P_N is the despread noise power, and SNR_{REQ} is the desired despread signal to noise ratio for the particular service type; and

$$e_2 = P_r - P_o \tag{47}$$

where Pr is a measure of the received power and Po is the automatic gain control (AGC) circuit set point. The weights α_1 and α_2 in equation (33) are chosen for each service type and APC update rate.

Maintenance Power Control

[0265] During the sleep phase of the SU, the interference noise power of the CDMA RF channel may change. The present invention includes a maintenance power control feature (MPC) which periodically adjusts the SU's initial transmit power with respect to the interference noise power of the CDMA channel. The MPC is the process whereby the transmit power level of an SU is maintained within close proximity of the minimum level for the RCS to detect the SU's signal. The MPC process compensates for low frequency changes in the required SU transmit power.

[0266] The maintenance control feature uses two global channels: one is called the status channel (STCH) on reverse link, and the other is called the check-up channel (CUCH) on forward link. The signals transmitted on these channels carry no data and they are generated the same way the short codes used in initial power ramp-up are generated. The STCH and CUCH codes are generated from a "reserved" branch of the global code generator.

[0267] The MPC process is as follows. At random intervals, the SU sends a symbol length spreading code periodically for 3 ms on the status channel (STCH). If the RCS detects the sequence, it replies by sending a symbol length code sequence within the next 3 ms on the check-up channel (CUCH). When the SU detects the response from the RCS, it reduces its . transmit power by a particular step size. If the SU does not see any response from the RCS within that 3 ms period, it increases its transmit power by the step size. Using this method, the RCS response is transmitted at a power level that is enough to maintain a 0.99 detection probability at all SU's.

[0268] The rate of change of traffic load and the number of active users is related to the total interference noise power of the CDMA channel. The update rate and step size of the maintenance power update signal for the present invention is determined by using queuing theory methods well known in the art of communication theory. By modeling the call origination process as an exponential random variable with mean 6.0 mins, numerical computation shows the maintenance power level of a SU should be updated once every 10 seconds or less to be able to follow the changes in interference level using 0.5 dB step size. Modeling the call origination process as a Poisson random variable with exponential interarrival times, arrival rate of $2x10^{-4}$ per second per user, service rate of 1/360 per second, and the total subscriber population is 600 in the RCS service area also yields by numerical computation that an update rate of once every 10 seconds is sufficient when 0.5 dB step size is used.

[0269] Maintenance power adjustment is performed periodically by the SU which changes from sleep phase to awake phase and performs the MPC process. Consequently, the process for the MPC feature is shown in Figure 26 and is as follows: First, at step 2601, signals are exchanged between the SU and the RCS maintaining a transmit power level that is close to the required level for detection: the SU periodically sends a symbol length spreading code in the STCH, and the RCS periodically sends a symbol length spreading code in the CUCH as response.

[0270] Next, at step 2602, if the SU receives a response within 3 ms after the STCH message it sent, it decreases its transmit power by a particular step size at step 2603; but if the SU does not receive a response within 3 ms after the STCH message, it increases its transmit power by the same step size at step 2604.

[0271] The SU waits, at step 2605, for a period of time before sending another STCH message, this time period is determined by a random process which averages 10 seconds.

[0272] Thus, the transmit power of the STCH messages from the SU is adjusted based on the RCS response periodically, and the transmit power of the CUCH messages from the RCS is fixed.

Mapping of Power Control Signal to Logical Channels For APC

[0273] Power control signals are mapped to specified Logical Channels for controlling transmit power levels of forward and reverse assigned channels. Reverse global channels are also controlled by the APC algorithm to maintain sufficient signal power to interference noise power ratio (SIR) on those reverse channels, and to stabilize and minimize system output power. The present invention uses a closed loop power control method in which a receiver periodically decides to incrementally raise or lower the output power of the transmitter at the other end. The method also conveys that decision back to the respective transmitter.

Table 13:

APC Signal Channel Assignments			
Link Channels and Signals	Call/Connection Status	Power Control Method	
		Initial Value	Continuous
Reverse link AXCH AXPT	Being Established	as determined by power ramping	APC bits in forward APC channel
Reverse link APC, OW, TRCH, pilot signal	In-Progress	level established during call set-up	APC bits in forward APC channel
Forward link APC, OW, TRCH	In-Progress	fixed value	APC bits in reverse APC channel

[0274] Forward and reverse links are independently controlled. For a call/connection in process, forward link (TRCHs APC, and OW) power is controlled by the APC bits transmitted on the reverse APC channel. During the call/connection establishment process, reverse link (AXCH) power is also controlled by the APC bits transmitted on the forward APC channel. Table 13 summarizes the specific power control methods for the controlled channels.

[0275] The required SIRs of the assigned channels TRCH, APC and OW and reverse assigned pilot signal for any particular SU are fixed in proportion to each other and these channels are subject to nearly identical fading, therfore, they are power controlled together.

Adaptive Forward Power Control

[0276] The AFPC process attempts to maintain the minimum required SIR on the forward channels during a call/connection. The AFPC recursive process, shown in Figure 27, consists of the steps of having an SU form the two error signals e_1 and e_2 in step 2701 where

$$e_1 = P_d - (1 + SNR_{REQ}) P_N \quad (47)$$

$$e_2 = P_r - P_o \quad (48)$$

and P_d is the despread signal plus noise power, P_N is the despread noise power, SNR_{REQ} is the required signal to noise ratio for the service type, P, is a measure of the total received power, and P_o is the AGC set point. Next, the SU modem forms the combined error signal $\alpha_1 e_1 + \alpha_2 e_2$ in step 2702. Here, the weights α_1 and α_2 are chosen for each service type and APC update rate. In step 2703, the SU hard limits the combined error signal and forms a single APC bit. The SU transmits the APC bit to the RCS in step 2704 and RCS modem receives the bit in step 2705. The RCS increases or decreases its transmit power to the SU in step 2706 and the algorithm repeats starting from step 2701.

Adaptive Reverse Power Control

[0277] The ARPC process maintains the minimum desired SIR on the reverse channels to minimize the total system reverse output power, during both call/connection establishment and while the call/connection is in progress. The recursive ARPC process, shown in Figure 28, begins at step 2801 where the RCS modem forms the two error signals e_1 and e_2 in step 2801 where

$$e_1 = P_d - (1 + SNR_{REQ})P_N \quad (49)$$

$$e_2 = P_{rt} - P_o \quad (50)$$

and P_d is the despread signal plus noise power, P_N is the despread noise power, SNR_{REQ} is the desired signal to noise ratio for the service type, P_{rt} is a measure of the average total power received by the RCS, and P_o is the AGC set point. The RCS modem forms the combined error signal $\alpha_1 e_1 + \alpha_2 e_2$ in step 2802 and hard limits this error signal to determine a single APC bit in step 2803. The RCS transmits the APC bit to the SU in step 2804, and the bit is received by the SU in step 2805. Finally, the SU adjusts its transmit power according to the received APC bit in step 2806, and the algorithm repeats starting from step 2801.

Table 14

Symbols/Thresholds Used for APC Computation		
Service or Call Type	Call/Connection Status	Symbol (and Threshold) Used for APC Decision
Don't care	Being Established	AXCH
ISDN D SU	In-Progress	one 1/64-kb/s symbol from TRCH (ISDN-D)
ISDN 1B+D SU	In-Progress	TRCH (ISDN-B)
ISDN 2B+D SU	In-Progress	TRCH (one ISDN-B)
POTS SU (64 KBPS PCM)	In-Progress	one 1/64-KBPS symbol from TRCH, use 64 KBPS PCM threshold
POTS SU (32 KBPS ADPCM)	In-Progress	one 1/64-KBPS symbol from TRCH, use 32 KBPS ADPCM threshold
Silent Maintenance Call (any SU)	In-Progress	OW (continuous during a maintenance call)

SIR and Multiple Channel Types

[0278] The required SIR for channels on a link is a function of channel format (e.g. TRCH, OW), service type (e.g. ISDN B, 32 KBPS ADPCM POTS), and the number of symbols over which data bits are distributed (e.g. two 64 kb/s symbols are integrated to form a single 32 kb/s ADPCM POTS symbol). Despreader output power corresponding to the required SIR for each channel and service type is predetermined. While a call/connection is in progress, several user CDMA logical channels are concurrently active; each of these channels transfers a symbol every symbol period. The SIR of the symbol from the nominally highest SIR channel is measured, compared to a threshold and used to determine the APC step up/down decision each symbol period. Table 14 indicates the symbol (and threshold) used for the APC computation by service and call type.

APC Parameters

[0279] APC information is always conveyed as a single bit of information, and the APC Data Rate is equivalent to the APC Update Rate. The APC update rate is 64 kb/s. This rate is high enough to accommodate expected Rayleigh and Doppler fades, and allow for a relatively high (~0.2) Bit Error Rate (BER) in the Uplink and Downlink APC channels, which minimizes capacity devoted to the APC.

[0280] The power step up/down indicated by an APC bit is nominally between 0.1 and 0.01 dB. The dynamic range for power control is 70 dB on the reverse link and 12 dB on the forward link for the exemplary embodiment of the present system.

An Alternative Embodiment of Multiplexing of APC information

[0281] The dedicated APC and OW logical channels described previously can also be multiplexed together in one logical channel. The APC information is transmitted at 64 kb/s. continuously whereas the OW information occurs in data bursts. The alternative multiplexed logical channel includes the unencoded, non-interleaved 64 kb/s. APC information on, for example, the In-phase channel and the OW information on the Quadrature channel of the QPSK signal.

Closed Loop Power Control Implementation

[0282] The closed loop power control during a call connection responds to two different variations in overall system power. First, the system responds to local behavior such as changes in power level of an SU, and second, the system responds to changes in the power level of the entire group of active users in the system.

[0283] The Power Control system of the exemplary embodiment of the present invention is shown in Figure 29. As shown, the circuitry used to adjust the transmitted power is similar for the RCS (shown as the RCS power control module 2901) and SU (shown as the SU power control module 2902). Beginning with the RCS power control module 2901, the reverse link RF channel signal is received at the RF antenna and demodulated to produce the reverse CDMA signal RMCH. The signal RMCH is applied to the variable gain amplifier (VGA1) 2910 which produces an input signal to the Automatic Gain Control (AGC) Circuit 2911. The AGC 2911 produces a variable gain amplifier control signal into the VGA1 2910. This signal maintains the level of the output signal of VGA1 2910 at a near constant value. The output signal of VGA1 is despread by the despread-demultiplexer (demux) 2912, which produces a despread user message signal MS and a forward APC bit. The forward APC bit is applied to the integrator 2913 to produce the Forward APC control signal. The Forward APC control signal controls the Forward Link VGA2 2914 and maintains the Forward Link RF channel signal at a minimum desired level for communication.

[0284] The signal power of the despread user message signal MS of the RCS power module 2901 is measured by the power measurement circuit 2915 to produce a signal power indication. The output of the VGA1 is also despread by the AUX despreader which despreads the signal by using an uncorrelated spreading code, and hence obtains a despread noise signal. The power measurement of this signal is multiplied by 1 plus the desired signal to noise ratio (SNR_R) to form the threshold signal S1. The difference between the despread signal power and the threshold value S1 is produced by the subtracter 2916. This difference is the error signal ES1, which is an error signal relating to the particular SU transmit power level. Similarly, the control signal for the VGA1 2910 is applied to the rate scaling circuit 2917 to reduce the rate of the control signal for VGA1 2910. The output signal of scaling circuit 2917 is a scaled system power level signal SP1. The Threshold Compute logic 2918 calculates the System Signal Threshold value SST from the RCS user channel power data signal RCSUSR. The complement of the Scaled system power level signal, SP1, and the System Signal Power Threshold value SST are applied to the adder 2919 which produces second error signal ES2. This error signal is related to the system transmit power level of all active SUs. The input Error signals ES1 and ES2 are combined in the combiner 2920 produce a combined error signal input to the delta modulator (DM1) 2921, and the output signal of the DM1 is the reverse APC bit stream signal, having bits of value +1 or -1, which for the

present invention is transmitted as a 64kb/sec signal.

[0285] The Reverse APC bit is applied to the spreading circuit 2922, and the output signal of the spreading circuit 2922 is the spread-spectrum forward APC message signal. Forward OW and Traffic signals are also provided to spreading circuits 2923, 2924, producing forward traffic message signals 1, 2, .. N. The power level of the forward APC signal, the forward OW, and traffic message signals are adjusted by the respective amplifiers 2925, 2926 and 2927 to produce the power level adjusted forward APC, OW, and TRCH channels signals. These signals are combined by the adder 2928 and applied to the VAG2 2914, which produces forward link RF channel signal.

[0286] The forward link RF channel signal including the spread forward APC signal is received by the RF antenna of the SU, and demodulated to produce the forward CDMA signal FMCH. This signal is provided to the variable gain amplifier (VGA3) 2940. The output signal of VGA3 is applied to the Automatic Gain Control Circuit (AGC) 2941 which produces a variable gain amplifier control signal to VGA3 2940. This signal maintains the level of the output signal of VGA3 at a near constant level. The output signal of VAG3 2940 is despread by the despread demux 2942, which produces a despread user message signal SUMS and a reverse APC bit. The reverse APC bit is applied to the integrator 2943 which produces the Reverse APC control signal. This reverse APC control signal is provided to the Reverse APC VGA4 2944 to maintain the Reverse link RF channel signal at a minimum power level.

[0287] The despread user message signal SUMS is also applied to the power measurement circuit 2945 producing a power measurement signal, which is added to the complement of threshold value S2 in the adder 2946 to produce error signal ES3. The signal ES3 is an error signal relating to the RCS transmit power level for the particular SU. To obtain threshold S2, the despread noise power indication from the AUX despreader is multiplied by 1 plus the desired signal to noise ratio SNR_R. The AUX despreader despreads the input data using an uncorrelated spreading code, hence its output is an indication of the despread noise power.

[0288] Similarly, the control signal for the VGA3 is applied to the rate scaling circuit to reduce the rate of the control signal for VGA3 in order to produce a scaled received power level RP1 (see Fig. 29). The threshold compute circuit computes the received signal threshold RST from the SU measured power signal SUUSR. The complement of the scaled received power level RP1 and the received signal threshold RST are applied to the adder which produces error signal ES4. This error is related to the RCS transmit power to all other SUs. The input error signals ES3 and ES4 are combined in the combiner and input to the delta modulator DM2 2947. The output signal of DM2 2947 is the forward APC bit stream signal, with bits having value of value +1 or -1. In the exemplary embodiment of the present invention, this signal is transmitted as a 64kb/sec signal.

[0289] The Forward APC bit stream signal is applied to the spreading circuit 2948, to produce the output reverse spread-spectrum APC signal. Reverse OW and Traffic signals are also input to spreading circuits 2949, 2950, producing reverse OW and traffic message signals 1, 2, .. N, and the reverse pilot is generated by the reverse pilot generator 2951. The power level of the reverse APC message signal, reverse OW message signal, reverse pilot, and the reverse traffic message signals are adjusted by amplifiers 2952, 2953, 2954, 2955 to produce the signals which are combined by the adder 2956 and input to the reverse APC VGA4 2944. It is this VGA4 2944 which produces the reverse link RF channel signal.

[0290] During the call connection and bearer channel establishment process, the closed loop power control of the present invention is modified, and is shown in Figure 30. As shown, the circuits used to adjust the transmitted power are different for the RCS, shown as the Initial RCS power control module 3001; and for the SU, shown as the Initial SU power control module 3002. Beginning with the Initial RCS power control module 3001, the reverse link RF channel signal is received at the RF antenna and demodulated producing the reverse CDMA signal IRMCH which is received by the first variable gain amplifier (VGA1) 3003. The output signal of VGA1 is detected by the Automatic Gain Control Circuit (AGC1) 3004 which provides a variable gain amplifier control signal to VGA1 3003 to maintain the level of the output signal of VAG1 at a near constant value. The output signal of VGA1 is despread by the despread demultiplexer 3005, which produces a despread user message signal IMS. The Forward APC control signal, ISET, is set to a fixed value, and is applied to the Forward Link Variable Gain Amplifier (VGA2) 3006 to set the Forward Link RF channel signal at a predetermined level.

[0291] The signal power of the despread user message signal IMS of the Initial RCS power module 3001 is measured by the power measure circuit 3007, and the output power measurement is subtracted from a threshold value S3 in the subtracter 3008 to produce error signal ES5, which is an error signal relating to the transmit power level of a particular SU. The threshold S3 is calculated by multiplying the despread power measurement obtained from the AUX despreader by 1 plus the desired signal to noise ratio SNR_R. The AUX despreader despreads the signal using an uncorrelated spreading code, hence its output signal is an indication of despread noise power. Similarly, the VGA1 control signal is applied to the rate scaling circuit 3009 to reduce the rate of the VGA1 control signal in order to produce a scaled system power level signal SP2. The threshold computation logic 3010 determines an Initial System Signal Threshold value (ISST) computed from the user channel power data signal (IRCSUSR). The complement of the Scaled system power level signal SP2 and the ISST are provided to the adder 3011 which produces a second error signal ES6, which is an error signal relating to the system transmit power level of all active SUs. The value of ISST is the desired transmit

power for a system having the particular configuration. The input Error signals ES5 and ES6 are combined in the combiner 3012 produce a combined error signal input to the delta modulator (DM3) 3013. DM3 produces the initial reverse APC bit stream signal, having bits of value +1 or -1, which in the exemplary embodiment is transmitted as a 64 kb/s signal.

[0292] The Reverse APC bit stream signal is applied to the spreading circuit 3014, to produce the initial spread-spectrum forward APC signal. The CTCH information is spread by the spreader 3016 to form the spread CTCH message signal. The spread APC and CTCH signals are scaled by the amplifiers 3015 and 3017, and combined by the combiner 3018. The combined signal is applied to VAG2 3006, which produces the forward link RF channel signal.

[0293] The forward link RF channel signal including the spread forward APC signal is received by the RF antenna of the SU and demodulated to produce the initial forward CDMA signal (EFMCH) which is applied to the variable gain amplifier (VGA3) 3020. The output signal of VGA3 is detected by the Automatic Gain Control Circuit (AGC2) 3021 which produces a variable gain amplifier control signal for the VGA3 3020. This signal maintains the output power level of the VGA3 3020 at a near constant value. The output signal of VAG3 is despread by the despread demultiplexer 3022, which produces an initial reverse APC bit that is dependent on the output level of VGA3. The reverse APC bit is processed by the integrator 3023 to produce the Reverse APC control signal. The Reverse APC control signal is provided to the Reverse APC VGA4 3024 to maintain Reverse link RF channel signal at a defined power level.

[0294] The global channel AXCH signal is spread by the spreading circuits 3025 to provide the spread AXCH channel signal. The reverse pilot generator 3026 provides a reverse pilot signal, and the signal power of AXCH and the reverse pilot signal are adjusted by the respective amplifiers 3027 and 3028. The spread AXCH channel signal and the reverse pilot signal are summed by the adder 3029 to produce reverse link CDMA signal. The reverse link CDMA signal is received by the reverse APC VGA4 3024, which produces the reverse link RF channel signal output to the RF transmitter.

System Capacity Management

[0295] The system capacity management algorithm of the present invention optimizes the maximum user capacity for an RCS area, called a cell. When the SU comes within a certain value of maximum transmit power, the SU sends an alarm message to the RCS. The RCS sets the traffic lights which control access to the system, to "red" which, as previously described, is a flag that inhibits access by the SUs. This condition remains in effect until the call to the alarming SU terminates, or until the transmit power of the alarming SUs, measured at the SU, is a value less than the maximum transmit power. When multiple SUs send alarm messages, the condition remains in effect until either all calls from alarming SU terminate, or until the transmit power of the alarming SU, measured at the SU, is less than the maximum transmit power. An alternative embodiment monitors the bit error rate measurements from the FEC decoder, and holds the RCS traffic lights at "red" until the bit error rate is less than a predetermined value.

[0296] The blocking strategy of the present invention includes a method which uses the power control information transmitted from the RGS to an SU, and the received power measurements at the RCS. The RCS measures its transmit power level, detects that a maximum value is reached, and determines when to block new users. An SU preparing to enter the system blocks itself if the SU reaches the maximum transmit power before successful completion of a bearer channel assignment.

[0297] Each additional user in the system has the effect of increasing the noise level for all other users, which decreases the signal to noise ratio (SNR) that each user experiences. The power control algorithm maintains a desired SNR for each user. Therefore, in the absence of any other limitations, addition of a new user into the system has only a transient effect and the desired SNR is regained.

[0298] The transmit power measurement at the RCS is done by measuring either the root mean square (rms) value of the baseband combined signal or by measuring the transmit power of the RF signal and feeding it back to digital control circuits. The transmit power measurement may also be made by the SUs to determine if the unit has reached its maximum transmit power. The SU transmit power level is determined by measuring the control signal of the RF amplifier, and scaling the value based on the service type, such as POTS, FAX, or ISDN.

[0299] The information that an SU has reached the maximum power is transmitted to the RCS by the SU in a message on the Assigned Channels. The RCS also determines the condition by measuring reverse APC changes because, if the RCS sends APC messages to the SU to increase SU transmit power and the SU transmit power, measured at the RCS is not increased, the SU has reached the maximum transmit power.

[0300] The RCS does not use traffic lights to block new users who have finished ramping-up using the short codes. These users are blocked by denying them the dial tone and letting them time out. The RCS sends all 1's (go down commands) on the APC Channel to make the SU lower its transmit power. The RCS also sends either no CTCH message or a message with an invalid address which would force the FSU to abandon the access procedure and start over. The SU, however, does not start the acquisition process immediately because the traffic lights are red.

[0301] When the RCS reaches its transmit power limit, it enforces blocking in the same manner as when an SU

reaches its transmit power limit. The RCS turns off all the traffic lights on the FBCH, starts sending all 1 APC bits (go down commands) to those users who have completed their short code ramp-up but have not yet been given a dial tone, and either sends no CTCH message to these users or sends messages with invalid addresses to force them to abandon the access process.

[0302] The self blocking process of the SU is as follows. When the SU starts transmitting the AXCH, the APC starts its power control operation using the AXCH and the SU transmit power increases. While the transmit power is increasing under the control of the APC, it is monitored by the SU controller. If the transmit power limit is reached, the SU abandons the access procedure and starts over.

System Synchronization

[0303] The RCS is synchronized either to the PSTN Network Clock signal through one of the Line interfaces, as shown in Figure 10, or to the RCS system clock oscillator, which free-runs to provide a master timing signal for the system. The Global Pilot Channel, and therefore all Logical channels within the CDMA channel, are synchronized to the system clock signal of the RCS. The Global Pilot (GLPT) is transmitted by the RCS and defines the timing at the RCS transmitter.

[0304] The SU receiver is synchronized to the GLPT, and so behaves as a slave to the Network Clock oscillator. However, the SU timing is retarded by the propagation delay. In the present embodiment of the invention, the SU modem extracts a 64 KHz and 8 KHz clock signal from the CDMA RF Receive channel, and a PLL oscillator circuit creates 2 MHz and 4 MHz clock signals

[0305] The SU transmitter and hence the LAXPT or ASPT are slaved to the timing of the SU receiver.

[0306] The RCS receiver is synchronized to the LAXPT or the ASPT transmitted by the SU, however, its timing may be retarded by the propagation delay. Hence, the timing of the RCS receiver is that of the RCS transmitter retarded by twice the propagation delay.

[0307] Furthermore, the system can be synchronized via a reference received from a Global Positioning System receiver (GPS). In a system of this type, a GPS receiver in each RCS provides a reference clock signal to all submodules of the RCS. Because each RCS receives the same time reference from the GPS, all of the system clock signals in all of the RCSs are synchronized.

[0308] Although the invention has been described in terms of multiple exemplary embodiments, it is understood by those skilled in the art that the invention may be practiced with modifications to the embodiments that are within the scope of the invention as defined by the following claims.

0	67	134	201	268	335	402	469	536	603	670	737
1	68	135	202	269	336	403	470	537	604	671	738
2	69	136	203	270	337	404	471	538	605	672	739
3	70	137	204	271	338	405	472	539	606	673	740
4	71	138	205	272	339	406	473	540	607	674	741
5	72	139	206	273	340	407	474	541	608	675	742
6	73	140	207	274	341	408	475	542	609	676	743
7	74	141	208	275	342	409	476	543	610	677	744
8	75	142	209	276	343	410	477	544	611	678	745
9	76	143	210	277	344	411	478	545	612	679	746
10	77	144	211	278	345	412	479	546	613	680	747
11	78	145	212	279	346	413	480	547	614	681	748
12	79	146	213	280	347	414	481	548	615	682	749
13	80	147	214	281	348	415	482	549	616	683	750
14	81	148	215	282	349	416	483	550	617	684	751
15	82	149	216	283	350	417	484	551	618	685	752
16	83	150	217	284	351	418	485	552	619	686	753
17	84	151	218	285	352	419	486	553	620	687	754
18	85	152	219	286	353	420	487	554	621	688	755
19	86	153	220	287	354	421	488	555	622	689	756
20	87	154	221	288	355	422	489	556	623	690	757
21	88	155	222	289	356	423	490	557	624	691	758
22	89	156	223	290	357	424	491	558	625	692	759

(continued)

23	90	157	224	291	358	425	492	559	626	693	760
24	91	158	225	292	359	426	493	560	627	694	761
25	92	159	226	293	360	427	494	561	628	695	762
26	93	160	227	294	361	428	495	562	629	696	763
27	94	161	228	295	362	429	496	563	630	697	764
28	95	162	229	296	363	430	497	564	631	698	765
29	96	163	230	297	364	431	498	565	632	699	766
30	97	164	231	298	365	432	499	566	633	700	767
31	98	165	232	299	366	433	500	567	634	701	768
32	99	166	233	300	367	434	501	568	635	702	769
33	100	167	234	301	368	435	502	569	636	703	770
34	101	168	235	302	369	436	503	570	637	704	771
35	102	169	236	303	370	437	504	571	638	705	772
36	103	170	237	304	371	438	505	572	639	706	m
37	104	171	238	305	372	439	506	573	640	707	774
38	105	172	239	306	373	440	507	574	641	708	775
39	106	173	240	307	374	441	508	575	642	709	776
40	107	174	241	308	375	442	509	576	643	710	777
41	108	175	242	309	376	443	510	577	644	711	778
42	109	176	243	310	377	444	511	578	645	712	779
43	110	177	244	311	378	445	512	579	646	713	780
44	111	178	245	312	379	446	513	580	647	714	781
45	112	179	246	313	380	447	514	581	648	715	782
46	113	180	247	314	381	448	515	582	649	716	783
47	114	181	248	315	382	449	516	583	650	717	784
48	115	182	249	316	383	450	517	584	651	718	785
49	116	183	250	317	384	451	518	585	652	719	786
50	117	184	251	318	385	452	519	586	653	720	787
51	118	185	252	319	386	453	520	587	654	721	788
52	119	186	253	320	387	454	521	588	655	722	789
53	120	187	254	321	388	455	522	589	656	723	790
54	121	188	255	322	389	456	523	590	657	724	791
55	122	189	256	323	390	457	524	591	658	725	792
56	123	190	257	324	391	458	525	592	659	726	793
57	124	191	258	325	392	459	526	593	660	727	794
58	125	192	259	326	393	460	527	594	661	728	795
59	126	193	260	327	394	461	528	595	662	729	796
60	127	194	261	328	395	462	529	596	663	730	797
61	128	195	262	329	396	463	530	597	664	731	798
62	129	196	263	330	397	464	531	598	665	732	799
63	130	197	264	331	398	465	532	599	666	733	800
64	131	198	265	332	399	466	533	600	667	734	801
65	132	199	266	333	400	467	534	601	668	735	802
66	133	200	267	334	401	468	535	602	669	736	803
804	871	938	1005	1072	2241	2308	2375	2442	2509	2576	2643
805	872	939	1006	1073	2242	2309	2376	2443	2510	2577	2644
806	873	940	1007	1074	2243	2310	2377	2444	2511	2578	2645
807	874	941	1008	1075	2244	2311	2378	2445	2512	2579	2646
808	875	942	1009	1076	2245	2312	2379	2446	2513	2580	2647
809	876	943	1010	1077	2246	2313	2380	2447	2514	2581	2648
810	877	944	1011	1078	2247	2314	2381	2448	2515	2582	2649

(continued)

811	878	945	1012	1079	2248	2315	2382	2449	2516	2583	2650
812	879	946	1013	1080	2249	2316	2383	2450	2517	2584	2651
813	880	947	1014	1081	2250	2317	2384	2451	2518	2585	2652
814	881	948	1015	1082	2251	2318	2385	2452	2519	2586	2653
815	882	949	1016	1083	2252	2319	2386	2453	2520	2587	2654
816	883	950	1017	1084	2253	2320	2387	2454	2521	2588	2655
817	884	951	1018	1085	2254	2321	2388	2455	2522	2589	2656
818	885	952	1019	1086	2255	2322	2389	2456	2523	2590	2657
819	886	953	1020	1087	2256	2323	2390	2457	2524	2591	2658
820	887	954	1021	1088	2257	2324	2391	2458	2525	2592	2659
821	888	955	1022	1089	2258	2325	2392	2459	2526	2593	2660
822	889	956	1023	1090	2259	2326	2393	2460	2527	2594	2661
823	890	957	1024	1091	2260	2327	2394	2461	2528	2595	2662
824	891	958	1025	1092	2261	2328	2395	2462	2529	2596	2663
825	892	959	1026	1093	2262	2329	2396	2463	2530	2597	2664
826	893	960	1027	1094	2263	2330	2397	2464	2531	2598	2665
827	894	961	1028	1095	2264	2331	2398	2465	2532	2599	2666
828	895	962	1029	1096	2265	2332	2399	2466	2533	2600	2667
829	896	963	1030	1097	2266	2333	2400	2467	2534	2601	2668
830	897	964	1031	1098	2267	2334	2401	2468	2535	2602	2669
831	898	965	1032	1099	2268	2335	2402	2469	2536	2603	2670
832	899	966	1033	1100	2269	2336	2403	2470	2537	2604	2671
833	900	967	1034	1101	2270	2337	2404	2471	2538	2605	2672
834	901	968	1035	2204	2271	2338	2405	2472	2539	2606	2673
835	902	969	1036	2205	2272	2339	2406	2473	2540	2607	2674
836	903	970	1037	2206	2273	2340	2407	2474	2541	2608	2675
837	904	971	1038	2207	2274	2341	2408	2475	2542	2609	2676
838	905	972	1039	2208	2275	2342	2409	2476	2543	2610	2677
839	906	973	1040	2209	2276	2343	2410	2477	2544	2611	2678
840	907	974	1041	2210	2277	2344	2411	2478	2545	2612	2679
841	908	975	1042	2211	2278	2345	2412	2479	2546	2613	2680
842	909	976	1043	2212	2279	2346	2413	2480	2547	2614	2681
843	910	977	1044	2213	2280	2347	2414	2481	2548	2615	2682
844	911	978	1045	2214	2281	2348	2415	2482	2549	2616	2683
845	912	979	1046	2215	2282	2349	2416	2483	2550	2617	2684
846	913	980	1047	2216	2283	2350	2417	2484	2551	2618	2685
847	914	981	1048	2217	2284	2351	2418	2485	2552	2619	2686
848	915	982	1049	2218	2285	2352	2419	2486	2553	2620	2687
849	916	983	1050	2219	2286	2353	2420	2487	2554	2621	2688
850	917	984	1051	2220	2287	2354	2421	2488	2555	2622	2689
851	918	985	1052	2221	2288	2355	2422	2489	2556	2623	2690
852	919	986	1053	2222	2289	2356	2423	2490	2557	2624	2691
853	920	987	1054	2223	2290	2357	2424	2491	2558	2625	2692
854	921	988	1055	2224	2291	2358	2425	2492	2559	2626	2693
855	922	989	1056	2225	2292	2359	2426	2493	2560	2627	2694
856	923	990	1057	2226	2293	2360	2427	2494	2561	2628	2695
857	924	991	1058	2227	2294	2361	2428	2495	2562	2629	2696
858	925	992	1059	2228	2295	2362	2429	2496	2563	2630	2697
859	926	993	1060	2229	2296	2363	2430	2497	2564	2631	2698
860	927	994	1061	2230	2297	2364	2431	2498	2565	2632	2699
861	928	995	1062	2231	2298	2365	2432	2499	2566	2633	2700

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862	929	996	1063	2232	2299	2366	2433	2500	2567	2634	2701
863	930	997	1064	2233	2300	2367	2434	2501	2568	2635	2702
864	931	998	1065	2234	2301	2368	2435	2502	2569	2636	2703
865	932	999	1066	2235	2302	2369	2436	2503	2570	2637	2704
866	933	1000	1067	2236	2303	2370	2437	2504	2571	2638	2705
867	934	1001	1068	2237	2304	2371	2438	2505	2572	2639	2706
868	935	1002	1069	2238	2305	2372	2439	2506	2573	2640	2707
869	936	1003	1070	2239	2306	2373	2440	2507	2574	2641	2708
870	937	1004	1071	2240	2307	2374	2441	2508	2575	2642	2709
2710	2777	2844	2911	2978	3045	3112	3179	3246	4415	4482	4549
2711	2778	2845	2912	2979	3046	3113	3180	3247	4416	4483	4550
2712	2779	2846	2913	2980	3047	3114	3181	3248	4417	4484	4551
2713	2780	2847	2914	2981	3048	3115	3182	3249	4418	4485	4552
2714	2781	2848	2915	2982	3049	3116	3183	3250	4419	4486	4553
2715	2782	2849	2916	2983	3050	3117	3184	3251	4420	4487	4554
2716	2783	2850	2917	2984	3051	3118	3185	3252	4421	4488	4555
2717	2784	2851	2918	2985	3052	3119	3186	3253	4422	4489	4556
2718	2785	2852	2919	2986	3053	3120	3187	3254	4423	4490	4557
2719	2786	2853	2920	2987	3054	3121	3188	3255	4424	4491	4558
2720	2787	2854	2921	2988	3055	3122	3189	3256	4425	4492	4559
2721	2788	2855	2922	2989	3056	3123	3190	3257	4426	4493	4560
2722	2789	2856	2923	2990	3057	3124	3191	3258	4427	4494	4561
2723	2790	2857	2924	2991	3058	3125	3192	3259	4428	4495	4562
2724	2791	2858	2925	2992	3059	3126	3193	3260	4429	4496	4563
2725	2792	2859	2926	2993	3060	3127	3194	3261	4430	4497	4564
2726	2793	2860	2927	2994	3061	3128	3195	3262	4431	4498	4565
2727	2794	2861	2928	2995	3062	3129	3196	3263	4432	4499	4566
2728	2795	2862	2929	2996	3063	3130	3197	3264	4433	4500	4567
2729	2796	2863	2930	2997	3064	3131	3198	3265	4434	4501	4568
2730	2797	2864	2931	2998	3065	3132	3199	3266	4435	4502	4569
2731	2798	2865	2932	2999	3066	3133	3200	3267	4436	4503	4570
2732	2799	2866	2933	3000	3067	3134	3201	3268	4437	4504	4571
2733	2800	2867	2934	3001	3068	3135	3202	3269	4438	4505	4572
2734	2801	2868	2935	3002	3069	3136	3203	3270	4439	4506	4573
2735	2802	2869	2936	3003	3070	3137	3204	3271	4440	4507	4574
2736	2803	2870	2937	3004	3071	3138	3205	3272	4441	4508	4575
2737	2804	2871	2938	3005	3072	3139	3206	3273	4442	4509	4576
2738	2805	2872	2939	3006	3073	3140	3207	3274	4443	4510	4577
2739	2806	2873	2940	3007	3074	3141	3208	3275	4444	4511	4578
2740	2807	2874	2941	3008	3075	3142	3209	3276	4445	4512	4579
2741	2808	2875	2942	3009	3076	3143	3210	3277	4446	4513	4580
2742	2809	2876	2943	3010	3077	3144	3211	3278	4447	4514	4581
2743	2810	2877	2944	3011	3078	3145	3212	3279	4448	4515	4582
2744	2811	2878	2945	3012	3079	3146	3213	3280	4449	4516	4583
2745	2812	2879	2946	3013	3080	3147	3214	3281	4450	4517	4584
2746	2813	2880	2947	3014	3081	3148	3215	3282	4451	4518	4585
2747	2814	2881	2948	3015	3082	3149	3216	3283	4452	4519	4586
2748	2815	2882	2949	3016	3083	3150	3217	3284	4453	4520	4587
2749	2816	2883	2950	3017	3084	3151	3218	3285	4454	4521	4588
2750	2817	2884	2951	3018	3085	3152	3219	3286	4455	4522	4589
2751	2818	2885	2952	3019	3086	3153	3220	3287	4456	4523	4590

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2752	2819	2886	2953	3020	3087	3154	3221	3288	4457	4524	4591
2753	2820	2887	2954	3021	3088	3155	3222	3289	4458	4525	4592
2754	2821	2888	2955	3022	3089	3156	3223	3290	4459	4526	4593
2755	2822	2889	2956	3023	3090	3157	3224	3291	4460	4527	4594
2756	2823	2890	2957	3024	3091	3158	3225	3292	4461	4528	4595
2757	2824	2891	2958	3025	3092	3159	3226	3293	4462	4529	4596
2758	2825	2892	2959	3026	3093	3160	3227	3294	4463	4530	4597
2759	2826	2893	2960	3027	3094	3161	3228	3295	4464	4531	4598
2760	2827	2894	2961	3028	3095	3162	3229	3296	4465	4532	4599
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2764	2831	2898	2965	3032	3099	3166	3233	3300	4469	4536	4603
2765	2832	2899	2966	3033	3100	3167	3234	3301	4470	4537	4604
2766	2833	2900	2967	3034	3101	3168	3235	3302	4471	4538	4605
2767	2834	2901	2968	3035	3102	3169	3236	3303	4472	4539	4606
2768	2835	2902	2969	3036	3103	3170	3237	3304	4473	4540	4607
2769	2836	2903	2970	3037	3104	3171	3238	3305	4474	4541	4608
2770	2837	2904	2971	3038	3105	3172	3239	4408	4475	4542	4609
2771	2838	2905	2972	3039	3106	3173	3240	4409	4476	4543	4610
2772	2839	2906	2973	3040	3107	3174	3241	4410	4477	4544	4611
2773	2840	2907	2974	3041	3108	3175	3242	4411	4478	4545	4612
2774	2841	2908	2975	3042	3109	3176	3243	4412	4479	4546	4613
2775	2842	2909	2976	3043	3110	3177	3244	4413	4480	4547	4614
2776	2843	2910	2977	3044	3111	3178	3245	4414	4481	4548	4615
4616	4683	4750	4817	4884	4951	5018	5085	5152	5219	5286	5353
4617	4684	4751	4818	4885	4952	5019	5086	5153	5220	5287	5354
4618	4685	4752	4819	4886	4953	5020	5087	5154	5221	5288	5355
4619	4686	4753	4820	4887	4954	5021	5088	5155	5222	5289	5356
4620	4687	4754	4821	4888	4955	5022	5089	5156	5223	5290	5357
4621	4688	4755	4822	4889	4956	5023	5090	5157	5224	5291	5358
4622	4689	4756	4823	4890	4957	5024	5091	5158	5225	5292	5359
4623	4690	4757	4824	4891	4958	5025	5092	5159	5226	5293	5360
4624	4691	4758	4825	4892	4959	5026	5093	5160	5227	5294	5361
4625	4692	4759	4826	4893	4960	5027	5094	5161	5228	5295	5362
4626	4693	4760	4827	4894	4961	5028	5095	5162	5229	5296	5363
4627	4694	4761	4828	4895	4962	5029	5096	5163	5230	5297	5364
4628	4695	4762	4829	4896	4963	5030	5097	5164	5231	5298	5365
4629	4696	4763	4830	4897	4964	5031	5098	5165	5232	5299	5366
4630	4697	4764	4831	4898	4965	5032	5099	5166	5233	5300	5367
4631	4698	4765	4832	4899	4966	5033	5100	5167	5234	5301	5368
4632	4699	4766	4833	4900	4967	5034	5101	5168	5235	5302	5369
4633	4700	4767	4834	4901	4968	5035	5102	5169	5236	5303	5370
4634	4701	4768	4835	4902	4969	5036	5103	5170	5237	5304	5371
4635	4702	4769	4836	4903	4970	5037	5104	5171	5238	5305	5372
4636	4703	4770	4837	4904	4971	5038	5105	5172	5239	5306	5373
4637	4704	4771	4838	4905	4972	5039	5106	5173	5240	5307	5374
4638	4705	4772	4839	4906	4973	5040	5107	5174	5241	5308	5375
4639	4706	4773	4840	4907	4974	5041	5108	5175	5242	5309	5376
4640	4707	4774	4841	4908	4975	5042	5109	5176	5243	5310	5377
4641	4708	4775	4842	4909	4976	5043	5110	5177	5244	5311	5378

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4642	4709	4776	4843	4910	4977	5044	5111	5178	5245	5312	5379
4643	4710	4777	4844	4911	4978	5045	5112	5179	5246	5313	5380
4644	4711	4778	4845	4912	4979	5046	5113	5180	5247	5314	5381
4645	4712	4779	4846	4913	4980	5047	5114	5181	5248	5315	5382
4646	4713	4780	4847	4914	4981	5048	5115	5182	5249	5316	5383
4647	4714	4781	4848	4915	4982	5049	5116	5183	5250	5317	5384
4648	4715	4782	4849	4916	4983	5050	5117	5184	5251	5318	5385
4649	4716	4783	4850	4917	4984	5051	5118	5185	5252	5319	5386
4650	4717	4784	4851	4918	4985	5052	5119	5186	5253	5320	5387
4651	4718	4785	4852	4919	4986	5053	5120	5187	5254	5321	5388
4652	4719	4786	4853	4920	4987	5054	5121	5188	5255	5322	5389
4653	4720	4787	4854	4921	4988	5055	5122	5189	5256	5323	5390
4654	4721	4788	4855	4922	4989	5056	5123	5190	5257	5324	5391
4655	4722	4789	4856	4923	4990	5057	5124	5191	5258	5325	5392
4656	4723	4790	4857	4924	4991	5058	5125	5192	5259	5326	5393
4657	4724	4791	4858	4925	4992	5059	5126	5193	5260	5327	5394
4658	4725	4792	4859	4926	4993	5060	5127	5194	5261	5328	5395
4659	4726	4793	4860	4927	4994	5061	5128	5195	5262	5329	5396
4660	4727	4794	4861	4928	4995	5062	5129	5196	5263	5330	5397
4661	4728	4795	4862	4929	4996	5063	5130	5197	5264	5331	5398
4662	4729	4796	4863	4930	4997	5064	5131	5198	5265	5332	5399
4663	4730	4797	4864	4931	4998	5065	5132	5199	5266	5333	5400
4664	4731	4798	4865	4932	4999	5066	5133	5200	5267	5334	5401
4665	4732	4799	4866	4933	5000	5067	5134	5201	5268	5335	5402
4666	4733	4800	4867	4934	5001	5068	5135	5202	5269	5336	5403
4667	4734	4801	4868	4935	5002	5069	5136	5203	5270	5337	5404
4668	4735	4802	4869	4936	5003	5070	5137	5204	5271	5338	5405
4669	4736	4803	4870	4937	5004	5071	5138	5205	5272	5339	5406
4670	4737	4804	4871	4938	5005	5072	5139	5206	5273	5340	5407
4671	4738	4805	4872	4939	5006	5073	5140	5207	5274	5341	5408
4672	4739	4806	4873	4940	5007	5074	5141	5208	5275	5342	5409
4673	4740	4807	4874	4941	5008	5075	5142	5209	5276	5343	5410
4674	4741	4808	4875	4942	5009	5076	5143	5210	5277	5344	5411
4675	4742	4809	4876	4943	5010	5077	5144	5211	5278	5345	5412
4676	4743	4810	4877	4944	5011	5078	5145	5212	5279	5346	5413
4677	4744	4811	4878	4945	5012	5079	5146	5213	5280	5347	5414
4678	4745	4812	4879	4946	5013	5080	5147	5214	5281	5348	5415
4679	4746	4813	4880	4947	5014	5081	5148	5215	5282	5349	5416
4680	4747	4814	4881	4948	5015	5082	5149	5216	5283	5350	5417
4681	4748	4815	4882	4949	5016	5083	5150	5217	5284	5351	5418
4682	4749	4816	4883	4950	5017	5084	5151	5218	5285	5352	5419
5420	5487	6656	6723	6790	6857	6924	6991	7058	7125		
5421	5488	6657	6724	6791	6858	6925	6992	7059	7126		
5422	5489	6658	6725	6792	6859	6926	6993	7060	7127		
5423	5490	6659	6726	6793	6860	6927	6994	7061	7128		
5424	5491	6660	6727	6794	6861	6928	6995	7062	7129		
5425	5492	6661	6728	6795	6862	6929	6996	7063	7130		
5426	5493	6662	6729	6796	6863	6930	6997	7064	7131		
5427	5494	6663	6730	6797	6864	6931	6998	7065	7132		
5428	5495	6664	6731	6798	6865	6932	6999	7066	7133		
5429	5496	6665	6732	6799	6866	6933	7000	7067	7134		

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5430	5497	6666	6733	6800	6867	6934	7001	7068	7135		
5431	5498	6667	6734	6801	6868	6935	7002	7069	7136		
5432	5499	6668	6735	6802	6869	6936	7003	7070	7137		
5433	5500	6669	6736	6803	6870	6937	7004	7071	7138		
5434	5501	6670	6737	6804	6871	6938	7005	7072	7139		
5435	5502	6671	6738	6805	6872	6939	7006	7073	7140		
5436	5503	6672	6739	6806	6873	6940	7007	7074	7141		
5437	5504	6673	6740	6807	6874	6941	7008	7075	7142		
5438	5505	6674	6741	6808	6875	6942	7009	7076	7143		
5439	5506	6675	6742	6809	6876	6943	7010	7077	7144		
5440	5507	6676	6743	6810	6877	6944	7011	7078	7145		
5441	5508	6677	6744	6811	6878	6945	7012	7079	7146		
5442	5509	6678	6743	6812	6879	6946	7013	7080	7147		
5443	6612	6679	6746	6813	6880	6947	7014	7081	7148		
5444	6613	6680	6747	6814	6881	6948	7015	7082	7149		
5445	6614	6681	6748	6815	6882	6949	7016	7083	7150		
5446	6615	6682	6749	6816	6883	6950	7017	7084	7151		
5447	6616	6683	6750	6817	6884	6951	7018	7085	7152		
5448	6617	6684	6751	6818	6885	6952	7019	7086	7153		
5449	6618	6685	6752	6819	6886	6953	7020	7087	7154		
5450	6619	6686	6753	6820	6887	6954	7021	7088	7155		
5451	6620	6687	6754	6821	6888	6955	7022	7089	7156		
5452	6621	6688	6755	6822	6889	6956	7023	7090	7157		
5453	6622	6689	6756	6823	6890	6957	7024	7091	7158		
5454	6623	6690	6757	6824	6891	6958	7025	7092	7159		
5455	6624	6691	6758	6825	6892	6959	7026	7093	7160		
5456	6625	6692	6759	6826	6893	6960	7027	7094	7161		
5457	6626	6693	6760	6827	6894	6961	7028	7095	7162		
5458	6627	6694	6761	6828	6895	6962	7029	7096	7163		
5459	6628	6695	6762	6829	6896	6963	7030	7097	7164		
5460	6629	6696	6763	6830	6897	6964	7031	7098	7165		
5461	6630	6697	6764	6831	6898	6965	7032	7099	7166		
5462	6631	6698	6765	6832	6899	6966	7033	7100	7167		
5463	6632	6699	6766	6833	6900	6967	7034	7101	7168		
5464	6633	6700	6767	6834	6901	6968	7035	7102	7169		
5465	6634	6701	6768	6835	6902	6969	7036	7103	7170		
5466	6635	6702	6769	6836	6903	6970	7037	7104	7171		
5467	6636	6703	6770	6837	6904	6971	7038	7105	7172		
5468	6637	6704	6771	6838	6905	6972	7039	7106	7173		
5469	6638	6705	6772	6839	6906	6973	7040	7107	7174		
5470	6639	6706	6773	6840	6907	6974	7041	7108	7175		
5471	6640	6707	6774	6841	6908	6975	7042	7109	7176		
5472	6641	6708	6775	6842	6909	6976	7043	7110	7177		
5473	6642	6709	6776	6843	6910	6977	7044	7111	7178		
5474	6643	6710	6777	6844	6911	6978	7045	7112	7179		
5475	6644	6711	6778	6845	6912	6979	7046	7113	7180		
5476	6645	6712	6779	6846	6913	6980	7047	7114	7181		
5477	6646	6713	6780	6847	6914	6981	7048	7115	7182		
5478	6647	6714	6781	6848	6915	6982	7049	7116	7183		
5479	6648	6715	6782	6849	6916	6983	7050	7117	7184		
5480	6649	6716	6783	6850	6917	6984	7051	7118			

(continued)

5481	6650	6717	6784	6851	6918	6985	7052	7119			
5482	6651	6718	6785	6852	6919	6986	7053	7120			
5483	6652	6719	6786	6853	6920	6987	7054	7121			
5484	6653	6720	6787	6854	6921	6988	7055	7122			
5485	6654	6721	6788	6855	6922	6989	7056	7123			
5486	6655	6722	6789	6856	6923	6990	7057	7124			

Claims

1. A fast acquisition apparatus for quickly synchronizing a spread code phase of a spread-spectrum communication system to a transmitted code signal having a transmitted in-phase I-code signal and a transmitted quadrature Q-code signal, said transmitted I-code signal including a first spreading code sequence and said transmitted Q-code signal including a second spreading code sequence; the transmitted I-code signal and transmitted Q-code signal having a predetermined mutual code sequence phase relationship value, and including receiving means for receiving the transmitted code signal, the apparatus **characterized by**:

the receiving means (301-302) including means for separating from the received code signal the transmitted I-code signal and the transmitted Q-code signal;
a correlating means (304) for correlating code sequences with the transmitted code signal, and comprising an I-code signal correlator and a Q-code signal correlator;
a local code sequence generator (303) responsive to a code control signal value to generate a local portion of the I-code sequence having an I-code phase value and a local portion of the Q-code sequence having a Q-code phase value; and
a controller connected to the I-code signal correlator, the Q-code signal correlator, and the local code sequence generator (303), said controller for determining, obtaining, and maintaining code sequence lock wherein said I-code signal correlator correlates said local portion of the I-code sequence with said transmitted I-code signal and generates an I-high value when the I-code phase value of the local portion of the I-code sequence and a code phase value of the transmitted I-code signal have matching code phase values and wherein said Q-code signal correlator correlates said local portion of the Q-code sequence with said transmitted Q-code signal and generates a Q-high value when the Q-code phase value of the local portion of the Q-code sequence and a code phase value of the transmitted Q-code signal have matching code phase values;

wherein said controller generates the code control signal value to lock the I-code phase value of the local portion of the I-code sequence responsive to the I-high value and to set the Q-code phase value of the local portion of the Q-code sequence, and generates the code control signal value to lock the Q-code phase value of the local portion of the Q-code sequence responsive to the Q-high value and to set the I-code phase value of the local portion of the I-code sequence,

said controller is responsive to the absence of the I-high value and the Q-high value to generate the code control signal value which adjusts the I-code phase value and the Q-code phase value,

the first spreading code sequence and the second spreading code sequence are each chosen from a plurality of fast acquisition sequences of length L code chips; each of said fast acquisition sequences including a short code portion having length N code chips and a long code portion having length M code chips and having a mean search value of log 2L phases wherein said short code portion occurs repetitively,

said local portion of the I-code sequence includes an I-sequence equivalent to the short code portion of the respective fast acquisition sequence, and said local portion of the Q-code sequences includes a Q-sequence equivalent to the short code portion of the respective fast acquisition sequence,

said I-code signal correlator further includes means for generating an I-middle value when the I-code phase value of the local portion of the I-code sequence and the code phase of the transmitted I-code signal have code phase values which correspond to the I-sequence in phase with one occurrence of the respective short code sequence of the first spreading code sequence,

said Q-code signal correlator further includes means for generating a Q-middle value when the Q-code phase of the local portion of the Q-code sequence and the code phase of the transmitted Q-code signal have code phase values which correspond to the Q-sequence in phase with one occurrence of the respective short code sequence of the second spreading code sequence, and

said controller is responsive to the I-middle value and to the absence of the I-high value and the Q-high value for generating the code control signal value which adjusts the I-code phase value and the Q-code phase value to maintain the respective local short code sequence portion of the local portion of the I-code sequence in phase with each respective occurrence of the short code sequence of the first spreading code sequence; and being responsive to the Q-middle value and the absence of the I-high value and the Q-high value for generating the code control signal value for adjusting the I-code phase value and the Q-code phase value to maintain the respective Q-sequence of the local portion of the Q-code sequence in phase with each respective occurrence of the short code sequence of the second spreading code sequence.

2. The fast acquisition apparatus of claim 1, wherein the first spreading code sequence is equivalent to the second spreading code sequence, and the transmitted I-code signal and the transmitted Q code signal have the predetermined mutual code sequence phase relationship such that the respective code phases are not identical.

3. The fast acquisition apparatus of claim 1, wherein the short code portion has length N code chips where N is an even integer and long code portion has length M code chips where M is an odd integer.

4. The fast acquisition apparatus of claim 1, wherein the short code portion has length N code chips where N is an odd integer and long code portion has length M code chips where M is an even integer.

5. The fast acquisition apparatus of claim 1, wherein each of said fast acquisition sequences includes a short code portion having length N code chips and a long code portion having length M code chips, and the plurality of fast acquisition sequences, has length L code chips, where L, M and N are integers and L is equal to M multiplied by N.

6. The fast acquisition apparatus of claim 1, wherein each of said fast acquisition sequences including a short code portion having length N code chips and a long code portion having length M code chips, and the plurality of fast acquisition sequences, . has length L code chips, where L, M and N are integers and L is equal to the least common multiple of M and N.

7. The fast acquisition apparatus of claim 3, wherein the first spreading code sequence and the second spreading code sequence are equivalent fast acquisition sequences chosen from the plurality of fast acquisition sequences.

Patentansprüche

1. Schnellerfassungsgerät zum schnellen Synchronisieren einer Spreizcodephase eines Spreizspektrum-Kommunikationssystems auf ein gesendetes Codesignal mit einem gesendeten in-Phase I-Codesignal und einem gesendeten Quadratur Q-Codesignal, wobei das gesendete I-Codesignal eine erste Spreizcodesequenz und das gesendete Q-Codesignal eine zweite Spreizcodesequenz aufweist; wobei das gesendete I-Codesignal und das gesendete Q-Codesignal einen vorbestimmten gemeinsamen Codesequenzphasenverhältniswert aufweisen, und mit einer Empfangsvorrichtung zum Empfang des gesendeten Codesignals; wobei das Schnellerfassungsgerät **dadurch gekennzeichnet ist,**

dass die Empfangsvorrichtung (301-302) eine Vorrichtung zum Aussondern des gesendeten I-Codesignals und des gesendeten Q-Codesignals aus dem empfangenen Codesignal aufweist;

dass eine Korrelationsvorrichtung (304) zur Korrelation von Codesequenzen mit dem gesendeten Codesignal vorhanden ist, und diese einen I-Codesignalkorrelator und einen Q-Codesignalkorrelator umfasst;

dass eine Vorrichtung (303) zur Erzeugung einer lokalen Codesequenz vorhanden ist, die als Reaktion auf einen Codesteuersignalwert hin einen lokalen Abschnitt der I-Codesequenz mit einem I-Codephasenwert sowie einen lokalen Abschnitt der Q-Codesequenz mit einem Q-Codephasenwert erzeugt; sowie

dass eine mit dem I-Codesignalkorrelator, dem Q-Codesignalkorrelator und der Vorrichtung (303) zur Erzeugung einer lokalen Codesequenz verbundene Steuerung vorhanden ist, welche zur Bestimmung, zum Erhalt und zur Aufrechterhaltung einer Codesequenzsperre dient, worin der I-Codesignalkorrelator den lokalen Abschnitt der I-Codesequenz mit dem gesendeten I-Codesignal korreliert und einen Wert "I hoch" erzeugt, wenn der I-Codephasenwert des lokalen Abschnitts der I-Codesequenz und ein Codephasenwert des gesendeten I-Codesignals übereinstimmende Codephasenwerte haben, und worin der Q-Codesignalkorrelator den lokalen Abschnitt der Q-Codesequenz mit dem gesendeten Q-Codesignal korreliert und einen Wert "Q hoch" erzeugt, wenn der Q-Codephasenwert des lokalen Abschnitts der Q-Codesequenz und ein Codephasenwert des gesendeten Q-Codesignals übereinstimmende Codephasenwerte haben,

worin die Steuerung den Codesteuersignalwert erzeugt, um den 1-Codephasenwert des lokalen Abschnitts

der I-Codesequenz als Reaktion auf den Wert "I hoch" zu sperren und den Q-Codephasenwert des lokalen Abschnitts der Q-Codesequenz zu setzen, und den Codesteuersignalwert erzeugt, um den Q-Codephasenwert des lokalen Abschnitts der Q-Codesequenz als Reaktion auf den Wert "Q hoch" zu sperren und den I-Codephasenwert des lokalen Abschnitts der I-Codesequenz zu setzen,

die Steuerung als Reaktion auf die Abwesenheit der Werte "I hoch" und "Q hoch" den Codesteuersignalwert erzeugt, der den 1-Codephasenwert und den Q-Codephasenwert einstellt,

die erste und die zweite Spreizcodesequenz jeweils aus einer Vielzahl von Schnellerfassungssequenzen mit Codechips der Länge L ausgewählt sind; wobei jede dieser Schnellerfassungssequenzen einen kurzen Codeabschnitt mit Codechips der Länge N sowie einen langen Codeabschnitt mit Codechips der Länge M und einen mittleren Suchwert von log 2L Phasen aufweist, worin der kurze Codeabschnitt wiederholt auftritt,

der lokale Abschnitt der I-Codesequenz eine I-Sequenz aufweist, die dem kurzen Codeabschnitt der entsprechenden Schnellerfassungssequenz äquivalent ist, und der lokale Abschnitt der Q-Codesequenzen eine Q-Sequenz aufweist, die dem kurzen Codeabschnitt der entsprechenden Schnellerfassungssequenz äquivalent ist,

der I-Codesignalkorrelator des weiteren eine Vorrichtung zum Erzeugen eines Wertes "I mittel" aufweist, wenn der I-Codephasenwert des lokalen Abschnitts der I-Codesequenz und die Codephase des gesendeten I-Codesignals Codephasenwerte aufweisen, die der I-Sequenz in Phase mit einem Auftreten der entsprechenden kurzen Codesequenz der ersten Spreizcodesequenz entsprechen,

der Q-Codesignalkorrelator des weiteren eine Vorrichtung zum Erzeugen eines Wertes "Q mittel" aufweist, wenn die Q-Codephase des lokalen Abschnitts der Q-Codesequenz und die Codephase des gesendeten Q-Codesignals Codephasenwerte aufweisen, die der Q-Sequenz in Phase mit einem Auftreten der entsprechenden kurzen Codesequenz der zweiten Spreizcodesequenz entsprechen, und

die Steuerung als Reaktion auf den Wert "I mittel" und die Abwesenheit der Werte "I hoch" und "Q hoch" den Codesteuersignalwert erzeugt, der den I-Codephasenwert und den Q-Codephasenwert einstellt, um den jeweiligen lokalen kurzen Codesequenzabschnitt des lokalen Abschnitts der I-Codesequenz in Phase mit jedem jeweiligen Auftreten der kurzen Codesequenz der ersten Spreizcodesequenz zu halten; und als Reaktion auf den Wert "Q mittel" und die Abwesenheit der Werte "I hoch" und "Q hoch" den Codesteuersignalwert zur Einstellung des I-Codephasenwerts und des Q-Codephasenwerts erzeugt, um die jeweilige Q-Sequenz des lokalen Abschnitts der Q-Codesequenz in Phase mit jedem jeweiligen Auftreten der kurzen Codesequenz der zweiten Spreizcodesequenz zu halten.

2. Schnellerfassungsgerät nach Anspruch 1, worin die erste Spreizcodesequenz äquivalent mit der zweiten Spreizcodesequenz ist, und das gesendete I-Codesignal und das gesendete Q-Codesignal in dem vorbestimmten gemeinsamen Codesequenzphasenverhältnis zueinander stehen, so dass die jeweiligen Codephasen nicht identisch sind.

3. Schnellerfassungsgerät nach Anspruch 1, worin der kurze Codeabschnitt Codechips der Länge N aufweist, wobei N eine gerade ganze Zahl ist, und der lange Codeabschnitt Codechips der Länge M aufweist, wobei M eine ungerade ganze Zahl ist.

4. Schnellerfassungsgerät nach Anspruch 1, worin der kurze Codeabschnitt Codechips der Länge N aufweist, wobei N eine ungerade ganze Zahl ist, und der lange Codeabschnitt Codechips der Länge M aufweist, wobei M eine gerade ganze Zahl ist.

5. Schnellerfassungsgerät nach Anspruch 1, worin jede der Schnellerfassungssequenzen mit einem kurzen Codeabschnitt mit Codechips der Länge N und mit einem langen Codeabschnitt mit Codechips der Länge M, sowie die Vielzahl von Schnellerfassungssequenzen, Codechips der Länge L aufweist, wobei L, M und N ganze Zahlen sind, und L gleich M multipliziert mit N ist.

6. Schnellerfassungsgerät nach Anspruch 1, worin jede der Schnellerfassungssequenzen mit einem kurzen Codeabschnitt mit Codechips der Länge N und mit einem langen Codeabschnitt mit Codechips der Länge M, sowie die Vielzahl von Schnellerfassungssequenzen, Codechips der Länge L aufweist, wobei L, M und N ganze Zahlen sind, und L gleich dem kleinsten gemeinsamen Vielfachen von M und N ist.

7. Schnellerfassungsgerät nach Anspruch 3, worin die erste Spreizcodesequenz und die zweite Spreizcodesequenz mit aus der Vielzahl von Schnellerfassungssequenzen ausgewählten Schnellerfassungssequenzen äquivalent sind.

Revendications

1. Appareil d'acquisition rapide destiné à synchroniser rapidement une phase de code d'étalement d'un système de communication à étalement du spectre avec un signal de code transmis présentant un signal de code en phase 1 transmis et un signal de code en quadrature Q transmis, ledit signal de code 1 transmis comprenant une première séquence de codes d'étalement et ledit signal de code Q transmis comprenant une deuxième séquence de codes d'étalement ; le signal de code I transmis et le signal de code Q transmis présentant une valeur de rapport mutuel de phases de séquences de codes prédéterminée et comprenant des moyens de réception pour recevoir le signal de code transmis, l'appareil d'acquisition rapide comprenant :

les moyens de réception (301-302) comprenant des moyens pour séparer du signal de code reçu le signal de code I transmis et le signal de code Q transmis;
un moyen de corrélation (304) pour corréler les séquences de codes avec le signal de code transmis et comprenant un corrélateur de signaux de code I et un corrélateur de signaux de code Q ;
un générateur de séquences de codes locales (303) sensible à une valeur de signal de commande de code pour générer une partie locale de la séquence de codes I présentant une valeur de phase de code I et une partie locale de la séquence de codes Q présentant une valeur de phase de code Q ; et
un dispositif de commande connecté au corrélateur de signaux de code I, au corrélateur de signaux de code Q et au générateur de séquences de codes locales (303), ledit dispositif de commande étant destiné à déterminer, obtenir et maintenir un asservissement de séquences de codes dans lequel ledit corrélateur de signaux de code I corrèle ladite partie locale de la séquence de codes I avec ledit signal de code I transmis et génère une valeur supérieure I lorsque la valeur de phase de code I de la partie locale de la séquence de codes 1 et une valeur de phase de code du signal de code I transmis présentent des valeurs de phase de code correspondantes, et dans lequel ledit corrélateur de signaux de code Q corrèle ladite partie locale de la séquence de codes Q avec ledit signal de code Q transmis et génère une valeur supérieure Q lorsque la valeur de phase de code Q de la partie locale de la séquence de codes Q et une valeur de phase de code du signal de code Q transmis présentent des valeurs de phase de code correspondantes ;

dans lequel ledit dispositif de commande génère la valeur du signal de commande de code pour asservir la valeur de phase de code I de la partie locale de la séquence de codes I en réponse à la valeur supérieure I et pour définir la valeur de phase de code Q de la partie locale de la séquence de codes Q, et génère la valeur de signal de commande de code pour asservir la valeur de phase de code Q de la partie locale de la séquence de codes Q en réponse à la valeur supérieure Q et pour définir la valeur de phase de code I de la partie locale de la séquence de codes I ;

ledit dispositif de commande est sensible à l'absence de la valeur supérieure I et de la valeur supérieure Q pour générer la valeur du signal de commande de code qui règle la valeur de phase de code I et la valeur de phase de code Q ;

la première séquence de codes d'étalement et la deuxième séquence de codes d'étalement sont sélectionnées chacune parmi une pluralité de séquences d'acquisition rapide à impulsions de code de longueur L ; chacune desdites séquences d'acquisition rapide comprenant une partie de codes courts présentant des impulsions de code de longueur N et une partie de codes longs présentant des impulsions de longueur M et présentant une valeur de recherche moyenne de phases log 2L, dans laquelle la partie de codes courts apparaît de manière répétitive ;

ladite partie locale de la séquence de codes I comprend une séquence I équivalente à la partie de codes courts de la séquence d'acquisition rapide respective, et ladite partie locale des séquences de codes Q comprend une séquence Q équivalente à la partie de codes courts de la séquence d'acquisition rapide correspondante ;

ledit corrélateur de signaux de code I comprend en outre des moyens pour générer une valeur moyenne I lorsque la valeur de phase de code I de la partie locale de la séquence de codes I et la phase de code du signal de code I transmis présentent des valeurs de phase de code correspondant à la séquence I en phase avec une occurrence de la séquence de codes courts respective de la première séquence de codes d'étalement ;

ledit corrélateur de signaux de code Q comprend en outre des moyens pour générer une valeur moyenne Q lorsque la valeur de phase de code Q de la partie locale de la séquence de codes Q et la phase de code du signai de code Q transmis présentent des valeurs de phase de code correspondant à la séquence Q en phase avec une occurrence de la séquence de codes courts respective de la première séquence de codes d'étalement ; et

ledit dispositif de commande est sensible à la valeur moyenne I et à l'absence de la valeur supérieure I et de la valeur supérieure Q pour générer la valeur de signal de commande de code qui règle la valeur de phase de code I et la valeur de phase de code Q pour maintenir la partie locale de séquence de codes courts de la partie locale de la séquence de codes I en phase avec chaque occurrence respective de la séquence de codes courts

de la première séquence de codes d'étalement ; ledit dispositif de commande est également sensible à la valeur moyenne Q et à l'absence de la valeur supérieur I et de la valeur supérieure Q pour générer la valeur de signal de commande de code qui règle la valeur de phase de code I et la valeur de phase de code Q pour maintenir la séquence Q respective de la partie locale de la séquence de codes Q en phase avec chaque occurrence respective de la séquence de codes courts de la deuxième séquence de codes d'étalement.

2. Appareil d'acquisition rapide selon la revendication 1, dans lequel la première séquence de codes d'étalement est équivalente à la deuxième séquence de codes d'étalement et le signal de code I transmis ainsi que le signal de code Q transmis présentent une valeur de rapport mutuel de phases de séquences de codes prédéterminée, de façon à ce que les phases de codes respectives ne soient pas identiques.

3. Appareil d'acquisition rapide selon la revendication 1, dans lequel la partie de codes courts présente des impulsions de code de longueur N, où N est un entier pair, et la partie de codes longs présente des impulsions de code de longueur M, où M est un entier impair.

4. Appareil d'acquisition rapide selon la revendication 1, dans lequel la partie de codes courts présente des impulsions de code de longueur N, où N est un entier impair, et la partie de codes longs présente des impulsions de code de longueur M, où M est un entier pair.

5. Appareil d'acquisition rapide selon la revendication 1, dans lequel chacune desdites séquences d'acquisition rapide comprend une partie de codes courts qui présente des impulsions de code de longueur N et une partie de codes longs qui présente des impulsions de code de longueur M et la pluralité des séquences d'acquisition rapide présente des impulsions de code de longueur L, où L, M et N sont des entiers et L est égal à M multiplié par N.

6. Appareil d'acquisition rapide selon la revendication 1, dans lequel chacune desdites séquences d'acquisition rapide comprend une partie de codes courts qui présente des impulsions de code de longueur N et une partie de codes longs qui présente des impulsions de code de longueur M et la pluralité des séquences d'acquisition rapide présente des impulsions de code de longueur L, où L, M et N sont des entiers et L est égal au plus petit multiple commun de M et N.

7. Appareil d'acquisition rapide selon la revendication 3, dans lequel la première séquence de codes d'étalement et la deuxième séquence de codes d'étalement sont des séquences d'acquisition rapide équivalentes sélectionnées parmi la pluralité des séquences d'acquisition rapide.

FIG. 1

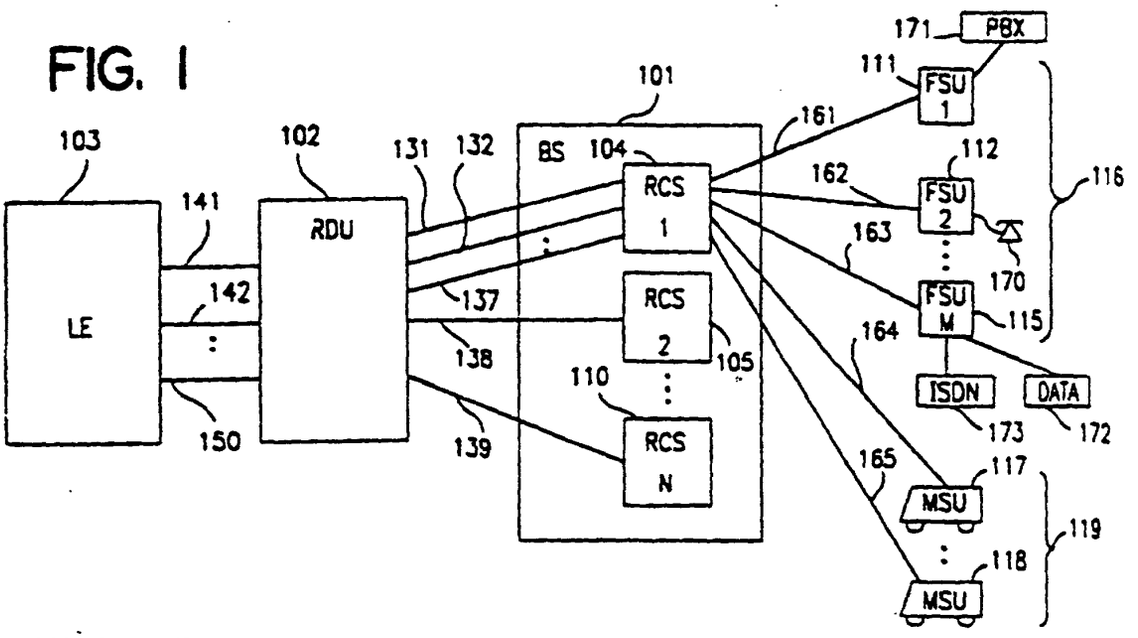


FIG. 2a

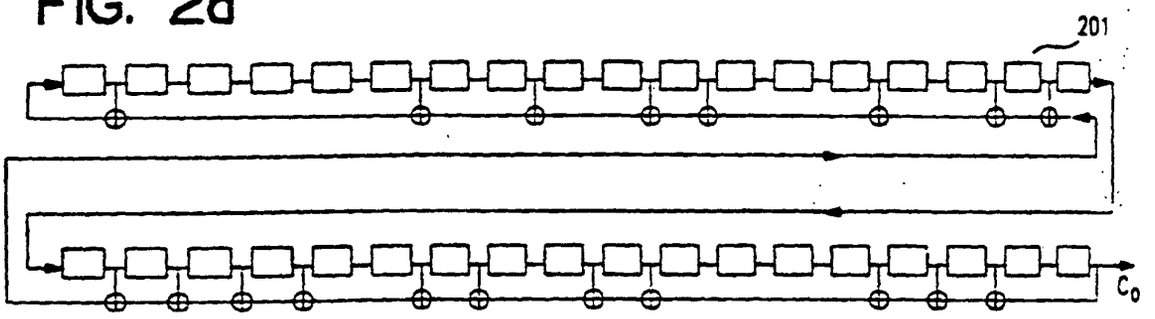


FIG. 2b

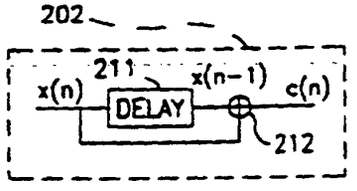


FIG. 2c

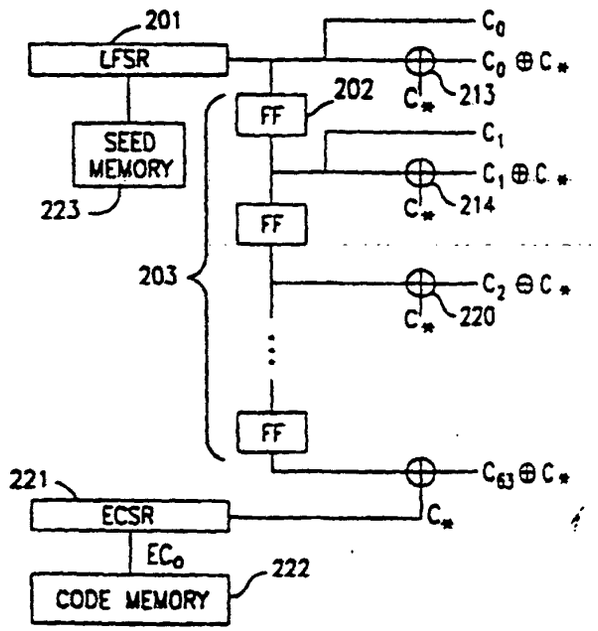
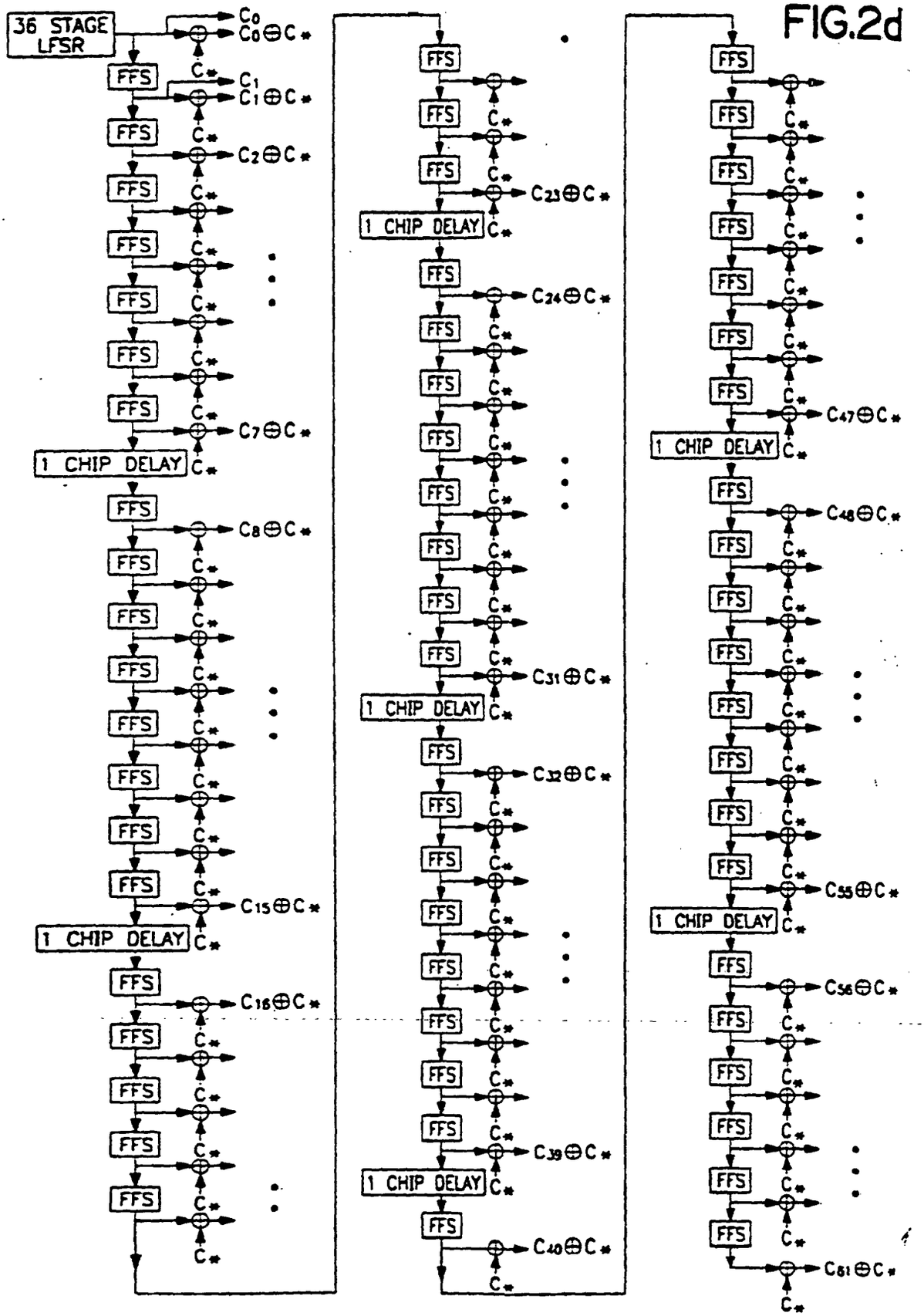


FIG.2d


36 STAGE LFSR
FFS
1 CHIP DELAY
C0
C0⊕C*
C1
C1⊕C*
C2⊕C*
C7⊕C*
C8⊕C*
C15⊕C*
C16⊕C*
C23⊕C*
C24⊕C*
C31⊕C*
C32⊕C*
C39⊕C*
C40⊕C*
C47⊕C*
C48⊕C*
C55⊕C*
C56⊕C*
C61⊕C*
C*

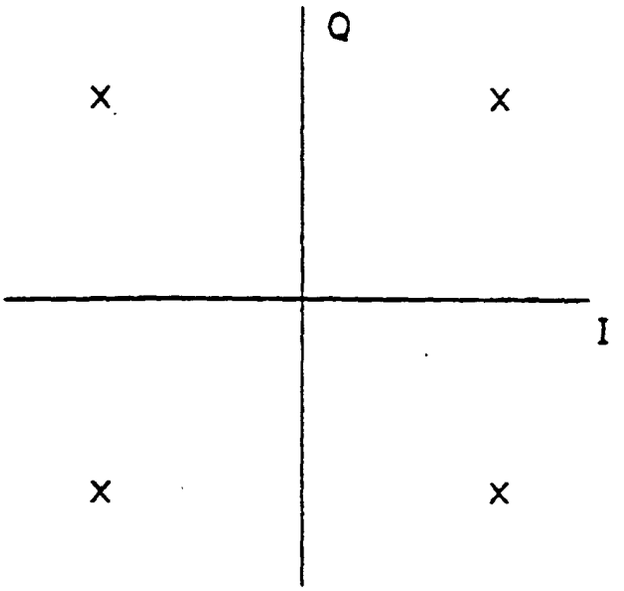


FIG. 3a

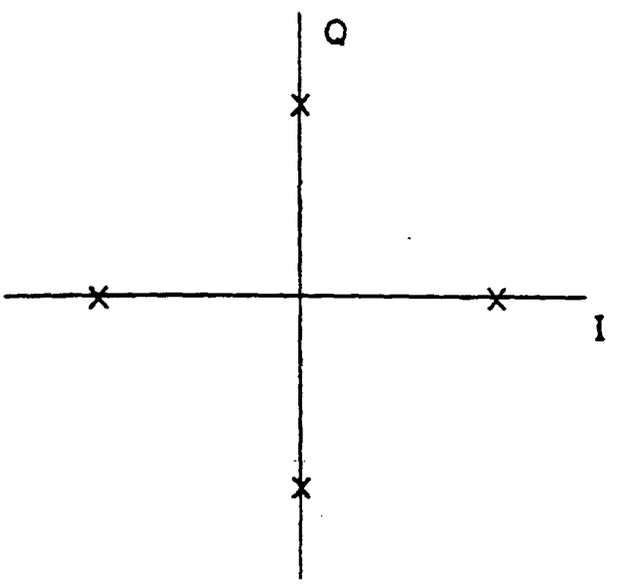


FIG. 3b

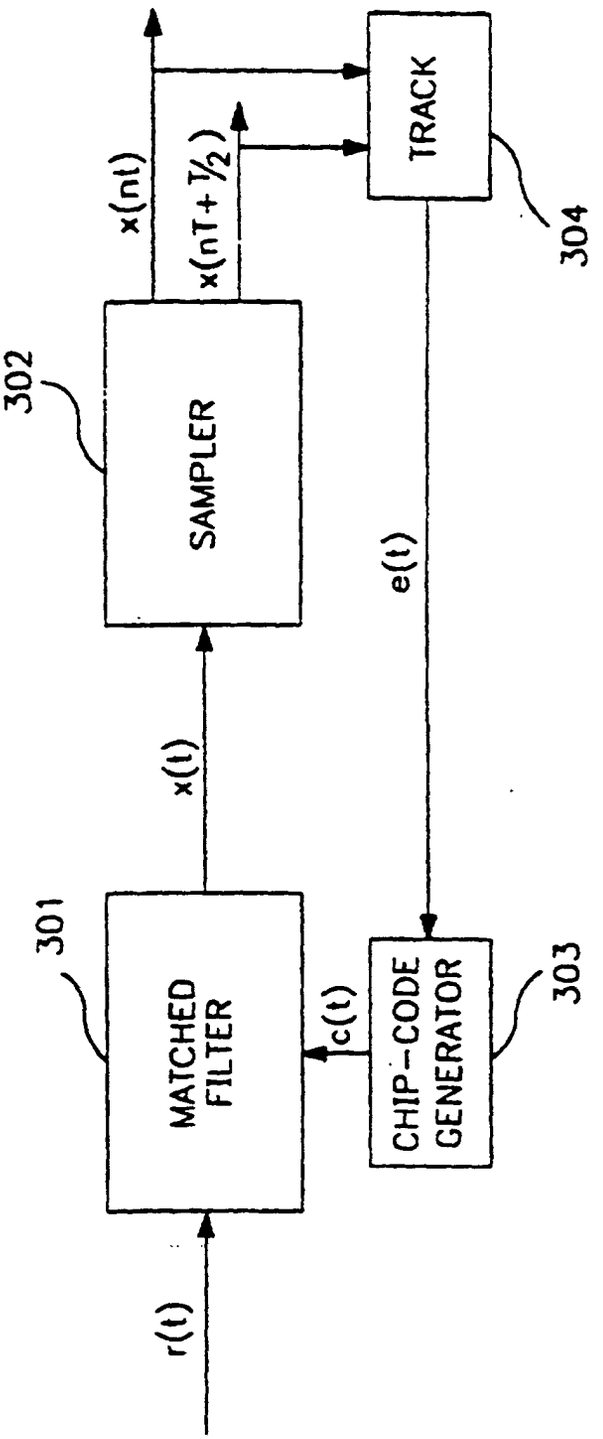

r(t)
MATCHED FILTER
301
x(t)
SAMPLER
302
x(nt)
x(nT+T/2)
TRACK
304
e(t)
c(t)
CHIP-CODE GENERATOR
303

FIG. 3c

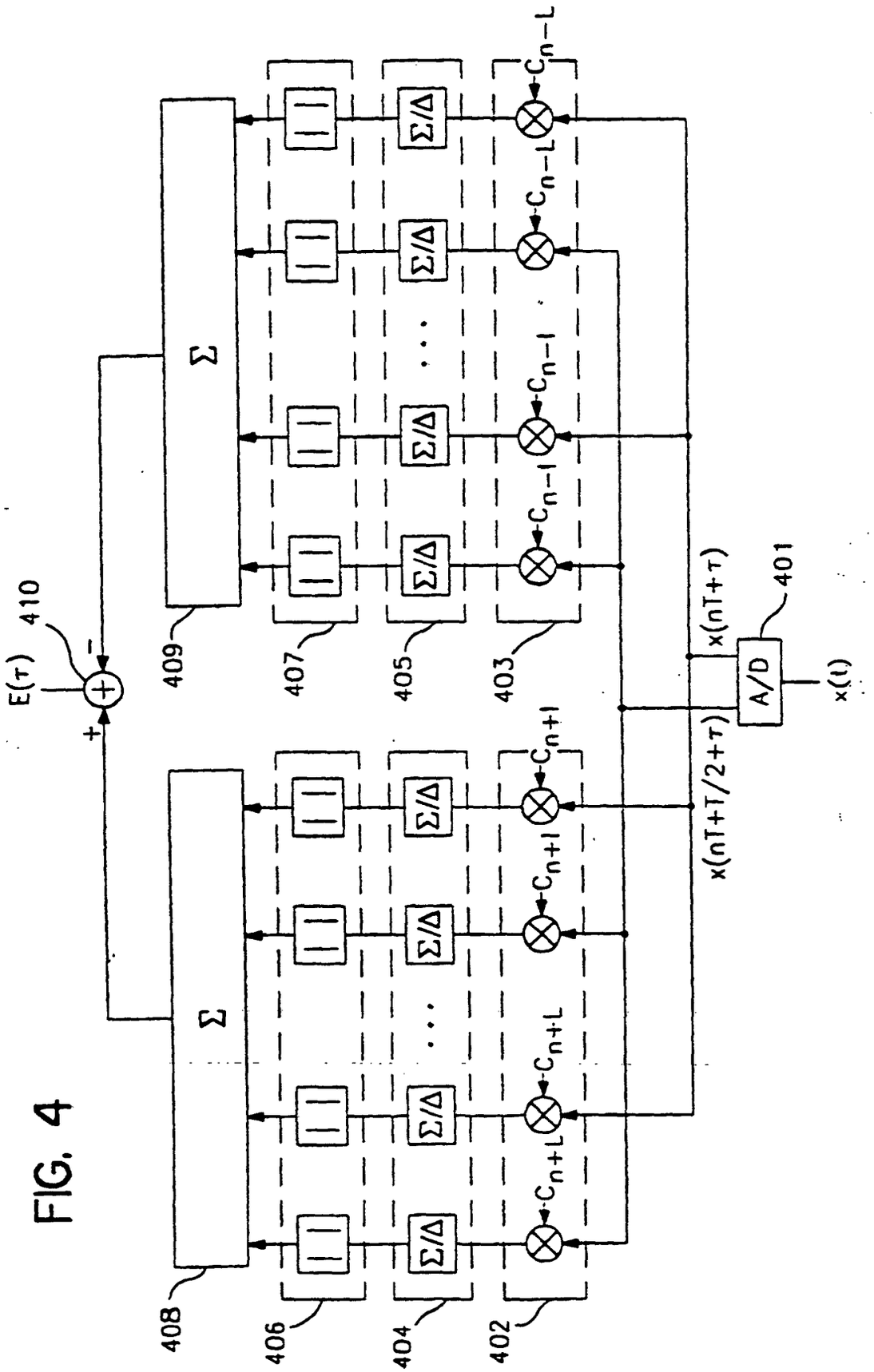

E(τ)
410
+
−
Σ
Σ/Δ
C_{n-L}
C_{n-1}
C_{n+1}
C_{n+L}
C_{n-1}
C_{n+1}
C_{n+L}
409
407
405
403
408
406
404
402
x(nT+τ)
x(nT+T/2+τ)
A/D
401
x(t)

FIG. 4

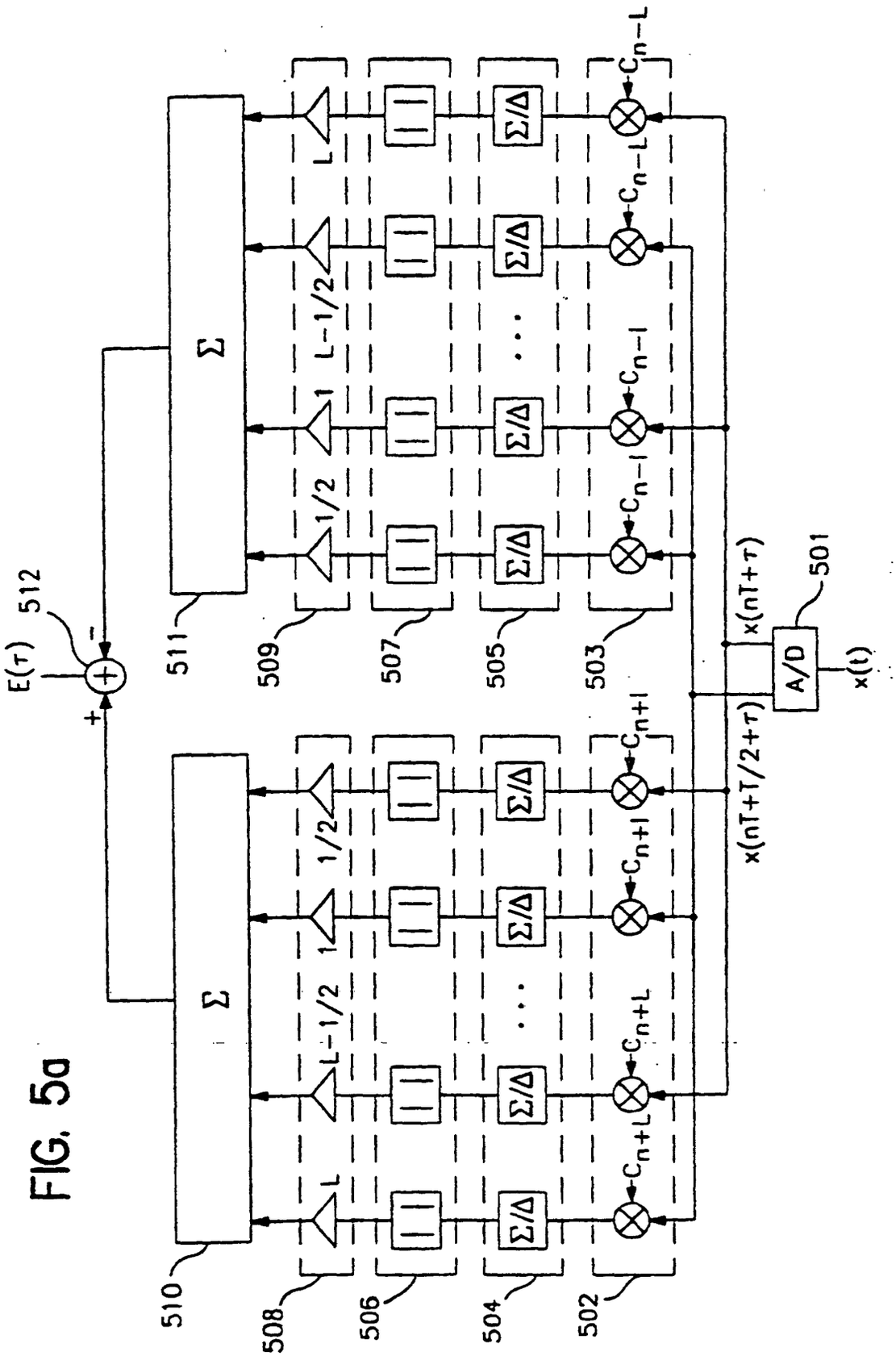
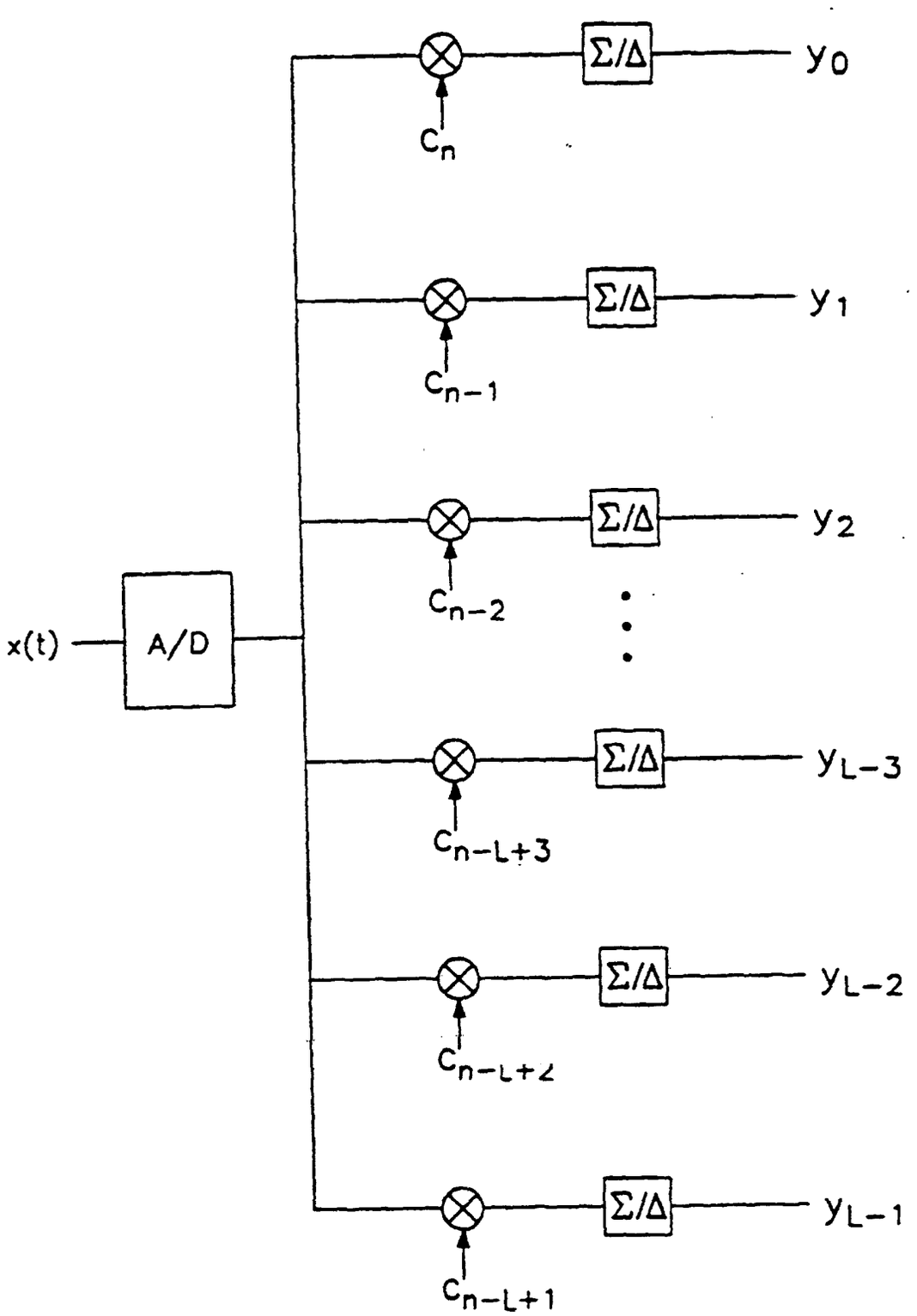

E(τ)
512
+
−
Σ
511
510
509
508
507
506
505
504
503
502
1/2
1
L−1/2
L
Σ/Δ
C_{n-L}
C_{n-l}
C_{n+l}
C_{n+L}
x(nT+τ)
x(nT+T/2+τ)
A/D
501
x(t)

FIG. 5a

FIG. 5b


x(t)
A/D
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
y_0
y_1
y_2
y_{L-3}
y_{L-2}
y_{L-1}
c_n
c_{n-1}
c_{n-2}
c_{n-L+3}
c_{n-L+2}
c_{n-L+1}

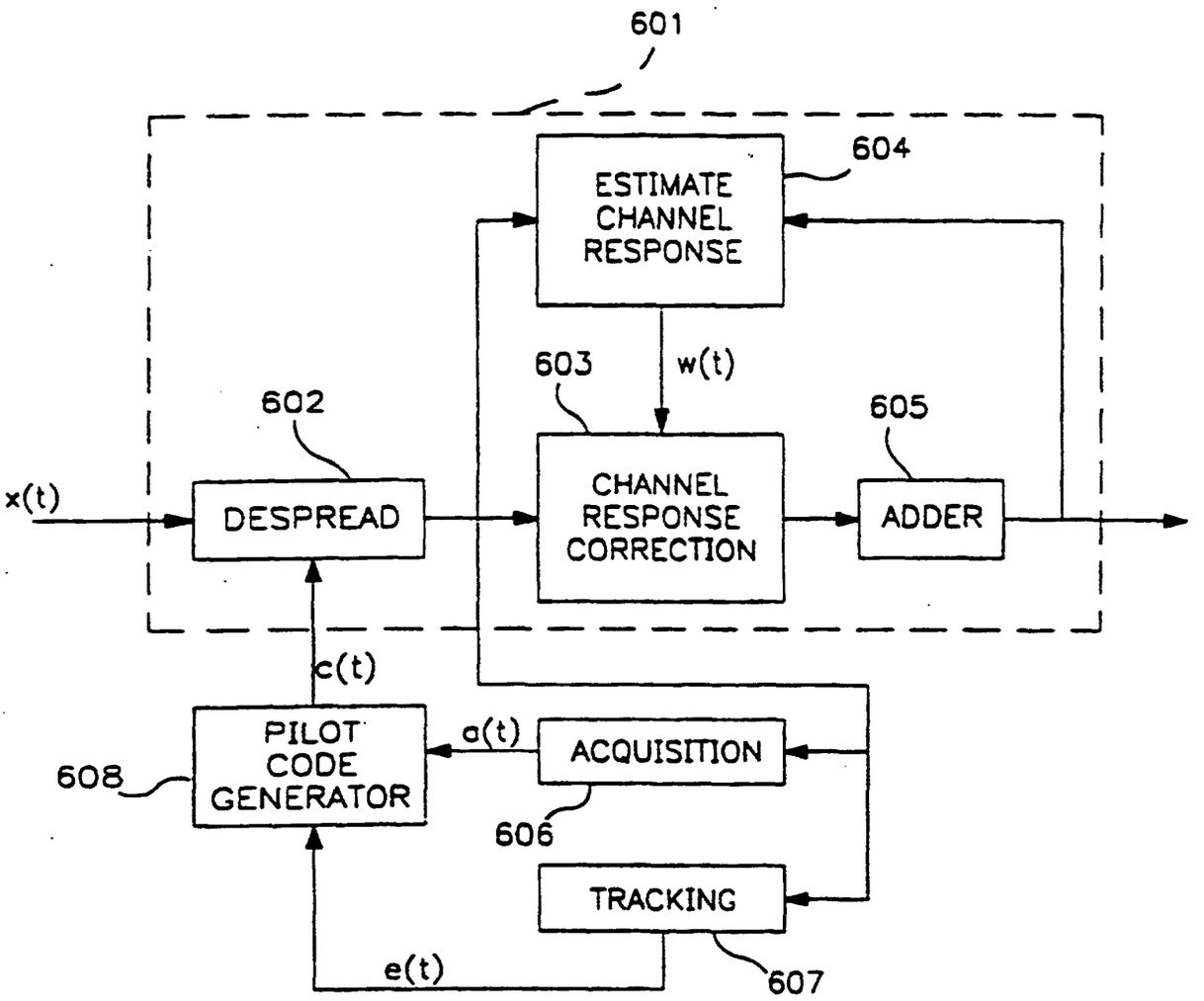

601
604
ESTIMATE CHANNEL RESPONSE
603
w(t)
602
605
x(t)
DESPREAD
CHANNEL RESPONSE CORRECTION
ADDER
c(t)
PILOT CODE GENERATOR
608
a(t)
ACQUISITION
606
TRACKING
e(t)
607

FIG. 6

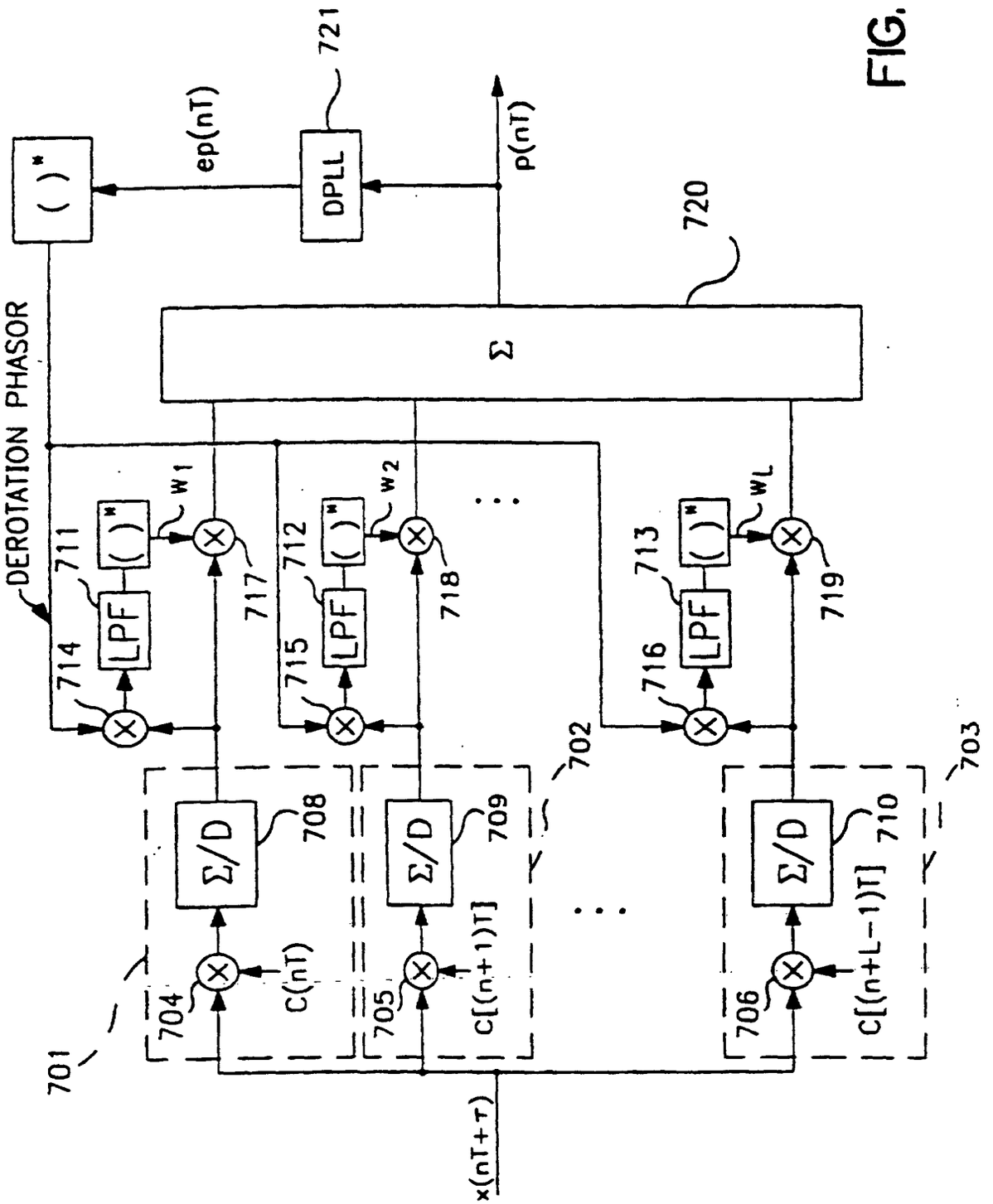

DEROTATION PHASOR
( )*
ep(nT)
721
DPLL
p(nT)
720
Σ
711
712
713
( )*
W1
W2
WL
LPF
714
715
716
717
718
719
Σ/D
708
709
710
C(nT)
C[(n+1)T]
C[(n+L-1)T]
704
705
706
701
702
703
x(nT+τ)

FIG. 7

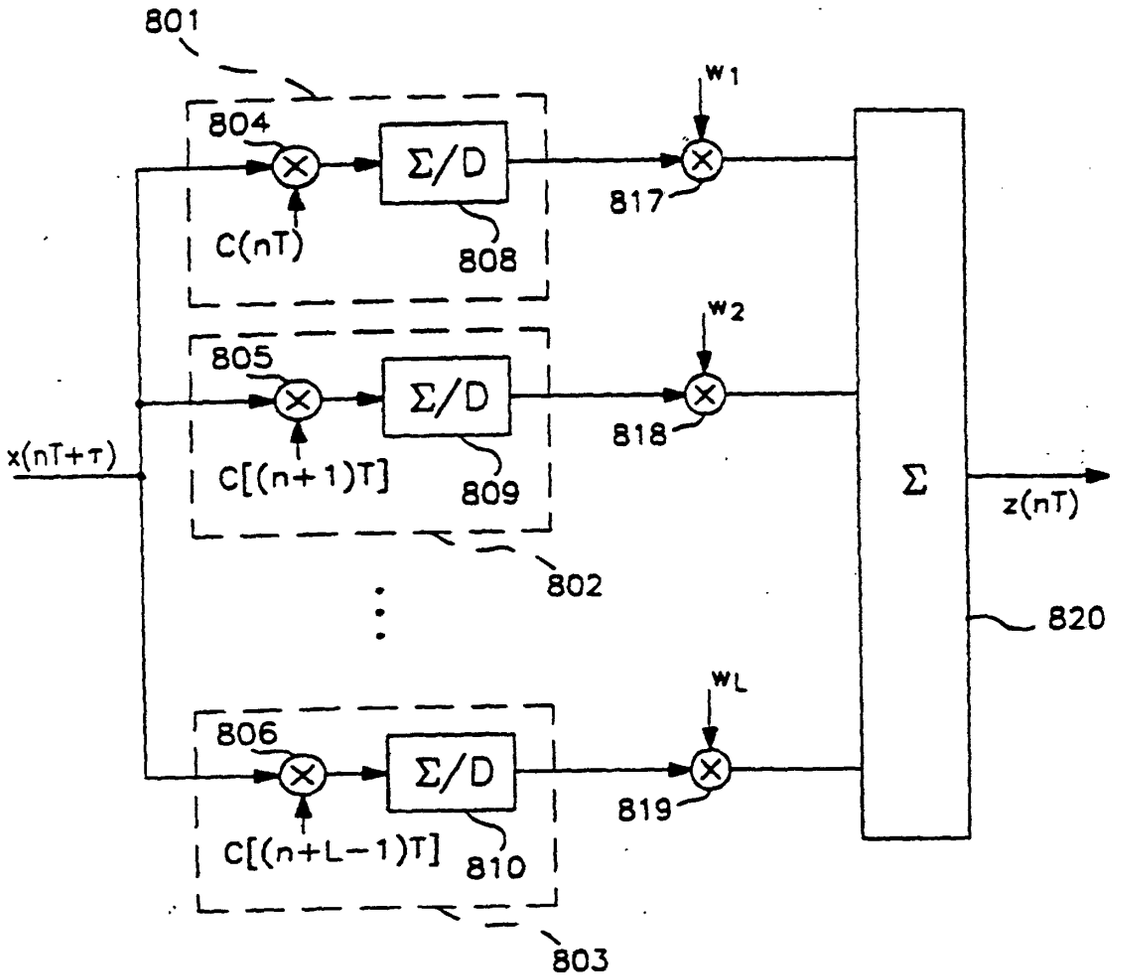

801
804
Σ/D
C(nT)
808
817
w1
805
Σ/D
C[(n+1)T]
809
818
w2
x(nT+τ)
802
Σ
z(nT)
820
806
Σ/D
C[(n+L−1)T]
810
819
wL
803

FIG. 8a

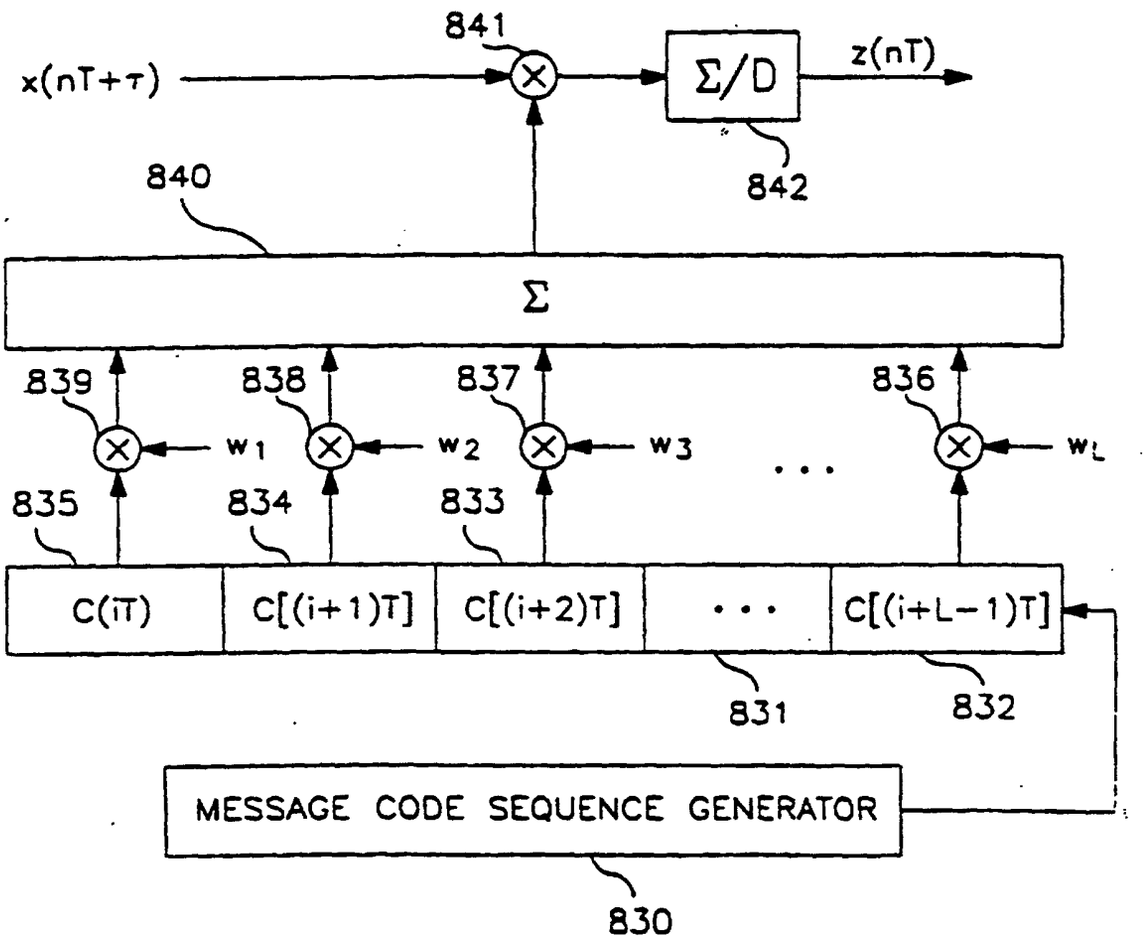

841
x(nT+τ)
Σ/D
z(nT)
842
840
Σ
839
838
837
836
w1
w2
w3
wL
835
834
833
C(iT)
C[(i+1)T]
C[(i+2)T]
C[(i+L−1)T]
831
832
MESSAGE CODE SEQUENCE GENERATOR
830

FIG. 8b

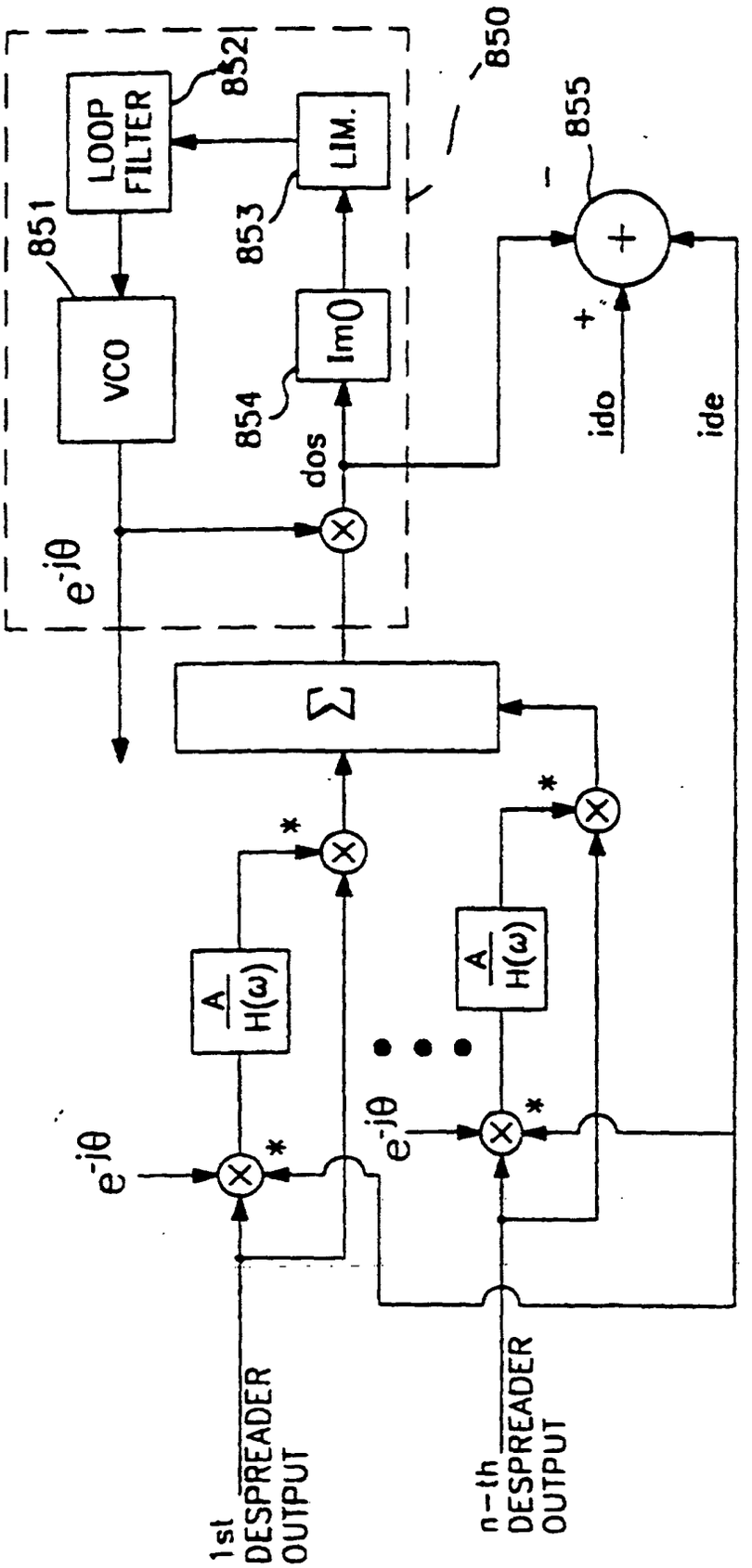

850
LOOP FILTER
852
LIM.
853
851
VCO
Im()
854
dos
855
ido
ide
$e^{-j\theta}$
Σ
$\frac{A}{H(\omega)}$
1st DESPREADER OUTPUT
n-th DESPREADER OUTPUT

FIG. 8c

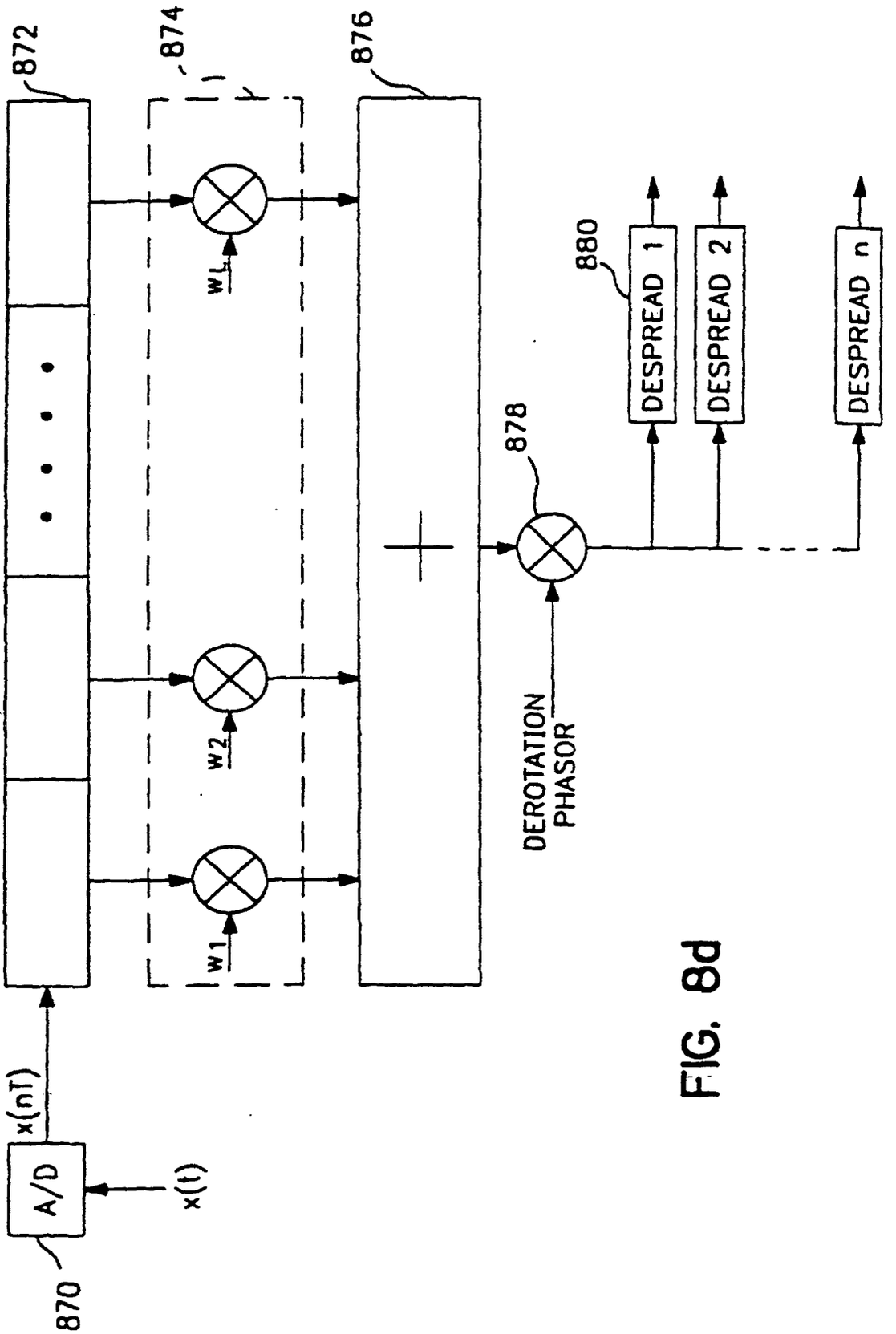

872
874
876
880
878
870
A/D
x(nT)
x(t)
W1
W2
WL
DESPREAD 1
DESPREAD 2
DESPREAD n
DEROTATION PHASOR

FIG. 8d

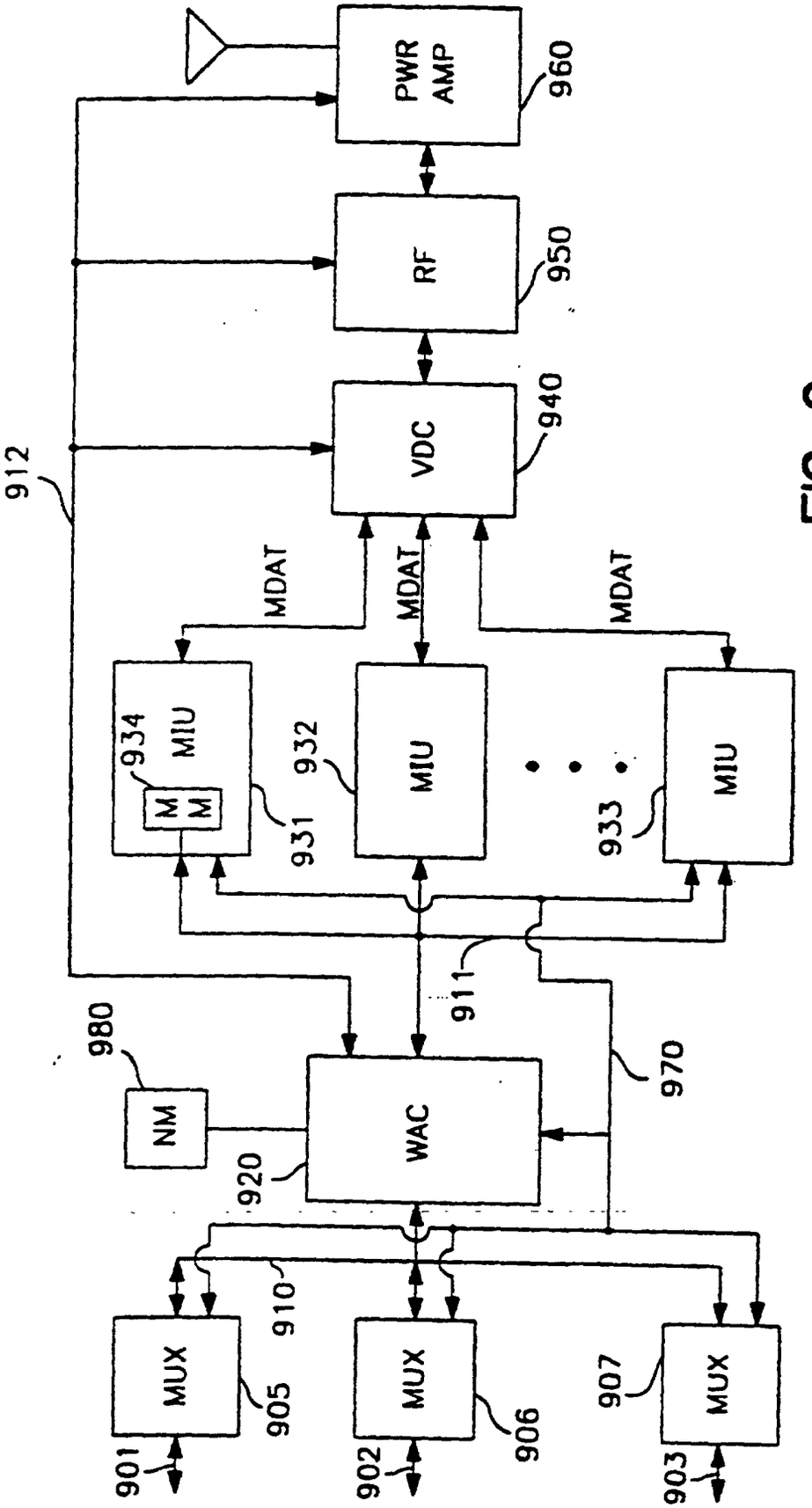

PWR AMP
960
RF
950
VDC
940
912
MDAT
MDAT
MDAT
934
MIU
M
M
931
932
MIU
933
MIU
911
980
NM
WAC
920
970
910
MUX
905
MUX
906
907
MUX
901
902
903

FIG. 9

FIG. 10

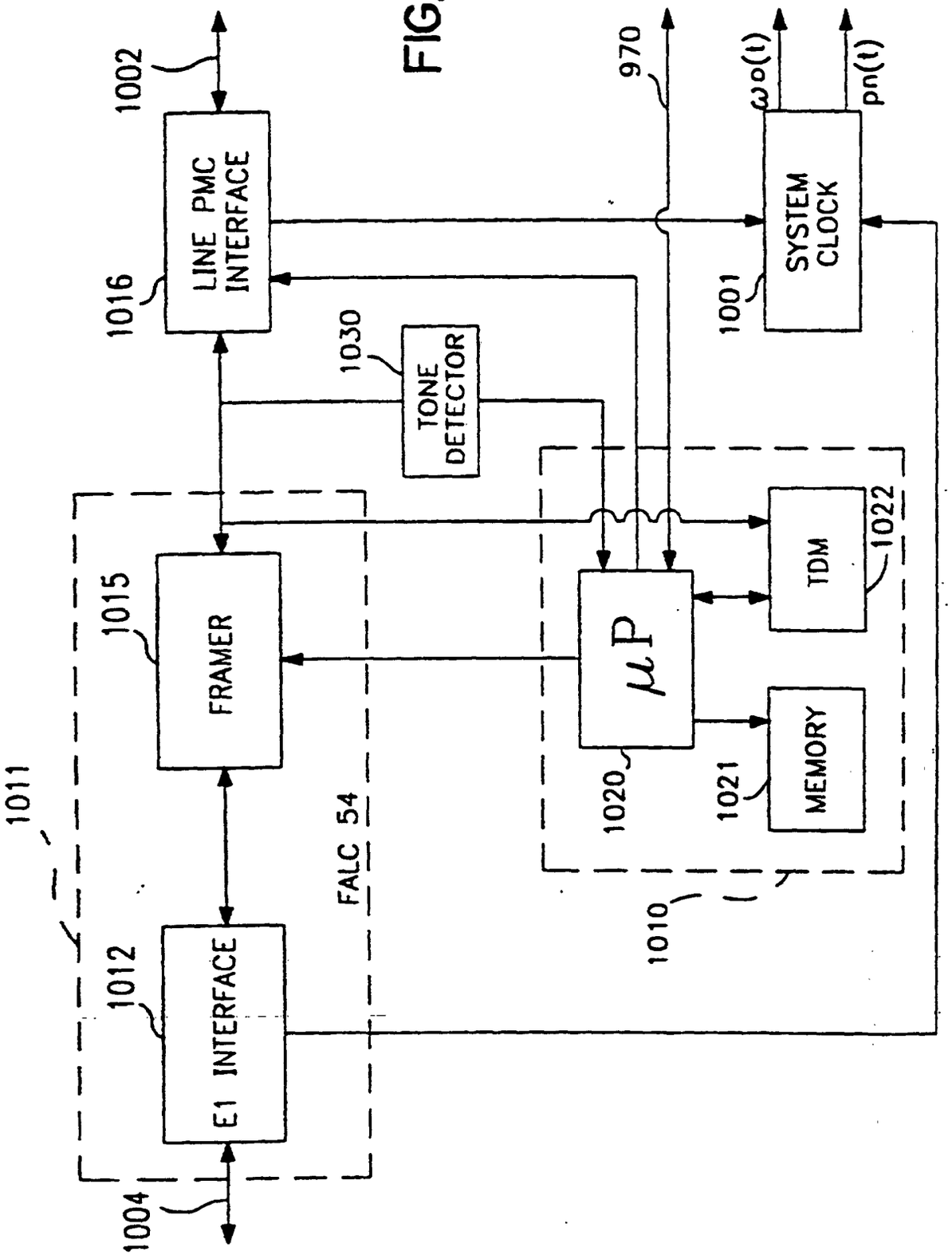
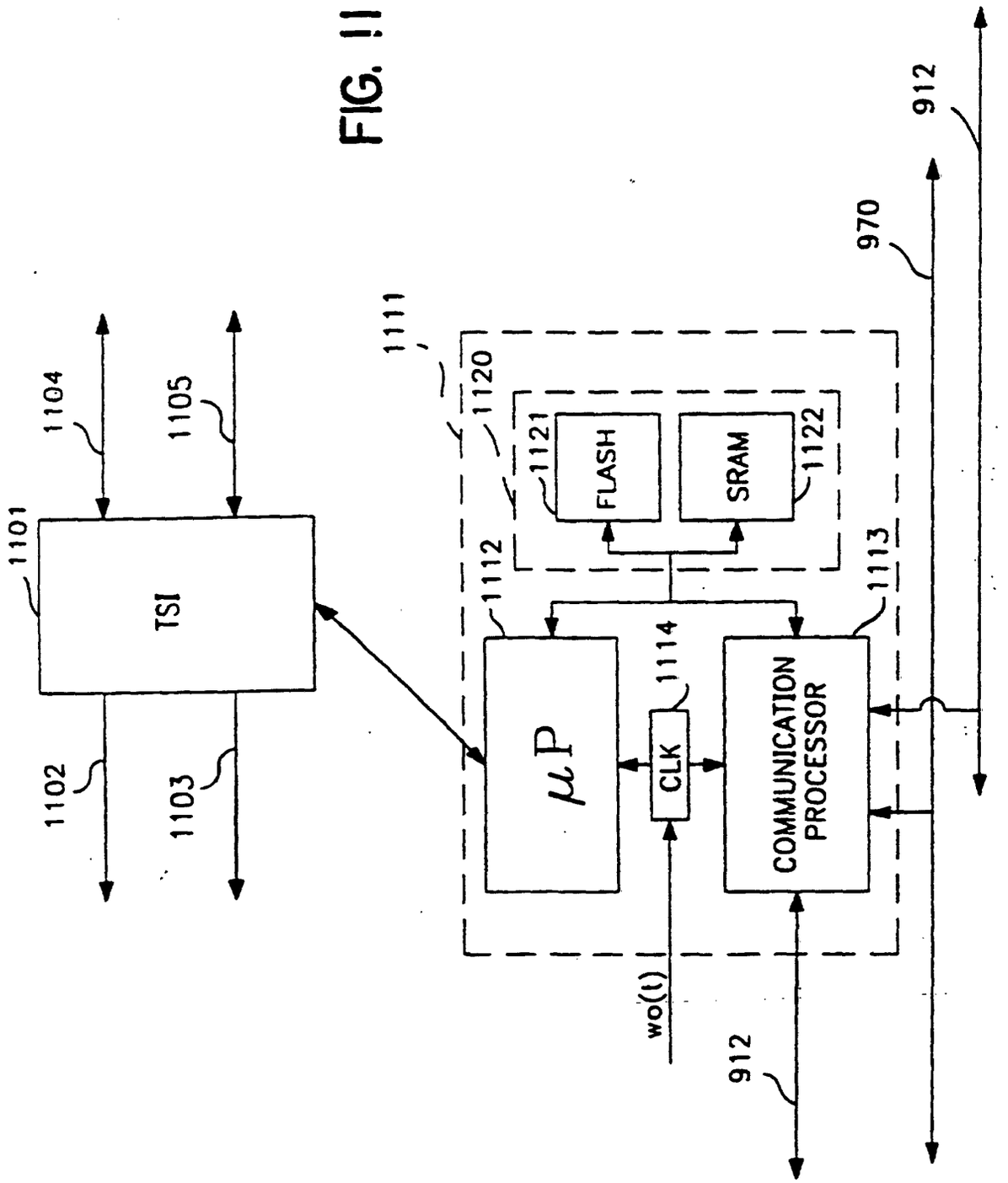

1002
LINE PMC INTERFACE
1016
970
ω0(t)
pn(t)
SYSTEM CLOCK
1001
1030
TONE DETECTOR
1022
TDM
1015
FRAMER
μP
1020
MEMORY
1021
1011
FALC 54
1010
1012
E1 INTERFACE
1004

FIG. 11


1101
TSI
1102
1103
1104
1105
1111
1112
1113
1114
1120
1121
FLASH
1122
SRAM
μP
CLK
COMMUNICATION PROCESSOR
wo(t)
912
970
912

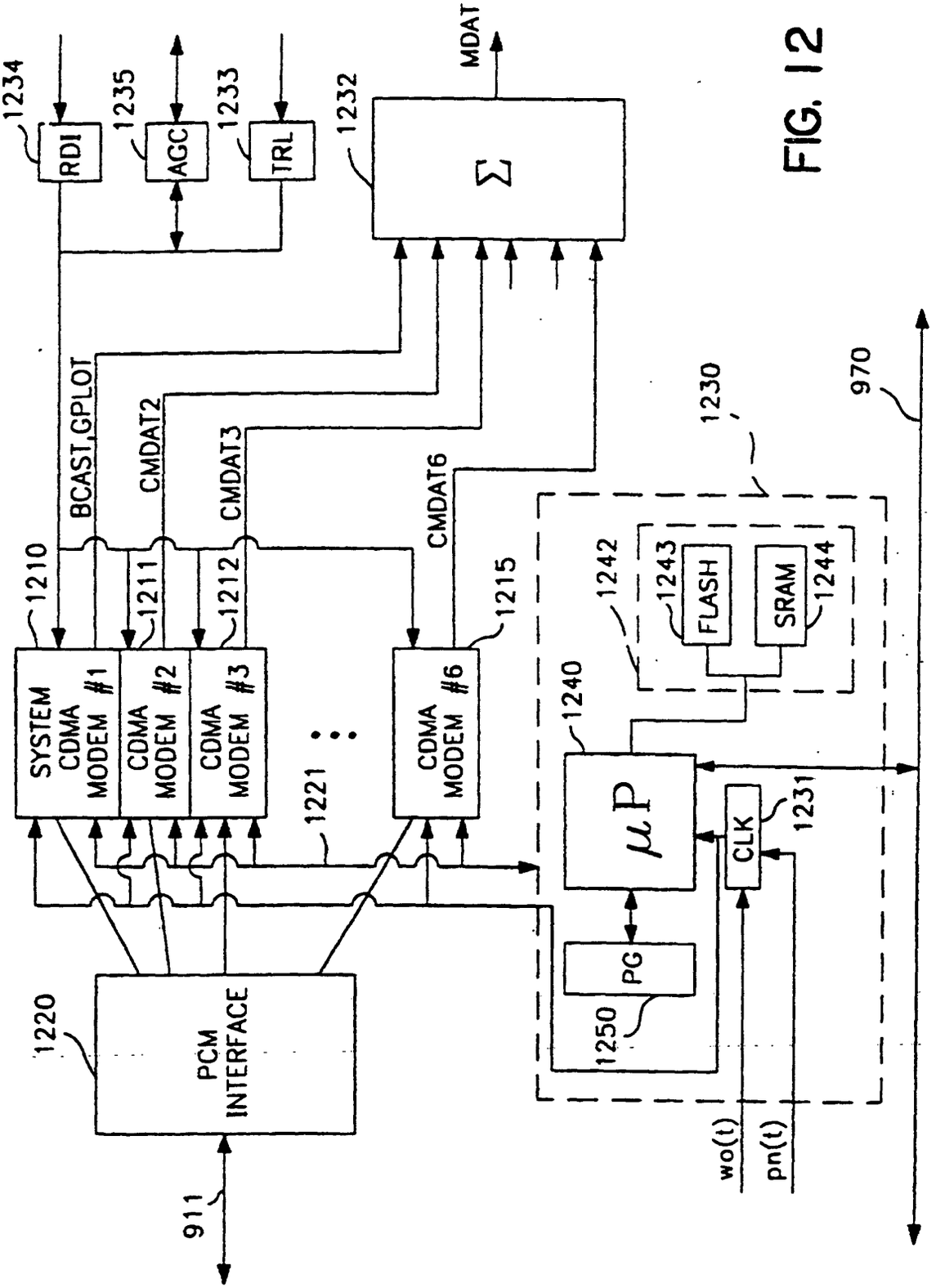

1234
RDI
1235
AGC
1233
TRL
1232
Σ
MDAT
BCAST,GPLOT
CMDAT2
CMDAT3
CMDAT6
1210
1211
1212
1215
1230
970
1242
1243
FLASH
SRAM
1244
SYSTEM CDMA MODEM #1
CDMA MODEM #2
CDMA MODEM #3
1221
CDMA MODEM #6
1240
μP
CLK
1231
PG
1250
1220
PCM INTERFACE
911
wo(t)
pn(t)

FIG. 12

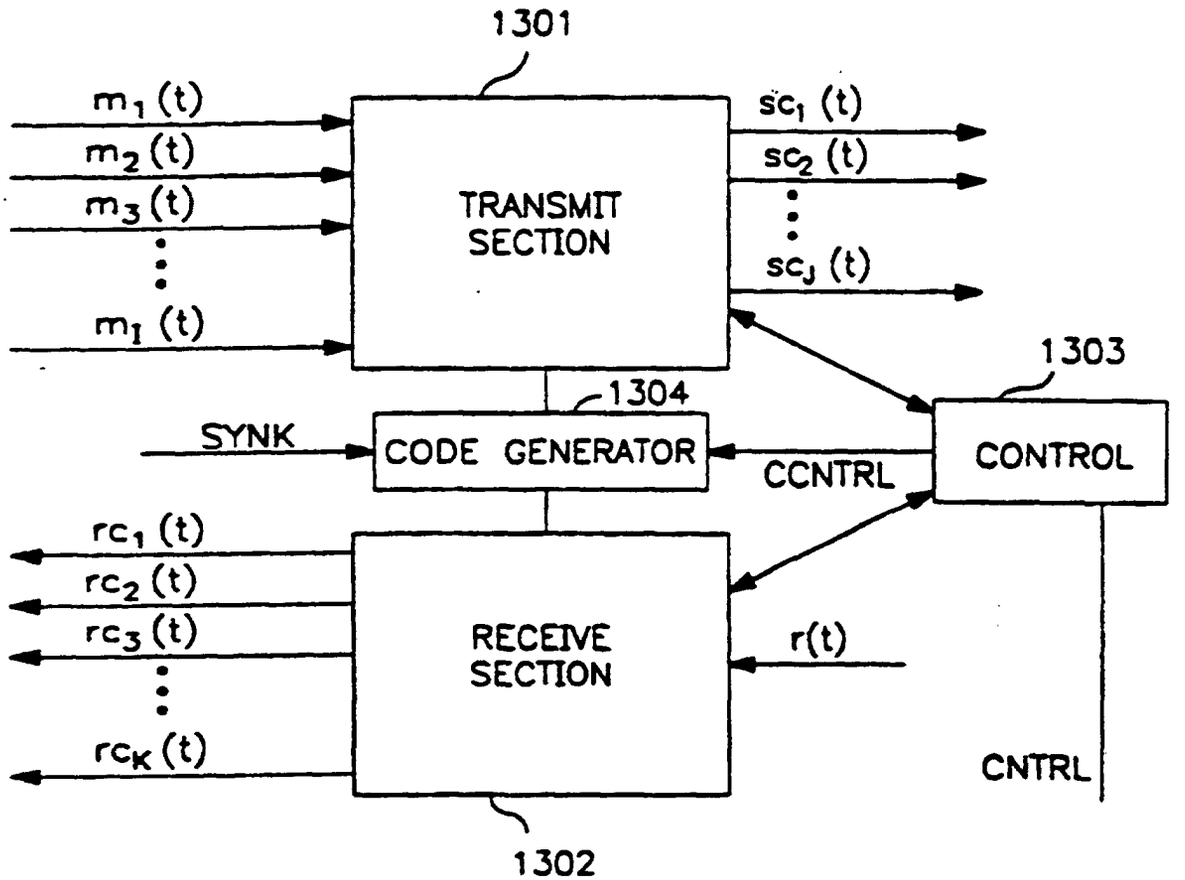

1301
$m_1(t)$
$m_2(t)$
$m_3(t)$
$m_I(t)$
TRANSMIT SECTION
$sc_1(t)$
$sc_2(t)$
$sc_J(t)$
1303
1304
SYNK
CODE GENERATOR
CCNTRL
CONTROL
$rc_1(t)$
$rc_2(t)$
$rc_3(t)$
$rc_K(t)$
RECEIVE SECTION
r(t)
CNTRL
1302

FIG. 13

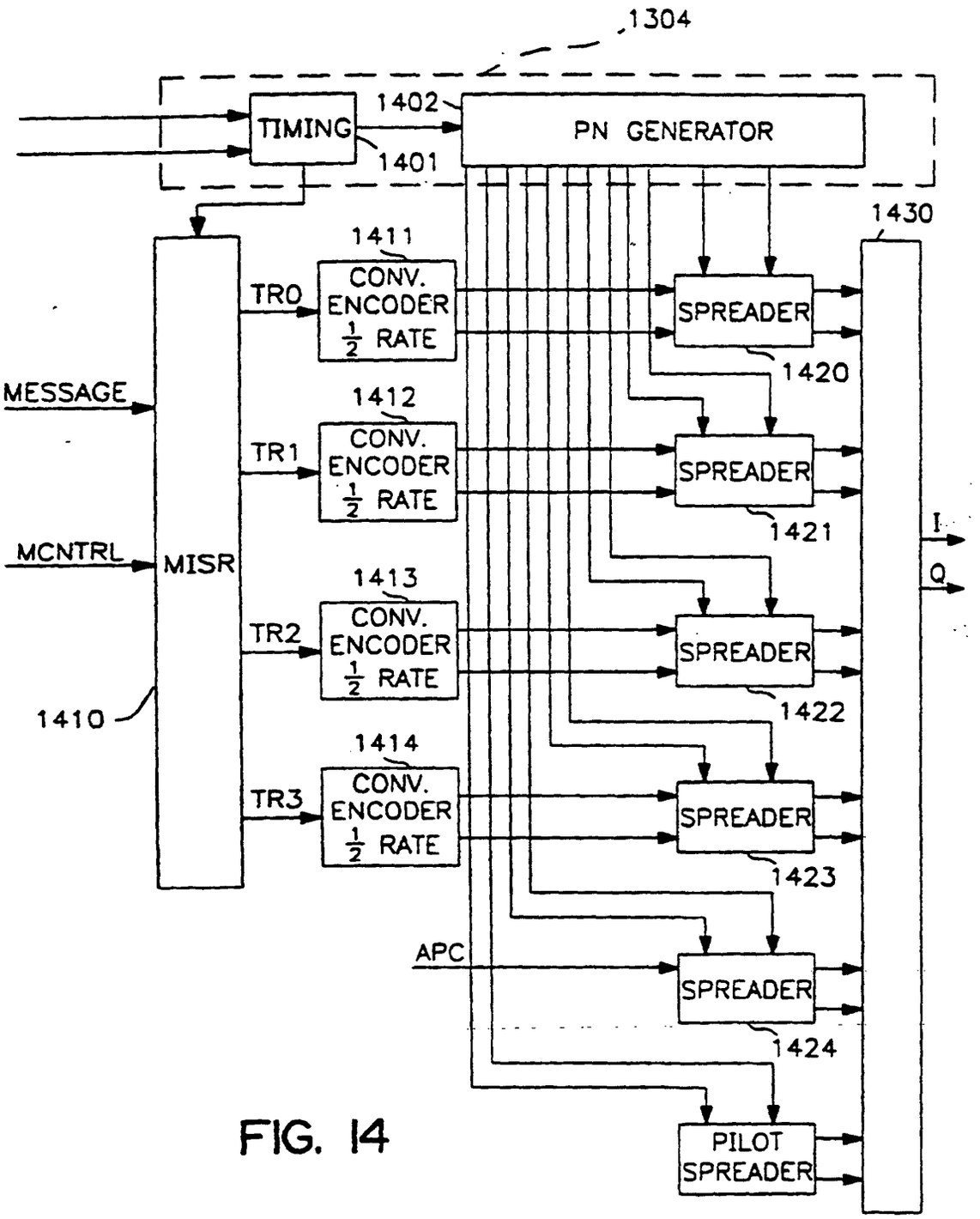

1304
TIMING
1402
1401
PN GENERATOR
1430
1411
CONV. ENCODER ½ RATE
TR0
SPREADER
1420
MESSAGE
1412
CONV. ENCODER ½ RATE
TR1
SPREADER
1421
I
MCNTRL
MISR
Q
1413
CONV. ENCODER ½ RATE
TR2
SPREADER
1422
1410
1414
CONV. ENCODER ½ RATE
TR3
SPREADER
1423
APC
SPREADER
1424
PILOT SPREADER

FIG. 14

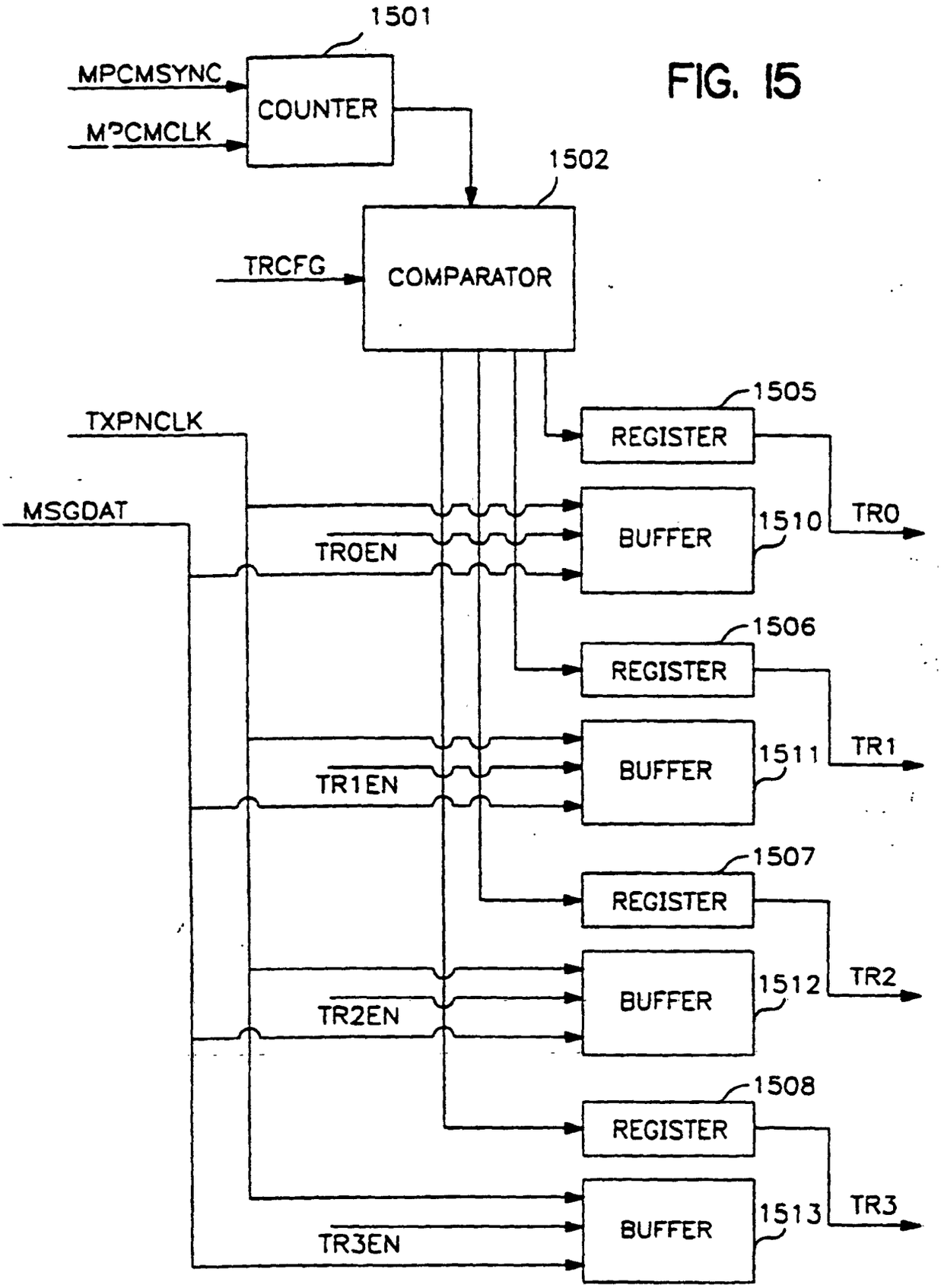

1501
MPCMSYNC
MPCMCLK
COUNTER
1502
TRCFG
COMPARATOR
TXPNCLK
MSGDAT
1505
REGISTER
BUFFER
1510
TR0
TR0EN
1506
REGISTER
BUFFER
1511
TR1
TR1EN
1507
REGISTER
BUFFER
1512
TR2
TR2EN
1508
REGISTER
BUFFER
1513
TR3
TR3EN

FIG. 15

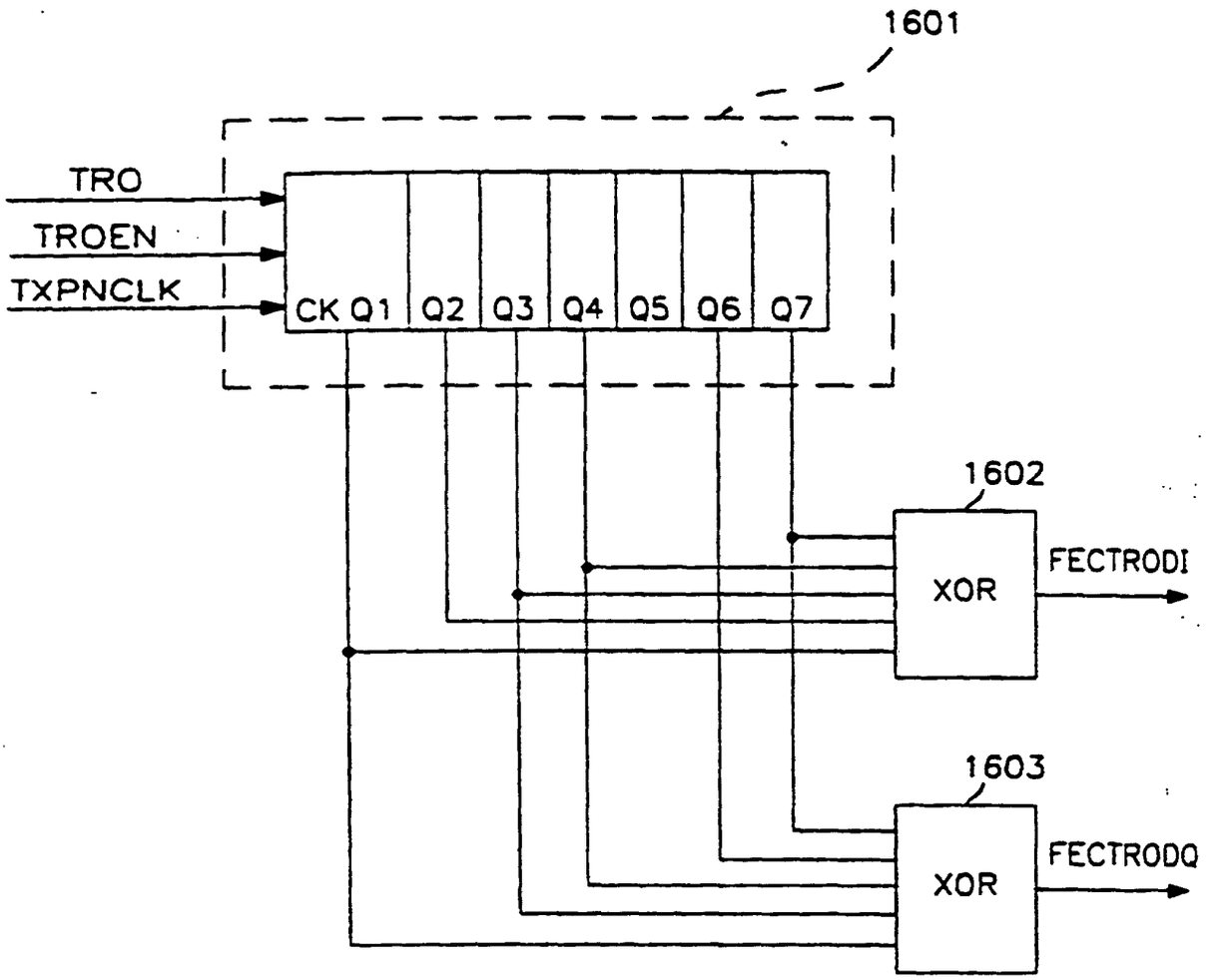

1601
TRO
TROEN
TXPNCLK
CK Q1
Q2
Q3
Q4
Q5
Q6
Q7
1602
XOR
FECTRODI
1603
XOR
FECTRODQ

FIG. 16

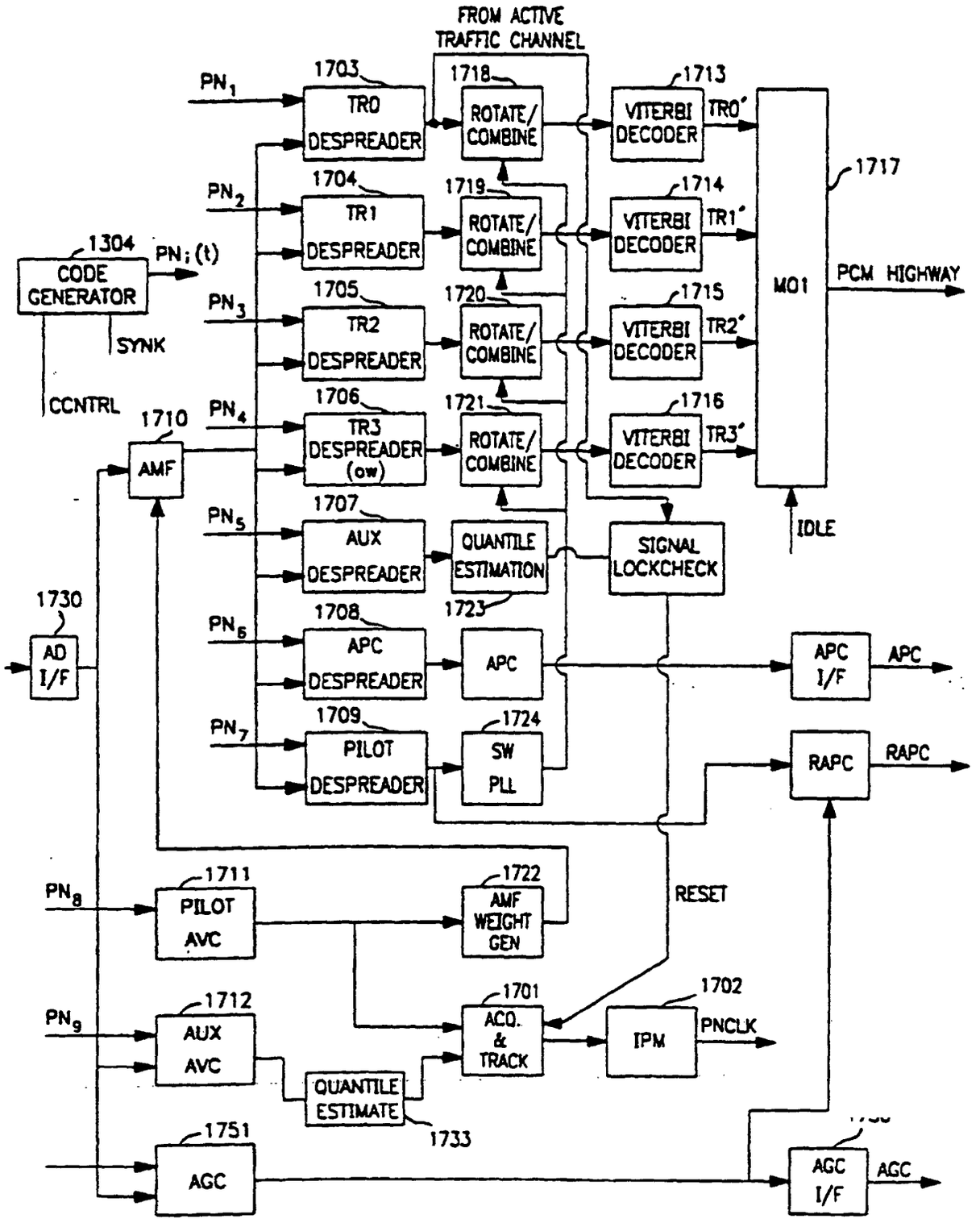

FROM ACTIVE TRAFFIC CHANNEL
PN1
1703
TR0 DESPREADER
1718
ROTATE/ COMBINE
1713
VITERBI DECODER
TR0'
PN2
1704
TR1 DESPREADER
1719
ROTATE/ COMBINE
1714
VITERBI DECODER
TR1'
1717
1304
CODE GENERATOR
PN;(t)
SYNK
CCNTRL
PN3
1705
TR2 DESPREADER
1720
ROTATE/ COMBINE
1715
VITERBI DECODER
TR2'
MOI
PCM HIGHWAY
PN4
1706
TR3 DESPREADER (ow)
1721
ROTATE/ COMBINE
1716
VITERBI DECODER
TR3'
1710
AMF
PN5
1707
AUX DESPREADER
QUANTILE ESTIMATION
1723
SIGNAL LOCKCHECK
IDLE
1730
AD I/F
PN6
1708
APC DESPREADER
APC
APC I/F
APC
PN7
1709
PILOT DESPREADER
1724
SW PLL
RAPC
RAPC
PN8
1711
PILOT AVC
1722
AMF WEIGHT GEN
RESET
PN9
1712
AUX AVC
1701
ACQ. & TRACK
1702
IPM
PNCLK
QUANTILE ESTIMATE
1733
1751
AGC
AGC I/F
AGC

FIG. 17

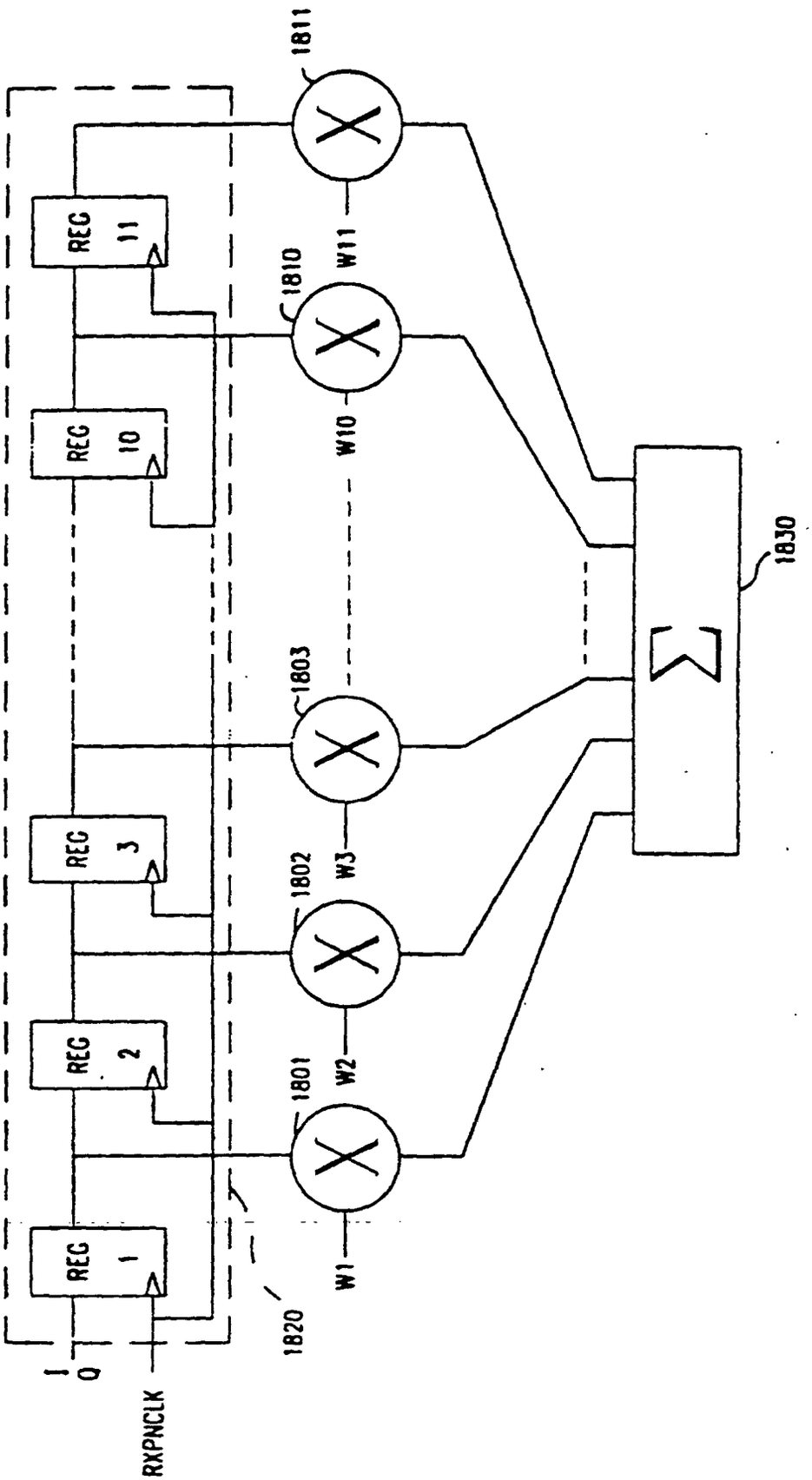

1811
1810
1803
1802
1801
REG 11
REG 10
REG 3
REG 2
REG 1
W11
W10
W3
W2
W1
1830
1820
I
Q
RXPNCLK

FIG. 18

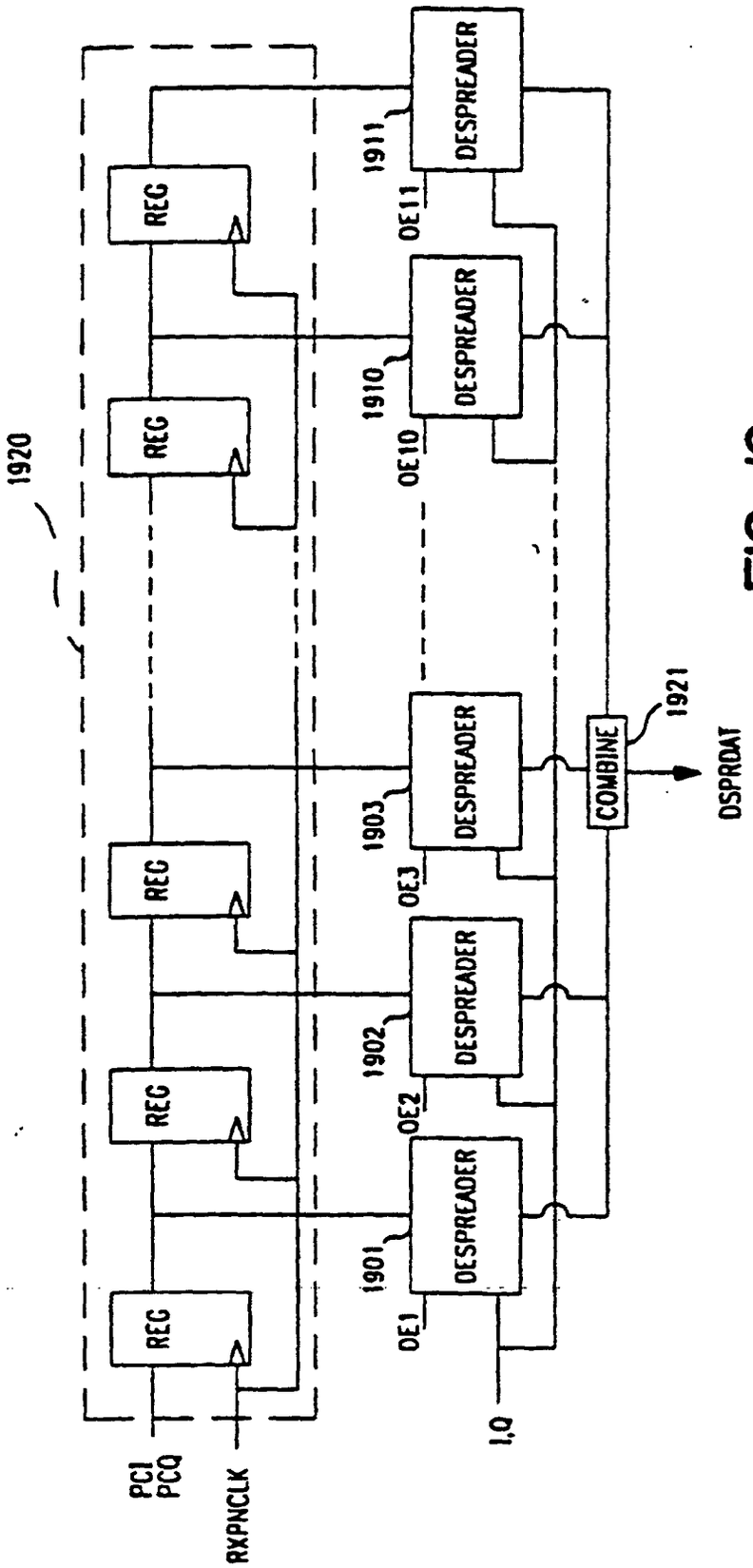

1920
REG
REG
REG
REG
REG
PCI
PCQ
RXPNCLK
DESPREADER
1911
OE11
DESPREADER
1910
OE10
DESPREADER
1903
OE3
DESPREADER
1902
OE2
DESPREADER
1901
OE1
I,Q
COMBINE
1921
DSPRDAT

FIG. 19

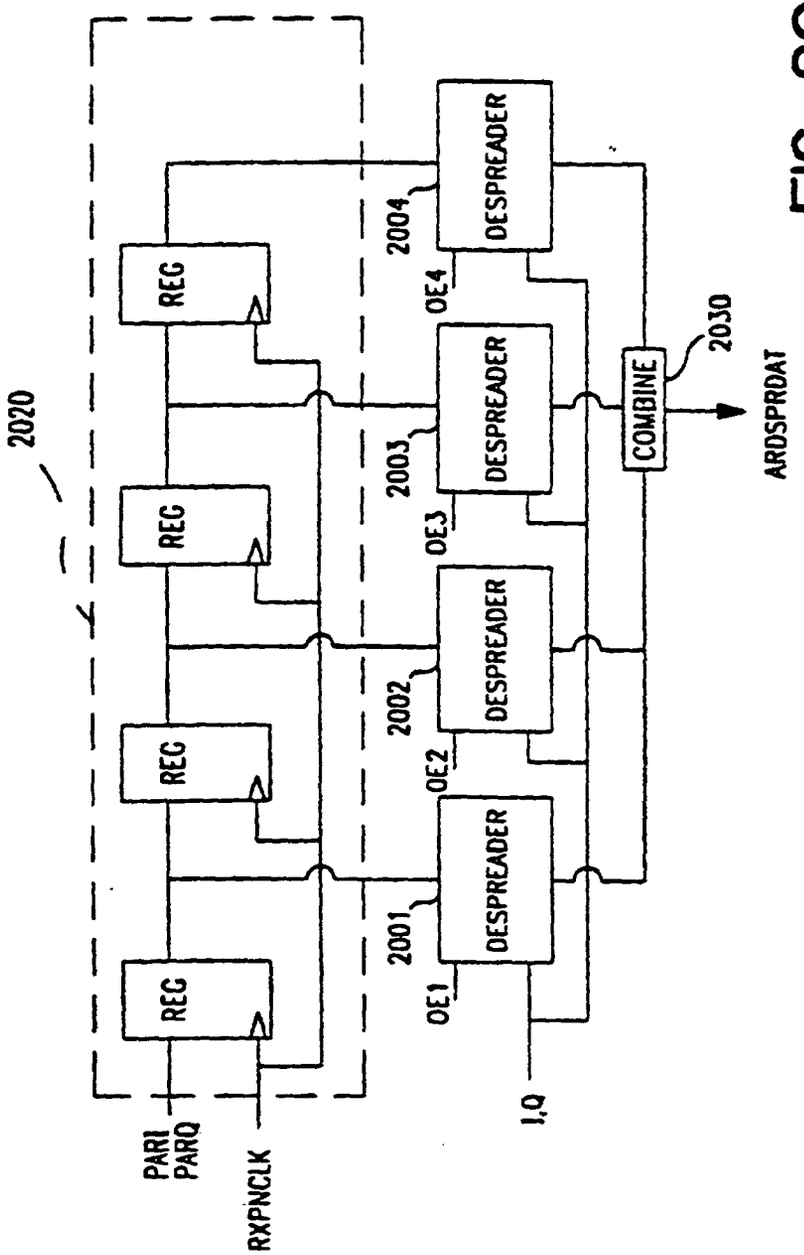
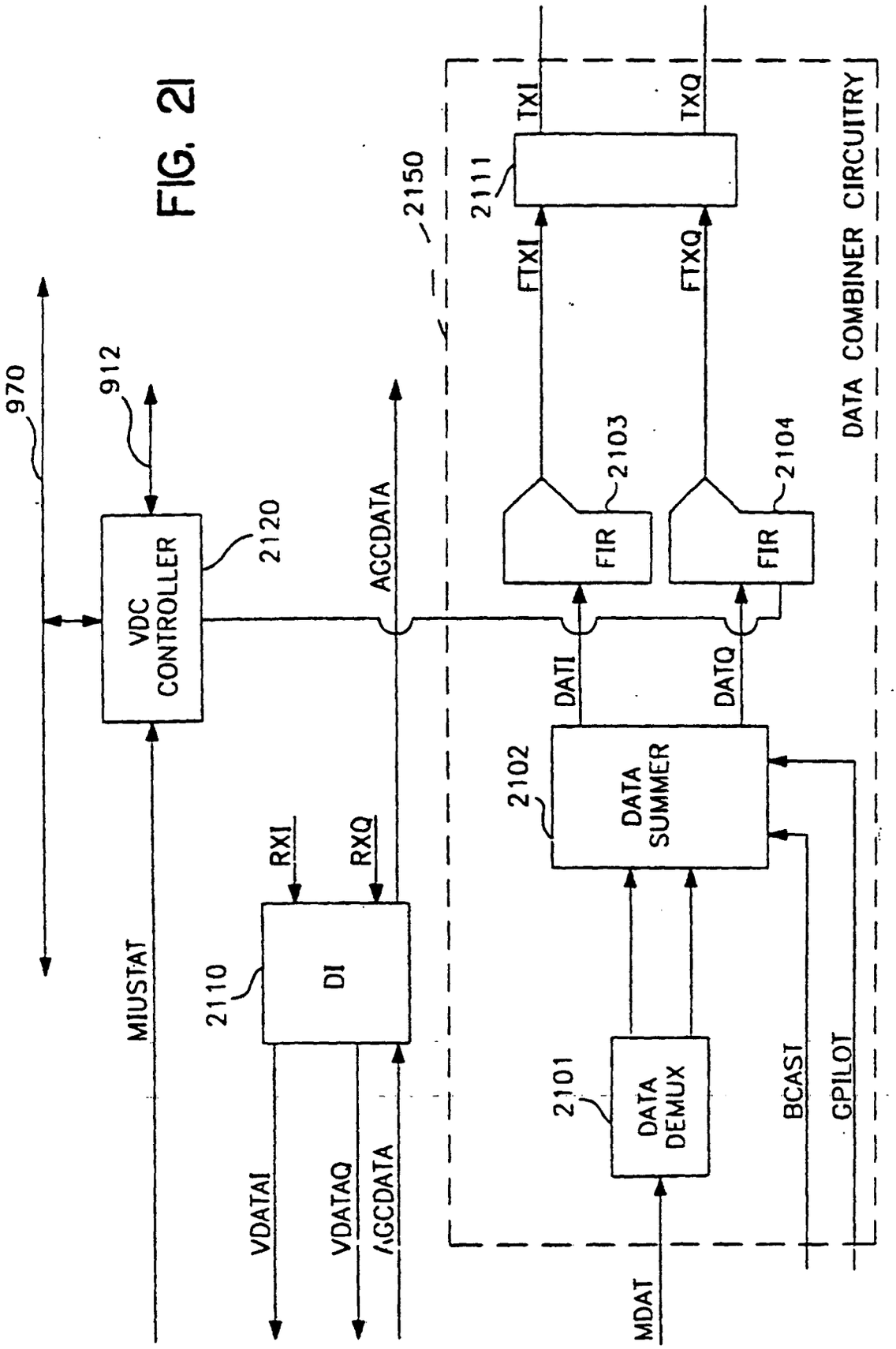

2020
REG
REG
REG
REG
PARI
PARQ
RXPNCLK
2004
2003
2002
2001
DESPREADER
DESPREADER
DESPREADER
DESPREADER
OE4
OE3
OE2
OE1
I,Q
COMBINE
2030
ARDSPRDAT

FIG. 20

FIG. 21


970
912
VDC CONTROLLER
2120
AGCDATA
2150
2111
TXI
TXQ
FTXI
FTXQ
2103
2104
FIR
FIR
DATA COMBINER CIRCUITRY
DATI
DATQ
2102
DATA SUMMER
RXI
RXQ
2110
DI
MIUSTAT
2101
DATA DEMUX
BCAST
CPILOT
VDATAI
VDATAQ
AGCDATA
MDAT

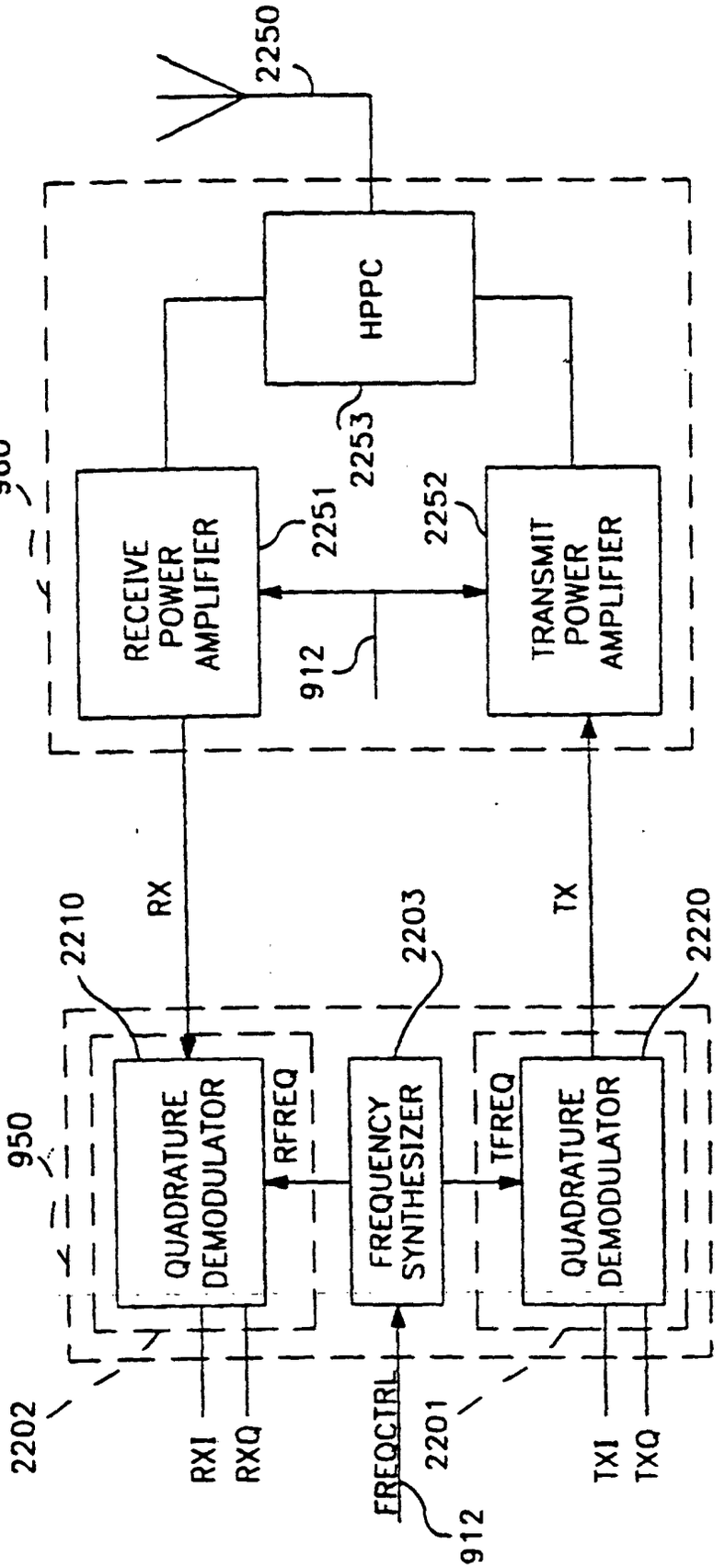

2250
HPPC
960
2253
2251
2252
RECEIVE POWER AMPLIFIER
TRANSMIT POWER AMPLIFIER
912
RX
TX
2210
2203
2220
950
QUADRATURE DEMODULATOR
RFREQ
FREQUENCY SYNTHESIZER
TFREQ
QUADRATURE DEMODULATOR
2202
2201
RXI
RXQ
FREQCTRL
912
TXI
TXQ

FIG. 22

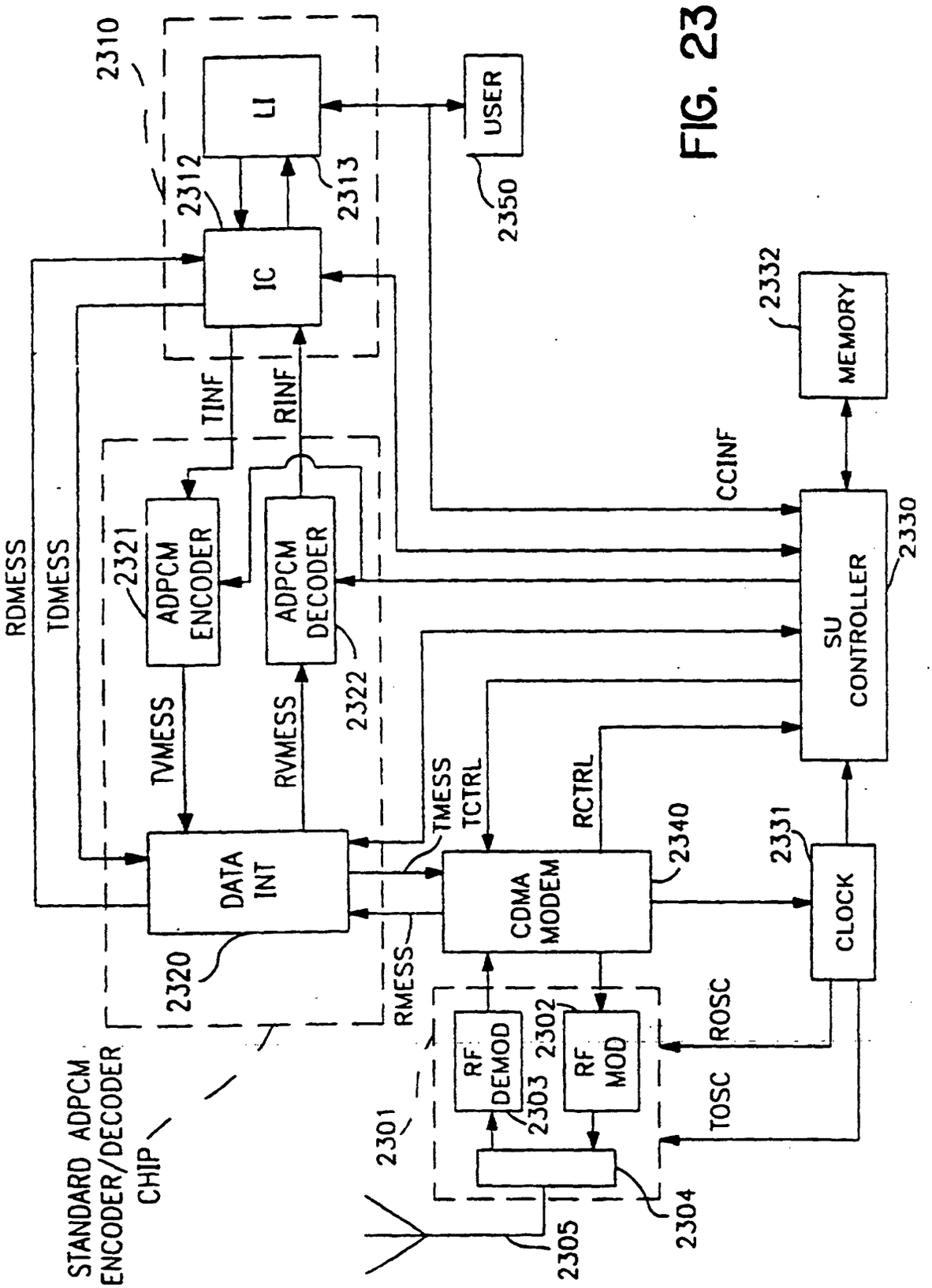

STANDARD ADPCM ENCODER/DECODER CHIP
2310
LI
2312
2313
IC
USER
2350
TINF
RINF
ADPCM ENCODER
2321
ADPCM DECODER
2322
RDMESS
TDMESS
TVMESS
RVMESS
DATA INT
2320
TMESS
TCTRL
RCTRL
CDMA MODEM
2340
RMESS
RF DEMOD
2303
RF MOD
2302
2301
2305
2304
ROSC
TOSC
CLOCK
2331
SU CONTROLLER
2330
CCINF
MEMORY
2332

FIG. 23

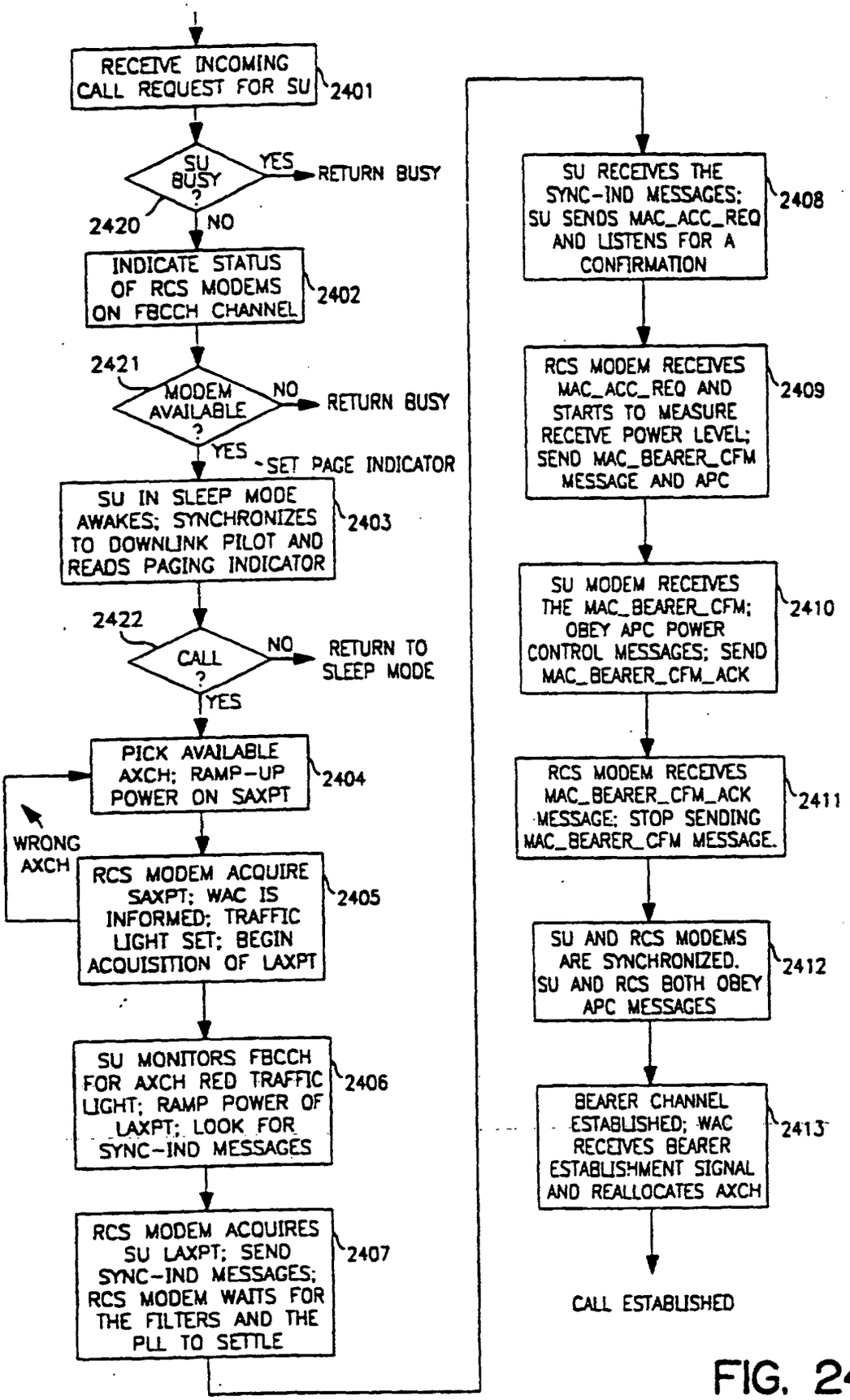

RECEIVE INCOMING CALL REQUEST FOR SU
2401
SU BUSY ?
YES
RETURN BUSY
2420
NO
INDICATE STATUS OF RCS MODEMS ON FBCCH CHANNEL
2402
2421
MODEM AVAILABLE ?
NO
RETURN BUSY
YES
SET PAGE INDICATOR
SU IN SLEEP MODE AWAKES; SYNCHRONIZES TO DOWNLINK PILOT AND READS PAGING INDICATOR
2403
2422
CALL ?
NO
RETURN TO SLEEP MODE
YES
PICK AVAILABLE AXCH; RAMP-UP POWER ON SAXPT
2404
WRONG AXCH
RCS MODEM ACQUIRE SAXPT; WAC IS INFORMED; TRAFFIC LIGHT SET; BEGIN ACQUISITION OF LAXPT
2405
SU MONITORS FBCCH FOR AXCH RED TRAFFIC LIGHT; RAMP POWER OF LAXPT; LOOK FOR SYNC-IND MESSAGES
2406
RCS MODEM ACQUIRES SU LAXPT; SEND SYNC-IND MESSAGES; RCS MODEM WAITS FOR THE FILTERS AND THE PLL TO SETTLE
2407
SU RECEIVES THE SYNC-IND MESSAGES; SU SENDS MAC_ACC_REQ AND LISTENS FOR A CONFIRMATION
2408
RCS MODEM RECEIVES MAC_ACC_REQ AND STARTS TO MEASURE RECEIVE POWER LEVEL; SEND MAC_BEARER_CFM MESSAGE AND APC
2409
SU MODEM RECEIVES THE MAC_BEARER_CFM; OBEY APC POWER CONTROL MESSAGES; SEND MAC_BEARER_CFM_ACK
2410
RCS MODEM RECEIVES MAC_BEARER_CFM_ACK MESSAGE; STOP SENDING MAC_BEARER_CFM MESSAGE.
2411
SU AND RCS MODEMS ARE SYNCHRONIZED. SU AND RCS BOTH OBEY APC MESSAGES
2412
BEARER CHANNEL ESTABLISHED; WAC RECEIVES BEARER ESTABLISHMENT SIGNAL AND REALLOCATES AXCH
2413
CALL ESTABLISHED

FIG. 24

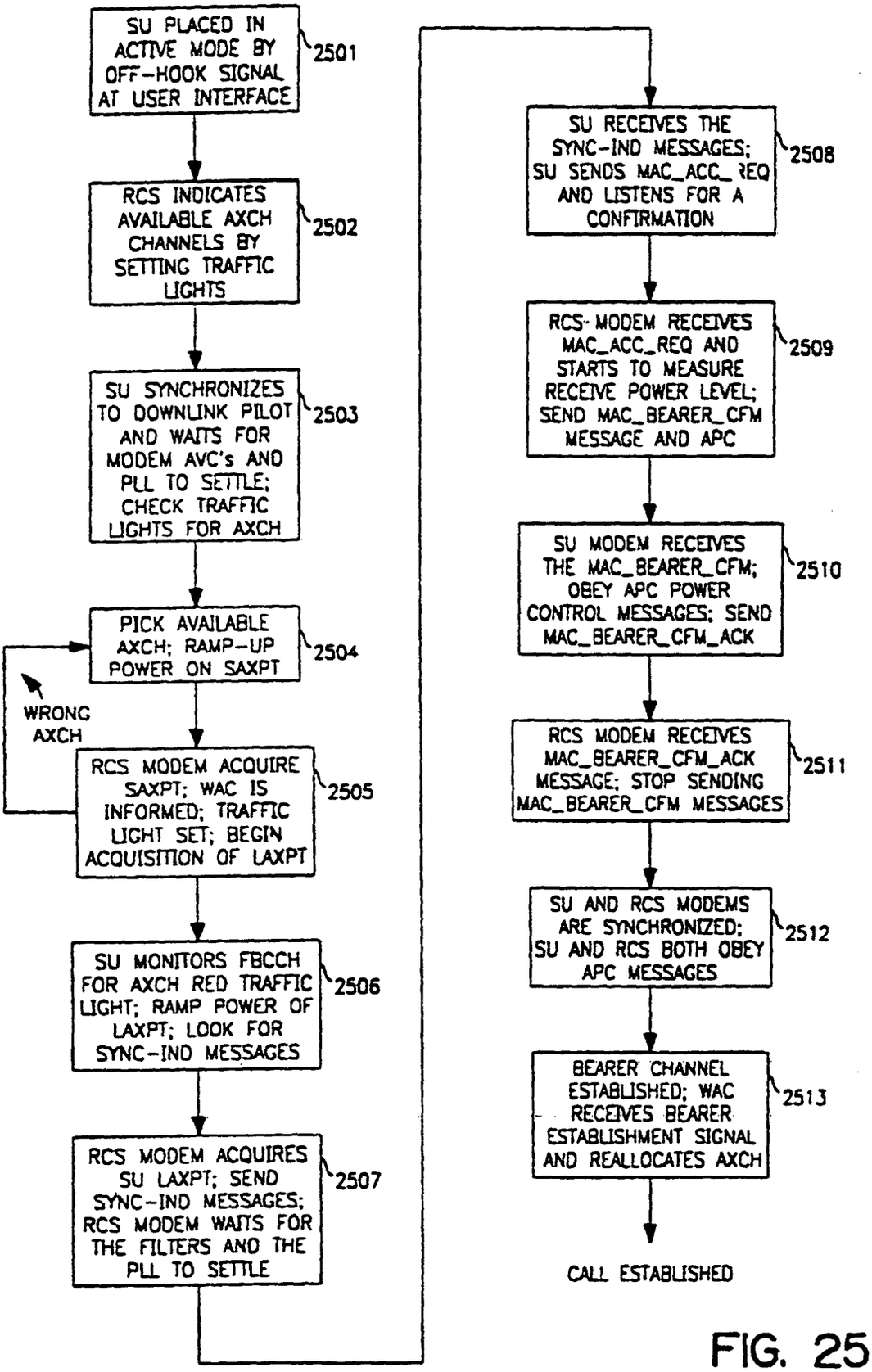

SU PLACED IN ACTIVE MODE BY OFF-HOOK SIGNAL AT USER INTERFACE
2501
RCS INDICATES AVAILABLE AXCH CHANNELS BY SETTING TRAFFIC LIGHTS
2502
SU SYNCHRONIZES TO DOWNLINK PILOT AND WAITS FOR MODEM AVC's AND PLL TO SETTLE; CHECK TRAFFIC LIGHTS FOR AXCH
2503
PICK AVAILABLE AXCH; RAMP-UP POWER ON SAXPT
2504
WRONG AXCH
RCS MODEM ACQUIRE SAXPT; WAC IS INFORMED; TRAFFIC LIGHT SET; BEGIN ACQUISITION OF LAXPT
2505
SU MONITORS FBCCH FOR AXCH RED TRAFFIC LIGHT; RAMP POWER OF LAXPT; LOOK FOR SYNC-IND MESSAGES
2506
RCS MODEM ACQUIRES SU LAXPT; SEND SYNC-IND MESSAGES; RCS MODEM WAITS FOR THE FILTERS AND THE PLL TO SETTLE
2507
SU RECEIVES THE SYNC-IND MESSAGES; SU SENDS MAC_ACC_REQ AND LISTENS FOR A CONFIRMATION
2508
RCS MODEM RECEIVES MAC_ACC_REQ AND STARTS TO MEASURE RECEIVE POWER LEVEL; SEND MAC_BEARER_CFM MESSAGE AND APC
2509
SU MODEM RECEIVES THE MAC_BEARER_CFM; OBEY APC POWER CONTROL MESSAGES; SEND MAC_BEARER_CFM_ACK
2510
RCS MODEM RECEIVES MAC_BEARER_CFM_ACK MESSAGE; STOP SENDING MAC_BEARER_CFM MESSAGES
2511
SU AND RCS MODEMS ARE SYNCHRONIZED; SU AND RCS BOTH OBEY APC MESSAGES
2512
BEARER CHANNEL ESTABLISHED; WAC RECEIVES BEARER ESTABLISHMENT SIGNAL AND REALLOCATES AXCH
2513
CALL ESTABLISHED

FIG. 25

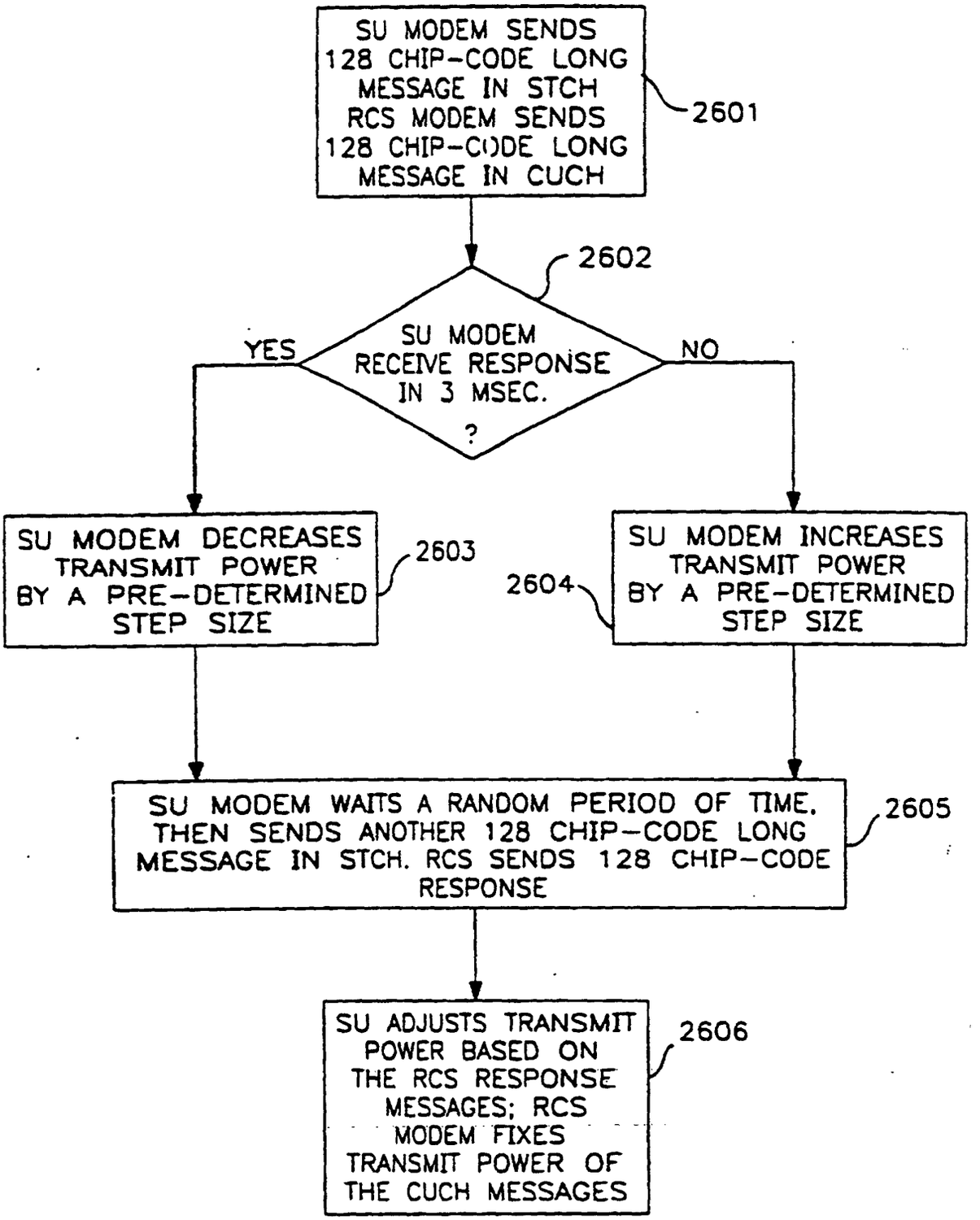

SU MODEM SENDS 128 CHIP-CODE LONG MESSAGE IN STCH RCS MODEM SENDS 128 CHIP-CODE LONG MESSAGE IN CUCH
2601
2602
SU MODEM RECEIVE RESPONSE IN 3 MSEC. ?
YES
NO
SU MODEM DECREASES TRANSMIT POWER BY A PRE-DETERMINED STEP SIZE
2603
2604
SU MODEM INCREASES TRANSMIT POWER BY A PRE-DETERMINED STEP SIZE
SU MODEM WAITS A RANDOM PERIOD OF TIME. THEN SENDS ANOTHER 128 CHIP-CODE LONG MESSAGE IN STCH. RCS SENDS 128 CHIP-CODE RESPONSE
2605
SU ADJUSTS TRANSMIT POWER BASED ON THE RCS RESPONSE MESSAGES; RCS MODEM FIXES TRANSMIT POWER OF THE CUCH MESSAGES
2606

FIG. 26

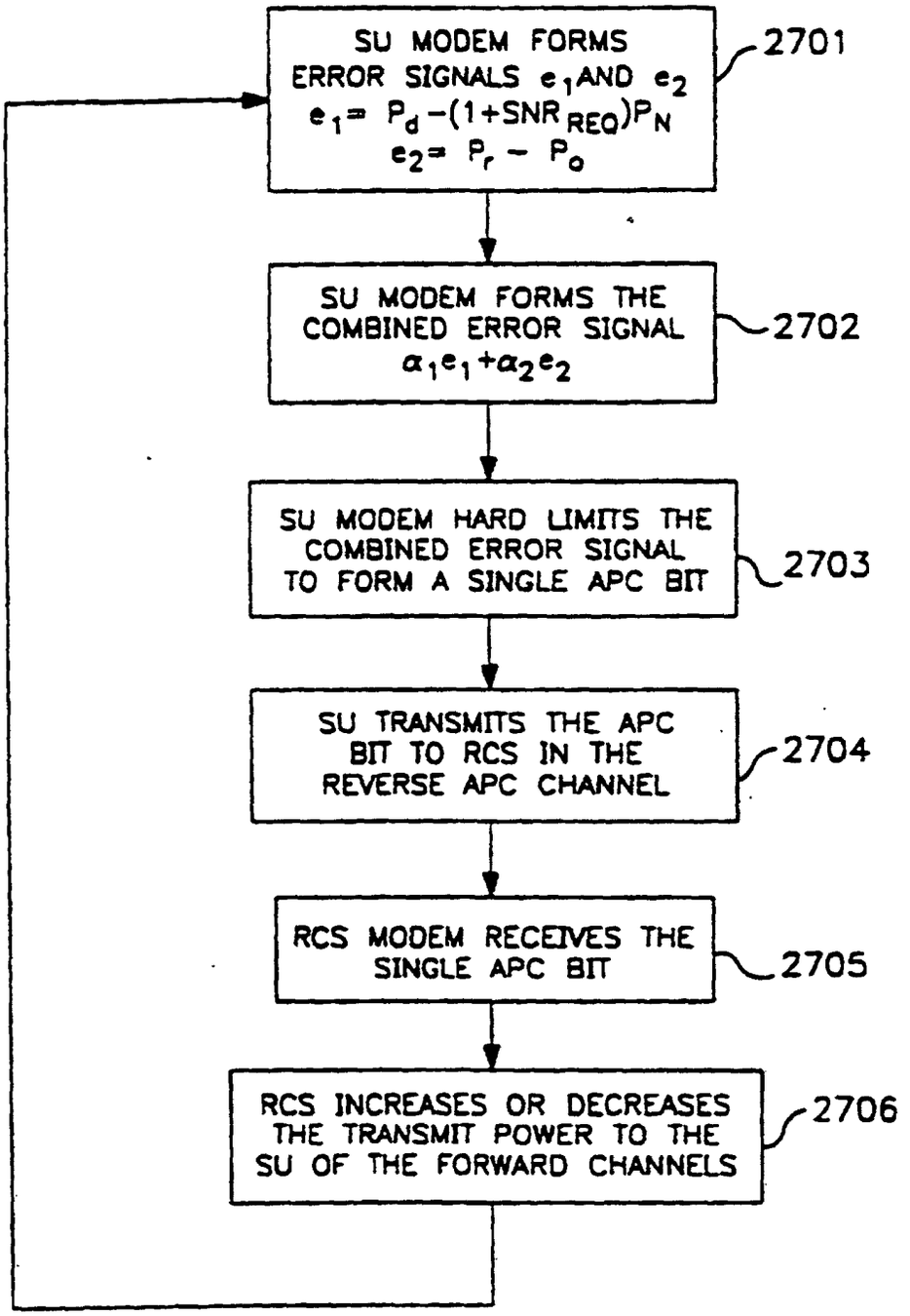

SU MODEM FORMS ERROR SIGNALS e_1 AND e_2
$e_1 = P_d - (1+SNR_{REQ})P_N$
$e_2 = P_r - P_o$
2701
SU MODEM FORMS THE COMBINED ERROR SIGNAL
$\alpha_1 e_1 + \alpha_2 e_2$
2702
SU MODEM HARD LIMITS THE COMBINED ERROR SIGNAL TO FORM A SINGLE APC BIT
2703
SU TRANSMITS THE APC BIT TO RCS IN THE REVERSE APC CHANNEL
2704
RCS MODEM RECEIVES THE SINGLE APC BIT
2705
RCS INCREASES OR DECREASES THE TRANSMIT POWER TO THE SU OF THE FORWARD CHANNELS
2706

FIG. 27

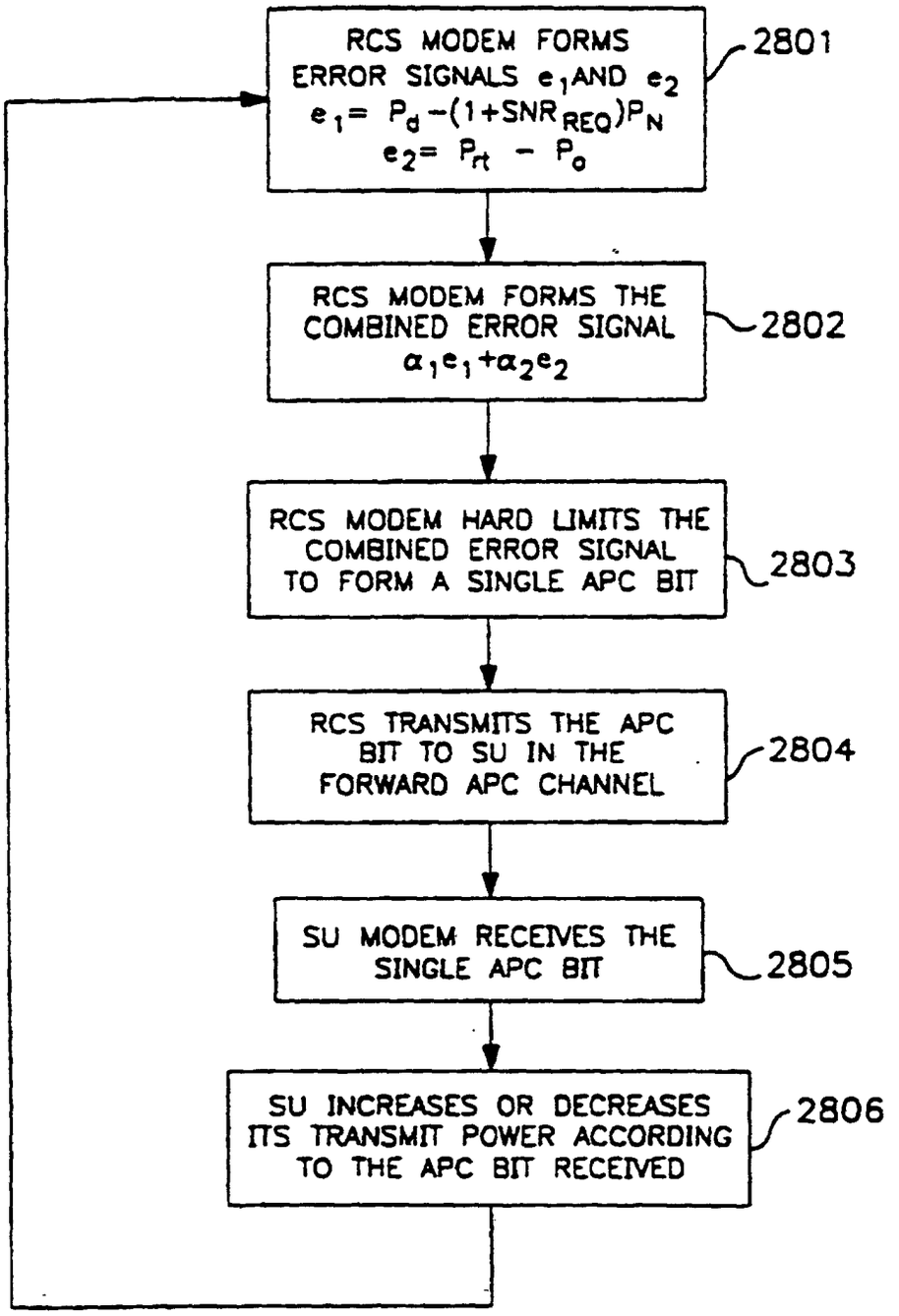

RCS MODEM FORMS ERROR SIGNALS e_1 AND e_2
$e_1 = P_d - (1+SNR_{REQ})P_N$
$e_2 = P_{rt} - P_o$
2801
RCS MODEM FORMS THE COMBINED ERROR SIGNAL
$\alpha_1 e_1 + \alpha_2 e_2$
2802
RCS MODEM HARD LIMITS THE COMBINED ERROR SIGNAL TO FORM A SINGLE APC BIT
2803
RCS TRANSMITS THE APC BIT TO SU IN THE FORWARD APC CHANNEL
2804
SU MODEM RECEIVES THE SINGLE APC BIT
2805
SU INCREASES OR DECREASES ITS TRANSMIT POWER ACCORDING TO THE APC BIT RECEIVED
2806

FIG. 28

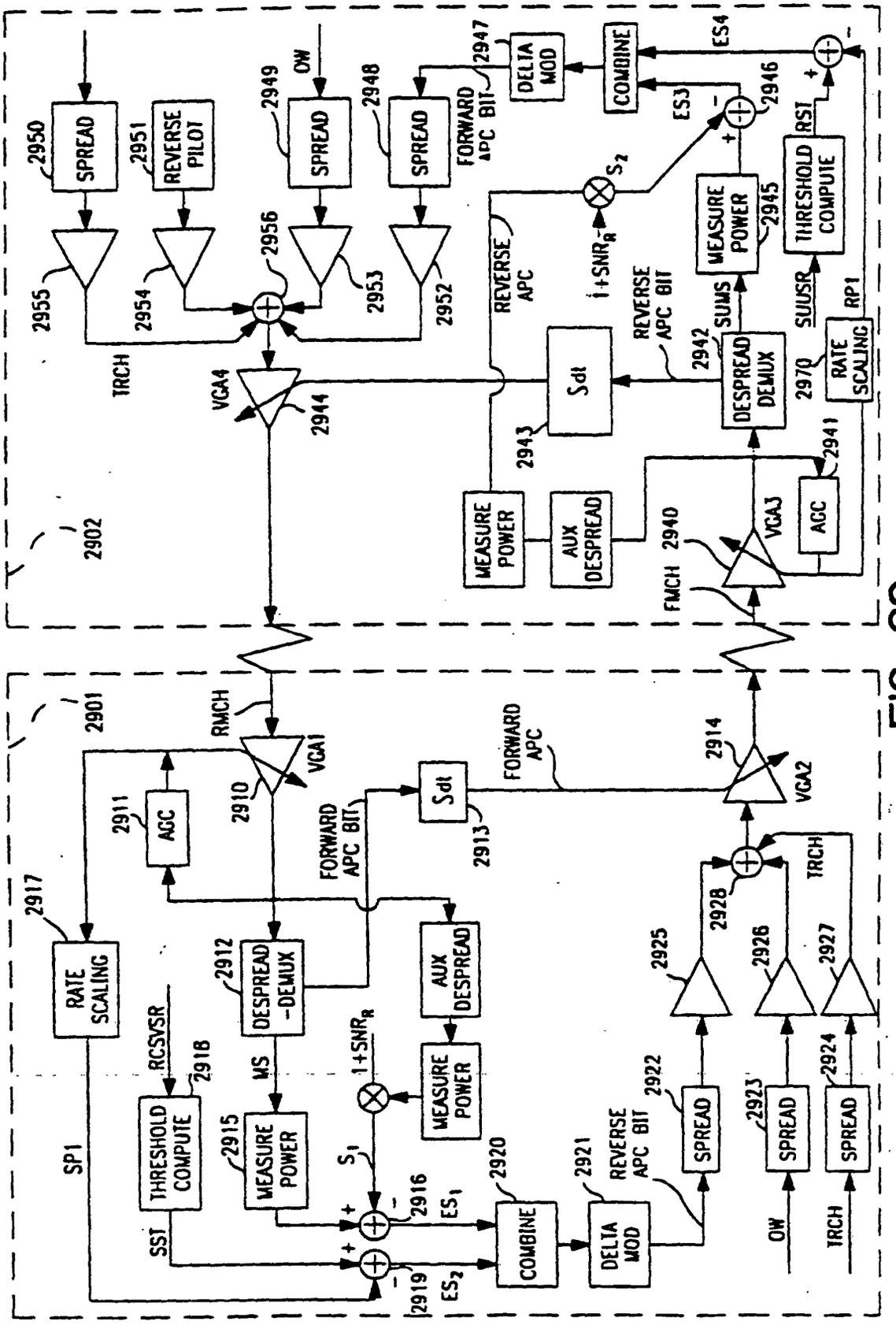

2902
2901
2950
SPREAD
2951
REVERSE PILOT
2949
OW
SPREAD
2948
SPREAD
2947
FORWARD APC BIT
DELTA MOD
COMBINE
ES4
2955
2954
2956
2953
2952
TRCH
VGA4
2944
REVERSE APC
S_2
$1+SNR_R$
ES3
2946
MEASURE POWER
2945
THRESHOLD COMPUTE
RSI
SUUS
SUUSR
RP1
2942
DESPREAD DEMUX
2970
RATE SCALING
Sdt
2943
REVERSE APC BIT
MEASURE POWER
AUX DESPREAD
FMCH
2940
VGAJ
AGC
2941
RMCH
VGA1
2910
2911
AGC
FORWARD APC BIT
Sdt
2913
FORWARD APC
2914
VGA2
2917
RATE SCALING
2912
DESPREAD -DEMUX
AUX DESPREAD
2928
TRCH
2925
2926
2927
RCSYSR
2918
MS
$1+SNR_R$
MEASURE POWER
SP1
THRESHOLD COMPUTE
2915
S_1
2916
ES_1
2920
COMBINE
2921
REVERSE APC BIT
DELTA MOD
2922
SPREAD
2923
SPREAD
2924
SPREAD
SSI
2919
ES_2
OW
TRCH

FIG. 29

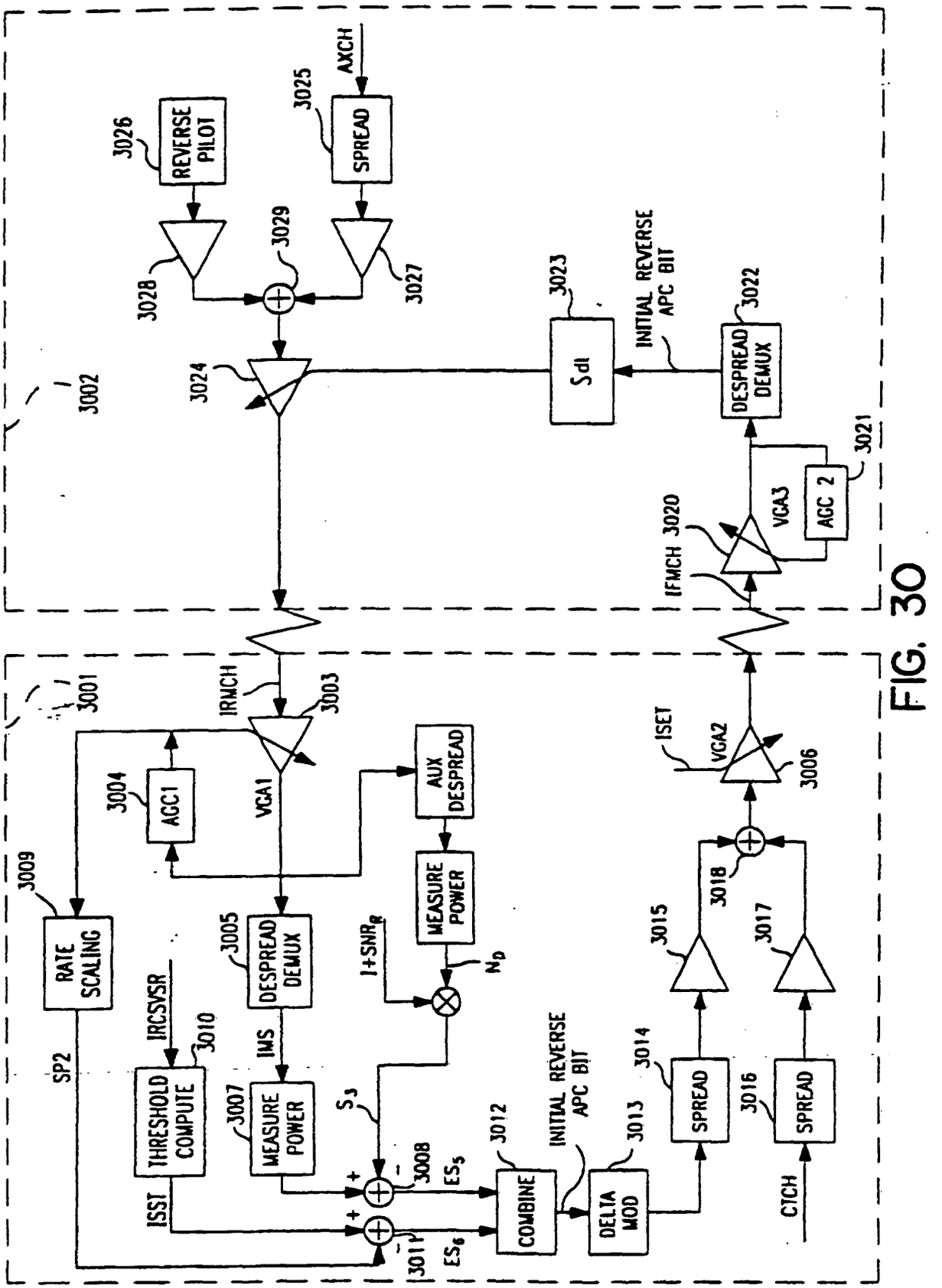

3002
3026
REVERSE PILOT
3025
AXCH
SPREAD
3028
3029
3027
3024
3023
Sdl
INITIAL REVERSE APC BIT
3022
DESPREAD DEMUX
3021
AGC 2
VGA3
3020
IFMCH
3001
IRMCH
3003
3004
AGC1
VGA1
AUX DESPREAD
MEASURE POWER
3009
RATE SCALING
3005
DESPREAD DEMUX
I+SNR_R
N_D
IRCSYSR
3010
SP2
IMS
THRESHOLD COMPUTE
3007
MEASURE POWER
S_3
3008
ES_5
3012
INITIAL REVERSE APC BIT
3013
ISST
3011
ES_6
COMBINE
DELTA MOD
3014
3015
SPREAD
3018
ISET
VGA2
3006
3016
3017
SPREAD
CTCH

FIG. 30