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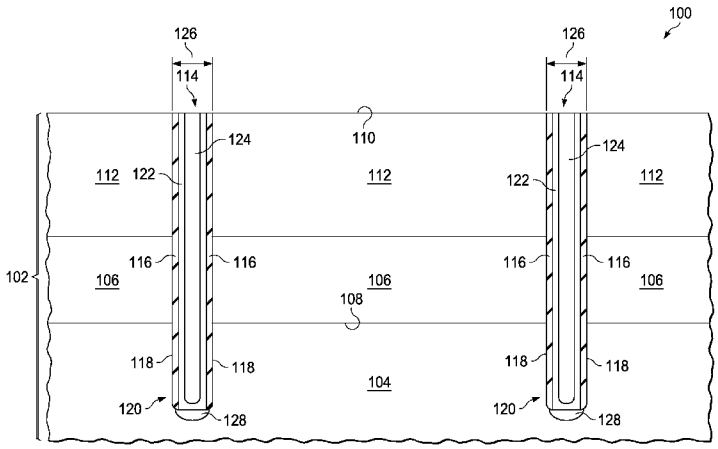

FIG. 1

(57) Abstract: A semiconductor device (100) is formed by forming a deep trench (120) in a substrate (102) and a dielectric liner (116) on sidewalls (118) of the deep trench (120). A first undoped polysilicon layer (122) is formed on the semiconductor device (100), extending into the deep trench (120) on the dielectric liner (116), but not filling the deep trench (120). Dopants are implanted into the first polysilicon layer (122). A second layer of polysilicon (124) is formed on the first layer of polysilicon (122). A thermal drive anneal activates and diffuses the dopants. In one version, the dielectric liner (116) is removed at the bottom of the deep trench (120) before the first polysilicon layer (122) is formed, so that the polysilicon (122) in the deep trench (120) provides a contact to the substrate (102). In another version, the polysilicon (122) in the deep trench (120) is isolated from the substrate (102) by the dielectric liner (116).

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POLY SANDWICH FOR DEEP TRENCH FILL

[0001] This relates generally to semiconductor devices, and more particularly to deep trench structures in semiconductor devices.

BACKGROUND

[0002] A semiconductor device has a deep trench structure with a dielectric liner on sidewalls of the deep trench and doped polycrystalline silicon (polysilicon) on the dielectric liner filling the deep trench. Attaining a desirably low sheet resistance in the polysilicon in the deep trench requires in situ doping as the polysilicon is deposited, which undesirably causes dopant contamination on the backside of the substrate of the semiconductor device and stress in the semiconductor device after the deposited polysilicon is annealed. Both undesirable effects can degrade performance and reliability of the semiconductor device. Alternatively, undoped polysilicon may be deposited and implanted at the top surface of the semiconductor device, requiring a long thermal drive to attain a desired uniformity of dopant distribution in the deep trench, which may be over 20 microns deep. The long thermal drive adversely affects doped structures in the substrate, such as buried layers.

SUMMARY

[0003] A semiconductor device is formed by forming a deep trench in a substrate of the semiconductor device. A dielectric liner is formed on sidewalls of the deep trench. A first undoped polysilicon layer is formed on the semiconductor device, extending into the deep trench on the dielectric liner, but not filling the deep trench. Dopants are implanted into the first polysilicon layer. A second layer of polysilicon is formed on the first layer of polysilicon. A thermal drive anneal activates and diffuses the dopants. Polysilicon of the first layer of polysilicon and second layer of polysilicon is removed from over a top surface of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a cross section of an example semiconductor device.

[0005] FIG. 2A through FIG. 2J are cross sections of the semiconductor device of FIG. 1, depicted in successive stages of fabrication.

[0006] FIG. 3 is a cross section of another example semiconductor device.

[0007] FIG. 4A and FIG. 4B are cross sections of the semiconductor device of FIG. 3, depicted in successive stages of fabrication.

[0008] FIG. 5 is a cross section of an alternate semiconductor device containing a buried layer and deep trench structures with a self-aligned sinker to the buried layer.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0009] The following co-pending patent applications are related and hereby incorporated herein by reference: Application No. US 14/555,209; Application No. US 14/555,330; and Application No. US 14/555,359.

[0010] The figures are not drawn to scale. Some acts may occur in different orders and/or concurrently with other acts or events. Furthermore, not all illustrated acts or events are required to implement a methodology in accordance with example embodiments.

[0011] A semiconductor device is formed by forming a deep trench at least 10 microns deep in a substrate of the semiconductor device. A dielectric liner is formed on sidewalls of the deep trench. A first undoped polysilicon layer is formed on the semiconductor device, extending into the deep trench on the dielectric liner, but not filling the deep trench. Dopants are implanted into the first polysilicon layer. A second undoped layer of polysilicon is formed on the first layer of polysilicon. A thermal drive anneal activates the dopants and diffuses them throughout the first and second polysilicon layers. Polysilicon of the first layer of polysilicon and second layer of polysilicon is removed from over a top surface of the substrate. In one example, dielectric material of the dielectric liner may be removed at a bottom of the deep trench, so as to expose the substrate. The first layer of polysilicon then makes an electrical connection to the substrate at the bottom of the deep trench, such as to a region under a buried layer. In another example, the first layer of polysilicon is electrically isolated from the substrate at the bottom of the deep trench by the dielectric liner. The isolated polysilicon in the deep trench may provide a resistor or capacitor of the semiconductor device.

[0012] For the purposes of this disclosure, the term undoped as applied to forming a layer of polysilicon on a semiconductor device means that at most an insignificant amount of dopants are included in reactant gases to form the polysilicon layer. Some dopants already present in the semiconductor device may diffuse into the polysilicon layer as the polysilicon layer is formed, but this does not negate the undoped nature of the formation of the polysilicon layer.

[0013] FIG. 1 is a cross section of an example semiconductor device 100, which is formed in a

substrate 102 including semiconductor material 104, such as p-type silicon. A buried layer 106, such as an n-type buried layer 106, may be disposed in the substrate 102, so that a bottom surface 108 of the buried layer 106 is more than 10 microns below a top surface 110 of the substrate 102. The substrate 102 may include an upper layer 112 over the buried layer 106, such as a p-type epitaxial layer 112. In this example, the semiconductor material 104 below the buried layer 106 may be electrically isolated from the upper layer 112 by the buried layer 106.

[0014] The semiconductor device 100 includes one or more deep trench structures 114, which extend at least 10 microns deep in the substrate 102. Each deep trench structure 114 includes a dielectric liner 116 on sidewalls 118 of a deep trench 120 of the deep trench structure 114. A first layer of polysilicon 122 is disposed on the dielectric liner 116, extending to a bottom of the deep trench structure 114. A second layer of polysilicon 124 is disposed on the first layer of polysilicon 122, and extends into the deep trench 120. Dopants are distributed in the first layer of polysilicon 122 and the second layer of polysilicon 124 with an average doping density of at least 1×10^{18} cm^{-3}. A width 126 of the deep trench structure 114 is 1.5 microns to 3.5 microns.

[0015] In this example, dielectric material of the dielectric liners 116 is removed at bottoms of the deep trench structures 114, and contact regions 128 are disposed in the substrate 102 at the bottoms of the deep trench structures 114, so that the first layer of polysilicon 122 makes electrical connections to the substrate 102 through the contact regions 128. The contact regions 128 may have an average doping density of at least 5×10^{18} cm^{-3}. The deep trench structures 114 thus provides electrical connections from the top surface 110 of the substrate 102 to the semiconductor material 104 below the buried layer 106 with an advantageously low resistance due to the average doping density of at least 5×10^{18} cm^{-3}. The deep trench structures 114 may have a closed-loop configuration, so as to surround and thus isolate a portion of the upper layer 112 and a component of the semiconductor device 100 in the upper layer 112 portion.

[0016] FIG. 2A through FIG. 2J are cross sections of the semiconductor device of FIG. 1, depicted in successive stages of fabrication. Referring to FIG. 2A, the buried layer 106 and the upper layer 112 are formed on the semiconductor material 104. The buried layer 106 and the upper layer 112 may be formed by implanting n-type dopants into the p-type semiconductor material 104, followed by a thermal drive anneal and a subsequent epitaxial process to grow the p-type upper layer 112, so that the buried layer 106 is formed by diffusion and activation of the implanted n-type dopants.

[0017] A layer of pad oxide 130 is formed at the top surface 110 of the substrate, such as by thermal oxidation. The layer of pad oxide 130 may include 5 nanometers to 30 nanometers of silicon dioxide. A layer of pad nitride 132 is formed on the layer of pad oxide 130, such as by low pressure chemical vapor deposition (LPCVD) using ammonia and silane. The layer of pad nitride 132 may include 100 nanometers to 300 nanometers of silicon nitride. A layer of hard mask oxide 134 is formed over the layer of pad nitride 132, such as by a plasma enhanced chemical vapor deposition (PECVD) using tetraethyl orthosilicate, also called tetraethoxysilane (TEOS), or using a high density plasma (HDP) process. The layer of hard mask oxide 134 may include 500 nanometers to 2 microns of silicon dioxide. The layer of pad nitride 132 provides an etch stop layer for subsequent etching of the layer of hard mask oxide 134.

[0018] A trench mask 136 is formed over the layer of hard mask oxide 134, so as to expose areas for the deep trench structures 114 of FIG. 1. The trench mask 136 may include photoresist formed by a photolithographic process, and may further include a hard mask layer and/or an anti-reflection layer.

[0019] Referring to FIG. 2B, a hard mask etch process removes material from the layer of hard mask oxide 134 in the areas exposed by the trench mask 136. Subsequently, a stop layer etch process removes the layer of pad nitride 132 and the layer of pad oxide 130 in the areas exposed by the trench mask 136. A trench etch process removes material from the substrate 102 in the areas exposed by the trench mask 136 to form the deep trenches 120, which extend to below the bottom surface of the buried layer 106. In examples, the deep trenches 120 may be 12 microns to 35 microns deep. A significant portion, as depicted in FIG. 2B, and possibly all of the trench mask 136, and possibly a portion of the layer of hard mask oxide 134, may be eroded by the trench etch process. Any remaining trench mask 136 is removed after the deep trenches 120 are formed.

[0020] Referring to FIG. 2C, a layer of thermal oxide 138 is formed on the sidewalls 118 and bottoms of the deep trenches 120. In examples, the layer of thermal oxide 138 may be 50 nanometers to 400 nanometers thick. A layer of silicon dioxide 140 is formed on the layer of thermal oxide 138, such as by a sub-atmospheric chemical vapor deposition (SACVD) process. In examples, the layer of silicon dioxide 140 may be 50 nanometers to 500 nanometers thick. The layer of thermal oxide 138 combined with the layer of silicon dioxide 140 provide the dielectric liner 116.

[0021] Referring to FIG. 2D, the dielectric liner 116 is removed at bottoms of the deep trenches 120, so as to expose the semiconductor material 104. The dielectric material may be removed, such as by a reactive ion etch (RIE) process using fluorine radicals, which leaves the dielectric liner 116 on the sidewalls 118 substantially intact.

[0022] Referring to FIG. 2E, p-type dopants 142 are implanted into the exposed semiconductor material 104 at the bottoms of the deep trenches 120 to form the contact regions 128. The dopants 142 are selected, so that the contact regions 128 are the same conductivity type as the semiconductor material 104. In this example, the semiconductor material 104 is p-type, and the dopants 142 include boron. The dopants 142 may be implanted at an example dose of 2×10^{14} cm^{-2} to 2×10^{15} cm^{-2} at a tilt angle of substantially zero degrees.

[0023] Referring to FIG. 2F, the first layer of polysilicon 122 is formed on the existing semiconductor device 100, extending into the deep trenches 120 and making electrical contacts to the contact regions 128. The first layer of polysilicon 122 may have a thickness of 150 nanometers to 200 nanometers, so as not to fill the deep trenches 120. In examples, the first layer of polysilicon 122 may be formed at a temperature of about 620 °C by providing 500 standard cubic centimeters per minute (sccm) to 600 sccm of silane gas (SiH_4) at a pressure of about 200 millitorr. The first layer of polysilicon 122 is substantially undoped as formed, which advantageously reduces doping contamination of a backside of the substrate 102 compared to processes using doped polysilicon.

[0024] Referring to FIG. 2G, p-type dopants 144 are implanted into the first layer of polysilicon 122 at an example dose of 1×10^{15} cm^{-2} to 1×10^{16} cm^{-2} in 4 sub-doses at tilt angles of about zero degrees and twist angles of about 45 degrees. Alternatively, the p-type dopants 144 may implanted in 4 sub-doses at tilt angles of about 1 degree to 2 degrees and twist angles of about zero degrees. The p-type dopants 144 may include boron, which advantageously has a higher diffusion coefficient than other common p-type dopants, such as gallium and indium. The total dose of the p-type dopants 144 may be selected based on depths and widths of the deep trenches 120 to provide desired sheet resistance values in the first layer of polysilicon 122 and subsequently-formed second layer of polysilicon 124.

[0025] Referring to FIG. 2H, the second layer of polysilicon 124 is formed on the first layer of polysilicon 122, extending into the deep trenches 120. The second layer of polysilicon 124 may have a thickness of 800 nanometers to 1.5 microns, and may substantially fill the deep trenches

120. The second layer of polysilicon 124 may be formed using similar process conditions as described for the first layer of polysilicon 122 in reference to FIG. 2F. The second layer of polysilicon 124 is substantially undoped as formed, which also advantageously reduces doping contamination of a backside of the substrate 102 compared to processes using doped silicon layers.

[0026] Referring to FIG. 2I, a thermal drive anneal 146 heats the substrate 102, so as to activate the implanted dopants 144 of FIG. 2G, and to diffuse the implanted dopants 144 throughout the first layer of polysilicon 122 and the second layer of polysilicon 124. The thermal drive anneal may be a furnace anneal at 1000 °C to 1100 °C for 100 minutes to 150 minutes in a nitrogen ambient. The thermal drive anneal advantageously provides a desired uniformity of the implanted dopants 144 in the first layer of polysilicon 122 and the second layer of polysilicon 124.

[0027] Referring to FIG. 2J, the second layer of polysilicon 124, the first layer of polysilicon 122, the layer of hard mask oxide 134 of FIG. 2I, and a portion of the layer of pad nitride 132 are removed using a chemical mechanical polish (CMP) process 148 depicted in FIG. 2J as a CMP pad 148. The remaining layer of pad nitride 132, and the layer of pad oxide 130 are subsequently removed to provide the structure of FIG. 1. Alternatively, the layer of pad oxide 130 may be left in place during subsequent implants and anneals, and removed later in the fabrication process.

[0028] In an alternate version of this example, an analogous semiconductor device with n-type semiconductor material in the substrate may be formed by implanting n-type dopants, such as phosphorus, into the first layer of polysilicon. The resulting deep trench structure provides an electrical connection from a top surface of the semiconductor device to the n-type semiconductor material in the substrate.

[0029] FIG. 3 is a cross section of another example semiconductor device 300, which is formed in a substrate 302 including semiconductor material 304, such as silicon. The semiconductor device 300 includes one or more deep trench structures 314, which extend at least 10 microns below a top surface 310 of the substrate 302. Each deep trench structure 314 includes a dielectric liner 316 on sidewalls 318 and a bottom of a deep trench 320 of the deep trench structure 314. A first layer of polysilicon 322 is disposed on the dielectric liner 316, extending to a bottom of the deep trench structure 314. A second layer of polysilicon 324 is

disposed on the first layer of polysilicon 322. Dopants are distributed in the first layer of polysilicon 322 and the second layer of polysilicon 324 with an average doping density of at least 1×10^{18} cm^{-3}. A width 326 of the deep trench structure 314 is 1.5 microns to 3.5 microns.

[0030] In this example, the dielectric liner 316 isolates the first layer of polysilicon 322 from the substrate 302. The deep trench structures 314 may provide resistors or capacitors, which advantageously do not occupy much surface space of the semiconductor device 300, enabling a reduced size and hence lower fabrication costs.

[0031] FIG. 4A and FIG. 4B are cross sections of the semiconductor device of FIG. 3, depicted in successive stages of fabrication. Referring to FIG. 4A, a layer of pad oxide 330 is formed at the top surface 310 of the substrate. A layer of pad nitride 332 is formed on the layer of pad oxide 330. A layer of hard mask oxide 334 is formed over the layer of pad nitride 332. The layer of hard mask oxide 334, the layer of pad nitride 332 and the layer of pad oxide 330 may be formed as described in reference to FIG. 2A. Deep trenches 320 are formed through the layer of hard mask oxide 334, the layer of pad nitride 332 and the layer of pad oxide 330, and into the substrate 302 at least 10 microns. In examples, the deep trenches 320 may be 12 microns to 35 microns deep. The deep trenches 320 may be formed as described in reference to FIG. 2B. The dielectric liner 316 is formed over the layer of hard mask oxide 334 and extending onto the sidewalls 318 of the deep trenches 320. The dielectric liner may include a layer of thermal oxide and a layer of deposited oxide, as described in reference to FIG. 2C, or may be formed by other methods. The first layer of polysilicon 322 is formed on the dielectric liner 316, extending into (but not filling) the deep trenches 320. The first layer of polysilicon 322 may have a thickness of 150 nanometers to 200 nanometers . The first layer of polysilicon 322 is substantially undoped, accruing the advantage discussed in reference to FIG. 2F, and may be formed as described in reference to FIG. 2F. Dopants 344 are implanted into the first layer of polysilicon 322 at an example dose of 2×10^{15} cm^{-2} to 1×10^{16} cm^{-2} in 4 sub-doses at tilt angles of 1 degree to 2 degrees and twist angles of about zero degrees. The dopants 344 may be p-type dopants and include boron, or may be n-type dopants and include phosphorus and/or possibly arsenic. The total dose of the dopants 344 may be selected based on depths and widths of the deep trenches 320 to provide desired sheet resistance values in the first layer of polysilicon 322 and subsequently-formed second layer of polysilicon 324.

[0032] Referring to FIG. 4B, the second layer of polysilicon 324 is formed on the first layer of

polysilicon 322, extending into the deep trenches 320. The second layer of polysilicon 324 may have a thickness of 800 nanometers to 1.5 microns, and may substantially fill the deep trenches 320. The second layer of polysilicon 324 may be formed using similar process conditions as described in reference to FIG. 2F. The second layer of polysilicon 324 is substantially undoped as formed, accruing the advantage discussed in reference to FIG. 2H. A thermal drive anneal 346 heats the substrate 302, so as to activate the implanted dopants 344 of FIG. 4A, and to diffuse the implanted dopants 344 throughout the first layer of polysilicon 322 and the second layer of polysilicon 324. The thermal drive anneal may be similar to that discussed in reference to FIG. 2I, and advantageously provides a desired uniformity of the implanted dopants 344 in the first layer of polysilicon 322 and the second layer of polysilicon 324. Formation of the first layer of polysilicon 322 and the second layer of polysilicon 324 as undoped layers accrues the advantage discussed in reference to FIG. 2I. The second layer of polysilicon 324, the first layer of polysilicon 322, the layer of hard mask oxide 334, and a portion of the layer of pad nitride 332 are removed using a CMP process. The remaining layer of pad nitride 332, and the layer of pad oxide 330 are subsequently removed to provide the structure of FIG. 3.

[0033] FIG. 5 is a cross section of an alternate semiconductor device containing a buried layer and deep trench structures with a self-aligned sinker to the buried layer. The semiconductor device 500 is formed in a substrate 502 including a p-type base semiconductor layer 504 of semiconductor material, an n-type buried layer 506 of semiconductor material and a p-type upper semiconductor layer 512 extending to a top surface 510 of the substrate 502. The p-type base semiconductor layer 504 may be an epitaxial semiconductor layer with a resistivity of 5 ohm-cm to 10 ohm-cm. The p-type upper semiconductor layer 512 may also be an epitaxial semiconductor layer with a resistivity of 5 ohm-cm to 10 ohm-cm. The n-type buried layer 506 may include a main layer 548, which straddles the boundary between the base semiconductor layer 504 and the upper semiconductor layer 512, extending at least a micron into the base semiconductor layer 504 and at least a micron into the upper semiconductor layer 512. The n-type buried layer 506 may also include a lightly-doped layer 550 extending at least 2 microns below the main layer 548, disposed in the base semiconductor layer 504. The n-type buried layer 506 may be formed as described in Application No. US 14/555,330.

[0034] The semiconductor device 500 includes one or more deep trench structures 514, which extend at least 10 microns deep in the substrate 502. Each deep trench structure 514 includes a

dielectric liner 516 on sidewalls 518 of a deep trench 520 of the deep trench structure 514. A first layer of polysilicon 522 is disposed on the dielectric liner 516, extending to a bottom of the deep trench structure 514. A second layer of polysilicon 524 is disposed on the first layer of polysilicon 522, and extends into the deep trench 520. Dopants are distributed in the first layer of polysilicon 522 and the second layer of polysilicon 524 with an average doping density of at least 1×10^{18} cm^{-3}. The trench structures 514 may be formed as described in any of the examples herein.

[0035] In this example, dielectric material of the dielectric liners 516 is removed at bottoms of the deep trench structures 514, and contact regions 528 are disposed in the substrate 502 at the bottoms of the deep trench structures 514, so that the first layer of polysilicon 522 makes electrical connections to the substrate 502 through the contact regions 528. The contact regions 528 and the method of removing the dielectric liners 516 at the bottom of each deep trench structure 514 may be done as described in Application No. US 14/555,359.

[0036] N-type self-aligned sinkers 552 are disposed in the upper semiconductor layer 512 abutting the deep trench structures 514 and extending to the buried layer 506. The self-aligned sinkers 552 provide electrical connections to the buried layer 506. The self-aligned sinkers 552 may be formed as described in Application No. US 14/555,209.

[0037] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a substrate including s semiconductor material; and

a deep trench structure in the substrate, including: a deep trench at least 10 microns deep in the substrate; a dielectric liner disposed on sidewalls of the deep trench; a first layer of polysilicon disposed on the dielectric liner and extending to a bottom of the deep trench; and a second layer of polysilicon disposed on the first layer of polysilicon and extending into the deep trench, wherein dopants are distributed throughout the first layer of polysilicon and the second layer of polysilicon with an average doping density of at least 1×10^{18} cm^{-3}, and wherein a width of the deep trench structure is 1.5 microns to 3.5 microns.

2. The semiconductor device of claim 1, wherein the dielectric liner includes a layer of thermal oxide on the sidewalls and a layer of deposited silicon dioxide on the layer of thermal oxide.

3. The semiconductor device of claim 1, wherein the deep trench structure is 20 microns to 35 microns deep in the substrate.

4. The semiconductor device of claim 1, wherein the first layer of polysilicon has a thickness of 150 nanometers to 200 nanometers.

5. The semiconductor device of claim 1, wherein a bottom of the deep trench structure is free of the dielectric liner, so that the first layer of polysilicon makes an electrical contact to the semiconductor material of the substrate.

6. The semiconductor device of claim 5, wherein the substrate includes a buried layer, and the deep trench extends below a bottom surface of the buried layer.

7. The semiconductor device of claim 1, wherein the first layer of polysilicon is isolated from the substrate by the dielectric liner at a bottom of the deep trench structure.

8. A method of forming a semiconductor device, comprising:

providing a substrate including a semiconductor material;

forming a deep trench at least 10 microns deep in the substrate, the deep trench being 1.5 microns to 3.5 microns wide;

forming a dielectric liner on sidewalls of the deep trench;

forming a first layer of polysilicon on the dielectric liner, so that the first layer of

polysilicon extends into the deep trench, the first layer of polysilicon being formed as an undoped layer;

implanting dopants into the first layer of polysilicon;

forming a second layer of polysilicon on the first layer of polysilicon, so that the second layer of polysilicon extends into the deep trench, the second layer of polysilicon being formed as an undoped layer; and

annealing the substrate, so as to activate and diffuse the implanted dopants, so that an average doping density in the first layer of polysilicon and the second layer of polysilicon is at least 1×10^{18} cm^{-3}.

9. The method of claim 8, wherein the dopants are implanted at a dose of 2×10^{15} cm^{-2} to 1×10^{16} cm^{-2}.

10. The method of claim 8, wherein the dopants are implanted in 4 sub-doses at tilt angles of 1 degree to 2 degrees and twist angles of about zero degrees.

11. The method of claim 8, wherein the first layer of polysilicon has a thickness of 150 nanometers to 200 nanometers.

12. The method of claim 8, wherein the step of annealing the substrate includes a furnace anneal at 1000 °C to 1100 °C for 100 minutes to 150 minutes in a nitrogen ambient.

13. The method of claim 8, comprising forming a buried layer in the substrate before forming the deep trench, so that the deep trench extends below a bottom surface of the buried layer.

14. The method of claim 8, wherein forming the dielectric liner includes forming a layer of thermal oxide on the sidewalls and forming a layer of deposited silicon dioxide on the layer of thermal oxide.

15. The method of claim 8, comprising removing the dielectric liner at a bottom of the deep trench before forming the first layer of polysilicon, and forming the first layer of polysilicon to extend to a bottom of the deep trench, so that the first layer of polysilicon makes an electrical contact to the substrate at the bottom of the deep trench.

16. The method of claim 15, comprising implanting dopants into the semiconductor material of the substrate at the bottom of the deep trench, after removing the dielectric liner at a bottom of the deep trench and before forming the first layer of polysilicon.

17. The method of claim 8, wherein the first layer of polysilicon is formed extending to a bottom of the deep trench, so that the dielectric liner isolates the first layer of polysilicon from

the substrate.

18. A method of forming a semiconductor device, comprising:

providing a substrate including a semiconductor material;

forming a deep trench at least 10 microns deep in the substrate, the deep trench being 1.5 microns to 3.5 microns wide;

forming a dielectric liner on sidewalls of the deep trench;

removing the dielectric liner at a bottom of the deep trench;

implanting dopants into the semiconductor material of the substrate at the bottom of the deep trench;

forming a first layer of polysilicon on the dielectric liner, extending to a bottom of the deep trench, so that the first layer of polysilicon makes an electrical contact to the substrate at the bottom of the deep trench, the first layer of polysilicon being formed as an undoped layer;

implanting dopants into the first layer of polysilicon;

forming a second layer of polysilicon on the first layer of polysilicon, so that the second layer of polysilicon extends into the deep trench, the second layer of polysilicon being formed as an undoped layer; and

annealing the substrate, so as to activate and diffuse the implanted dopants, so that an average doping density in the first layer of polysilicon and the second layer of polysilicon is at least 1×10^{18} cm^{-3}.

19. The method of claim 18, wherein forming the dielectric liner includes forming a layer of thermal oxide on the sidewalls and forming a layer of deposited silicon dioxide on the layer of thermal oxide.

20. The method of claim 18, comprising forming a buried layer in the substrate before forming the deep trench, so that the deep trench extends below a bottom surface of the buried layer.

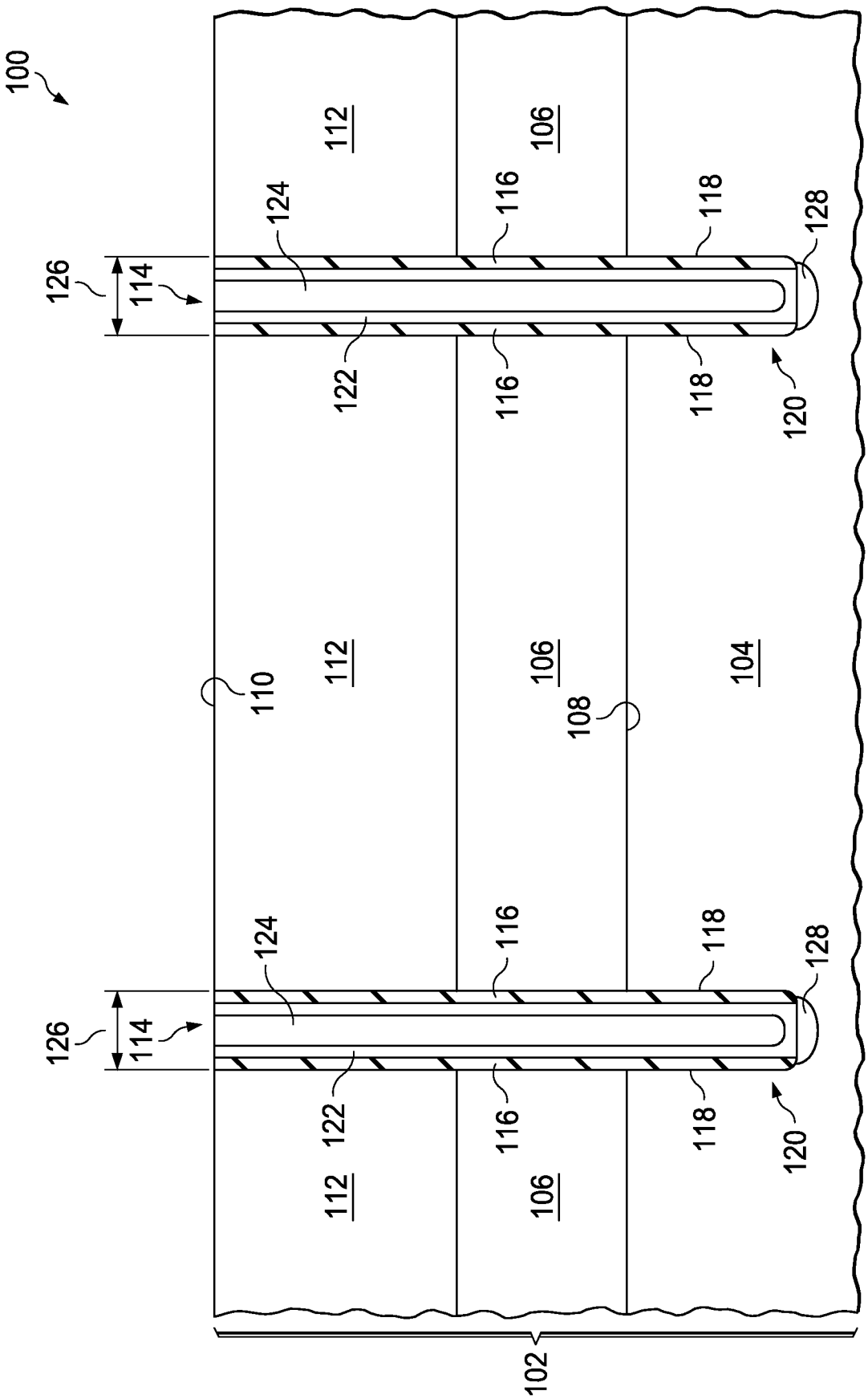
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FIG. 1

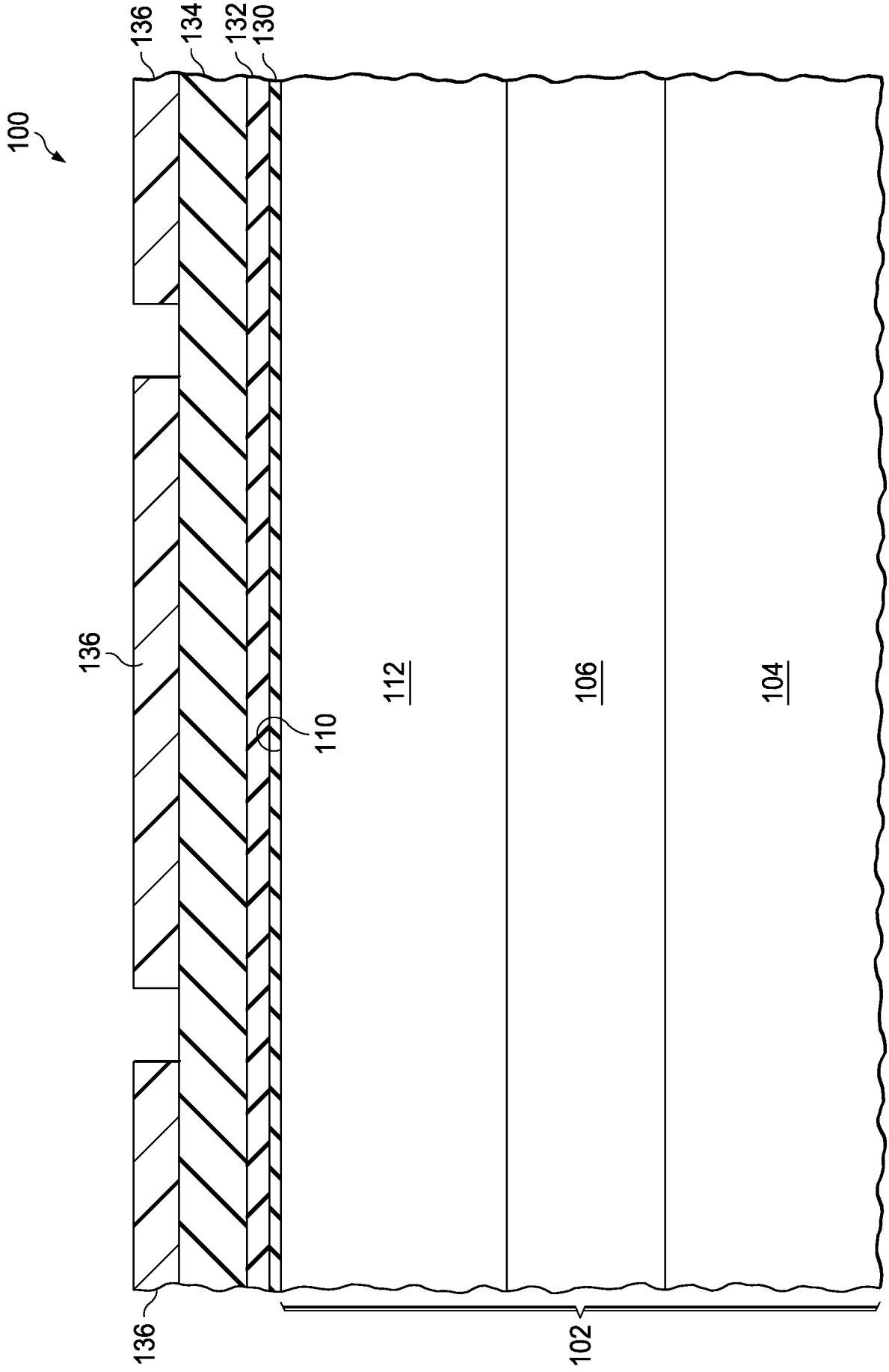

FIG. 2A

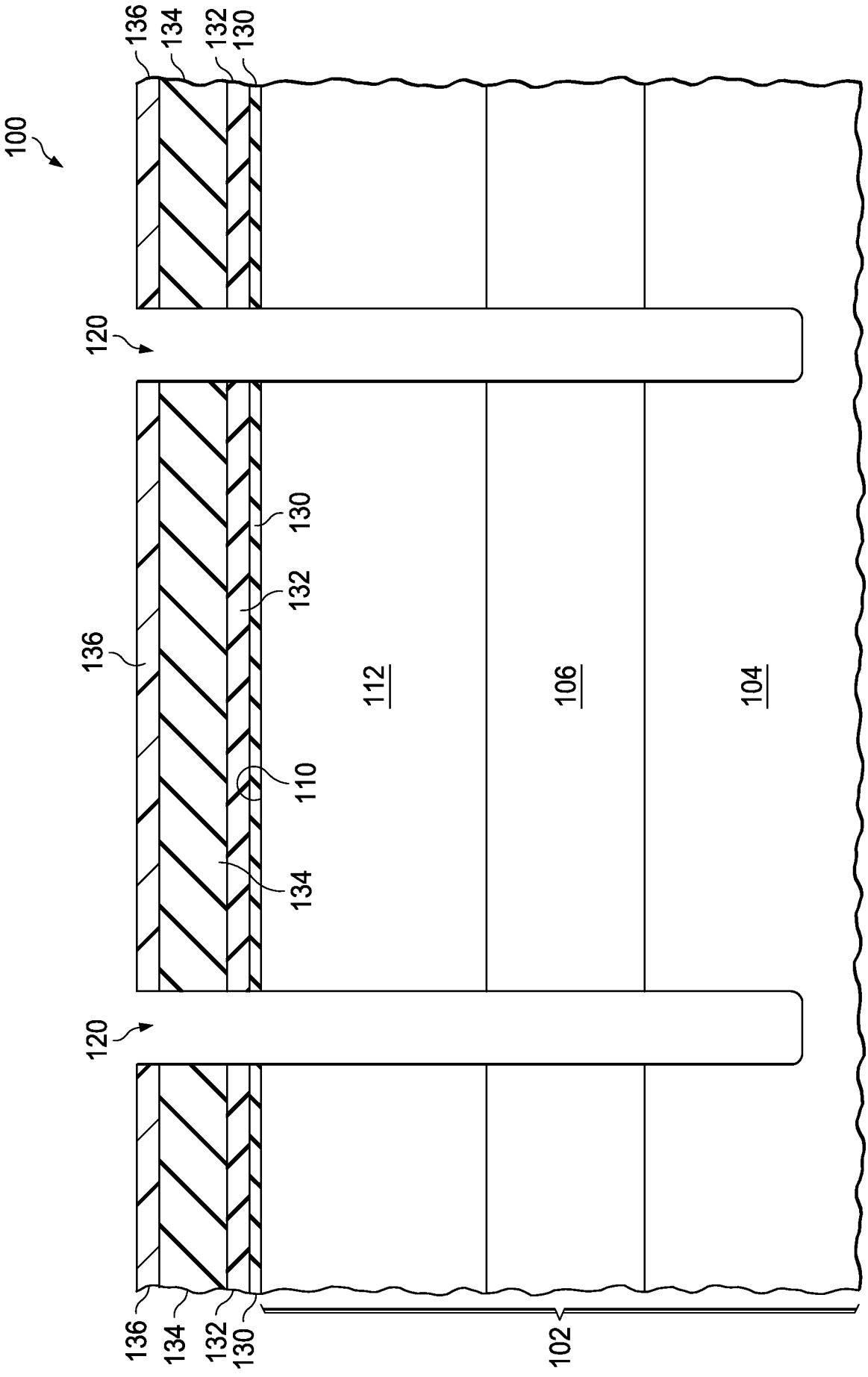
100
136
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FIG. 2B

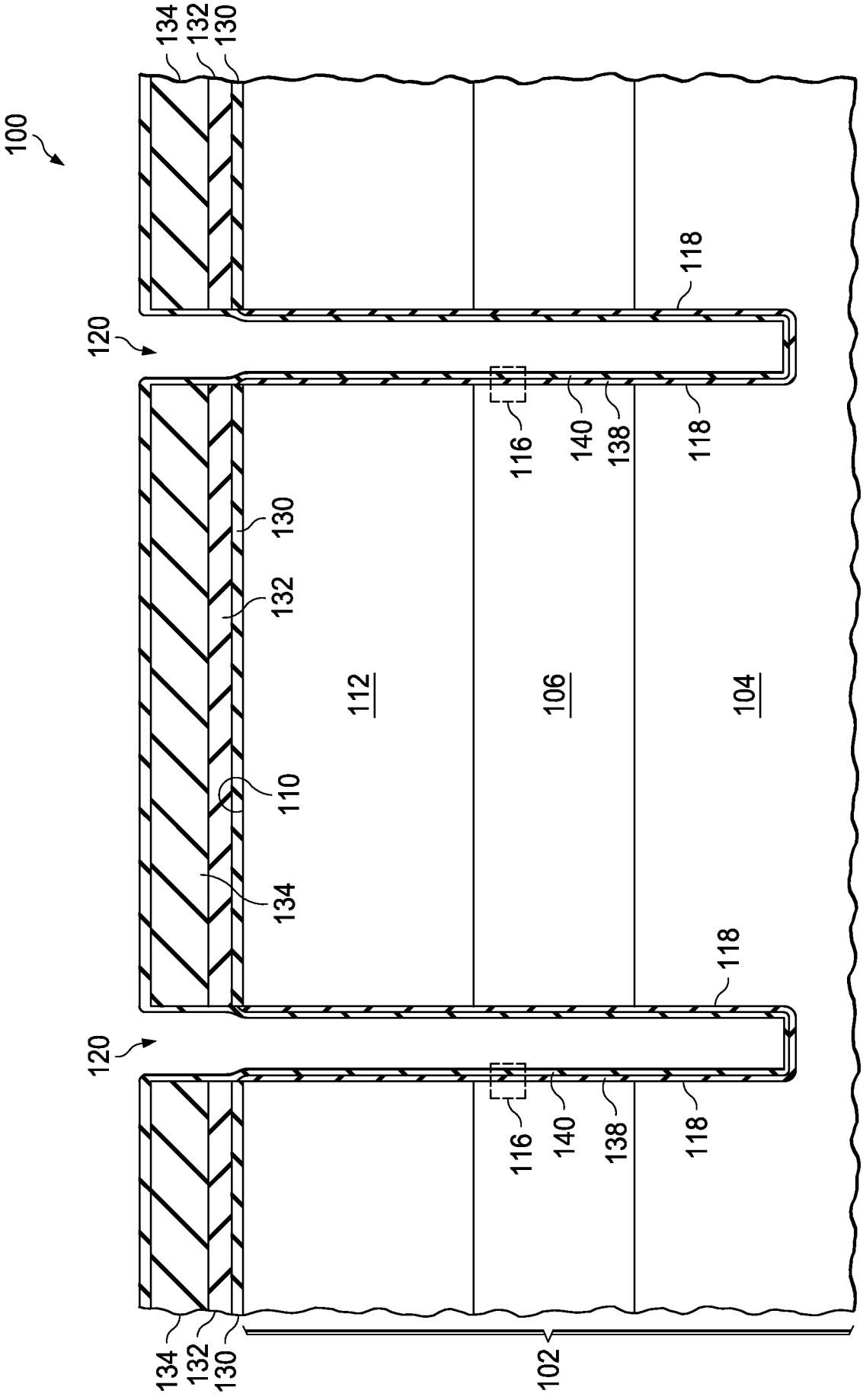
100
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FIG. 2C

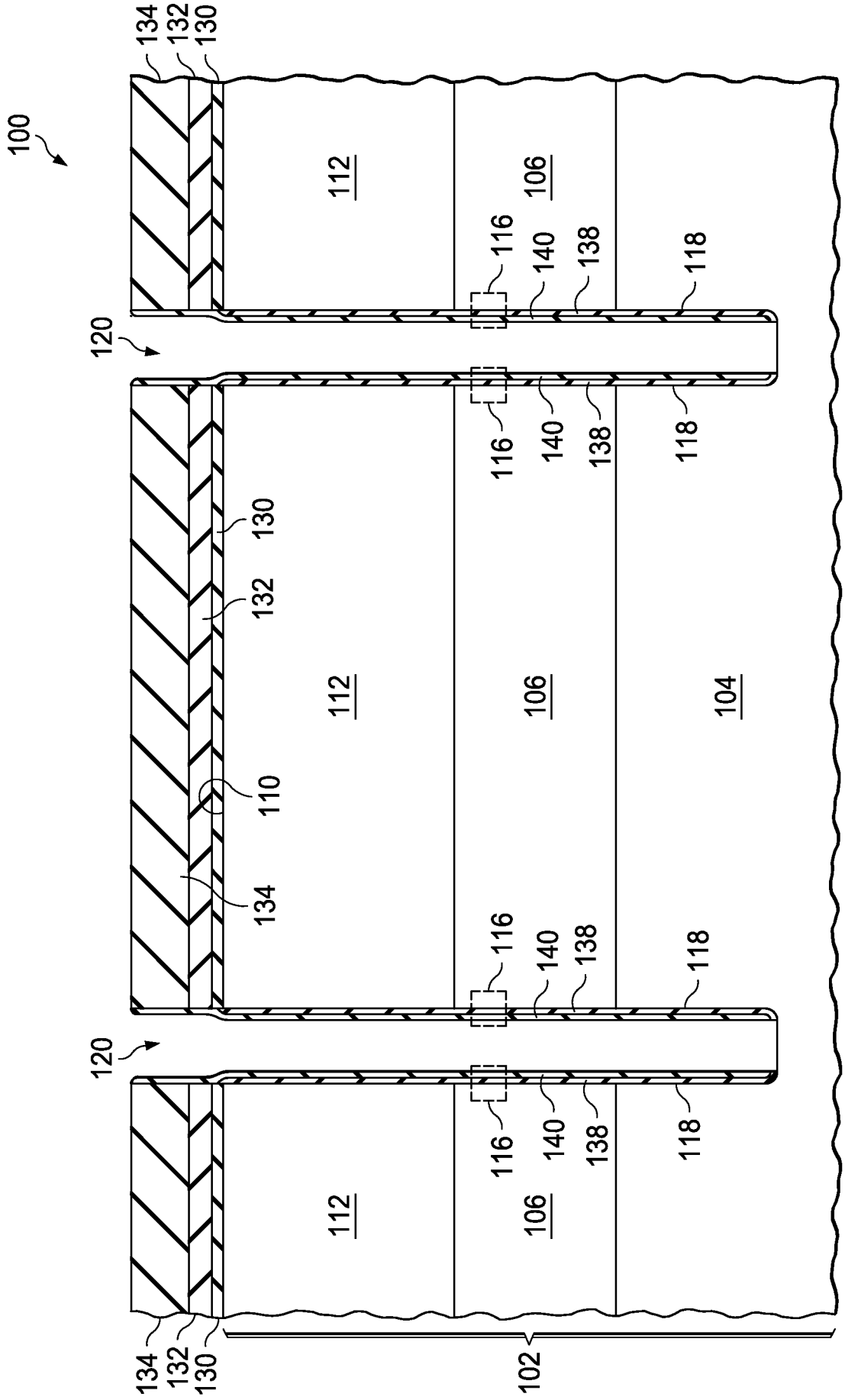

FIG. 2D

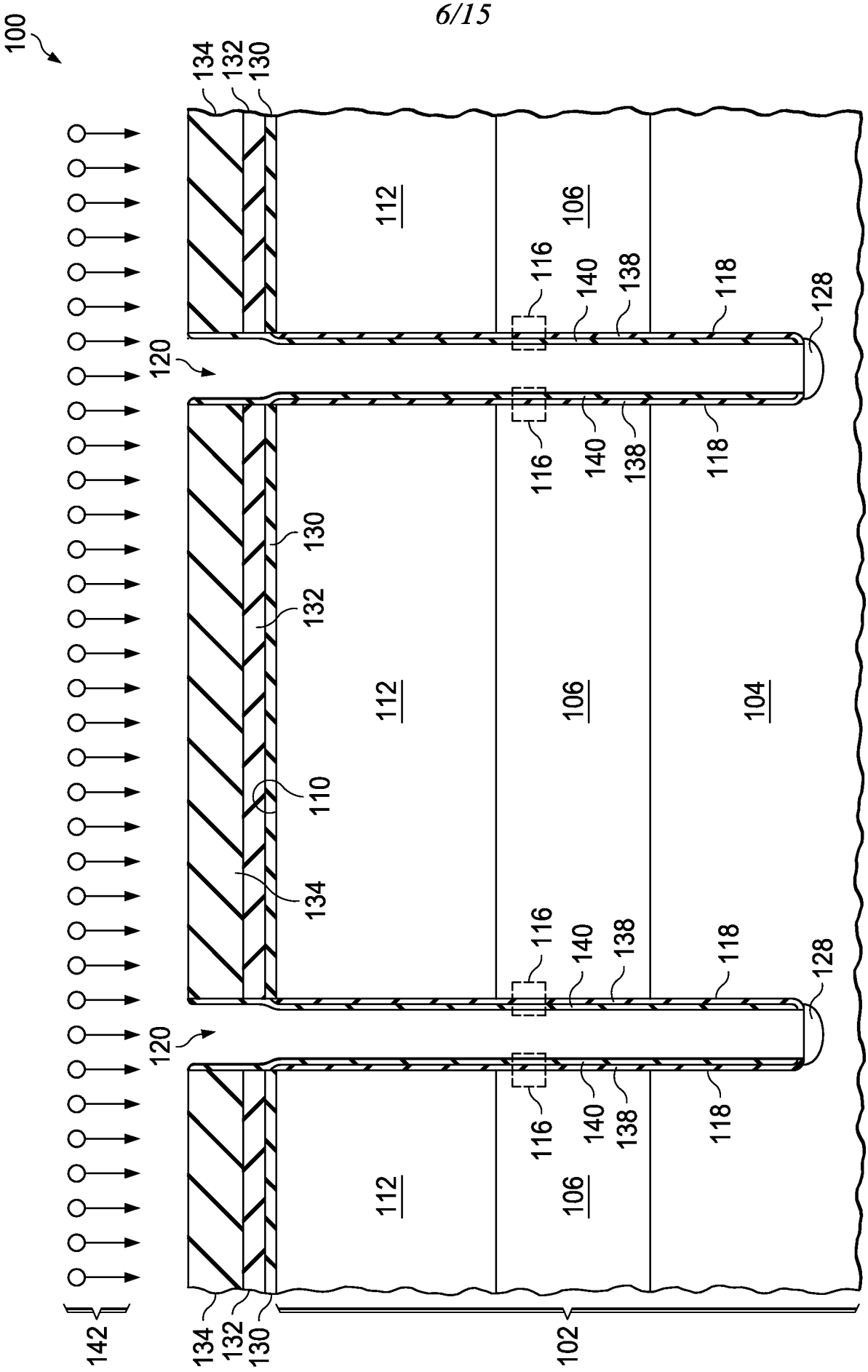

FIG. 2E

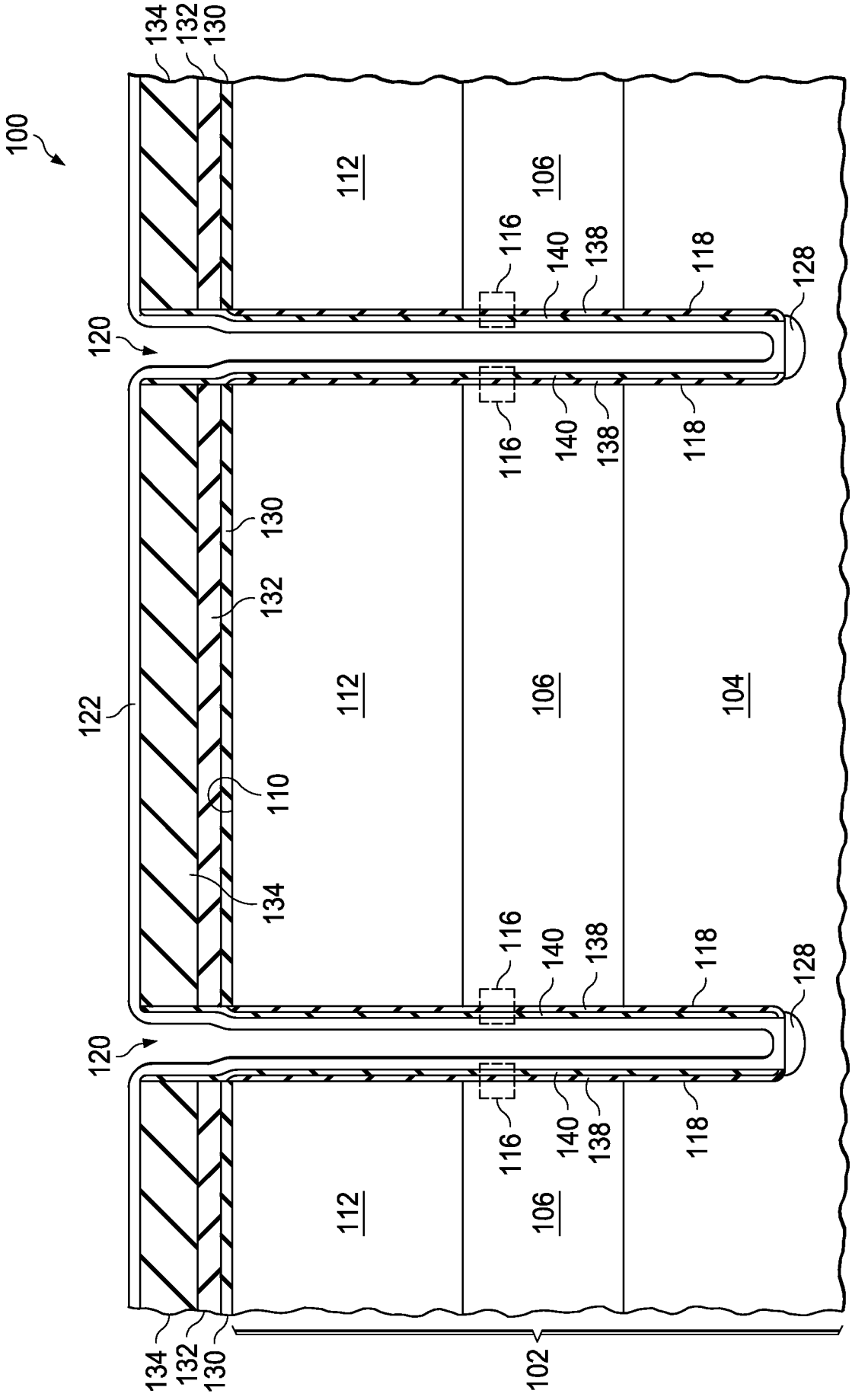

FIG. 2F

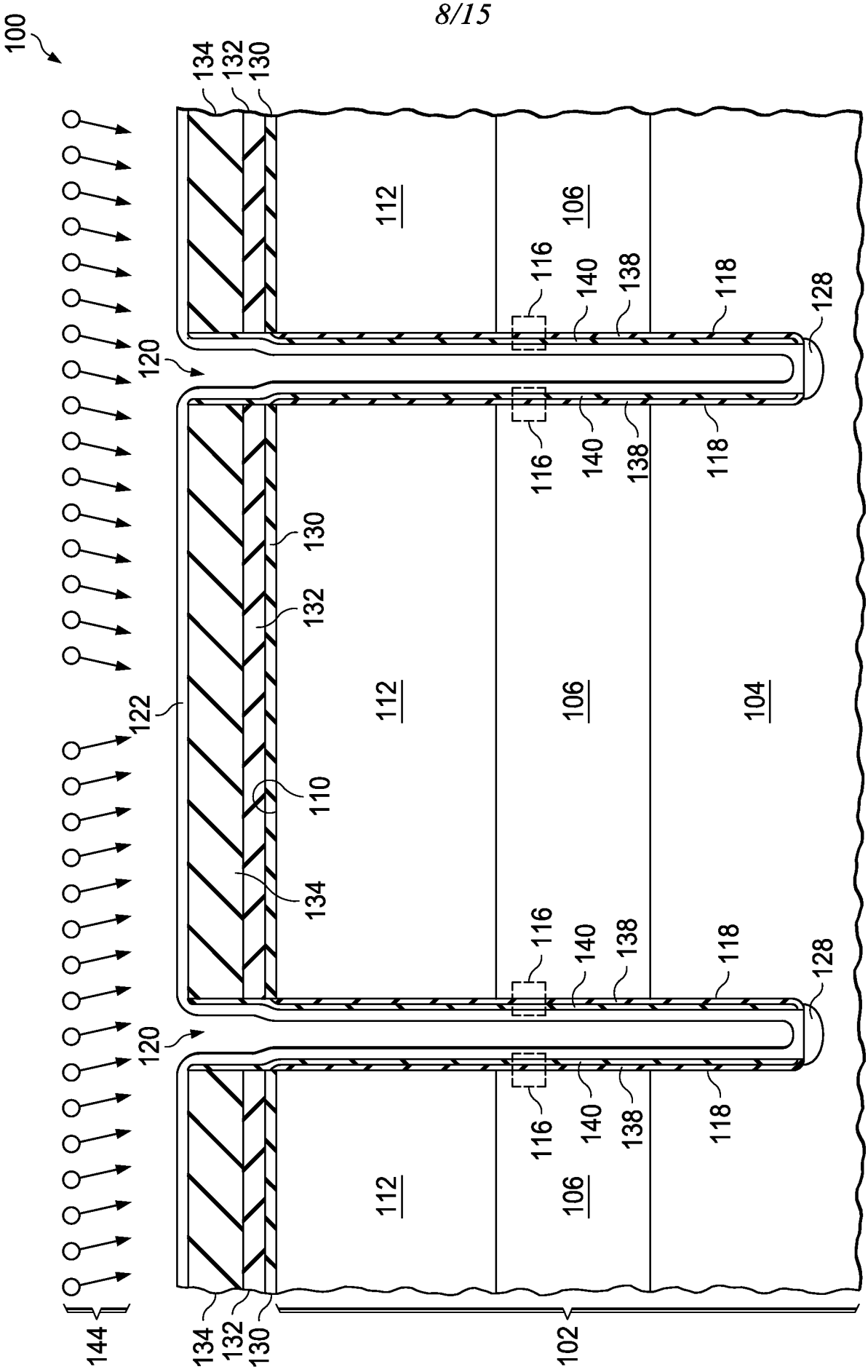
100
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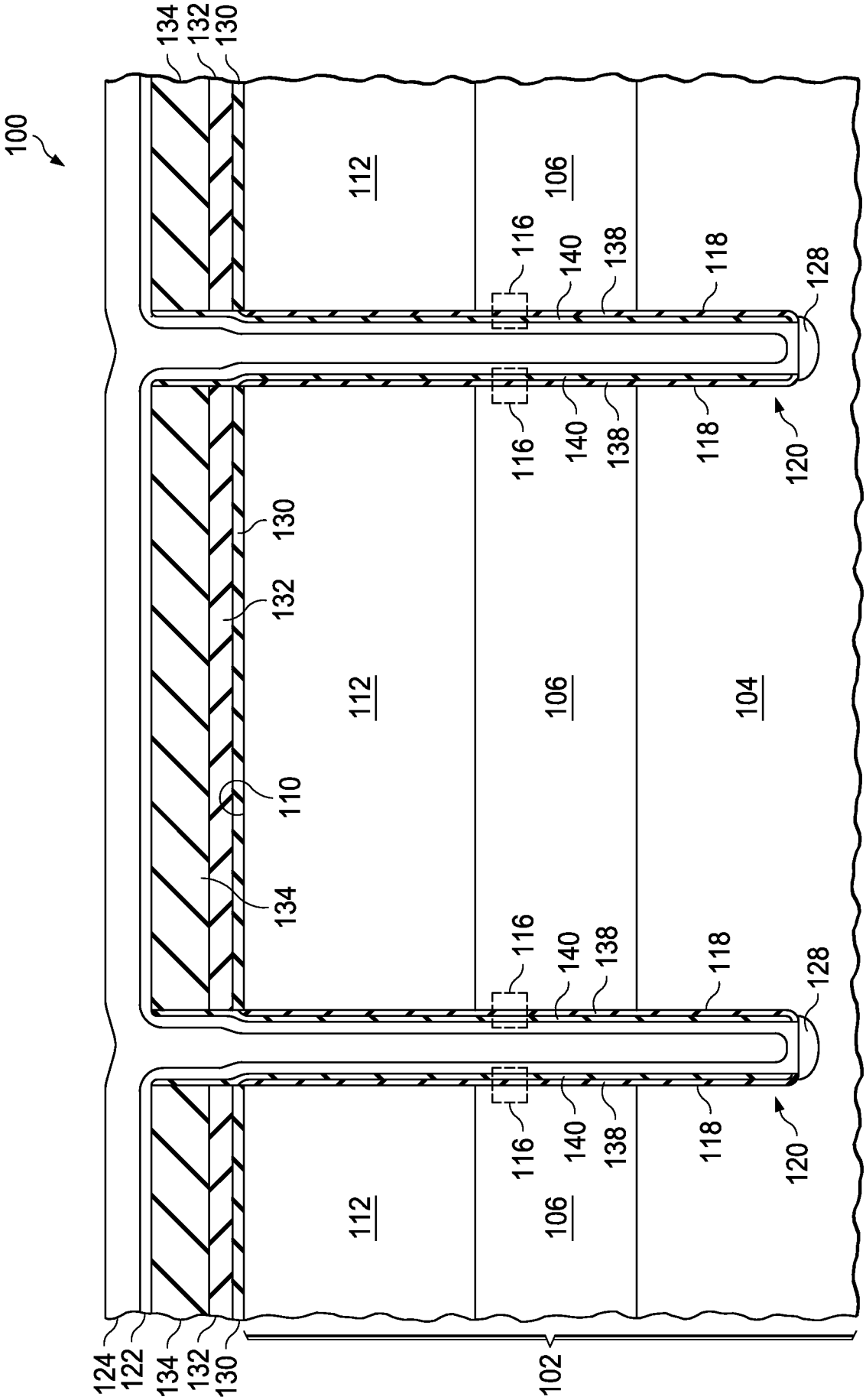
FIG. 2G


100
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130
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124
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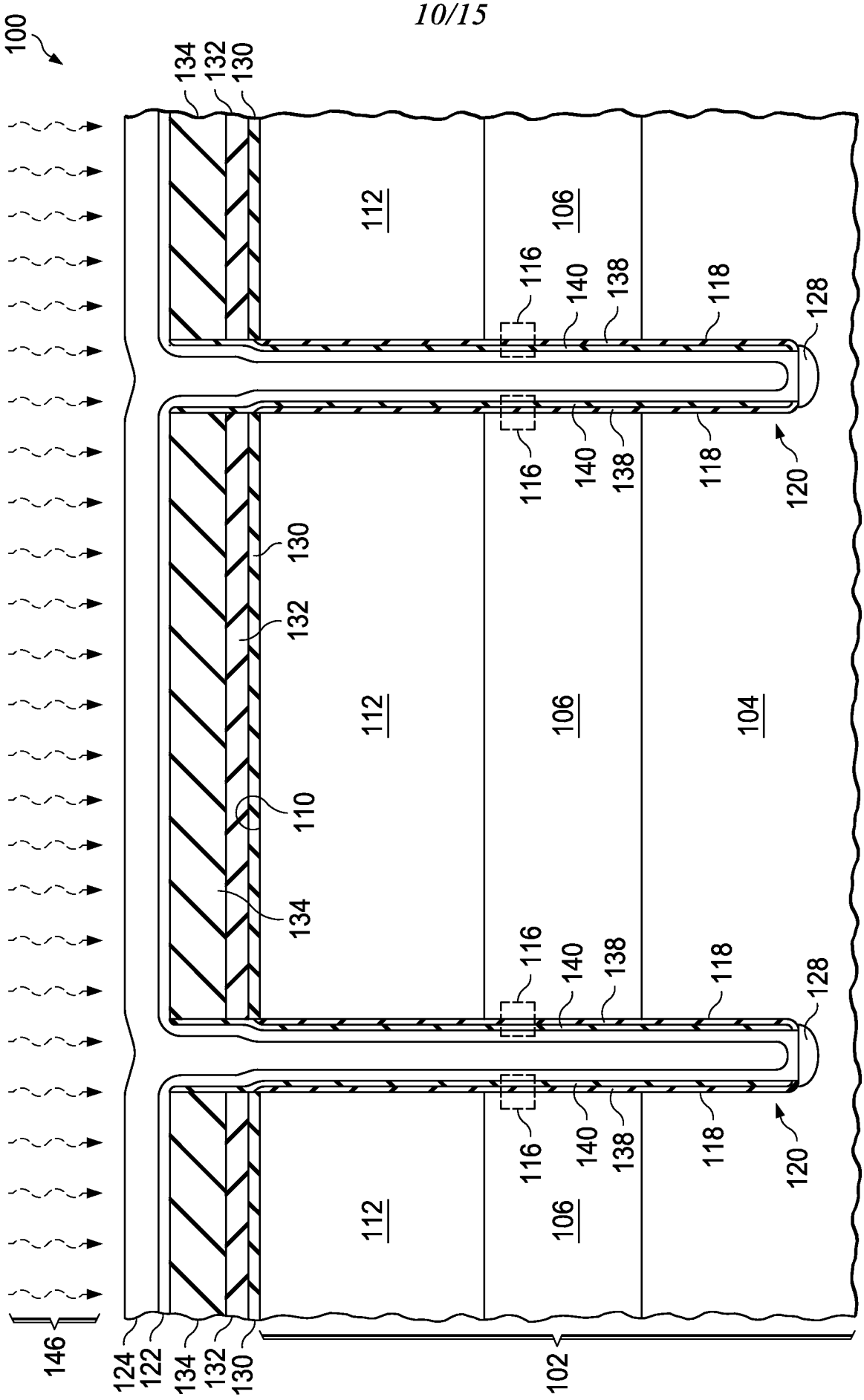
FIG. 2H


100
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132
130
112
106
116
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138
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128
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FIG. 2I

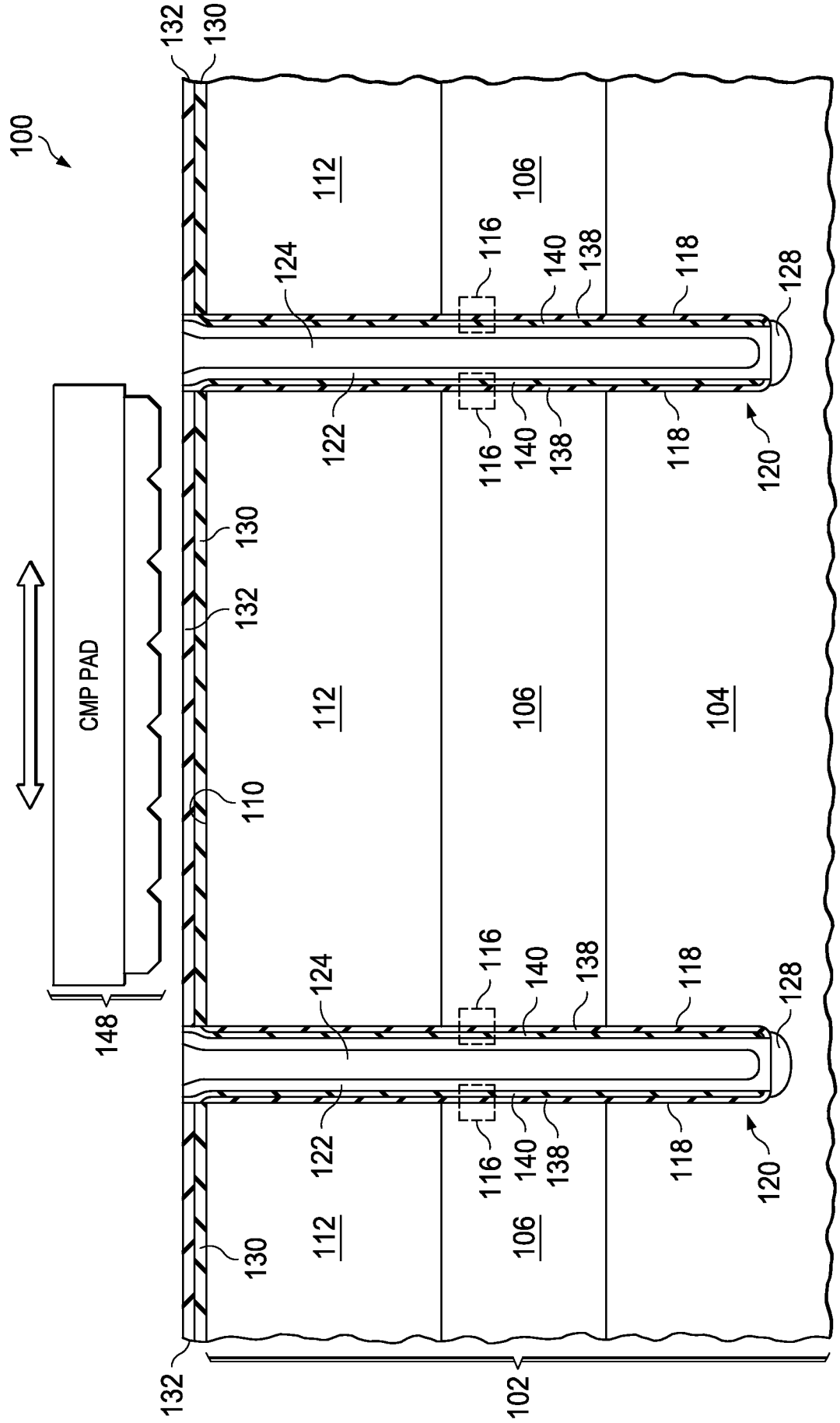
100
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FIG. 2J

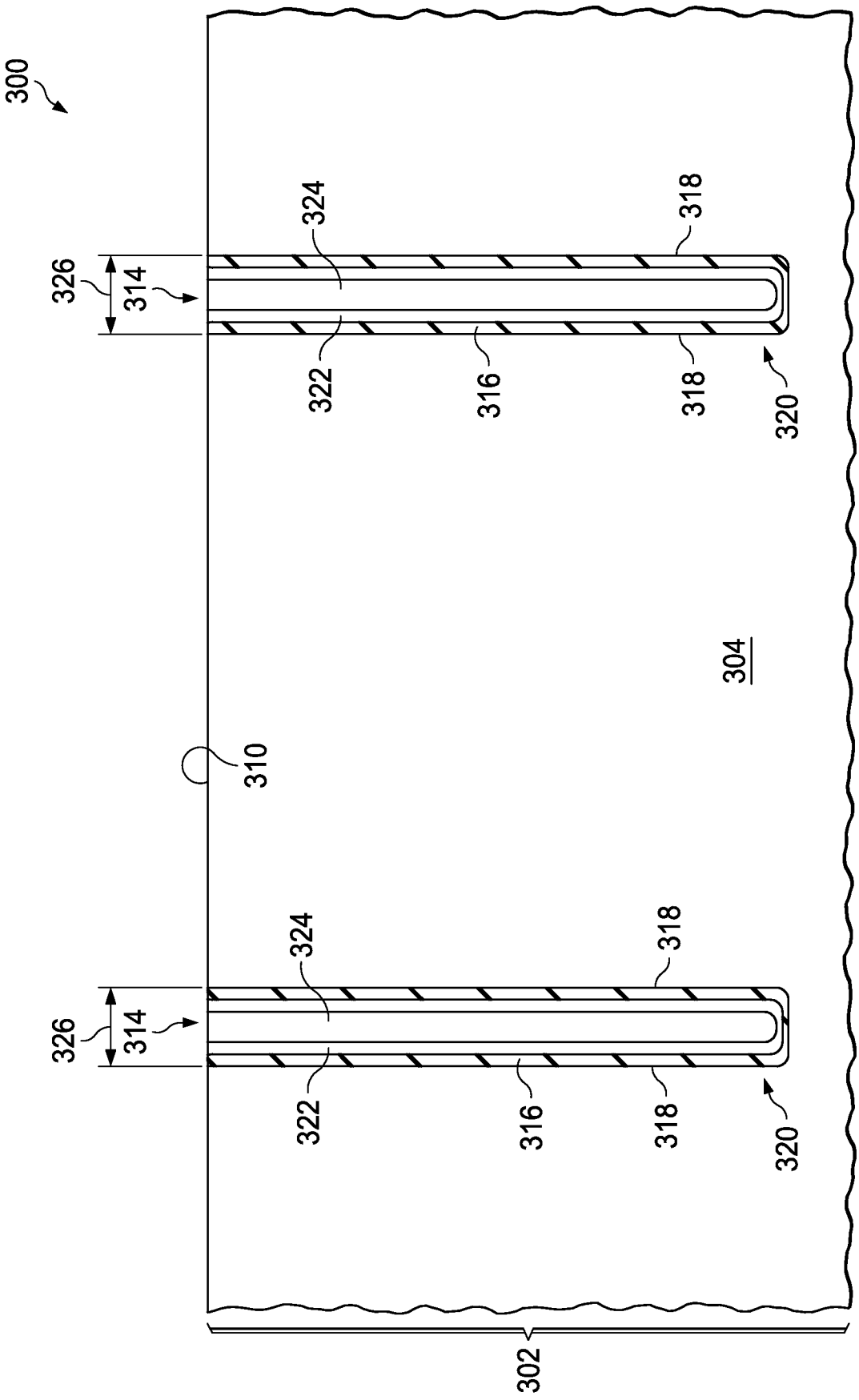
300
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FIG. 3

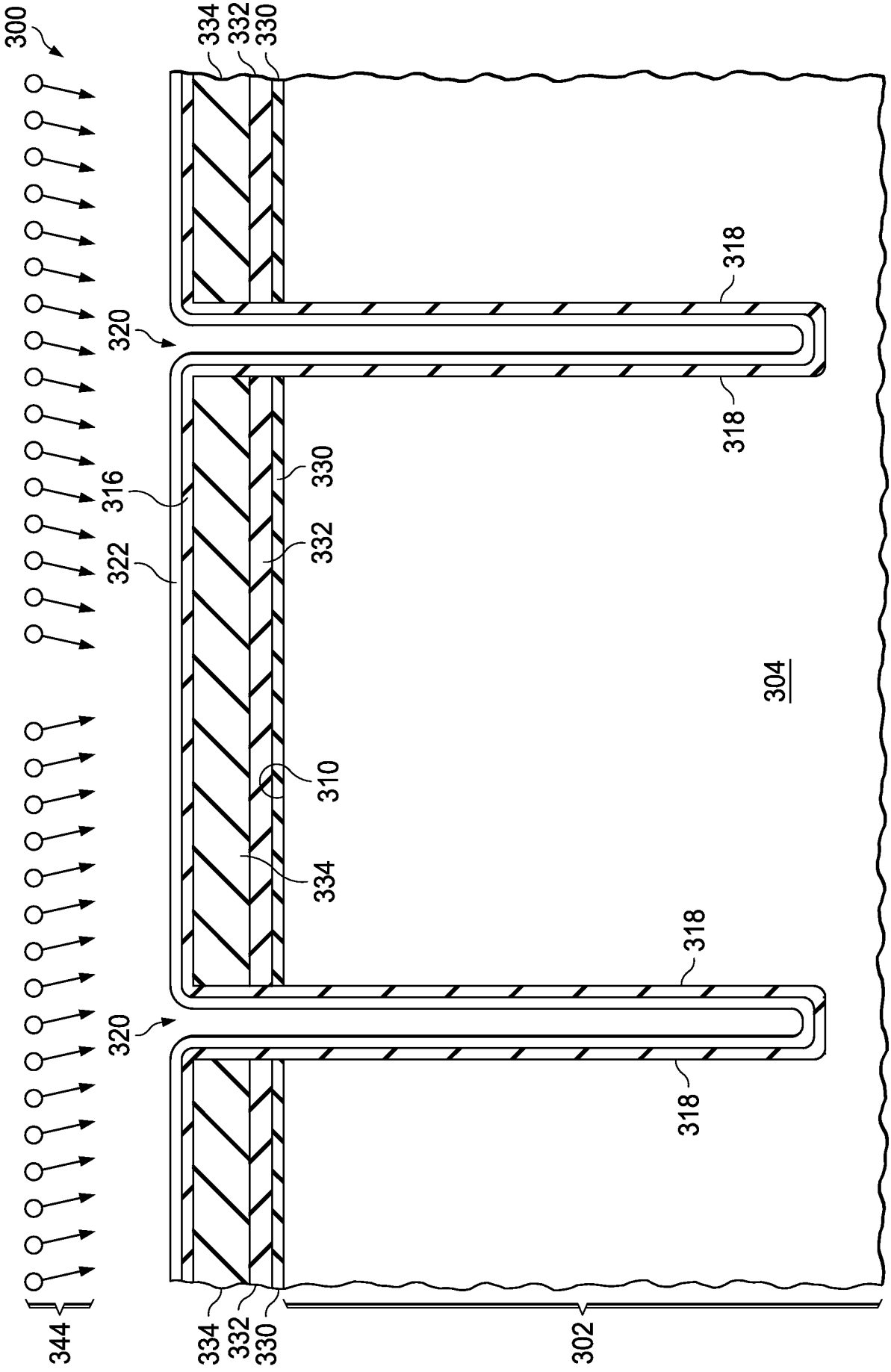
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FIG. 4A

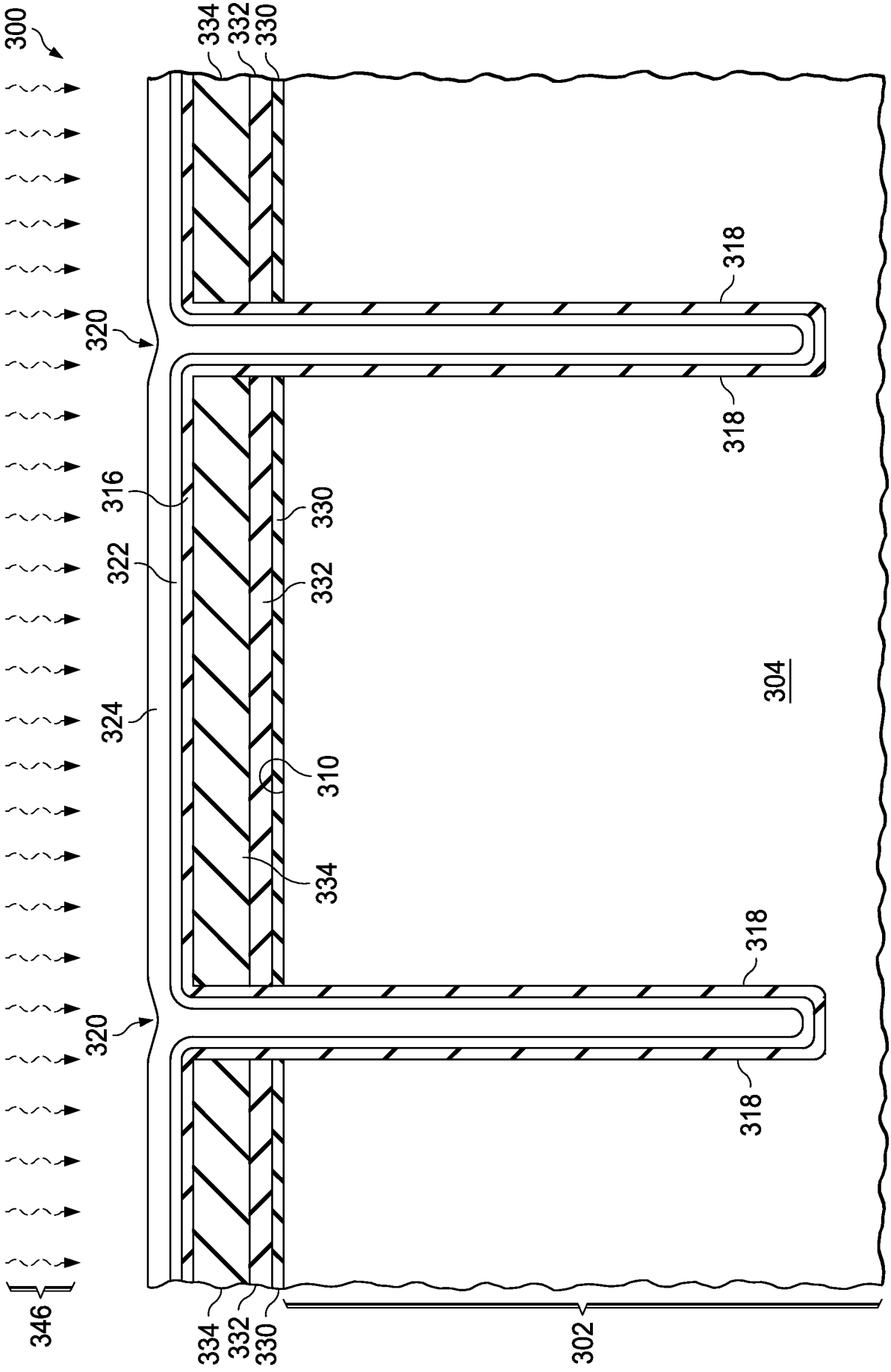
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FIG. 4B

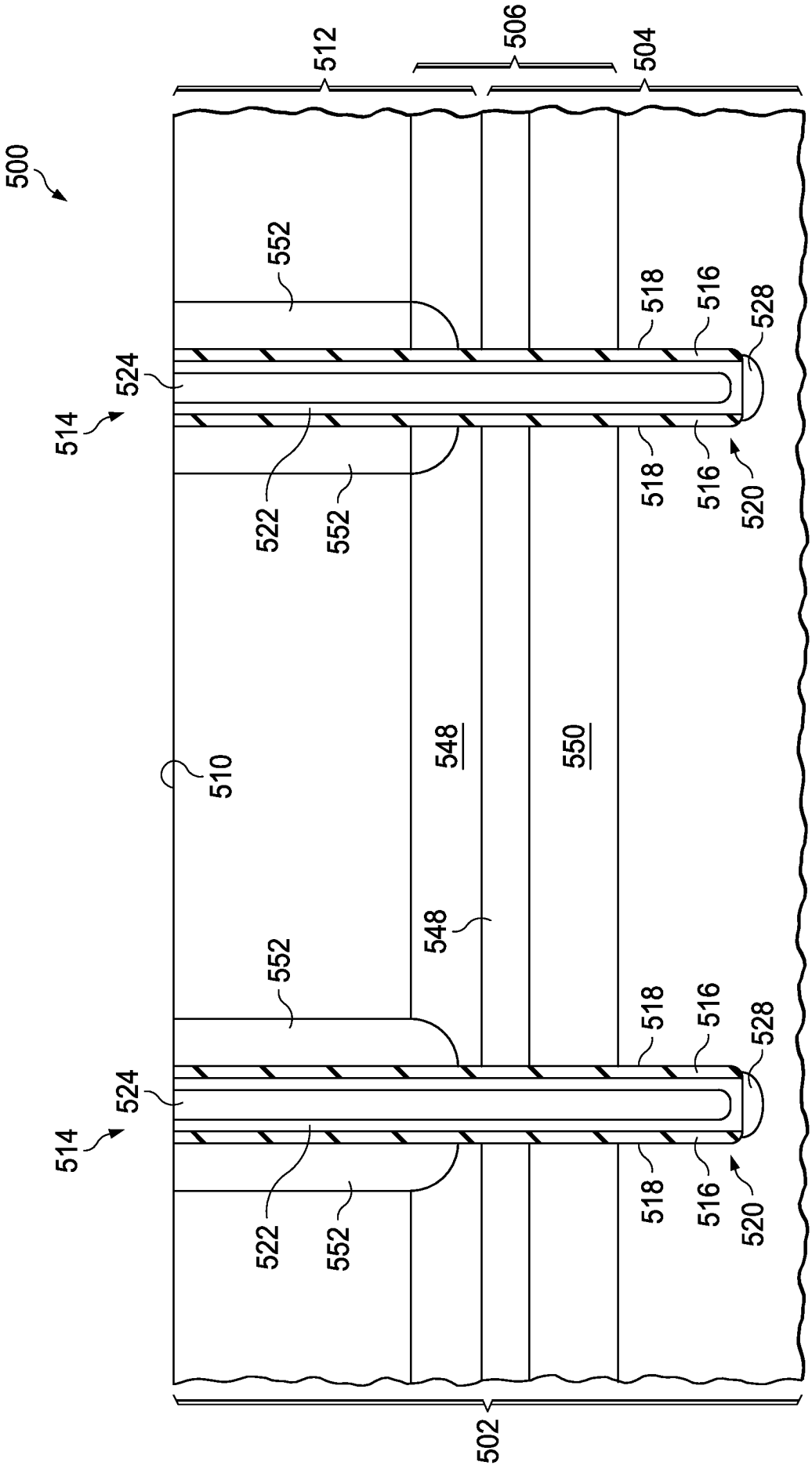
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FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2015/062265

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/762 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/00, 29/02, 29/06, 21/00, 21/02, 21/04, 21/18, 21/30, 21/302, 21/306, 21/66, 21/70, 21/76, 21/762

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014/0001596 A1 (BINGHUA HU et al.) 02.01.2014	1-20
A	US 6218722 B1 (GENNUM CORPORATION) 17.04.2001	1-20
A	US 4980747 A (TEXAS INSTRUMENTS INC.) 25.12.1990	1-20
A	US 4666556 A (INTERNATIONAL BUSINESS MACHINES CORPORATION) 19.05.1987	1-20
A	US 2011/0275168 A1 (TEXAS INSTRUMENTS INCORPORATED) 10.11.2011	1-20
A	US 2004/0032005 A1 (RICHARD K. WILLIAMS et al.) 19.02.2004	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 March 2016 (01.03.2016)	17 March 2016 (17.03.2016)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer M. Adireeva Telephone No. 499-240-25-91