Abstract

A Design Failure Mode Effect Analysis (DFMEA) method analyzes faults and failures in the design phase of electronic devices. A data-entry mask is used for recording some information concerning the performed analysis and a portion of the recording form is displayed to a user in an electronic display format. The method detects and records past design problems and their corresponding solutions, by a DFMEA method using the data-entry mask form; associates keywords in a database with each problem; associates data concerning each of the design problems, in the same database, including information concerning past fails occurred in similar applications; detects major changes and/or innovations, as well as any improved block or part of a new device with respect to other devices, thereby postulating possible new problems introduced by the new device; and records the new problems and their possible solutions, by the DFMEA method and using the form.

Potential Failure Mode and Effect Analysis

<table>
<thead>
<tr>
<th>Item/Function</th>
<th>Potential Failure Mode</th>
<th>Potential Effect of Failure</th>
<th>Potential Cause/Mechanism of Failure</th>
<th>Current Control</th>
<th>RPN</th>
<th>Recommended Action</th>
<th>Responsible and Target Completion Date</th>
<th>Action Taken</th>
<th>SEV</th>
<th>DET</th>
<th>RPN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming</td>
<td>Softprogram of the program reference cell</td>
<td>Failure for erase time</td>
<td>C</td>
<td>8</td>
<td>none</td>
<td>640</td>
<td>DETECTABILITY:</td>
<td>21-11-2000</td>
<td>8</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Reference cell [113_CELL]</td>
<td>Coupling between the VIF node and the drain of the reference cell that is floating during the execution of some instructions in</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
FIG. 1

DFMEA
On Web
VER. 2

<table>
<thead>
<tr>
<th>DFMEA NUMBER</th>
<th>ACTIVITY</th>
<th>RESPONSIBLE</th>
<th>RELATED DEVICE</th>
<th>Edit Current Settings</th>
<th>Open This Project</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFMEA-A4AO</td>
<td>Design in Progress</td>
<td>imperiale francesco</td>
<td>M28W160B (A4A0-16Mbit-Cmos17)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Create a new DFMEA Project

SEARCH

HOME
<table>
<thead>
<tr>
<th>Item/Function</th>
<th>Potential Failure Mode</th>
<th>Potential Cause of Failure</th>
<th>RPN</th>
<th>Recommended Action</th>
<th>Target Completion</th>
<th>Action Taken</th>
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<td></td>
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<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Potential Failure Mode and Effect Analysis

**DIVISION:** All

**ACTIVITY:** All

**FRONT-END LOCAT:** All

**DEMA ID-Code:** All

**REVISION:** All

**DATE:** All

**FIG. 2**
## Potential Failure Mode and Effect Analysis

**FIG. 3A**

<table>
<thead>
<tr>
<th>Item/Function</th>
<th>Potential Failure Mode</th>
<th>Potential Effect of Failure</th>
<th>OCC</th>
<th>Current Control</th>
<th>DET</th>
<th>RPN</th>
<th>Recommended Action</th>
<th>Responsible and target completion date</th>
<th>Action Token</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROGRAMMING</td>
<td>Softprogram of the program reference cell (REF CELLS)</td>
<td>Failure for erase time</td>
<td>A 8</td>
<td>none</td>
<td>10</td>
<td>640</td>
<td>DETECTABILITY: 1) To perform an eldo simulation of the reference cells giving a ramp voltage to VYP (from 4v to 8.75v) and to check the voltage of the drain of the reference cells. 2) In testing to perform a cycling with program</td>
<td>francesco imperiale; TO BE VALIDATED 21-11-2000</td>
<td>8 1 2 16</td>
</tr>
</tbody>
</table>

### Table Columns
- **Item/Function**: Description of the item or function.
- **Potential Failure Mode**: Type of potential failure.
- **Potential Effect of Failure**: Type of effect.
- **OCC**: Severity level.
- **Current Control**: Current level of control.
- **DET**: Detection level.
- **RPN**: Risk Priority Number.
- **Recommended Action**: Actions to be taken.
- **Responsible and target completion date**: Responsible party and target date.
- **Action Token**: Action identifier.
<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
<th>J</th>
<th>K</th>
<th>L</th>
<th>M</th>
<th>N</th>
<th>O</th>
<th>P</th>
<th>Q</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>program ÚM.</td>
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<td></td>
<td></td>
<td></td>
<td>testing to perform a cycling with program and erase ÚM.</td>
<td></td>
<td>and erase ÚM.</td>
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</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>Details</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>OCCURRENCE: 1) To modify the algorithm in such a way that the time when the program reference remain floating is lower. 2) To put to gnd the drain of the reference when the VIP node goes up.</td>
<td></td>
<td>SEVERITY:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EWS—BINNING</td>
<td>Row short fails.</td>
<td>The Foils have got the following features: 1. Whole rows don't pass ReadAllTs 2. The tail bits have got a drain current equal to zero (whatever are the gate and drain voltages) 3. There are no bitlineleakage fails.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DETECTABILITY:</td>
<td>fabio morgana</td>
<td>DETECTABILITY:</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>OCCURRENCE: --??--</td>
<td></td>
<td>OCCURRENCE:</td>
<td></td>
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<td></td>
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<td></td>
<td>SEVERITY: 12-01-2001</td>
<td></td>
<td>SEVERITY:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FIG. 3B**
Potential Failure Mode and Effect Analysis

DFMEA Number: Activity: DFMEA-A4A0 Design in Progress
Rev. ID: [C] [p] 21-11-2000
Rev. Status: EDITABLE
Rev. Protection: PRIVATE
View DFMEA
Freeze Rev
Chg Protection
Gener. Package
Readers Man

Device Info:
M28W160B (A4A0) 16Mbit - CmosT7

FIG. 4
### FIG. 6

#### Recommended Action (OCC)

1. To modify the algorithm in such a way that the time when the program reference remain floating is lower.

#### Recommended Action (DET)

1. To perform an elbow simulation of the reference cells giving a ramp voltage V_{RP} (from 4.1 to 8.75V) and to check the voltage hit and checking the voltage.

#### Action Token (OCC)

1. To modify the algorithm in such a way that the time when the program reference remain floating is lower.

#### Action Token (DET)

1. To perform an elbow simulation of the reference cells giving a ramp voltage V_{RP} (from 4.1 to 8.75V) and to check the voltage hit and checking the voltage.
DESIGN FAILURE MODE EFFECT ANALYSIS (DFMEA)

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention broadly relates to a method of analyzing faults and failures in the design of electronic apparatus and devices.

[0003] More specifically, the invention relates to a method wherein a DFMEA form or document is used for analyzing faults and failures in the design of electronic apparatus and devices, the DFMEA form including a data-entry mask through which information concerning the analysis are recorded and in which at least a portion of the document is displayed to a user in an electronic display format.

[0004] 2. Description of the Related Art

[0005] As is well known in this technical field, one of the best appreciated and widely used techniques for preventing faults and/or errors in the design of apparatus and/or devices for automotive applications is a method commonly referred to by the acronym FMEA (Failure Mode Effect Analysis).

[0006] This method or technique was developed in the States for the automotive industry, but soon spread to the suppliers of the US automotive manufacturers.

[0007] In the FMEA technique, under the guidance of a predetermined form to be filled, the user is directed to identify possible weakness areas in a product or a process, and this especially at the initial development stage.

[0008] There are two main divisions in the FMEA technique: a first division covers industrial processes and is known as PFMEA (Process FMEA); a second division is specific to the design of new parts and/or devices and known as DFMEA (Design FMEA).

[0009] The analysis is conducted by means of a form divided into two sections, as specified here below.

[0010] A right-side section is devoted to illustrate a potential problem by the following entries:

[0011] Item/Function: identifies the part affected by the problem;

[0012] Potential Failure Mode: indicates a failure mode;

[0013] Effect of Failure: is the failure mode effect on the application and operation;

[0014] Root Cause: is the prime cause that originated the failure mode; and

[0015] Current Control: is an existing control for finding the failure mode.

[0016] Conform with these entries of a descriptive nature are three columns that are used for weighing the degree of risk that associates with each entry. The weight marks may be, for example:

[0017] S (Severity), to provide a measure of how severe the failure mode effect is;

[0018] O (Occurrence), to quantify the rate at which the failure mode is generated; and

[0019] D (Detectivity), to detect the location within the control chain where the failure mode can be found.

[0020] All these marks carry a value scale from 1 to 10, with 1 being the lowest and 10 the highest degree of risk.

[0021] On completion of a preliminary analysis, a Risk Product Number (RPN) is arrived at by multiplying the marks S, O, and D together, this number indicating the degree of risk that associates with the potential failure mode detected.

[0022] When RPN exceeds a given threshold value, corrective actions must be taken to bring it down.

[0023] The second section of the form, which is reserved for the last-mentioned entry, comprises:

[0024] Recommended Action: the action proposed in order to bring RPN down;

[0025] Responsible and Completion Date: the responsible entity for the action and the action completion date; and

[0026] Action Taken: the action actually completed.

[0027] The three columns labeled S, O and D and to be re-calculated after completion of the corrective action specified, should be added to these columns.

[0028] The FMEA technique outlined above has gained widespread acceptance in the semiconductor industry. However, this is an industry devoted to the production of highly complex devices whose component parts to be analyzed may be millions.

[0029] The FMEA technique has been perfected under the concurrent urge of quality requirements enforced by a number of protocols, such as the QS9000 protocol.

[0030] Initially, the PFMEA technique grew in popularity, while the other DFMEA technique was only occasionally applied, but later the DFMEA technique would prove to be the more useful and profitable for the manufacturer. The few examples in existence only regard its use at meetings, or to fill demands arising from auditing operations or the like scrutinizing operations.

[0031] The reasons for this initial lack of interest in the DFMEA technique are summarized here below.

[0032] Any attempt to apply a DFMEA technique based upon the potential failure modes of individual elements included into a complex device is unthinkably and Utopian. Even a potential demand from clients and quality control groups missed to reflect the practical difficulties faced by the designer.

[0033] Even if one or more component parts were analyzed, the reference grid for reckoning the S, O, and D marks would approach a process analysis in a fashion far too sweeping, thereby occasioning interpretation difficulties making the reckoning ineffective.

[0034] The types of information that describe the aforementioned fields (e.g., Action Taken, Potential Failure Mode, etc.) often require that detailed descriptions and attendant graphs, diagrams, etc., be submitted which are impossible to abridge in a text like the one provided for in the known form. The suggestion to give a numeral reference to technical reports makes their retrieval a difficult, laborious and inefficient task, so that people are discouraged from attempting to read and understand a DFMEA.
The environment where the DFMEA technique was originally developed is that of an international holding where similar devices, potentially sharing the same recurrent problems, are frequently developed by different design departments residing in different towns, territories, or nations.

To summarize, while being advantageous on several counts, the DFMEA technique has limitations that delay its application by the designers of electronic apparatus and devices. Of these limitations, the following are more heavily felt:

1. Current rules that cannot be applied to highly complex devices;
2. Reference grids for the S, O, D mark that do not match the designing criteria;
3. No provisions for the inclusion of technical information in a text; and
4. Information that is difficult to have circulated through all the product development teams involved.

**BRIEF SUMMARY OF THE INVENTION**

An embodiment of this invention provides a novel method for applying the DFMEA technique, which method exhibits appropriate functional features to overcome the drawbacks and limitations of the prior art previously discussed.

The method provides the users of the DFMEA technique with an innovative tool for handling and utilizing the results of analytical activity.

The method provides an innovative approach of the DFMEA technique by shifting the objective from that of preventing the occurrence new faults, typical of the prior art approaches, to that of preventing the reappearance of problems already encountered in the past.

The invention relates to a DFMEA method of analyzing faults and failures in the design of electronic apparatus and devices, wherein an information recording form including a data-entry mask is used for recording some information concerning the performed analysis and in which at least a portion of said recording form is displayed to a user in an electronic display format. The method includes:

- Detecting and recording past design problems and their corresponding solutions, by a DFMEA method using the form;
- Associating keywords in a database with the problems as individual functions;
- Associating data concerning each of the design problems, in the same database, including information concerning past fails occurred in similar applications;
- Detecting major changes and/or innovations, as well as any improved block or part of a new device with respect to other devices, thereby postulating possible new problems introduced by the new device; and
- Recording the new problems and their possible solutions, by the DFMEA method and using the form.

The invention further relates to a DFMEA form or document device for analyzing faults and failures in the design of electronic apparatus and devices. A data-entry mask is provided to record some information concerning the performed analysis and at least a portion of the recording form is displayed to a user in an electronic display format. The portion includes at least one pushbutton or link button for connection to a file-associating tool that attaches electronic format files concerning the information to be entered through the mask.

The features and advantages of the method and the document device according to the invention will become apparent from the description of embodiments thereof, given by way of non-limiting examples with reference to the accompanying drawings.

**BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS**

**FIG. 1** shows a schematic example of a display mask for a data selection and entry form implementing the inventive method;

**FIG. 2** shows a schematic example of a more detailed display mask allowing the user to enter the initial data and information concerning a DFMEA project according to the inventive method;

**FIGS. 3A AND 3B** summarize in tabular form the information made available by the form of **FIG. 2**;

**FIG. 4** is a schematic view of a portion of a data-entry mask provided by the inventive method;

**FIG. 5** is a schematic view of another portion of a data-entry mask provided by the inventive method;

**FIG. 6** is a schematic view of a continuation portion of the data-entry mask shown in **FIG. 5**.

**DETAILED DESCRIPTION OF THE INVENTION**

In the drawing views, a display mask of a data and information recording system implementing the DFMEA fault and failure analysis method is generally shown at **1**. The recording system is mainly used in designing electronic apparatus and devices.

The mask 1 can be viewed as the initial representation of certain controls adapted to interact with a database wherein the items of information gathered by the analysis method of this invention are stored as they become available.

More particularly, shown in the example of **FIG. 1** is a portion of a starting form or document device 3. This form is provided preferably in an electronic display format, although there is no reason why it could not be provided on another type of support, e.g., a paper support.

The form 3 is derived from a typical DFMEA form, but has been modified in a qualifying manner according to this invention. More particularly, shown schematically in **FIG. 2** is the construction of a data entering portion 2 of the DFMEA form 3 according to the invention. This entering portion 2 is accessed selecting the choice “Create a new DFMEA project” in **FIG. 1**.

The portion 2 includes a grid 4 that includes a portion 5 of increasing severity for each parameter, block, or
device that allows to select the item or function under analysis. Then, at least three potential failure levels may be indicated and namely: a general failure mode; the effect of the failure and the potential cause or mechanism of the failure.

0064] Three additional levels dependent on the number of impacted applications; and namely: a current control; a recommended action and the action taken.

[0064] The FIGS. 3A and 3B report an example of a possible filled-in entering portion 2.

[0065] Moreover, these figures report an occurrence portion 6 including at least three different columns dependent on the DFMEA fill-in phase, which columns may be:

[0066] a first or “Design” column 7 for a qualitative estimate in conformity with the standard;

[0067] a second or “Qualification” column 8 for a percent estimate of output losses at the EWS (Electrical Wafer Sort) check; and

[0068] a third or “Post-qualification” column 9 for an estimate of faultiness in ppm, e.g., returns from field.

[0069] The features of each form 3 will now be reviewed in greater detail.

[0070] 1) The form 3 can be accessed from computer systems used to interconnect electronic processors, e.g., on an intranet network that can be accessed from any authorized peripheral units of a company.

[0071] 2) Access to each form 3 is controlled by a special password level that allows some of the information to be accessed for reading or writing, depending on the password level that has been allocated.

[0072] 3) A form-dedicated search motor can extract information from all the DFMEA forms in existence to place them at the user’s disposal.

[0073] As shown in FIG. 1, each form 3 has an entry mask 10, preferably in the PDF format, although alternative formats may be used for the same purposes. The entry mask 10 has two entry levels, namely:

[0074] a first level 11 for accessing projects that have been previously authorized; and

[0075] a second level 12 for accessing the search engine.

[0076] The procedure for accessing either levels will now be described briefly.

[0077] First level: once a special password is edited, the appropriate FMEA can be filled in by means of an “edit current settings” control; in order to make changes to the user levels and the document protection, an “open this project” control is used for editing the DFMEA document. The mask 15 of FIG. 4 is accessed by the “open this project” command and will now be described in greater detail:

[0078] The mask 15 is divided into two portions 13, 14. The portion 13 overhead allows the characteristics of the document to be set by filling it with the following series of information items:

[0079] personal information 19;

[0080] revision date 16;

[0081] status 17 (either editable or frozen, according to whether in progress or frozen);

[0082] protection levels 18, for any reserved accesses to a prearranged list (Readers Man);

[0083] Three pushbutton controls are also accessible in portion 13 of the mask 15, which serve the following functions:

[0084] View FMEA: allows the document to be edited in the html format, with a prearranged layout of pages, where data about the project and the project team is entered; the tabular format of this utility is shown in FIG. 4 along with all the items concerned;

[0085] Gen Package: allows the document to be compacted, and its files consolidated into a single file;

[0086] Readers Man: allows the document to be accessed to a pre-reserved list.

[0087] The portion 14 underneath makes the DFMEA easy to fill in, and allows files to be attached as may be found necessary in order to furnish the user with all the technical details of concern.

[0088] With reference to FIG. 5, it can be seen that the portion 14 of the mask 15 comprises:

[0089] an “Item” section 22 to set the line of the DFMEA form that is to be edited (e.g., 1 of 2);

[0090] an “Item/Function” section 23 to set the block or the function of the device affected by the fault mode; this field is preset since it is to be searched by the dedicated engine;

[0091] a “Potential Failure Mode” section 24 and a “Potential Effects of Failure” section 25, which are also provided for by standard FMEA; and

[0092] a “File” section 26 including a pushbutton for connection to the item that has been described briefly in text form; this pushbutton allows a file, report, schematic, picture, or whatever else may be necessary to understand the item, to be attached. The formats of the attached files may be any desired types, including the .pdf, .html, .gif, .jpeg, .txt, and .tar formats.

[0093] Shown in FIG. 6 is a continuation portion 14A of the mask 15, which portion 14A could not be represented in one diagram for page layout reasons.

[0094] This continuation portion 14A includes a plurality of “Recommended Actions” sections 27. A text description of the recommended actions can be appended a file that may be any of three different types, such as the following:

[0095] Schematics, Measures, or Simulations, according to the type of information that is entered.

[0096] A following section 28 allows the types of the actions actually taken to be recorded. The section 28 can be attached a file, classed by the type, similar as section 27.

[0097] Once the “File” part is accessed, the system allows all the files present in the processor to be accessed and displayed using a conventional browse function.

[0098] After a file is selected, the system allows it to be attached to the respective DFMEA area of origin, i.e., the area in which the files had been accessed by the “File” pushbutton.
Once all the items to be entered to the DFMEA are saved, and the respective files attached, the document is recorded at its dedicated DFMEA location.

To fight faults that have already been analyzed in connection with previous projects, it is important that different users be timely made aware of any problems encountered, for example, with devices, processes, or projects, as well as of their failure modes.

How the information is handled within each form 3 will now be explained. Besides handling information, the form 3 allows the informational contents of various DFMEAs to be shared and retrieved.

The method of this invention provides a few innovative guidelines to the implementation of a DFMEA technique by means of the form 3 just described. These guidelines are listed here below:

1) detecting and recording, by the DFMEA method on the form 3, previously encountered problems and their solutions, by the application of a keyword analysis at a function and/or keyword level;

2) taking into account all past application failures occurred in similar applications;

3) analyzing major changes and/or innovations, and any integration of blocks or parts, undergone by a new device from other devices, in order to foresee any potential occurrence of new problems in the new device.

At least three revisions of the DFMEA form are envisaged, corresponding to as many stages of maturity of the new device. In a preferred embodiment, three revisions are provided as listed here below:

a) Design;

b) Qualification; and

c) Production—Post-qualification.

For greater convenience in searching previous records and entering new data, a search motor is provided in which all the fields are present that may become the targets of a possible search criterion; some fields are pre-filled in and show a list of possible items, while other fields are left blank.

Once a search criterion is keyed in, the system extracts those items which correspond to the selected search criterion, along with any files attached thereto, from all the existing DFMEA records.

Using the search motor, a DFMEA by the function/block can be formed from existing data in the system.

In this way, a user on the point of designing an electrostatic discharge (ESD) protection block, for example, can obtain in DFMEA format the history of problems encountered with common products or processes and the solutions provided, with the addition of any appropriate technical topics concerning modified schematic files, simulations devised, measurements made, etc.

The method described above affords a number of advantages among which are:

1) a new approach to the use of the DFMEA technique so as to avoid the re-occurrence of events in a fail-prevention environment;

2) shared DFMEA information in a dedicated web environment;

3) efficient handling of the DFMEA form, by providing file linking facilities for attaching technical information and enhancing the document usefulness; and this in a web environment fill-in system wherein the document control and access rules are implemented automatically;

4) information access and flow controlled at various read/write levels using a search motor that is detailed and layered to utilize the informational contents so as to avoid re-occurrence of problems; and

5) DFMEA implemented by the key block/function.


From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

1. A design failure mode effect analysis (DFMEAs) device for analysis of faults and failures in the design of electronic apparatuses and devices, comprising:

   a data-entry mask to record some information concerning the analysis and in which at least a portion of said data-entry mask is displayed to a user in an electronic display format; and wherein said portion includes at least one link button; and

   a file-associating tool structured to attach to said data-entry mask electronic format files concerning the information to be entered through said data-entry mask, the link button enabling connection to the file-associating tool.

2. A DFMEA device according to claim 1, wherein the data-entry mask includes a portion that enables entry of text descriptions of a plurality of recommended actions for correction of the faults and failures.

3. A DFMEA device according to claim 1, wherein the data-entry mask enables the following information items to be introduced:

   personal information;

   a revision date for revising electronic apparatus and devices;

   a status of the design of the electronic apparatus and devices; and

   protection levels for controlling access to the information concerning the analysis.

4. A DFMEA device according to claim 1, further comprising a search engine that allows searching any field of said data-entry mask.

5. A DFMEA device according to claim 1 wherein the data-entry mask includes a portion for recording past design problems, the DFMEA device further comprising:
means for recording keywords in a database associating each of said past design problems to a corresponding keyword.

6. A DFMEA device according to claim 5, further comprising:

means for associating data in the database concerning each of said past design problems, including information concerning past failures that occurred in similar applications.

7. A DFMEA device according to claim 1, further comprising means for entry of at least three revisions of the data-entry mask corresponding to maturity stages of said designed device.

8. A DFMEA device according to claim 7, wherein said at least three revisions are performed at the following stages:

design of the designed device;

qualification of the designed device; and

production of the designed device—post-qualification.

9. A design failure mode effect analysis (DFMEA) method for analysis of faults and failures in the design of electronic devices, comprising:

displaying in an electronic display format at least a portion of a data-entry mask to record some information concerning the analysis, wherein the portion includes a link button;

in response to selection of the link button, enabling a user to indicate an electronic format file desired to be attached to the data-entry mask; and

attaching to the data-entry mask the electronic format file indicated by the user.

10. The method of claim 9, wherein the data-entry mask includes a portion that enables entry of text descriptions of a plurality of recommended actions for correction of the faults and failures.

11. The method of claim 9, wherein the data-entry mask enables the following information items to be introduced:

personal information;

a revision date for revising electronic apparatus and devices;

a status of the design of the electronic apparatus and devices; and

protection levels for controlling access to the information concerning the analysis.

12. The method of claim 9, further comprising searching any field of the data-entry mask.

13. The method of claim 9, further comprising:

detecting and recording, using the data-entry mask, past design problems.

14. The method of claim 13, further comprising:

recording keywords in a database associating each of said past design problems to a corresponding keyword.

15. The method of claim 14, further comprising:

associating data in the same database concerning each of said past design problems, including information concerning past failures that occurred in similar applications.

16. The method of claim 9, comprising at least three revisions of the data-entry mask corresponding to maturity stages of said designed apparatus or device.

17. The method of claim 16, wherein said at least three revisions are performed at the following stages:

design of the designed apparatus or device;

qualification of the designed apparatus or device; and

production of the designed apparatus or device—post-qualification.

18. An electronic design failure mode effect analysis (DFMEA) form for analysis of faults and failures in the design of electronic devices, comprising:

means for causing display in an electronic display format of at least a portion of a data-entry mask to record some information concerning the analysis, wherein the portion includes a link button;

means for responding to selection of the link button by enabling a user to indicate an electronic format file desired to be attached to the data-entry mask; and

means for causing the electronic format file indicated by the user to be attached to the data-entry mask.

19. The electronic DFMEA form of claim 18, wherein the data-entry mask includes a portion that enables entry of text descriptions of a plurality of recommended actions for correction of the faults and failures.

20. The electronic DFMEA form of claim 18, further comprising means for searching any field of the data-entry mask.

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