

- [54] **SPEED CONTROLLED TIMING LIGHT**
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- [52] U.S. Cl. **324/16 R, 324/17**
 [51] Int. Cl. **F02p 17/00**
 [58] Field of Search **324/15-18;**
 73/116-117.3, 118, 119 R, 119 A

FOREIGN PATENTS OR APPLICATIONS

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[57] **ABSTRACT**

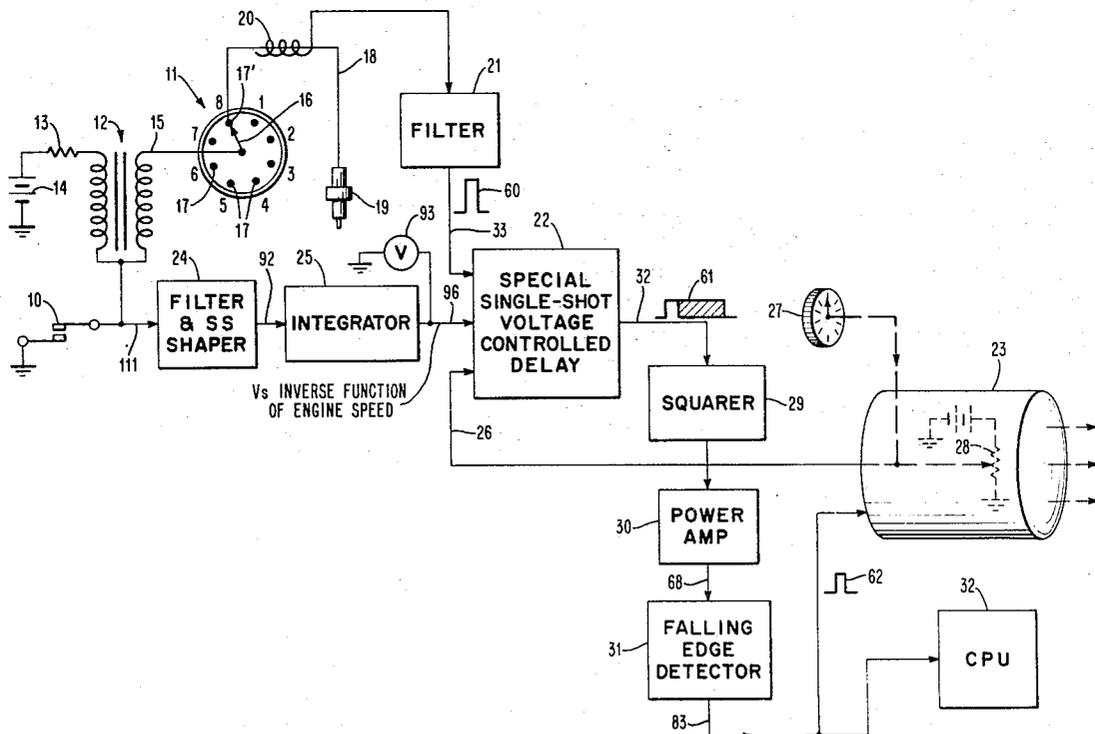
A control circuit for an internal combustion engine timing light includes an integrating circuit for producing a voltage inversely proportional to engine speed and a delay circuit which is activated by the firing of the last cylinder of the engine to initiate a time delay pulse varying in amount of delay as a function of engine speed in response to the voltage. The delay circuit has an output coupled through a falling edge detector which produces an output at the end of the time delay to actuate the timing light.

6 Claims, 6 Drawing Figures

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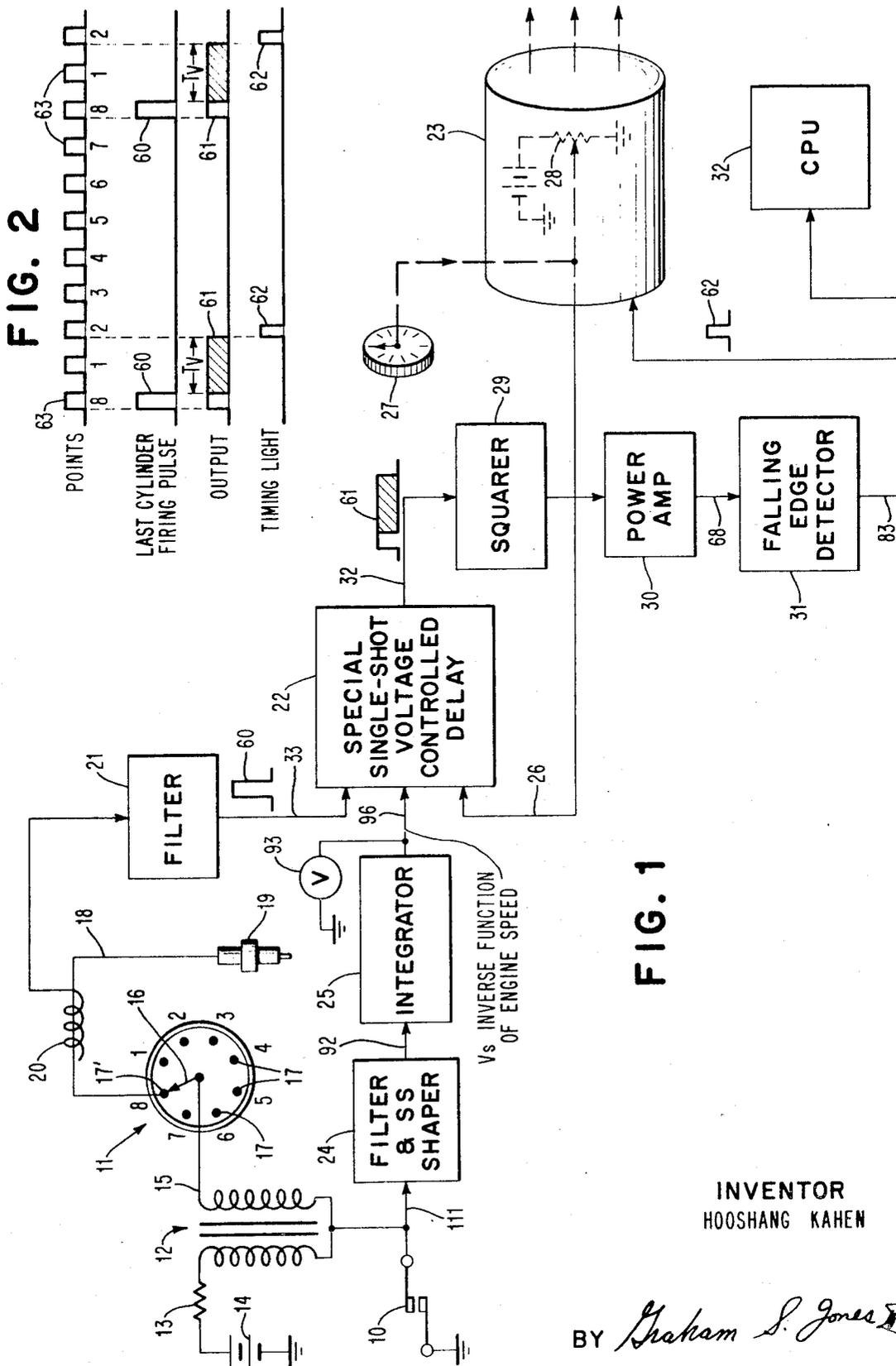
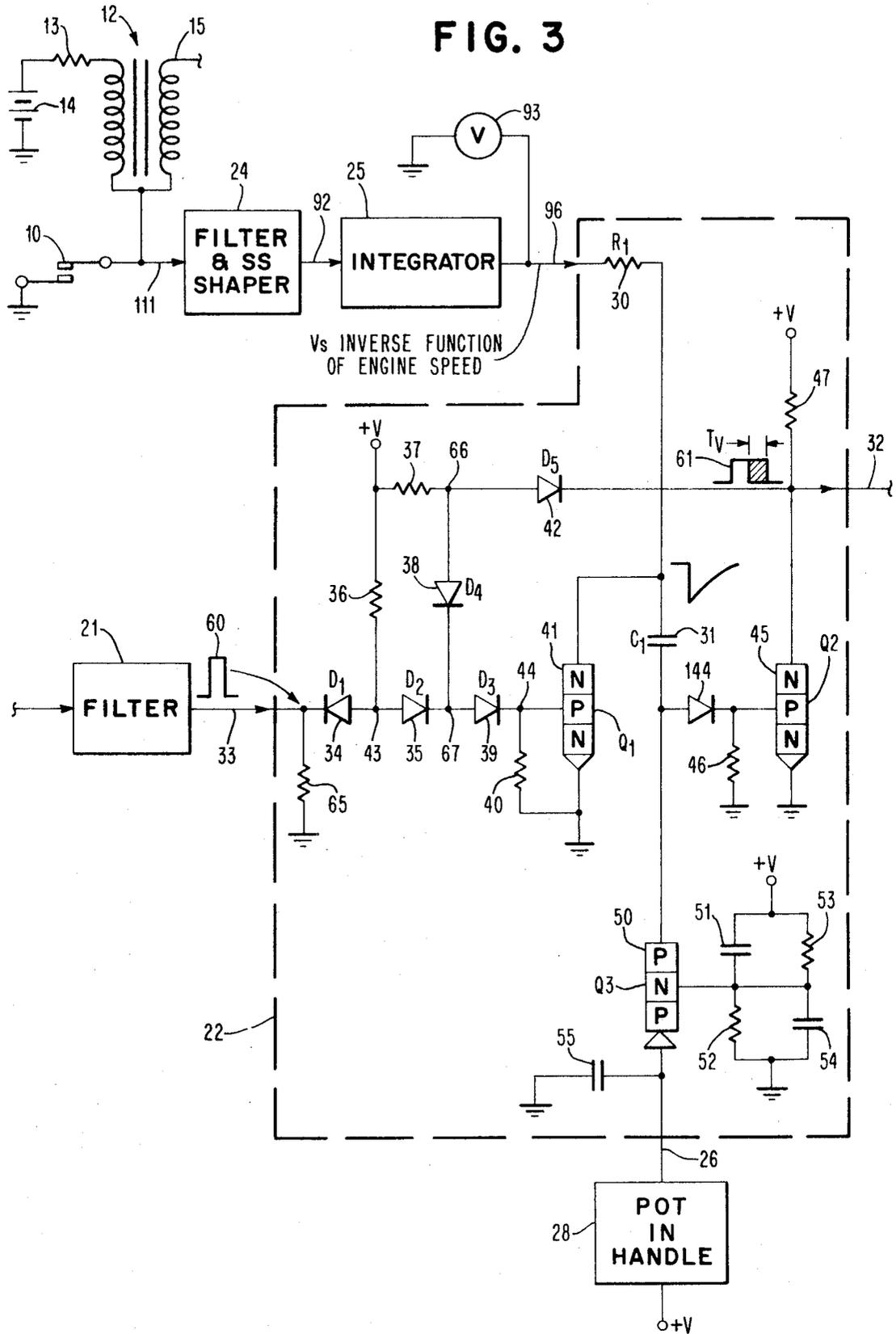


FIG. 1

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FIG. 3



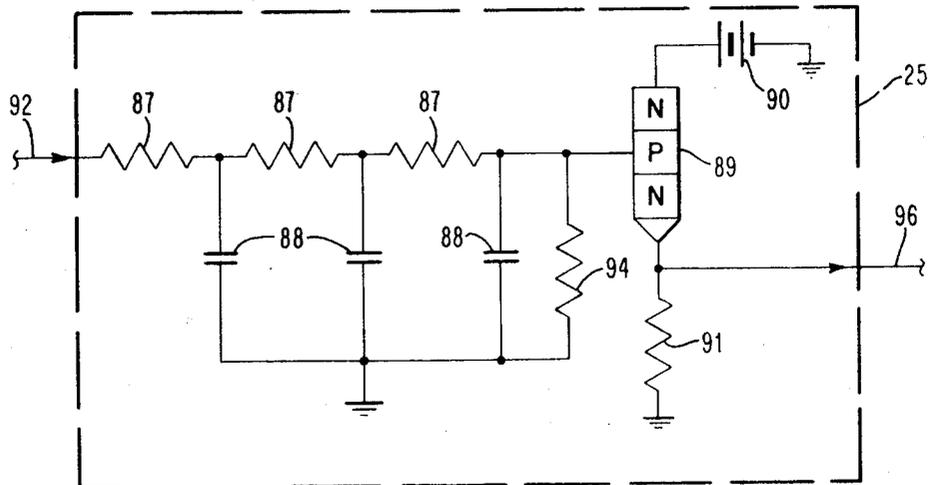
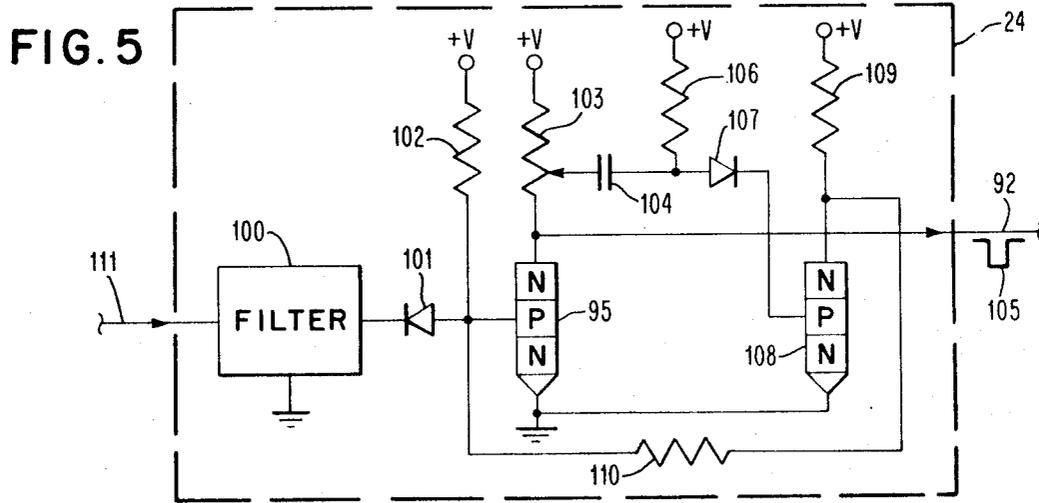
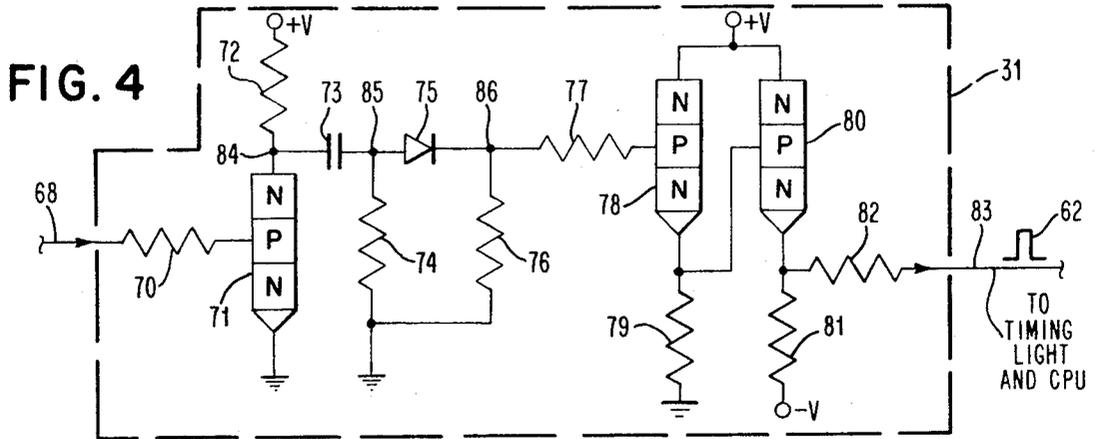


FIG. 6

SPEED CONTROLLED TIMING LIGHT BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to internal combustion engine timing light control circuits.

2. Description of the Prior Art

It is known in the prior art that since the ignition pulse from cylinders greater than the first cylinder merely fire at specific degree intervals relative to the first cylinders as specified by the cam shaft, therefore, for generating pulses used for timing purposes, all that is needed to generate timing pulses for a cylinder is to delay an ignition firing pulse to the preceding cylinder regardless of whether an advanced or a retarded position is desired. In practice, the output of the secondary of the coil of an automobile is passed through an adjustable delay unit connected in series with the coil. That combination is used to provide adjustable delay of one firing position or 90° in a four cylinder car, 60° in a six cylinder car or 45° in an eight cylinder car. Then the output of the delay unit is presented to the input of an additional coil which responds as if the delay unit were the points of the car, and the high voltage is then distributed through the distributor in the usual fashion. In addition, there is a control employed for adjusting the unit for the number of cylinders and a limited number of fixed engine test speeds. Another control adjusts the ignition to provide the desired retarding or advance for the selected engine and engine speed.

A problem associated with the prior art is that no provision has been made for automatic adjustment of the time delay afforded by the timing light control circuit so that the timing light would provide accurate timing for all speeds continuously regardless of changes in engine speed. While there is provision for adjustments of the timing to a few previously selected speeds in the prior art, a manual control is required, which requires use of a tachometer to make the engine speed adjustment accurately, and which requires careful adjustment of speed to set values and which increases the possibility of error in measurement. This is especially true where the engine is to be operated at several successive speeds, and time will be wasted by unnecessary manipulation in compensating for the shortening of the interval between firing of cylinders with increasing engine speed.

SUMMARY

In accordance with this invention, apparatus is provided for controlling a timing light for an internal combustion engine for producing a signal for triggering the timing light in timed relationship with the high voltage distributor output pulses. A variable time delay circuit is provided having a speed input for receiving an input signal indicating engine speed and a synchronization input for receiving a timing input signal. The variable time delay circuit provides an output signal which follows the synchronization input by a time interval which varies as a function of the engine speed input signal.

Further, in accordance with this invention, apparatus is provided for controlling the timing light for an internal combustion engine for producing a signal for triggering the timing light in timed relationship with the high voltage distributor output pulse. The apparatus includes an integrator circuit for coupling to the points of

the distributor for providing an output voltage related to input speed. A monostable circuit has a speed signal input and a triggering input connected to receive a timing pulse from firing of a spark plug and it is adapted to become active in response to a timing pulse and to remain active for a variable time delay determined by a timed delay circuit responsive to an input signal supplied to the speed signal input. An output signal pulse generator is coupled to the output of the monostable circuit to provide a pulse at the end of the active state of the monostable circuit.

An object of this invention is to provide a control circuit for an internal combustion engine timing light which includes a means for adjusting the time of firing the timing light as a function of engine speed while providing for retardation and advance relative to top dead center position of the number one cylinder, automatically without requiring a manual adjustment as engine speed changes.

The foregoing and other objects, features and advantages of this invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an overall block diagram of an embodiment of a timing light control system in accordance with this invention.

FIG. 2 shows timing relationships between various elements of the system by showing pulses which occur as a function of time.

FIG. 3 shows a detailed circuit diagram of the special, single-shot, voltage controlled, delay circuit shown in FIG. 1 connected to several other elements of the circuit of FIG. 1.

FIG. 4 is a detailed circuit diagram of a falling edge detector of the kind employed in the system of FIG. 1.

FIG. 5 shows details of the filter and single-shot shaper circuits of FIG. 1.

FIG. 6 shows details of the integrator of FIG. 1.

DESCRIPTION

Referring to FIG. 1, points 10 comprising electrical contacts within the distributor 11 (shown separately here for convenience of illustration) of an internal combustion engine are connected between one end of the windings of a transformer coil 12 which is connected at the opposite end of its primary to a resistor 13 and the battery 14 of the internal combustion engine. The battery 14 is connected at its opposite end to ground. Periodic opening of the points 10 as shown at the top of FIG. 2, once for each cylinder, in sequence, generates pulses in the primary and secondary of the coil 12 yielding a high voltage pulse at the opposite end 15 of the secondary of the coil 12 which high voltage pulse is connected to the rotor 16 of distributor 11 which provides distribution of pulses to a number of terminals 17 equivalent to the number of cylinders in the engine, conventionally. Terminal 17' associated with the eighth cylinder of the engine (which in a sequence of the eight cylinders in an eight cylinder engine is considered the last to be fired) is connected by cable 18 to spark plug 19 for the eighth cylinder. Induction coil 20 couples the cylinder firing pulses on cable

18 to the input of attenuating filter 21 which shapes the pulses and which couples filtered cylinder firing pulses 60 to an input of a special, single-shot, voltage-controlled, delay circuit 22.

The last cylinder firing pulse 60 shown on the second line in FIG. 2 is employed to commence a timing interval T_V shown on the output line on FIG. 2. The last cylinder firing pulse 60 as shown coincides with and is derived from the opening of the points for the eighth cylinder as shown by pulse 63 on the top line of FIG. 2. The delay circuit 22, shown in greater detail in FIG. 3, provides delay of the firing of a stroboscopic timing light 23 for an interval of time T_V shown in the shaded area of the output pulses 61 in FIG. 2. The time interval T_V permits timing of the firing of the light 23 prior to the top dead center position of the number one cylinder (advanced timing) or after that position (retarded timing) so that (for an eight cylinder engine) by utilizing the eighth cylinder firing pulse 60, the timing light may provide a broad range of timing light readings.

Another preceding cylinder can also be utilized to provide firing pulse timing if there is provided a time delay circuit which will yield a corresponding amount of time delay according to the number of additional cylinder positions involved. In fact, the number one cylinder can be used to provide spark plug firing pulses and then a counter can be connected to the points 10 to count the number of closures of the points 10 which will indicate the expected time of occurrence of firing of the last cylinder (e.g., 4, 6, 8, 10 or 12 cylinders, etc. depending upon the number of cylinders in the engine).

Another input to the delay circuit 22 is provided by the points 10, a filter and shaper 24 (FIG. 5) which provides an input voltage to integrator circuit 25 (FIG. 6) which will provide an output potential which is an inverse function of engine speed. The filter and shaper 24 includes a single shot circuit which serves as a pulse shaper, and the collector of the transistor in the single shot is connected to positive potential and to the output, which is connected to an integrator 25 which is discharged slightly by the single shot each time that it fires to reduce the potential at the output of the integrator 25 as a function of the frequency of closing of points 10. Voltmeter 93 measures the voltage on line 96 and is calibrated in RPMS to serve as a tachometer.

The output of integrator 25 is connected to another input of the delay circuit 22 to provide control of the length of the period of delay of the output from circuit 22 after pulse 60 to compensate for changes in engine speed so that the light 23 is caused to fire at the desired time in spite of the difference in speed of the engine from specified idling speeds.

In addition, line 26 is connected to delay circuit 22 to provide a biasing potential which will adjust the advance or retardation of firing of the light 23 so that the light will fire when the marker points to the top dead center position on the flywheel of the engine, but the timing will actually be retarded or advanced in angle by the number of degrees indicated on knob 27. Knob 27 adjusts the tap of potentiometer 28 which is connected between positive bias and ground.

Delay circuit 22 yields a positive output pulse 61 which is passed through squarer circuit 29 and power amplifier 30 which connects to falling edge detector

circuit 31 (FIG. 4) which responds to the trailing edge of the output square wave 61 shown on the third line of FIG. 2 to produce a pulse 62 which fires the timing light 23 and signals the CPU 32 of a computer or any other kind of data processing system.

In general then, a timing light for an internal combustion engine for an automobile is modified to include a potentiometer in the handle which is adapted to be used to adjust the amount of advance or retardation of the time at which the timing light is illuminated relative to the firing of the number 1 cylinder of the engine. A circuit is employed for the purpose of providing voltage controlled delay of the time at which the timing light operates. Whereas normally the timing light is operated by means of the pulse from the distributor for the number 1 cylinder, in this case, the pulse from the distributor for the last cylinder is employed to provide an input to the voltage controlled delay circuit. Concurrently, the points of the distributor in the primary circuit of the coil are employed to provide a pulse to the input of an integrator which produces an output voltage which is a function of engine speed. The output voltage of the integrator is also supplied to the voltage-controlled, delay circuit which includes a single shot or monostable circuit. Normally, the monostable circuit provides a low voltage output. In response to a last cylinder pulse, it immediately produces a positive output which will persist for a period of time determined as a function of the engine speed and as manually selected by the operator by means of the potentiometer in the handle of the timing light. At the end of the time delay which is provided as a function of the engine speed and in response to adjustment by means of the potentiometer, the output of the single shot will revert to its initial low voltage. This output signal will vary from full advance to the timing of the eighth cylinder (or the last cylinder) to retardation by an amount up to the period of time between firing of one cylinder and the next, e.g., from firing of the number 1 cylinder up to the time of firing of the number 2 cylinder. The trailing edge of the delay output pulse from the voltage controlled, delay, single shot will be passed on by a falling-edge detector circuit which functions for the purpose of passing only the falling edge of a square wave output. This falling edge will be employed for the purpose of actuating the timing light and providing a timing signal to a timer in the CPU or central processing unit of a computer which measures time and calculates engine degrees. The CPU prints out the value of the delay or advance provided in engine degrees.

Referring to FIG. 3, the potential from integrator 25, which is dependent upon engine speed, is coupled through resistor R_1 30 to charge capacitor C_1 31 to a potential which will delay the timing of the end of a pulse on line 32 by an amount of time proportional to the potential which in this embodiment has been selected to vary inversely with the speed of the engine, but which can be the reverse or can vary directly if desired by reversing potentials, etc.

The last cylinder pulse 60 received at input 33 from filter 21 is coupled to the cathode of diode D_1 34 and resistor 65 connected at its opposite end to ground. The anode of diode D_1 34 is connected to the anode of diode D_2 35 and through a resistor 36 to positive bias. The resistor 37 is connected from positive bias to point

66 connected to the anodes of diode D_4 38 and D_5 42. The cathode of diode D_5 is connected to output 32 and the collector of NPN transistor Q_2 45. Diode D_4 38 has its cathode connected to point 67 connected to the cathode of diode D_2 35 and the anode of diode D_3 39, whose cathode is connected to point 44 connected to the base of NPN transistor Q_1 41 and to ground through resistor 40 and to the emitter of normally-off, NPN transistor Q_1 , 41. The collector of transistor Q_1 41 is connected to the junction of resistor R_1 30 and capacitor C_1 31. In operation, normally diode D_1 34 is conducting through the low value resistance of resistor 65 to hold point 43 near ground in the absence of a pulse 60 on line 33. A pulse on line 33 turns off diode D_1 34 thereby raising the potential of point 43 at the anode of diode D_2 35 which causes a bias sufficient to turn on diode D_2 35 and diode D_3 39 which is sufficient to turn on the transistor Q_1 41 by raising the potential on the base connected to point 44 well above the potential of its emitter which is connected to ground. As transistor Q_1 41 is turned on, the collector potential falls near the emitter potential, i.e., ground, and pulls the upper end of capacitor C_1 31 down near ground retaining the charge thereacross to drive the opposite end of capacitor C_1 31 and the anode of diode 144 connected thereto negative, thereby driving the base of transistor Q_2 45 below cutoff. The base of transistor Q_2 45 and resistor 46 are connected to the cathode of diode 144. The emitter of NPN transistor Q_2 , 45 and the opposite end of resistor 46 are grounded. The collector of transistor Q_2 45 is connected to the cathode of diode D_5 42 and output line 32 as well as to resistor 47 connected at its opposite end to positive bias. When transistor Q_2 45 is turned off by transistor Q_1 41 as described above, the collector of transistor Q_2 45 rises abruptly thereby yielding the leading edge of a square wave 61 on line 32.

NPN transistor Q_3 50 has its collector connected to the junction of capacitor C_1 31 and diode 144. Its base is connected through the parallel combination of capacitor 51 and resistor 53 to positive bias and through the parallel combination of resistor 52 and capacitor 54 to ground. The emitter is connected through capacitor 55 to ground and directly to the output of potentiometer 28 by line 26. Transistor Q_3 provides isolation of potentiometer 28 from capacitor C_1 31 and serves to control the rate of flow of current therethrough serving to discharge and then slightly reverse the charge in the capacitor C_1 31 when the capacitor is driven down to turn off transistor Q_2 . When capacitor C_1 31 is sufficiently discharged through transistor Q_3 50, then diode 144 will conduct turning on transistor Q_2 45 to end the square wave 61 on line 32.

It should be noted that the discharge time for capacitor C_1 31 will vary as a function of its initial voltage as set by integrator 25 and by the adjustment of transistor Q_3 50 by the potentiometer 28 which can increase or decrease the delay time T_1 to control timing in terms of advance or retardation of the timing light 23.

When transistor Q_2 45 turns on, that clamps the base of transistor Q_1 41 near ground by means of diodes D_3 39, D_4 38, and D_5 42 by placing a low potential on the cathode of diode D_5 42 which increases current flow therethrough to raise the IR drop through resistor 37

and to lower the potential on junction 66 to draw current away from the diodes D_4 38 and D_3 39 and lower the potential at point 44. Also, at that time since pulse 60 has then ended diode D_1 34 conducts, thereby holding diode D_2 35 back biased so transistor Q_1 41 turns off.

Referring to FIG. 4, a falling edge detector circuit 31 is shown.

The input line 68 is connected to resistor 70 which is connected to the base of NPN transistor 71, whose emitter is connected to ground and whose collector is connected to point 84. Point 84 is connected to positive bias through resistor 72 and to point 85 by capacitor 73. Point 85 is connected to ground through resistor 74 and to point 86 through diode 75 which conducts from point 85 to point 86. Point 86 is connected to ground through resistor 76 and to the base of NPN transistor 78 through resistor 77. The collectors of NPN transistors 78 and 80 are connected to positive bias. The emitter of transistor 78 is connected to emitter follower resistor 79 and to the base of transistor 80. The emitter of transistor 80 is connected to resistor 81 and to output line 83 through resistor 82. Resistor 79 is connected at its opposite end to ground and resistor 81 is connected at its opposite end to negative bias. When the timing pulse 61 commences, a positive potential at input 68 turns NPN transistor 71 on, which produces a negative pulse at point 84 that is blocked by diode 75 so no output signal is passed to output line 83. When delay pulse 61 ends, NPN transistor 71 is turned off thereby generating a positive collector pulse at point 84 which passes through capacitor 73, diode 75, and resistor 77 to turn on emitter follower 78 and to provide amplification of the pulse on emitter follower 80, which amplified pulse 62 is passed to output line 83 to the timing light 23.

FIG. 5 shows the filter and single shot shaper 24 including input line 111 connected to a filter 100 for shaping the pulse provided by opening of points 10, a diode 101 for coupling the pulse to the base of NPN transistor 95 by blocking current through resistor 102 connected between positive bias and the base of transistor 95 which current normally flows through diode 101 and through the filter 100 to ground. The transistor 95 has its collector connected to positive bias through potentiometer 103 and its emitter connected to ground. The output line 92 is connected to the collector of transistor 95.

The pulse on line 111 turns transistor 95 on lowering its collector to generate a negative pulse 105 on line 92 which tends to discharge the capacitors 88 in integrator circuit 25. Capacitor 104 is coupled between potentiometer 103 and resistor 106 and the anode of diode 107. Resistor 106 is connected to positive bias at its opposite end. The cathode of diode 107 is connected to the base of transistor 108 whose emitter is connected to ground and whose collector is connected through resistor 109 to positive bias. The collector of transistor 108 is also connected through feedback resistor 110 to the base of transistor 95. When transistor 95 is turned on, the base of transistor 108 is driven below cutoff through capacitor 104 and diode 107. After an RC time constant capacitor 104 charges until diode 107 conducts so the base of transistor 108 turns on, thereby turning transistor 95 off by coupling a lower potential

from the collector of transistor 108 to the base of transistor 95. This will coincide with the end of the input pulse on line 111 which will permit diode 101 to conduct, also, driving transistor 95 off.

FIG. 6 shows an integrator circuit for smoothing the output of the single shot 24. Accordingly, three resistors 87 are connected in series between the input and the base of NPN emitter follower transistor 89. The junctions of resistors 87 with each other and with the base are connected to ground through the capacitors 88 which charge towards positive bias in the absence of negative pulses on line 92. Charging current flows from the collector of the transistor 95, when it is off. Thus, the more transistor 95 is off, the more positive is the potential supplied by capacitors 88 to the base of transistor 89 and the higher the potential on emitter follower resistors 91 will be, thereby providing a higher potential to capacitor C₁ 31. Resistor 94 is connected between the base of transistor 89 and ground to bias the base of emitter follower transistor 89.

What is claimed:

1. Apparatus for controlling a timing radiation source for an internal combustion engine for producing a signal for triggering said source in timed relationship with a high voltage distributor output pulse comprising:
a timing radiation source,
variable time delay means having a speed input for receiving an input signal indicative of engine speed and a synchronization input for receiving a timing input signal,
said variable time delay means providing an output signal following said synchronization input by a time interval varying as a function of a signal received at said speed input,
output means for coupling said output signal to said timing radiation source coupled to said delay means,
internal combustion engine electrical contact points operable in synchronism with said engine, signal means for generating a signal dependent upon a pulse rate having a speed indicating output coupled to said speed input of said delay means,
means for coupling said points to said signal means for providing pulses as a function of engine speed.
said synchronization input being coupled to a said high voltage output of said distributor.

2. Apparatus in accordance with claim 1 including

internal combustion engine electrical contact points operable in synchronism with said engine, signal means for generating a signal dependent upon a pulse rate having a speed indicating output coupled to said speed input of said delay means,

means for coupling said points to said signal means for providing pulses as a function of engine speed.

3. Apparatus in accordance with claim 1 wherein said output means comprises means for detecting the trailing edge of a pulse.

4. Apparatus in accordance with claim 3 wherein said means for detecting includes an output circuit coupled to the triggering input of said timing light.

5. Apparatus in accordance with claim 4 wherein said timing light includes a potentiometer connected to an input of said delay means for adjusting the delay provided by said means to advance or retard said trailing edge relative to high voltage pulses coupled to said synchronization input.

6. Apparatus for controlling a timing radiation source for an internal combustion engine for producing a signal for triggering said source in timed relationship with a high voltage distributor output pulse comprising:
a timing radiation source,

variable time delay means having a speed input for receiving an input signal indicative of engine speed and a synchronization input for receiving a timing input signal,

said variable time delay means providing an output signal following said synchronization input by a time interval varying as a function of a signal received at said speed input,

output means for coupling said output signal to said timing radiation source coupled to said delay means

an internal combustion engine high voltage distributor having a high voltage input and a plurality of high voltage outputs,

said synchronization input being coupled to a said high voltage output of said distributor,

internal combustion engine electrical contact points operable in synchronism with said engine,

signal means for generating a signal dependent upon a pulse rate having a speed indicating output coupled to said speed input of said delay means,

means for coupling said points to said signal means for providing pulses as a function of engine speed.

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