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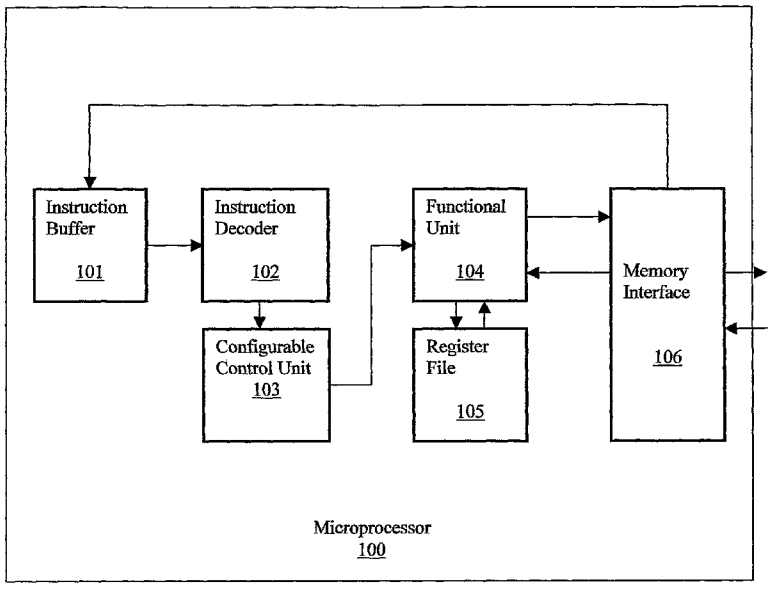
(54) **Title:** A MICROPROCESSOR WITH A CONFIGURABLE CONTROL UNIT



(57) **Abstract:** The invention relates to a microprocessor with a configurable control unit which is dynamically configurable. The information about when to read the operands, when to perform operations and when to write results are specified in the instructions of the microprocessor as control attributes. The control unit executes these instructions based on these attributes. This allows for easy configuration of the microprocessor and simplifies microprocessor design.

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A MICROPROCESSOR WITH A CONFIGURABLE CONTROL UNIT

FIELD OF THE INVENTION

The present invention relates to the field of microprocessors and more specifically to configurable microprocessors. More particularly the present invention relates to a microprocessor with a configurable control unit .

BACKGROUND OF THE INVENTION

A typical microprocessor includes data paths containing registers and one or more execution units and a control path to coordinate the program execution. The control unit is responsible for fetching program instructions from memory, decoding the instructions, fetching data required for the operation from memory or registers, generating control signals to perform required operation and then writing the result to memory or register.

The complexity of the control unit of a microprocessor depends on the number of execution paths, number of instructions and the number of stages in execution of an instruction. One way to design a control unit involves representing the control logic entirely though the interconnections between the various components of the logic circuitry. A control unit designed using such a method is known as a hardwired control unit. In this type of control unit, the logic circuit is responsible for generating appropriate control signals for each processor cycle based on the input instruction and the current state. For each cycle one basic operation is performed as specified by the control signals.

In contrast to a hardwired control unit, a micro-programmed control unit stores

the control signals as microinstructions in a memory area within the control unit. For each processor instruction, a sequence of microinstructions will be fetched from this memory and corresponding control signals will be activated to perform the required operations. A micro-programmed control unit can represent more complex operations and can be modified by updating the micro-program memory with updated microinstructions. However, it is generally slower than a hardwired control unit.

In the existing prior art, it is not possible to configure the control logic once the microprocessor is developed. To overcome this limitation, the present invention describes a control unit, which can be configured using the control information specified in the program instructions themselves.

SUMMARY OF THE INVENTION

The present invention relates to a microprocessor having a configurable control unit . It describes a microprocessor with a control unit that can be configured dynamically. The machine instructions themselves provide the information about when operands have to be fetched, when the execution should take place and when result of the operation should be written back to register or primary memory. This greatly simplifies the control logic of the processor.

The instructions of the processor according to the invention include control information associated with the operation code (opcode) and the operands. This control information is provided as clock cycle count and cycle type attributes. The instruction decoder of the processor reads the instruction and decodes it. The control unit then selects the component (opcode or operand) of the instruction with cycle

count as zero and performs the associated operation as specified by the cycle type attribute. The cycle type attribute could have one of the values "read", "execute" or "write". If cycle type of the selected component is "read", then the corresponding operand is read from memory or register. If the cycle type of the component is "write", then the operand corresponding to the component is written to memory or register file. If the cycle type of the component is "execute", then the operation specified by the component is performed. Once a read, write or execute operation is performed, the control unit decrements the cycle counts of all components of the current instruction. This process is repeated till the instruction has no component with cycle count zero, which means that the instruction execution is complete and the next instruction is fetched from memory.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a microprocessor with a configurable control unit implemented in accordance with an embodiment of the invention.

FIG. 2 is a block diagram of the configurable control unit implemented in accordance with an embodiment of the invention.

FIG. 3 is a diagram of the instruction format of a microprocessor implemented in accordance with an embodiment of the invention.

FIG. 4 is a flow diagram of a method describing the steps involved in the execution of instructions on a microprocessor implemented in accordance with an embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMIENT

FIG. 1 shows a particular embodiment of the microprocessor with configurable control unit according to the present invention. The microprocessor 100 according to the described embodiment includes an instruction buffer 101 in which the instructions fetched from memory is placed, an instruction decoder 102, which decodes the instruction, a configurable control unit 103, which controls instruction execution, one or more functional units 104, a register file 105 for storing data and a memory interface 106, which interfaces with the system memory.

FIG. 2 shows the configurable control unit 103 in detail. The control unit 103 contains a component selector 201, which selects a particular component (operand or operation code) of the decoded instruction for execution. The control logic 202 generates control signals to read or write operands or to perform an operation. This is done based on the cycle type attribute specified for the component selected by the component selector.

FIG. 3 shows the format of instructions for the present microprocessor. Each instructions includes an operation code (opcode) 200 which specifies the operation performed by the instruction, opcode control attributes 201 which is a set of values for cycle count and cycle type for the opcode and one or more operands 202 and operand control attributes 203 which again is a list of values for cycle count and cycle type for the operand. The cycle count is a numerical value, which specifies when a particular component of the instruction should be considered for execution. A component with cycle count of zero is considered first for execution. The cycle counts for each component of an instruction are assigned in the order in which the components should

be executed. The ordering should be in such a way that operands are first fetched from register or memory. So, input operands (operands that should be read from register or memory) of the instruction should have lower cycle counts. Then the operation specified by the instruction should be performed. So the opcode component should get a cycle count that is higher than that the input operands. Finally, the higher values of cycle count are assigned to output operand (operands which store the result of the operation or operands which are updated as a side-effect of the operation). The cycle type attribute of a component of an instruction can take one of three values -viz. read, write and execute. The read cycle type is used for input operands, the write cycle type for output operands and the execute cycle type for operations. The instructions with the corresponding attributes are either generated by a compiler tool which specifies the cycle attributes for each component of the instruction or they could be written manually be a programmer. FIG. 3 only shows a high-level format of the instructions for the microprocessor according to the present invention. A person skilled in the art can implement the actual representation of the instructions or the present microprocessor in many different ways.

FIG. 4 shows the steps of a method according to the preset invention for executing instructions of the microprocessor according to the invention. The method starts at block 400 where an instruction is fetched from memory for execution and placed in the inst ruction buffer 101.

At block 401 the instruction is taken from the instruction buffer 101 and decoded in the instruction decoder 102. Here the type of operation and the operands are identified.

At block 402 the component selector 201 of the configurable control unit 103 selects the component 205 of the instruction with cycle count zero.

At block 403 it is checked if any component with cycle count zero is available. If no such component is found, then processing returns to block 401. If a component with cycle count zero is found at block 403, then control flows to block 404.

At block 404, the cycle type associated with the instruction component 205 is checked by the control logic 202. If it is found to be a read cycle, then at block 405, the control logic 202 generates read control signals 203 to read (fetch) the operand from memory or from the register file 105 as specified in the instruction. From block 405 control proceeds to block 410. If, at block 404, the control logic 202 finds that the cycle type is not "read", then control goes to block 406 instead of 405.

At block 406, the control logic 202 checks if the cycle type of the instruction component 205 is execute. If it is, then control passes to block 407, where the control logic 202 generates execute control signals 204 to execute the operation specified by the opcode of the instruction on an appropriate functional unit 104. After block 407 control proceeds to block 410. If, at block 406, the control logic 202 finds that the cycle type is not "execute", then control goes to block 408 instead of 407.

At block 408, the control logic 202 checks if the cycle type of the instruction component 205 is "write". If it is, then control flows to block 409, where the control logic generates write control signals 203 to write data to memory or register file 105 as it is dictated by the operand. From block 409 and also from block 408 if cycle type is not "write", control goes to block 410.

At block 410, the control logic 202 decrements the cycle counts of all the

components of the instruction by one and then control passes back to block 401 to select another component of the instruction for execution.

The method according to FIG. 4 is illustrated with an example below.

Consider an instruction that adds the contents of two registers and places the result in another register. This is a basic instruction supported by any microprocessor. This instruction can be represented in assembly code as follows:

ADD R1, R2, R3

Here, ADD is the operation code representing addition, R1 and R2 are the input operands and R3 is the output operand for holding the result of the addition. For the microprocessor according to the present invention, the above instruction is expanded by attaching attributes to each component of the instruction. This can be represented as follows:

ADD {cycle count=2, cycle type=execute}
R1 {cycle count=0, cycle type=read},
R2 {cycle count=1, cycle type=read},
R3 {cycle count=3, cycle type=write}

The cycle count and cycle type attributes attached to each component of the instruction is shown within braces {}.

The instruction is fetched from memory and placed in instruction buffer 101.

Then the instruction decoder 102 decodes it. The component selector 201 of the control unit 103 obtains the decoded instruction and selects the component with cycle count zero. In the above case, the selected component will be the operand R1. The control logic 202 then checks the cycle type of this component and generates read control signals 203. This causes the value to be read from register R1 in the register file 105. Then the control logic decrements the cycle counts of all the components of the instruction. At this stage, the attribute values for the instruction will be as shown below:

ADD {cycle count=l, cycle type=execute}

RI {cycle count=-I, cycle type=read}, R2 {cycle count=O, cycle type=read}, R3 {cycle count=2, cycle type--write}

The above process is repeated and now R2 is selected and its value is read from register file 105. Again, the cycle counts of all components are decremented by one to obtain the following state:

ADD {cycle count=O, cycle type=execute}

RI {cycle count=-2, cycle type=read}, R2 {cycle count=-I, cycle type=read}, R3 {cycle count= I, cycle type=write}

Now, the operation ADD has cycle count zero and this is selected by the component selector 201 and executed. During the next cycle, the operand R3 will

have cycle count zero and the result of the addition will be written to R3 in register file 105. After this stage, no component of the instruction will have a cycle count of zero. So, the next instruction is fe1ched from memory and this process is repeated.

The above description and diagrams describe the invention with respect to certain preferred embodiments. It will be understood that various modifications are possible to the embodiments without deviating from the broader scope of the invention. Accordingly, the specification and drawings should be considered illustrative rather than restricting the invention to a particular embodiment.

We Claim:

1. A microprocessor (100) with a configurable control unit (103) comprising :

a register file (105) containing a plurality of registers for storing data;

a plurality of functional units (104) for executing instructions of the microprocessor (100);

an instruction decoder (102) for decoding the instructions fetched from memory of the microprocessor(100);

an instruction buffer (101) for placing the instructions which are fetched from the memory; and

a memory interface (106) for reading and writing instructions and data to and/or from the memory;

wherein said configurable control unit comprises a component selector (201) and control logic (202) and is configured by control attributes provided in the instructions of the microprocessor.

2. The microprocessor as claimed in claim 1 wherein a compiler is provided for generating control attributes for each component of the instructions of the microprocessor (100).

3. The microprocessor as claimed in claim 1 wherein the component selector (201) is provided for selecting a component of a decoded instruction for execution based on the control attributes corresponding to said component; and the control logic is provided for generating appropriate control signals for performing operations based

on the control attributes corresponding to the component of the instruction selected by said component selector (201).

4. The microprocessor as claimed in claim 1 wherein the control attributes comprise cycle count and cycle type for each component of the instruction.

5. A method for controlling instruction execution on a microprocessor having a configurable control unit , said configurable control unit being based on control attributes of cycle count and cycle type corresponding to components of an instruction of the microprocessor, said method comprising the steps of:

(a) fetching an instruction from memory;

(b) decoding the fetched instruction;

(c) selecting a component of the instruction having cycle count control attribute as zero value by a component selector ;

(d) repeating step (a) if no component having a cycle count of value zero is located in step (c);

(e) generating read control signals to read operands specified by the component selected in step (c) from memory or register file when the cycle type attribute of said component is "read";

(f) generating execute control signals to execute the operation specified by the component selected in step (c) when the cycle type attribute of said component is "execute";

(g) generating write control signals to write operands specified by the component

selected in step (c) into memory or register file when the cycle type attribute of said component is "write";

(h) decrementing the cycle count control attributes of all components of the instruction by a value of one; and

(i) repeating step (c).

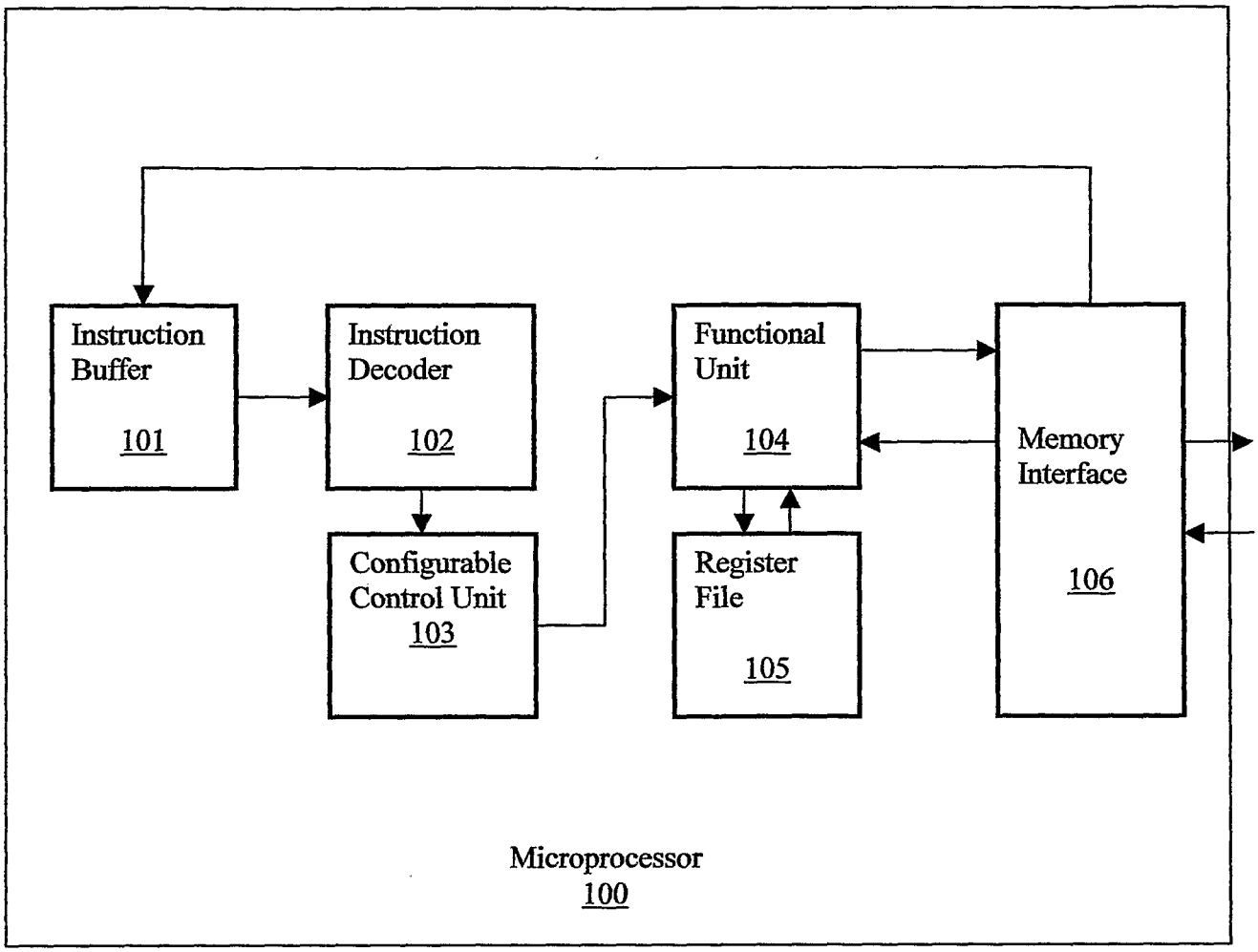
Instruction Buffer
101
Instruction Decoder
102
Functional Unit
104
Memory Interface
106
Configurable Control Unit
103
Register File
105
Microprocessor
100

FIG. 1

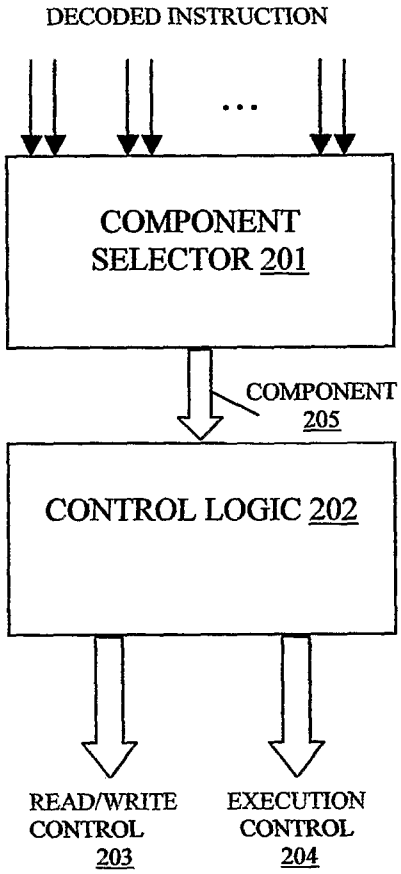
DECODED INSTRUCTION
...
COMPONENT SELECTOR 201
COMPONENT 205
CONTROL LOGIC 202
READ/WRITE CONTROL 203
EXECUTION CONTROL 204

FIG. 2

operation code (opcode) 300	opcode control attributes 301	operand 302	operand control attributes 303	operand	operand control attributes	...

FIG. 3

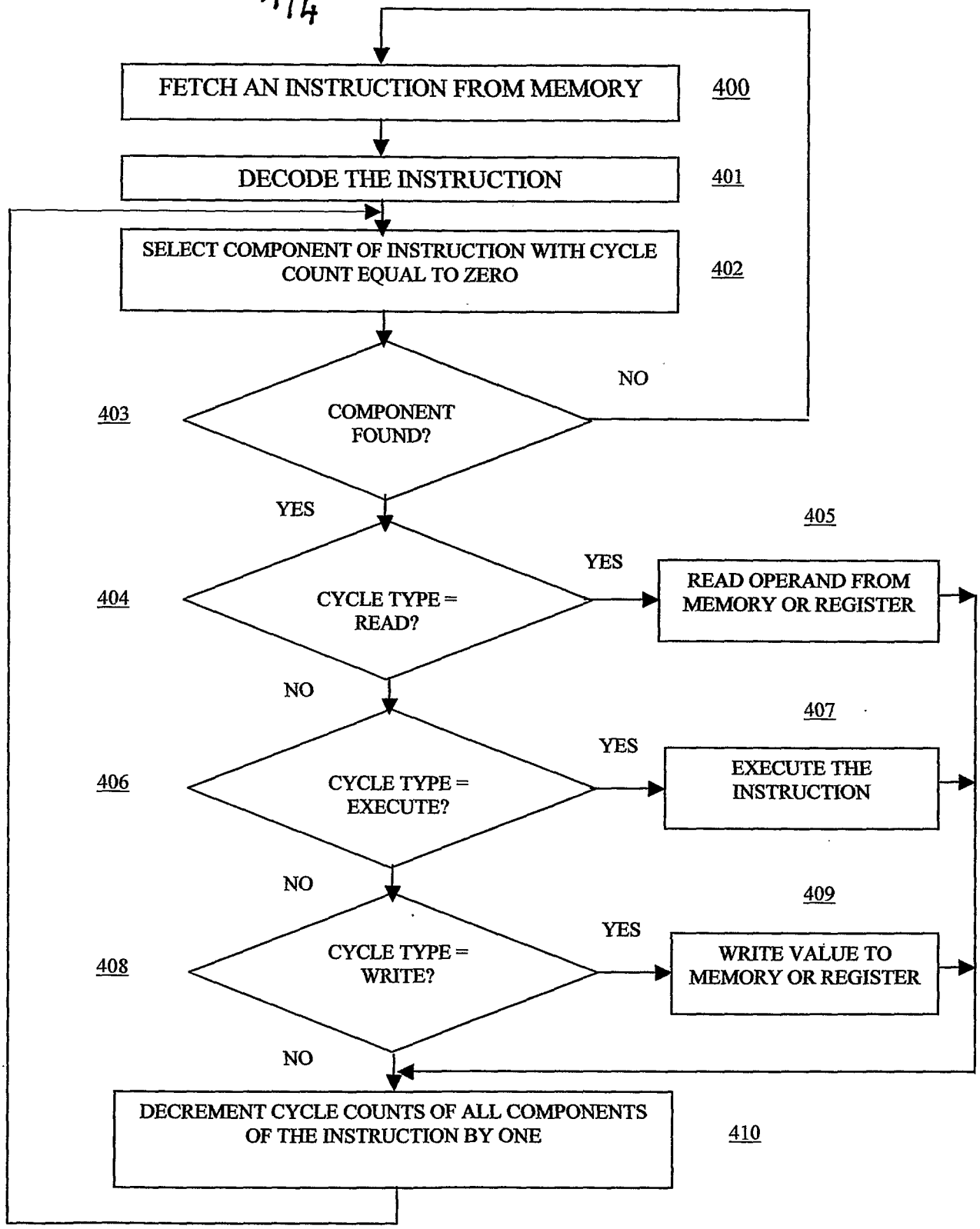
FETCH AN INSTRUCTION FROM MEMORY
400
DECODE THE INSTRUCTION
401
SELECT COMPONENT OF INSTRUCTION WITH CYCLE COUNT EQUAL TO ZERO
402
403
COMPONENT FOUND?
NO
YES
405
404
CYCLE TYPE = READ?
YES
READ OPERAND FROM MEMORY OR REGISTER
NO
407
406
CYCLE TYPE = EXECUTE?
YES
EXECUTE THE INSTRUCTION
NO
409
408
CYCLE TYPE = WRITE?
YES
WRITE VALUE TO MEMORY OR REGISTER
NO
DECREMENT CYCLE COUNTS OF ALL COMPONENTS OF THE INSTRUCTION BY ONE
410

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IN05/00261

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G06F 7/38
US CL : 712/248
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 712/248 712/248; 712/245

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 4,714,991 A (Eaton) 22 Deember 1987, column 2 lines 45-48 and 63-67, column 3 lines 40-67, column 4 lines 1-20, column 5 lines 5-31 and column 8 lines 40-67.	1-2 --- 3-4
Y	US 4,633,390 A (Yoshida) 30 December 1986, column 3 lines 1-57, column 5 lines 22-41.	3-4, 5
Y	US 6,026,490 A (Johns-Vano et al.) 15 February 2000, column 3 lines 8-45, column 4 lines 5-33 and 43-60.	5

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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