A plurality of video data pieces corresponding to one horizontal scan line of a display panel are classified into a first video data group and a second video data group different from the first video data group. Each piece of video data belonging to the first video data group is converted into a gradation voltage having an analog voltage value, and by interpolation based on each of the gradation voltages, a gradation voltage corresponding to each of the video data pieces belonging to said second video data group is obtained.
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FIG. 3

Diagram showing a process or system with inputs labeled PD and outputs labeled QD. The diagram includes multiple stages labeled PD1 to PDm-1, PDm, QD1 to QDm-1, and QDm, with arrows indicating the flow and extraction of 2 bits at various stages.
FIG. 5

KS1 ~ KS6

VA

VB

SS

AVERAGE COMPUTATION

WEIGHTED AVERAGE COMPUTATION

SELECTOR

VW

VM

Y

52

00

01

10

11

51

53
FIG. 9

GRADATION VOLTAGE SPECIFYING DATA

VD (PD, PD2, PD3, SQ4, SQ5, SQ6, PD7, PD8, SQ9, SQ10, SQ11, SQ12, PD13, PD14, PD15, ... SQm-5, SQm-4, SQm-3, PDm-2, PDm-1, PDm)

GRADATION VOLTAGE SPECIFYING DATA

PD1, PD2, PD3, SQ4, SQ5, SQ6, PD7, PD8, SQ9, SQ10, SQ11, SQ12, PD13, PD14, PD15, ... SQm-5, SQm-4, SQm-3, PDm-2, PDm-1, PDm

QD1, QD2, QD3, QD4, QD5, QD6, QD7, QD8, QD9, QD10, QD11, QD12, QD13, QD14, QD15, ... QDm-5, QDm-4, QDm-3, QDm-2, QDm-1, QDm
1
DISPLAY PANEL DRIVE DEVICE AND
DISPLAY PANEL DRIVE METHOD

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a display panel drive device, and more particularly to the display device for applying a gradation voltage to a data line of the display panel and a display panel drive method.

Description of the Related Arts

A liquid crystal display panel as an example of a planar display panel is provided with a plurality of scan lines extending in the horizontal direction of the two-dimensional screen which intersect a plurality of data lines extending in the vertical direction of the two-dimensional screen. Electrodes serving as a display cell are formed at the intersections of the data lines and the scan lines.

The liquid crystal display panel is provided with a data driver for applying a voltage based on an input video signal to each data line. The data driver is provided for each data line with a decoder for converting display data corresponding to each pixel into a gradation voltage having a voltage value corresponding to a brightness level (for example, see Japanese Patent Application Laid-Open No. 2006-292807).

Therefore, an increase in the number of data lines for a higher resolution of the liquid crystal display panel would lead to an increase in the number of decoders, resulting in the chip size of the data driver being increased.

In this context, suggested is a data driver which is capable of driving the data lines of a liquid crystal display panel, using a less number of decoders than the number of data lines, by driving three data lines with one decoder in a timesharing manner (for example, see Japanese Patent Application Laid-Open No. Hei. 11-259036).

It is possible for the aforementioned data driver to reduce the size of the chip size. However, driving based on display data for one horizontal scan can be carried out by being temporally divided. Thus, the operation frequency needs to be increased by the number of the divisions. Therefore, such a data driver increases the power consumption and the amount of generated heat by the increase in the operation frequency.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a display panel drive device and a display panel drive method which are capable of reducing the device size, the power consumption, and the amount of generated heat.

A display panel drive device according to the present invention receives input video data each including a series of video data pieces each indicative of a brightness level of each pixel and then applies gradation voltages corresponding to each of the video data pieces to the display panel. The drive device includes a D/A converter and a gradation voltage interpolation circuit. When the plurality of video data pieces corresponding to one horizontal scan line of data of the display panel are classified into a first video data group and a second video data group different from the first video data group, the D/A converter converts each of the video data pieces belonging to the first video data group into an analog voltage as a gradation voltage corresponding to said first video data group. The gradation voltage interpola-
pared with the case where all video data pieces for one horizontal scan line are subjected to the gradation voltage conversion by the D/A converter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view illustrating the configuration of a display device which includes a display panel drive device according to the present invention;

FIG. 2 is a block diagram illustrating the internal configuration of a data driver 12;

FIG. 3 is a view illustrating an example of the operation of a shift register 121;

FIG. 4 is a block diagram illustrating an example of the internal configuration of a gradation voltage output part 124;

FIG. 5 is a block diagram illustrating an example of the internal configuration of each of gradation voltage interpolation circuits KS1 to KS6;

FIG. 6 is a view illustrating another example of the operation of a shift register 121;

FIG. 7 is a block diagram illustrating another example of the internal configuration of each of the gradation voltage interpolation circuits KS1 to KS6;

FIG. 8 is a block diagram illustrating another example of the internal configuration of a gradation voltage output part 124; and

FIG. 9 is a view illustrating another example of the format of input video data VD and the operation of a shift register 121.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic view illustrating the configuration of a display device that includes a display panel drive device according to the present invention.

In FIG. 1, a display panel 20 as an example of a liquid crystal panel is provided with a liquid crystal layer (not shown), a horizontal scan lines S1 to Sn (n is an integer equal to two or greater) extending in the horizontal direction of the two-dimensional screen, and m data lines D1 to Dm (m is an integer equal to three or greater) extending in the vertical direction of the two-dimensional screen. At the intersecting regions between the horizontal scan lines and the data lines, a red display cell Pr serving for red color display, a green display cell Pg serving for green color display, or a blue display cell Pn serving for blue color display are formed.

The red display cell Pr is formed at the (3t-2)th data lines (t is a natural number from 1 to 320) of the data lines D1 to Dm, that is, D1, D2, D3, . . . , Dm. The green display cell Pg is formed at the (3t-1)th data lines of the data lines D1 to Dm, that is, D2, D3, D4, . . . , Dm. The blue display cell Pn is formed at the (3t)th data lines of the data lines D1 to Dm, that is, D3, D4, D5, . . . , Dm.

As shown in FIG. 1, on each of the horizontal scan lines S1 to Sn, the three display cells adjacent to each other, that is, the red display cell Pr, the green display cell Pg, and the blue display cell Pn form one pixel PX (the region surrounded by broken lines). On one horizontal scan line, (m/3) pixels PX are disposed side by side.

A drive control part 10 generates a scan control signal in synchronization with input video data VD, and the scan control signal is then supplied to a scan driver 11. The input video data VD includes a series of video data pieces each indicative of the brightness level corresponding to each pixel. One pixel PX is associated with three video data pieces: a piece of video data which represents the brightness level of the red component in eight bits; a piece of video data which represents the brightness level of the green color component in eight bits; and a piece of video data which represents the brightness level of the blue component in eight bits.

On the basis of the input video data VD, the drive control part 10 supplies to a data driver 12, for each pixel, video data PD serving as the video data pieces which represent the brightness level of each of the red display cell Pr, the green display cell Pg, and the blue display cell Pn corresponding to the pixel, for example, in eight bits.

The scan driver 11 generates scanning pulses in response to the scan control signal supplied from the drive control part 10, and the scanning pulses are then sequentially selectively applied to the horizontal scan lines S1 to Sn of the display panel 20.

The data driver 12 captures the series of video data PD supplied from the drive control part 10. Each time one horizontal scan line of data is captured, that is, m pieces of video data PD1 to PDm are captured, the data driver 12 generates pixel drive voltages G1 to Gm, having a gradation voltage corresponding to the brightness level indicated by each piece of video data PD, and then applies the pixel drive voltages G1 to Gm to the corresponding data lines D1 to Dm.

FIG. 2 is a block diagram illustrating the internal configuration of the data driver 12.

The series of video data PD supplied from the drive control part 10 is sequentially captured by a shift register 121. As shown in FIG. 3, each time one horizontal scan line of video data PD1 to PDm is completely captured, the shift register 121 supplies the video data QD1 to QDm, a data latch part 122. The (3t-2)th video data PD of the video data PD1 to PDm represents the red brightness component, for example, in eight bits. The (3t-1)th video data PD represents the green brightness component, for example, in eight bits. The (3t)th video data PD represents the blue brightness component, for example, in eight bits.

As shown in FIG. 3, for the (6t-5)th, (6t-4)th, and (6t-3)th video data PD of the video data PD1 to PDm (a first video data group), the shift register 121 supplies the eight-bit data expressed by the video data PD to the data latch part 122 as video data QD with no change made thereto. That is, for the video data PD corresponding to the odd-numbered pixel PX, the shift register 121 supplies the video data PD to the data latch part 122 as the video data QD with no change made thereto.

For the (6t-2)th, the (6t-1)th, and the (6t)th video data PD of the video data PD1 to PDm (a second video data group), the shift register 121 extracts, for example, the lower two bits from the video data PD and then supplies the extracted video data QD of the two bits to the data latch part 122. That is, the shift register 121 extracts the lower two bits from each video data PD corresponding to the even-numbered pixel PX of the (m/3) pixels PX disposed side by side on one horizontal scan line of the display panel 20, and then supplies each the extracted two-bit video data QD to the data latch part 122.

For example, the shift register 121 acquires the video data QD1 to QDm below from the video data PD1 to PDm corresponding to the second pixel PX arranged on one horizontal scan line, and then supplies the video data QD1 to QDm to the data latch part 122. That is, the shift register 121 supplies, to the data latch part 122, the video data QD1 made up of the lower two bits of the video data PD2; the video data QD2
made up of the lower two bits of the video data PDs, and the video data QRd made up of the lower two bits of the video data PQd.

The data latch part 122 captures the video data QD1 to QDm supplied from the shift register 121, and while sustaining the video data QD1 to QDm for one horizontal scan period, supplies each piece of the video data QD1 to QDm to a level shift part 123 as video data LD1 to LDm.

The level shift part 123 supplies, to a gradation voltage output part 124, video data SD1 to SDm obtained by shifting the level of the value of each of the video data LD1 to LDm by a predetermined level.

The gradation voltage output part 124 converts the video data SD1 to SDm into gradation voltages G1 to Gm individually corresponding to the brightness level represented by the video data, and then applies the gradation voltages G1 to Gm to the data lines D1 to Dm of the display panel 20.

FIG. 4 is a block diagram illustrating the internal configuration of the gradation voltage output part 124.

Note that FIG. 4 illustrates only those excerpted functional modules, which relate to the video data SD1 to SD12, among all the functional modules that constitute the gradation voltage output part 124.

In FIG. 4, a D/A converter C1 converts the video data SD1 into a gradation voltage corresponding to the brightness level represented by the video data SD1, and then supplies the gradation voltage as a gradation voltage V1 to an amplifier A1 and an input end VA of a gradation voltage interpolation circuit KS1.

A D/A converter C2 converts the video data SD2 into an analog gradation voltage corresponding to the brightness level represented by the video data SD2, and then supplies the analog gradation voltage as a gradation voltage V2 to an amplifier A2 and an input end VA of a gradation voltage interpolation circuit KS2.

A D/A converter C3 converts the video data SD3 into an analog gradation voltage corresponding to the brightness level represented by the video data SD3, and then supplies the analog gradation voltage as a gradation voltage V3 to an amplifier A3 and an input end VA of a gradation voltage interpolation circuit KS3.

A D/A converter C4 converts the video data SD4 into an analog gradation voltage corresponding to the brightness level represented by the video data SD4, and then supplies the analog gradation voltage as a gradation voltage V4 to an amplifier A4, an input end VB of the gradation voltage interpolation circuit KS4, and an input end VA of a gradation voltage interpolation circuit KS5.

A D/A converter C5 converts the video data SD5 into an analog gradation voltage corresponding to the brightness level represented by the video data SD5, and then supplies the analog gradation voltage as a gradation voltage V5 to an amplifier A5, an input end VB of the gradation voltage interpolation circuit KS6, and an input end VA of a gradation voltage interpolation circuit KS6.

A D/A converter C6 converts the video data SD6 into an analog gradation voltage corresponding to the brightness level represented by the video data SD6, and then supplies the analog gradation voltage as a gradation voltage V6 to an amplifier A6, an input end VB of the gradation voltage interpolation circuit KS7, and an input end VA of a gradation voltage interpolation circuit KS7.

The gradation voltage interpolation circuits KS1 to KS6 have the same internal configuration.

FIG. 5 is a block diagram illustrating the internal configuration of each of the gradation voltage interpolation circuits KS1 to KS6.
weighted average gradation voltage $V_{W}$ based on $V_{1}$ and $V_{15}$, and then supplies the selected voltage to an amplifier A10 as a gradation voltage $V_{15}$. Note that the gradation voltage $V_{13}$ is produced by a D/A converter (not shown) for converting the video data $SD_{13}$ into an analog gradation voltage.

On the basis of the video data $SD_{1}$ supplied to the selection control end SS, the gradation voltage interpolation circuit KS5 selects one of the gradation voltage $V_{9}$ produced at the D/A converter C5, a gradation voltage $V_{14}$, the average gradation voltage $VM$ based on $V_{1}$ and $V_{14}$, and the weighted average gradation voltage $VW$ based on $V_{6}$ and $V_{14}$, and then supplies the selected voltage to an amplifier A11 as a gradation voltage $V_{14}$. Note that the gradation voltage $V_{14}$ is produced by a D/A converter (not shown) for converting video data $SD_{14}$ into an analog gradation voltage.

The amplifiers A1 to A12 apply, to the data lines D1 to D12 of the display panel 20, gradation voltages $G_{1}$ to $G_{12}$ obtained by individually amplifying the gradation voltages $V_{1}$ to $V_{12}$ supplied from the D/A converters C1 to C6 and the gradation voltage interpolation circuits KS1 to KS6. Note that each of the amplifiers A1 to A12 to be employed may also be a voltage follower circuit with an operational amplifier.

As described above, as a function block for converting the video data $SD_{1}$ to $SD_{12}$ into the gradation voltages $V_{1}$ to $V_{12}$, the gradation voltage output part 124 is provided, in the same manner as in FIG. 4, with the same function block as that of the D/A converters C1 to C6, the gradation voltage interpolation circuits KS1 to KS6, and the amplifiers A1 to A12.

As described above, the gradation voltage output part 124 allows the D/A converter to perform the gradation voltage conversion only on the video data $SD_{1}$ corresponding to the odd-numbered pixels PX of the (m/3) pixels PX disposed side by side along one horizontal scan line of the display panel 20. That is, the gradation voltage output part 124 classifies a plurality of video data pieces corresponding to one horizontal scan line of the display panel into the first video data group (for example, $SD_{1}$ to $SD_{3}$ and $SD_{5}$ to $SD_{7}$) and the second video data group (for example, $SD_{4}$ to $SD_{6}$ and $SD_{8}$ to $SD_{10}$), and selects a bit corresponding to the odd video data pieces belonging to the first video data group (for example, $V_{1}$ to $V_{15}$ and $V_{16}$ to $V_{12}$) having an analog voltage value.

On the other hand, in the gradation voltage output part 124, by the interpolation based on each of the gradation voltages produced at the D/A converters, the gradation voltage interpolation circuits (for example, KS1 to KS6) acquire the gradation voltages ($V_{9}$ to $V_{15}$ and $V_{16}$ to $V_{12}$) each corresponding to each of the video data pieces belonging to the second video data group.

More specifically, the average computation part 51 of the gradation voltage interpolation circuit determines, as the average gradation voltage (VM), the average value of a first gradation voltage (for example, $V_{1}$) generated by the D/A converter on the basis of one piece of video data (for example, $SD_{1}$) of the video data pieces belonging to the first video data group and a second gradation voltage (for example, $V_{12}$) generated by the D/A converter on the basis of another piece of video data (for example, $SD_{12}$) belonging to the first video data group. The weighted average computation part 53 of the gradation voltage interpolation circuit determines the weighted average of the first gradation voltage and the second gradation voltage, which have been mentioned above, as the weighted average gradation voltage (WV). Then, on the basis of a piece of video data (for example, $SD_{4}$) belonging to the second video data group, the selector 52 of the gradation voltage interpolation circuit selects one of the first gradation voltage, the second gradation voltage, the average gradation voltage, and the weighted average gradation voltage, which have been mentioned above, and then outputs the selected voltage as the gradation voltage (for example, $V_{14}$) corresponding to the piece of video data belonging to the second video data group.

The circuit size and the power consumption of the gradation voltage interpolation circuits (KS1 to KS6) are less than the circuit size and the power consumption of the D/A converters (C1 to C6).

Therefore, according to the configuration shown in FIG. 4, it is possible to reduce the circuit size, the power consumption, and the amount of generated heat when compared with the case where the D/A converters perform the gradation voltage conversion on all the pieces of video data $SD_{1}$ to $SD_{12}$ of one horizontal scan line.

Furthermore, in the aforementioned configuration, since the video data pieces corresponding to even-numbered pixels PX (for example, $SD_{2}$ to $SD_{2}$ and $SD_{4}$ to $SD_{10}$) have two bits, the circuit size and the power consumption of the data latch part 122 and the level shift part 123 are reduced.

Furthermore, the aforementioned configuration allows the gradation voltages $G_{1}$ to $G_{12}$ corresponding to one horizontal scan line of video data $PD_{1}$ to $PD_{12}$ to be simultaneously applied to the data lines D1 to D12 of the display panel 20. Therefore, it is possible to reduce the operation frequency as compared with the case where the gradation voltage is applied in a timesharing manner within a horizontal scan period.

As described above, the data driver 12 according to this embodiment makes it possible to reduce the device size, the power consumption, and the amount of generated heat.

Note that in the aforementioned embodiment, as shown in FIG. 3, the shift register 121 extracts the lower two bits from the video data $PD$ corresponding to the even-numbered pixel PX and then supplies the video data $QD$ of two bits to the data latch part 122. However, the number of bits to be extracted from the video data $PD$ is not limited to two bits. For example, as shown in FIG. 6, the shift register 121 may also extract the lower three bits from the video data $PD$ corresponding to the even-numbered pixel PX and then apply the video data $QD$ of three bits to the data latch part 122. At this time, for example, the configuration shown in FIG. 7 may be employed as each of the gradation voltage interpolation circuits KS1 to KS6 corresponding to the three-bit video data $QD$.

In FIG. 7, the average computation part 51 computes the average value of the gradation voltage supplied to the input end VA and the gradation voltage supplied to the input end VB, and then supplies, to the selector 52, the average gradation voltage VM indicative of the average value.

The weighted average computation part 53 computes an average value of a first multiplication result acquired by multiplying the gradation voltage supplied to the input end
VA by a coefficient (for example 0.2) and a second multiplication result acquired by multiplying the gradation voltage supplied to the input end VA by a coefficient (for example 0.8), and then supplies, to the selector $S_2a$, the weighted average gradation voltage $V_{W_1}$ indicative of the average value.

The weighted average computation part $S_3b$ computes an average value of a first multiplication result acquired by multiplying the gradation voltage supplied to the input end VA by a coefficient (for example 0.3) and a second multiplication result acquired by multiplying the gradation voltage supplied to the input end VB by a coefficient (for example 0.7), and then supplies, to the selector $S_2a$, the weighted average gradation voltage $V_{W_2}$ indicative of the average value.

The weighted average computation part $S_3c$ computes an average value of a first multiplication result acquired by multiplying the gradation voltage supplied to the input end VA by a coefficient (for example 0.4) and a second multiplication result acquired by multiplying the gradation voltage supplied to the input end VB by a coefficient (for example 0.6), and then supplies, to the selector $S_2a$, the weighted average gradation voltage $V_{W_3}$ indicative of the average value.

The weighted average computation part $S_3d$ computes an average value of a first multiplication result acquired by multiplying the gradation voltage supplied to the input end VA by a coefficient (for example 0.6) and a second multiplication result acquired by multiplying the gradation voltage supplied to the input end VB by a coefficient (for example 0.4), and then supplies, to the selector $S_2a$, the weighted average gradation voltage $V_{W_4}$ indicative of the average value.

On the basis of the 3-bit video data supplied to the selection control end $S_S$, the selector $S_2a$ selects one of the gradation voltages supplied to the input end VA, the gradation voltage supplied to the input end VB, the average gradation voltage $V_M$, and the weighted average gradation voltages $V_{W_1}$ to $V_{W_4}$, and then outputs the selected voltage via the output end $Y$.

For example, when the 3-bit video data supplied to the selection control end $S_S$ is indicative of [000], the selector $S_2a$ selects the gradation voltage supplied to the input end VA, and then outputs the selected voltage via the output end $Y$. Furthermore, when the video data is indicative of [001], the selector $S_2a$ selects the average gradation voltage $V_M$, and then outputs the average gradation voltage $V_M$ via the output end $Y$. Furthermore, when the video data is indicative of [010], the selector $S_2a$ selects the gradation voltage supplied to the input end VB, and then outputs the selected voltage via the output end Y. Furthermore, when the video data is indicative of [011], the selector $S_2a$ selects the weighted average gradation voltage $V_{W_1}$, and then outputs the weighted average gradation voltage $V_{W_1}$ via the output end $Y$. Furthermore, when the video data is indicative of [100], the selector $S_2a$ selects the weighted average gradation voltage $V_{W_2}$, and then outputs the weighted average gradation voltage $V_{W_2}$ via the output end $Y$. Furthermore, when the video data is indicative of [101], the selector $S_2a$ selects the weighted average gradation voltage $V_{W_3}$, and then outputs the weighted average gradation voltage $V_{W_3}$ via the output end $Y$. Furthermore, when the video data is indicative of [110], the selector $S_2a$ selects the weighted average gradation voltage $V_{W_4}$, and then outputs the weighted average gradation voltage $V_{W_4}$ via the output end $Y$. Furthermore, when the video data is indicative of [111], the selector $S_2a$ selects the weighted average gradation voltage $V_{W_4}$, and then outputs the weighted average gradation voltage $V_{W_4}$ via the output end $Y$.

Therefore, the configuration shown in FIG. 7 includes five types of weighted average gradation voltages, i.e., the five systems of the weighted average gradation voltages $V_{W_1}$ to $V_{W_4}$, and thus, can provide a gradation voltage with high accuracy when compared with the configuration which employs one system of the weighted average gradation voltage $V_M$ as shown in FIG. 5.

In the aforementioned embodiment, the D/A converter is used to perform the gradation voltage conversion only on the video data SD corresponding to the odd-numbered pixel PX to generate a gradation voltage, and then on the basis of the gradation voltage, provides the gradation voltage corresponding to the even-numbered pixel PX. However, it may also be acceptable to perform the gradation voltage conversion using the D/A converter only on the video data SD corresponding to the even-numbered or odd-numbered pixels PX on one horizontal scan line, that is, the pixels PX that are alternately disposed on one horizontal scan line.

However, it may also be acceptable to perform the gradation voltage conversion using the D/A converter only on the video data SD (the first video data group) corresponding to the pixels PX that are disposed at intervals of k (k is a natural number) on one horizontal scan line. At this time, by the interpolation based on each gradation voltage generated by the D/A converter, the gradation voltage corresponding to another piece of video data SD (the second video data group) is provided.

FIG. 8 is a block diagram illustrating another configuration of the gradation voltage output part 124 developed in view of such an aspect.

In FIG. 8, a D/A converter $C_1a$ converts the video data $S_{D_1}$ into a gradation voltage corresponding to the brightness level represented by the 8-bit data, and then supplies the converted gradation voltage as the gradation voltage $V_1$, to the input end VA of each of gradation voltage interpolation circuits $K_{S1a}$ and $K_{S4a}$ and the amplifier $A_1$.

The D/A converter $C_2a$ converts the video data $S_{D_2}$ into an analog gradation voltage corresponding to the brightness level represented by the 8-bit data, and then supplies the converted analog gradation voltage as the gradation voltage $V_2$ to the input end VA of each of gradation voltage interpolation circuits $K_{S2a}$ and $K_{S5a}$ and the amplifier $A_2$.

The D/A converter $C_3a$ converts the video data $S_{D_3}$ into an analog gradation voltage corresponding to the brightness level represented by the 8-bit data, and then supplies the converted analog gradation voltage as the gradation voltage $V_3$ to the input end VA of each of gradation voltage interpolation circuits $K_{S6a}$ and $K_{S6a}$ and the amplifier $A_3$. 
The D/A converter C4a converts the video data SD10 into an analog gradation voltage corresponding to the brightness level represented by the 8-bit data, and then supplies the converted analog gradation voltage as the gradation voltage Vg to the input end VB of each gradation voltage interpolation circuits KS1a and KS4a and the amplifier A10.

The D/A converter C5a converts the video data SD12 into an analog gradation voltage corresponding to the brightness level represented by the 8-bit data, and then supplies the converted analog gradation voltage as the gradation voltage Vn to the input end VB of each of gradation voltage interpolation circuits KS2a and KS5a and the amplifier A11.

The D/A converter C6a converts the video data SD13 into an analog gradation voltage corresponding to the brightness level represented by the 8-bit data, and then supplies the converted analog gradation voltage as the gradation voltage Vm to the input end VB of each of gradation voltage interpolation circuits KS3a and KS6a and the amplifier A12.

Each of the gradation voltage interpolation circuits KS1a to KS6a has, for example, the configuration shown in FIG. 5 or FIG. 7.

On the basis of the video data SD supplied to the selection control end SS, the gradation voltage interpolation circuit KS1a selects one of the gradation voltage Vg generated at the D/A converter C1a, the gradation voltage V10 generated at the D/A converter C4a, the average gradation voltage VM based on Vg and V10, and the weighted average gradation voltage VW on the basis of Vg and V10, and then supplies the selected voltage to the amplifier A4 as the gradation voltage Vg.

On the basis of the video data SD supplied to the selection control end SS, the gradation voltage interpolation circuit KS2a selects one of the gradation voltage Vg generated at the D/A converter C2a, the gradation voltage V11 generated at the D/A converter C5a, the average gradation voltage VM based on Vg and V11, and the weighted average gradation voltage VW based on Vg and V11, and then supplies the selected voltage to the amplifier A5 as the gradation voltage Vg.

On the basis of the video data SD supplied to the selection control end SS, the gradation voltage interpolation circuit KS3a selects one of the gradation voltage Vg generated at the D/A converter C3a, the gradation voltage V12 generated at the D/A converter C6a, the average gradation voltage VM based on Vg and V12, and the weighted average gradation voltage VW based on Vg and V12, and then supplies the selected voltage to the amplifier A6 as the gradation voltage Vg.

On the basis of the video data SD supplied to the selection control end SS, the gradation voltage interpolation circuit KS4a selects one of the gradation voltage Vg generated at the D/A converter C4a, the gradation voltage V10 generated at the D/A converter C7a, the average gradation voltage VM based on Vg and V10, and the weighted average gradation voltage VW based on Vg and V10, and then supplies the selected voltage to the amplifier A7 as the gradation voltage Vg.

On the basis of the video data SD supplied to the selection control end SS, the gradation voltage interpolation circuit KS5a selects one of the gradation voltage Vg generated at the D/A converter C5a, the gradation voltage V11 generated at the D/A converter C8a, the average gradation voltage VM based on Vg and V11, and the weighted average gradation voltage VW based on Vg and V11, and then supplies the selected voltage to the amplifier A8 as the gradation voltage Vg.

On the basis of the video data SD supplied to the selection control end SS, the gradation voltage interpolation circuit KS6a selects one of the gradation voltage Vg generated at the D/A converter C6a, the gradation voltage V12 generated at the D/A converter C3a, the average gradation voltage VM based on Vg and V12, and the weighted average gradation voltage VW based on Vg and V12, and then supplies the selected voltage to the amplifier A9 as the gradation voltage Vg.

The amplifiers A1 to A12 apply, to the data lines D1 to D12 of the display panel 20, the gradation voltages G1 to G12 obtained by individually amplifying the gradation voltages Vg to V12 supplied from the D/A converter C1a to C6a and the gradation voltage interpolation circuits KS1a to KS6a.

As described above, the configuration shown in FIG. 8 is configured to perform the gradation voltage conversion by the D/A converters (C1a to C6a) on the video data pieces (for example, SD1 to SD3, and SD10 to SD12) corresponding to the pixels PX that are disposed at intervals of two on one horizontal scan line. This allows for producing the gradation voltages (for example, V1 to V12) corresponding to the video data pieces. Then, by the interpolation based on each gradation voltage generated by the D/A converter, the gradation voltages (for example, V4 to V6) corresponding to other video data pieces (for example, SD4 to SD6) are obtained.

Therefore, by employing the configuration shown as the gradation voltage output part 124 in FIG. 8, (m/3) D/A converters may be provided for one horizontal scan line of m pieces of pixel data SD1 to SDm. Thus, when compared with the case where employed is the configuration shown in FIG. 4 that requires (m/2) D/A converters for one horizontal scan line of m pieces of pixel data SD1 to SDm, it is possible to reduce the circuit size of the D/A converter provided in the data driver 12. This makes it possible to reduce the chip size of the data driver 12 and reduce the power consumption and the amount of generated heat. In the aforementioned embodiment, the piece of video data (PD, QD, LD, SD) have eight bits. However, the number of bits of the piece of video data is not limited to eight bits.

The display device shown in FIG. 1 is intended to receive the input video data voltage of a series of video data pieces each indicative of the brightness level corresponding to each pixel, but may also receive the input video data voltage as below. That is, in the series of video data pieces of the input video data voltage, the video data pieces corresponding to the pixel PX that is not to be subjected to the gradation voltage conversion by the aforementioned D/A converter are to be received after being changed to pieces of gradation voltage specifying data. Note that the piece of gradation voltage specifying data is to specify the gradation voltage to be selected by the aforementioned selector 52 or 52a.

For example, in the case where the configuration shown in FIG. 4 is employed as the gradation voltage output part 124, the input video data voltage having the format shown in FIG. 9 is to be entered to the display device shown in FIG. 1.

The input video data voltage shown in FIG. 9 is provided with a series of video data PD1 to PD3, PD4 to PD6, PD10, PD12, to PD14, . . ., and PDm-2 to PDm, each being made up of, for example, eight bits, corresponding to each odd-numbered pixel PX (the first pixel group) on a horizontal scan line of the display panel 20. The input video data voltage is also provided with a series of gradation voltage specifying data SQ1 to SQm, SQ10 to SQ12, . . ., and SQm-5 to SQm-3, each
being made up of, for example, two bits, corresponding to each even-numbered pixel PX (the second pixel group) on the horizontal scan line.

When the input video data VD shown in FIG. 9 is entered, the shift register 121 of the data driver 12 supplies, to the data latch 122 as the video data QD₁ to QD₅, a series of video data pieces (PD) and pieces of gradation voltage specifying data (SQ) resulting from the input video data VD each time one horizontal scan line of input video data VD is completely acquired.

This allows the D/A converter (for example, C1 to C6) of the gradation voltage output part 124 to convert, into an analog voltage value, each piece of video data (for example, SD₁ to SD₅ and SD₁ to SD₅) corresponding to each pixel PX belonging to the aforementioned first pixel group and thereby acquire a gradation voltage (for example, V₁ to V₅ and V₁ to V₅) having the voltage value.

By the interpolation based on each gradation voltage generated by the D/A converter, the gradation voltage interpolation circuit (for example, KSI to KS6) of the gradation voltage output part 124 acquires a gradation voltage (V₁ to V₅ and V₁ to V₅) corresponding to each piece of video data belonging to the second video data group. That is, the average computation part (S1) of the gradation voltage interpolation circuit determines, as an average gradation voltage, the average value of the first gradation voltage generated by the D/A converter on the basis of one of the video data pieces belonging to the first pixel group and the second gradation voltage generated by the D/A converter on the basis of another of the video data pieces belonging to the first pixel group. The weighted average computation part (S3) of the gradation voltage interpolation circuit determines the weighted average of the first gradation voltage and the second gradation voltage as a weighted average gradation voltage. Then, on the basis of the pieces of gradation voltage selection data corresponding to the pixels belonging to the second pixel group, the selector (S2) of the gradation voltage interpolation circuit selects one of the first gradation voltage, the second gradation voltage, the average gradation voltage, and the weighted average gradation voltage, and then outputs the selected voltage as the gradation voltage corresponding to the pixels belonging to the second pixel group.

This application is based on Japanese Patent Application No. 2014-106075 which is herein incorporated by reference.

What is claimed is:

1. A display panel drive device for receiving input video data signals each including a series of video data pieces respectively representing brightness levels of pixels aligned with each other along a single horizontal scan line and for applying gradation voltages corresponding to the video data pieces to a display panel, each of the video data pieces belonging to either one of first and second video data groups which are different from each other, said display panel drive device comprising:
   a D/A converter configured to convert each of the video data pieces belonging to said first video data group into a first analog gradation voltage; and
   a gradation voltage interpolation circuit configured to obtain a second analog gradation voltage each corresponding to the video data pieces belonging to said second video data group by interpolation based on the first analog gradation voltages respectively corresponding to at least two of the pixels.

2. The display panel drive device according to claim 1, wherein said first video data group includes the video data pieces corresponding to pixels disposed at intervals of k (k is a natural number) in an array of pixels disposed side by side along said horizontal scan line of said display panel.

3. The display panel drive device according to claim 2, wherein said gradation voltage interpolation circuit includes:
   an average computation part for determining, as an average gradation voltage, an average value of a first gradation voltage generated by said D/A converter on the basis of one piece of the video data belonging to said first video data group and a second gradation voltage generated by said D/A converter on the basis of another piece of the video data which belongs to said first video data group and is different from said one piece of the video data; and
   a selector for selecting one of said first gradation voltage, said second gradation voltage, and said average gradation voltage on the basis of the video data pieces belonging to said second video data group, and then outputting the selected voltage as the gradation voltage corresponding to the video data pieces belonging to said second video data group.

4. The display panel drive device according to claim 3, further comprising a weighted average computation part for determining a weighted average of said first gradation voltage and said second gradation voltage as a weighted average gradation voltage, and wherein said selector selects one of said first gradation voltage, said second gradation voltage, said average gradation voltage, and said weighted average gradation voltage on the basis of the video data pieces belonging to said second video data group, and then outputs the selected voltage as the gradation voltage corresponding to the video data pieces belonging to said second video data group.

5. The display panel drive device according to claim 2, wherein in an array of pixels disposed side by side along the horizontal scan line, the video data pieces corresponding to odd-numbered pixels belong to said first video data group, and the video data pieces corresponding to even-numbered pixels belong to said second video data group.

6. The display panel drive device according to claim 3, wherein in an array of pixels disposed side by side along the horizontal scan line, the video data pieces corresponding to odd-numbered pixels belong to said first video data group, and the video data pieces corresponding to even-numbered pixels belong to said second video data group.

7. The display panel drive device according to claim 4, wherein in an array of pixels disposed side by side along the horizontal scan line, the video data pieces corresponding to odd-numbered pixels belong to said first video data group, and the video data pieces corresponding to even-numbered pixels belong to said second video data group.

8. The display panel drive device according to claim 1, wherein:
   each of the pixels of said display panel includes three display cells being responsible for red, green, and blue colors, respectively, the three display cells being disposed side by side along the horizontal scan line; the video data pieces corresponding to each pixel include the piece of video data responsible for a red component, the piece of video data responsible for a green color component, and the piece of video data responsible for a blue component; and
by interpolation based on said first gradation voltage and said second gradation voltage generated by said D/A converter on the basis of each of the video data pieces responsible for the same color component, said gradation voltage interpolation circuit provides the gradation voltage corresponding to the video data pieces responsible for the same color component and belonging to said second video data group.

9. The display panel drive device according to claim 2, wherein:

each of the pixels of said display panel includes three display cells being responsible for red, green, and blue colors, respectively, the three display cells being disposed side by side along the horizontal scan line; the video data pieces corresponding to each pixel include the piece of video data responsible for a red component of the piece of video data responsible for a green color component, and the piece of video data responsible for a blue component; and

by interpolation based on said first gradation voltage and said second gradation voltage generated by said D/A converter on the basis of each of the video data pieces responsible for the same color component, said gradation voltage interpolation circuit provides the gradation voltage corresponding to the video data pieces responsible for the same color component and belonging to said second video data group.

10. The display panel drive device according to claim 3, wherein:

each of the pixels of said display panel includes three display cells being responsible for red, green, and blue colors, respectively, the three display cells being disposed side by side along the horizontal scan line; the video data pieces corresponding to each pixel include the piece of video data responsible for a red component, the piece of video data responsible for a green color component, and the piece of video data responsible for a blue component; and

by interpolation based on said first gradation voltage and said second gradation voltage generated by said D/A converter on the basis of each of the video data pieces responsible for the same color component, said gradation voltage interpolation circuit provides the gradation voltage corresponding to the video data pieces responsible for the same color component and belonging to said second video data group.

11. The display panel drive device according to claim 4, wherein:

each of the pixels of said display panel includes three display cells being responsible for red, green, and blue color, respectively, the three display cells being disposed side by side along the horizontal scan line; the video data pieces corresponding to each pixel include the piece of video data responsible for a red component, the piece of video data responsible for a green color component, and the piece of video data responsible for a blue component; and

by interpolation based on said first gradation voltage and said second gradation voltage generated by said D/A converter on the basis of each of the video data pieces responsible for the same color component, said gradation voltage interpolation circuit provides the gradation voltage corresponding to the video data pieces responsible for the same color component and belonging to said second video data group.

12. The display panel drive device according to claim 5, wherein:

each of the pixels of said display panel includes three display cells being responsible for red, green, and blue colors, respectively, the three display cells being disposed side by side along the horizontal scan line; the video data pieces corresponding to each pixel include the piece of video data responsible for a red component, the piece of video data responsible for a green color component, and the piece of video data responsible for a blue component; and

by interpolation based on said first gradation voltage and said second gradation voltage generated by said D/A converter on the basis of each of the video data pieces responsible for the same color component, said gradation voltage interpolation circuit provides the gradation voltage corresponding to the video data pieces responsible for the same color component and belonging to said second video data group.

13. A display panel drive device for receiving input video data that has a series of video data pieces each indicative of a brightness level of each pixel and then applying gradation voltage corresponding to each of the video data pieces to said display panel, wherein, when a plurality of pixels disposed side by side on a horizontal scan line of said display panel are classified into a first pixel group and a second pixel group different from said first pixel group, said input video data includes a plurality of video data pieces each corresponding to each of the pixels belonging to said first pixel group and pieces of gradation voltage selection data corresponding to each of the pixels belonging to said second pixel group.

said display panel drive device comprising:

a D/A converter for converting each of the video data pieces each corresponding to each of the pixels belonging to said first pixel group into an analog voltage as a gradation voltage corresponding to said first pixel group;

an average computation part for determining, as an average gradation voltage, an average value of a first gradation voltage generated by said D/A converter on the basis of one piece of the video data belonging to said first pixel group and a second gradation voltage generated by said D/A converter on the basis of another piece of the video data different from the one piece of the video data belonging to said first pixel group;

a weighted average computation part for determining, as a weighted average gradation voltage, a weighted average of said first gradation voltage and said second gradation voltage; and

a selector for selecting one of said first gradation voltage, said second gradation voltage, said average gradation voltage, and said weighted average gradation voltage on the basis of the pieces of the gradation voltage selection data corresponding to the pixels belonging to said second pixel group, and then outputting the selected voltage as the gradation voltage corresponding to the pixels belonging to said second pixel group.

14. A display panel drive method of receiving input video data that has a series of video data pieces respectively representing brightness levels of pixels aligned with each other along a single horizontal scan line and then applying gradation voltages respectively corresponding to the video data pieces to a display panel, each of the video data pieces belonging to either one of first and second video data groups which are different from each other, said display panel drive method comprising:
converting each of the video data pieces belonging to said first video data group into a first analog gradation voltage; and obtaining, by interpolation based on the first analog gradation voltages corresponding respectively to at least two of the pixels, a second analog gradation voltage each corresponding to the video data pieces belonging to said second video data group.

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