A pixel cell (100) and method for making the same for an active matrix display includes a pixel pad (110) and a thin film field effect transistor (106) which selectively couples a signal to activate/deactivate the pixel pad. A field shield (112) is formed on an insulating layer (102) and connected to the pixel pad through the insulating layer such that the field shield extends over at least a portion of the pixel pad. The field shield may extend over the thin film transistor and form a second gate (215) used to enhance the performance of the thin film transistor and the pixel cell.
For two-letter codes and other abbreviations, refer to the “Guidance Notes on Codes and Abbreviations” appearing at the beginning of each regular issue of the PCT Gazette.
PIXEL PERFORMANCE IMPROVEMENT
BY USE OF A FIELD-SHIELD

[0001] This disclosure relates to pixel cells for active matrix displays and more particularly to thin film transistor devices which employ field shields to improve performance.

[0002] E-ink capsules react to voltages placed on them and are used for generating images. The capsule includes white and black ink (E-ink), which are reactive and move in accordance with the voltage applied to the capsule or cell. To change image content on an electrophoretic E-ink display, new image information is written for a certain amount of time (e.g., 500 ms - 1000 ms). As the refresh rate of an active-matrix is usually higher, this results in addressing the same image content during a number of frames (e.g., at a frame rate of 50 Hz, 25 to 50 frames).

[0003] Referring to FIG. 1, a schematic drawing of the E-ink capsule 12 is illustratively shown. Addressing of E-ink from black to white, for example, requires pixel capacitor plates 10a and 10b to be charged to -15 V during a 500 ms to 1000 ms interval. During this time the white particles drift towards the top (common) electrode, while the black particles drift towards the bottom (active-matrix back plane) electrode. Switching to black requires a positive pixel voltage. At 0 V on the pixel capacitor the E-ink does not switch.

[0004] Referring to FIG. 2, an equivalent circuit 20 of a pixel 22 in an active-matrix display is shown. A row electrode 24 forms a storage capacitor for the pixels in a next row. Active-matrix displays are driven a row-at-a-time. During one frame time, all the rows are sequentially selected by applying a voltage that changes thin film transistors (TFTs) 26 from a non-conducting state (+25V) to a conducting state (-25V). In this line selection time, the pixel capacitors 28 and 30 (i.e. the total capacitance at the drain side of the TFT) of the selected row are charged to the voltage supplied on a column electrode 32 (+/-15V, OV). During the remaining frame time (i.e. the hold time), the other rows are addressed. The TFTs 26 are then in their non-conducting state and the charge on the pixel capacitors 28 and 30
must be retained. Between image updates the active-matrix is at rest at 0 V for the row and
column electrodes, the pixel pads and the common electrode.

[0005] \( C_{DE} \) is the capacitor 30 providing the display effect, \( C_a \) is the storage capacitor 28
and \( C_{gd} \) is the parasitic gate-drain capacitor (not shown) in the TFT 26. In the circuit 20, the
previous row electrode forms the storage capacitor line.

[0006] In accordance with the invention, a pixel cell and method for making the same for an
active matrix displays includes a pixel pad and a thin film field effect transistor which
selectably couples a signal to activate/deactivate the pixel pad. A field shield is formed on an
insulating layer and connected to the pixel pad/transistor through the insulating layer such that
the field shield extends over at least a portion of pixel electrodes (e.g., the pixel pad) or the
transistor. The field shield may extend over the thin film transistor and form a second gate
used to enhance the performance of the thin film transistor and the pixel cell.

[0007] A method for forming a pixel for active matrix displays includes forming an insulator
over a pixel stack, the pixel stack including a thin film transistor, a pixel pad and addressing
lines, and patterning a conductive layer formed over the insulator to form a field shield which
connects to the pixel pad. The field shield connects to the pixel pad through the insulating
layer such that the field shield extends over at least a portion of the thin film transistor to form
a second gate, which enhances the transistor performance.

[0008] Other steps may include activating the pixel pad and field shield to increase on-
current for the thin film field effect transistor. The step of forming an insulator may include
setting a thickness of the insulator in accordance with performance criteria for the thin film
transistor. The step of patterning the conductive layer may include patterning the conductive
layer such that the field shield of a first pixel cell extends over a thin film transistor of an
adjacent cell or over a pixel pad of an adjacent cell.

[0009] This disclosure will present in detail the following description of preferred
embodiments with reference to the following figures wherein:
FIG. 1 is a schematic diagram showing an E ink display in accordance with the prior art;

FIG. 2 is a schematic diagram showing a pixel cell for an active matrix display including E ink displays in accordance with the prior art;

FIG. 3 is a cross-sectional view showing an illustrative stack for an active display pixel cell;

FIG. 4 is an elevation view of a pixel cell corresponding with the stack of FIG. 3;

FIG. 5 is a cross-sectional view showing an insulator and field shield formed on the stack of FIG. 3 in accordance with one embodiment;

FIG. 6 is an elevation view of the pixel cell corresponding with the stack of FIG. 5;

FIG. 7 is a schematic diagram showing the pixel cell for an active matrix display shown in FIGS. 6 and 7 showing a second gate;

FIG. 8 is a plot of characteristic curves for a thin film transistor in the pixel cell of FIG. 7;

FIGS. 9 and 10 show two alternate embodiments for formation of an insulation layer and field shield;

FIG. 11 is an elevation view of a pixel cell having the filed shield extending over a neighboring pixel cell's transistor in accordance with an alternate embodiment; and

FIG. 12 is a schematic diagram showing the pixel cell for an active matrix display shown in FIG. 11.
These and other objects, features and advantages of the present disclosure will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

The present disclosure provides an improved pixel circuit, which includes a field shield to enhance the performance of a thin film transistor associated with the pixel circuit. A field shielded backplane in accordance with embodiments of the present invention increases the optical performance of the display by adding an additional metal layer (e.g., a third metal layer) to a pixel stack. An additional function is further given to the field-shield layer, which includes improving the switching properties of the pixel TFTs by using the field-shield layer as a second gate of the TFTs. Embodiments herein enhance the on-current of the TFT, while retaining the high optical performance of the display.

Illustrative embodiments of the present invention will now be described in terms of organic TFT pixel circuits; however and TFT pixel circuit may benefit from the teachings of the present invention. In addition, the present invention may include any pixel circuits for devices such as liquid crystal displays, E ink displays or any other display or device.

Referring now to the drawings in which like numerals represent the same or similar elements and initially to FIG. 3, a stack 40 may be used in organic TFTs pixel circuits. An active-matrix circuit as shown in FIG. 3 is processed on, for example, plastic foils 42 (substrate) resulting in an active-matrix (AM) backplane that can be integrated into a flexible display. Possible materials that can be used for the various layers are shown in Table 1. The preferred stack 40 starts with a highly conductive gate layer 44 (e.g. noble metal or indium-tin oxide), followed by an organic insulator layer 46, a second conductive layer 48 and an organic semiconducting layer 50. The organic layers 46 and 50 are preferably deposited by spin-coating. The layers can be patterned by photolithography, either by use of the intrinsic photosensitivity of the layers (e.g. the insulator layer) or by use of a photoresist (e.g. for most of the semiconductors and conductors). Layer 48 forms a column electrode 47 and a pixel pad 110, and layer 44 forms the row electrode 45.
Table 1 shows illustrative materials which may be used for an active-matrix circuit with polymer electronics.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>Polycarbonate, Polyethylene naphtalene, …</td>
</tr>
<tr>
<td>Gate line</td>
<td>Au, Al, Cu, Indium-tin oxide …</td>
</tr>
<tr>
<td>Insulator layer</td>
<td>Photoresist: HPR504, SU8 …</td>
</tr>
<tr>
<td>Data line/ Pixel pad</td>
<td>Metal: Au, Pd, Pt, ZnSnO3, SnO2:F, Ag</td>
</tr>
<tr>
<td>Semiconductor</td>
<td>Poly-(thienylene vinylene), pentacene, …</td>
</tr>
</tbody>
</table>

* Base material that can be coated with a number of barrier layers.

Stack 40 may be employed as a basis for providing features in accordance with the present invention. Stack 40 may be replaced with other pixel circuits and may still benefit from the teachings of the present invention.

Referring to FIG. 4, a current pixel cell layout of the active matrix backplane is illustratively shown. First areas 55 show the positions of semiconductor islands. Second areas 60 denote the 1st metal layer. Third areas 65 show the 2nd metal layer, while the continuous insulator layer is not shown. Pixel layout of the backplane design in FIG. 4 does not yet include a field shield.

Referring to FIG. 5, a stack 100 includes a field-shielded stack for one pixel with an organic TFT to be employed for displays with organic electronics. In this embodiment, two layers are illustratively added to the stack 40 of FIG. 3. An insulator layer 102 and a conductive layer 104 are formed on stack 40. Some of the advantages of this stack 100 include higher contrast, lower optical crosstalk and a more uniform switching of the pixels due to the shielding of the electrical fields of the row and column electrodes by the field shield electrode.

Insulator 102 may include a photoresist material or other organic insulation material. Insulator 102 is formed over a semiconductor material 50 which forms a portion of a TFT 106. Semiconductor material 50 may include an inorganic or organic semiconductor material. In one embodiment, material 50 includes pentacene, although other materials may also be employed. After preparing insulator 102, conductive layer 104 is formed on insulator 102. Insulator 102 may be patterned to form openings to permit via connections 108 through
insulator 102. Vias 108 may be formed concurrently with conductive layer (e.g., using a dual damascene technique) or formed separately from layer 104. Conductive layer 104 may include, e.g., Au, Al, Cu, Indium-tin oxide, Pd, Pt, ZnSnO₃, SnO₂:F, Ag or any other suitable conductor.

[0030] Conductive layer 104 connects to a pixel pad 110 formed from layer 48 (FIG. 3). Conductive layer 104 forms a field shield 112 over pixel pad 110, and further extends over at least a portion of the pixel pad 110 (or other pixel electrodes) and in a preferred embodiment over at least a portion of TFT 106. In this way, field shield 112 forms a capacitive relationship with TFT 106, which may be employed to improve TFT performance as will be explained hereinbelow. The thin film field effect transistor 106 may include an organic interlayer dielectric layer 46 between conductive and/or semiconductive portions.

[0031] Referring to FIG. 6, the field-shielded pixel circuit of the active matrix backplane is illustratively shown. A first area 120 shows the conductive layer 104 (the field shield). Second areas 125 show the positions of the semiconductor islands. Third areas 130 denote the 1st metal layer. Fourth areas 135 show the 2nd metal layer, while the continuous insulator layer is not shown.

[0032] An ideal pixel TFT delivers a high on-current, while it occupies a small area in the pixel. One problem includes that this ideal is never reached, especially not with organic electronics. The higher the on-current, the larger the display that can be made. The smaller the TFT area, the higher the yield of the active-matrix backplane.

[0033] In accordance with the present invention, conductive layer 104 provides a field-shield for a display which offers the opportunity to increase the on-current of the TFT 106, while its area is not increased, by using the layer 104 as a "second gate" of the TFT 106 (see FIG. 7). The transfer characteristics are illustratively shown in FIG. 8 for different values of the second gate formed in the layer 104.

[0034] Referring to FIG. 7, an equivalent active-matrix pixel circuit 200 for a field shielded pixel is illustratively shown in accordance with one embodiment. A single pixel 202 is shown,
which may be part of a plurality of pixels forming an active-matrix display. A row electrode 224 forms a storage capacitor for the pixels in a next row. Active-matrix displays are driven a row-at-a-time. During one frame time, all the rows are sequentially selected by applying a voltage that changes thin film transistors (TFTs) 226 from a non-conducting state to a conducting state. In this line selection time, capacitors 228 and 230 and capacitance between the gate and drain of TFT 226 (i.e., the total capacitance at the drain side of the TFT) of the selected row are charged to the voltage supplied on a column electrode 232 (e.g., +/-15V, OV).

[0035] During the remaining frame time (i.e., the hold time), the other rows are addressed. The TFTs 226 are then in their non-conducting state and the charge on the pixel capacitors 228 and 230 is retained. Between image updates the active-matrix is at rest at 0 V for the row and column electrodes, the pixel pads and the common electrode.

[0036] $C_{DE}$ is the capacitor 230 providing the display effect, $C_s$ is the storage capacitor 228, and $C_{gd}$ is the parasitic gate-drain capacitor in the TFT 226. In the circuit 200, the previous row electrode forms the storage capacitor line. The pixel pad 110 forms a second gate 215 of the TFT 226.

[0037] Referring to FIG. 8, transfer characteristics of a field shielded organic TFT with a mobility of 0.01cm2V−1s−1 for the pixel electrode (i.e., the 3rd metal layer 104) voltages ($V_p$) from +100V to -100V, in steps of 20V are illustratively shown. Drain current $I_D$ through the transistor is plotted against gate voltage ($V_G$). An inset plot 300 shows extracted threshold voltage ($V_{th}$) as a function of pixel electrode voltage ($V_p$), where the channel length of the TFT is 5 microns and width of 1000 microns, with supply voltage $V_D$ = -1V.)

[0038] Without a field shield, the on-current of the TFT is lower when the pixel is charged to a negative voltage compared to charging to a positive voltage. This is due to the lower source-gate voltage when charging to a negative voltage. Pixel charging to a negative voltage is therefore one of the determining factors for the size of the pixel TFT.
With the field shielding, the on-current during charging to a negative voltage is increased due to the negative voltage on the second gate 215 (FIG. 7). The on-current during charging to a positive voltage will be lower. This results in more symmetric charging characteristics and the possibility for using a smaller pixel TFT.

A number of alternate embodiments may be employed using different configurations of second gate 215 in a display.

Referring to FIG. 9, insulator 102 may be patterned or otherwise altered to provide different thicknesses over TFT 106 and other areas of the pixel cell. This adjusts the second gate 215 (FIG. 7) by selecting an appropriate insulator thickness between semiconductor 50 and a field shield 113. It is preferable that the field shield insulator 102 be as thick as possible to avoid electrical crosstalk between the field shield 113 and the row and column electrodes in layers 44 and 48, respectively. When the insulator layer 102 is thin on the other hand the conductive layer 104 can increase the on-current of the TFT because of its effect as a second gate.

Referring to FIG. 10, two different insulator layers 150 and 152 may be employed for insulator 102. Layer 150 may be employed to provide the appropriate thickness of the dielectric between field shield 113 and semiconductor 50. Layer 152 may be formed and patterned on layer 150 providing a different thickness for the insulator in other areas. Layers 150 and 152 may include a same material or different materials. The layers 150 and 152 are patterned to form via holes or other structures. To avoid the compromise between a higher on-current and electrical crosstalk, a thin second insulator layer 150 in the region of the TFT 106 and a thick insulator layer 152 may be applied in the rest of the pixel. This maximizes the increase of the on-current, while the electrical crosstalk is minimized.

This stack can be made in a number of ways. One possibility is to omit stripping of the resist (layer 150) that is used for patterning the semiconductor 50, followed by patterning the second insulator layer 152 in the region of the TFT 106. The resist 150 may be about 1 micron thick, while the insulator layer 152 can be much thicker (e.g., 5 microns). Other thicknesses are also contemplated.
Referring to FIG. 11, a field-shielded stack for one pixel with an organic TFT is shown, where a second gate 215 is formed by an overlap of a field shield 112 between a TFT 226 and/or a pixel pad 110 in the next row. Using the second gate 215, a boost for the on-current is provided.

The second gate 215 is connected to the next pixel pad 110' in an adjacent pixel cell. An equivalent circuit is illustratively shown in FIG. 12.

Referring to FIG. 12, an active-matrix pixel schematic is shown for an embodiment for the field shielded pixel structure of FIG. 11. The pixel electrode 110' of an adjacent row is connected to the second gate 215 of the TFT 226 by a connection 231.

To illustrate some of the advantages of the structure shown in FIGS. 11 and 12, the following example is provided. The pixel pad 110 is driven between say, +15V and -15V. When the pixel is refreshed, the gate electrode (G) (e.g., the row line 224) is set from +25V to -25V. The gate electrode (G) is a storage capacitor of the next row of pixels. This next row of pixels is therefore set to a pixel voltage between -65V and -35V during the refresh period. By connecting the second gate 215 of the pixel to the pixel pad of the pixel in the next row, this large negative voltage is applied to the TFT 226 during the refresh. This leads to a factor of 3-5 times higher on-current during this time, as can be seen in FIG. 8. After the refresh period, the gate (G) is reset to +25V. The pixel pad 110 in the next row is then reset to the normal pixel voltage between +15V and -15V. This ensures that the leakage current in the pixel remains sufficiently low in the time between two refresh periods.

The field shield may extend over a portion of the thin film field effect transistor of an adjacent pixel cell to form a capacitive relationship with a thin film field effect transistor of the adjacent pixel cell to enhance performance of that transistor. Likewise, the field shield may extend over a portion of the pixel pad of an adjacent pixel cell to form a capacitive relationship with a pixel pad of the adjacent pixel cell to enhance performance of that pixel pad.
The embodiments described herein may be combined with other embodiments, for example, the gap between the field shield and the TFT (e.g., second gate) may be adjusted as described when the second gate is connected to the pixel pad of a next row. Other combinations are also contemplated.

Advantages aspects of the present invention include the TFT area can be made smaller while keeping the optical display performance optimal. This increases the yield of the displays and enables larger displays to be made with the current performance of the organic TFTs. Application areas include all active-matrix displays. These displays may include a field shielded design. The present invention can also be applied to other technologies other than organic electronics, for example, amorphous silicon or poly-crystalline silicon may also be employed.

Having described preferred embodiments for pixel performance improvement by use of a field-shield (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments of the disclosure disclosed which are within the scope and spirit of the embodiments disclosed herein as outlined by the appended claims. Having thus described the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.
1. A pixel cell for an active matrix display, comprising:
   a pixel pad (110);
   a thin film field effect transistor (106) which selectably couples a signal to activate/deactivate the pixel pad;
   a field shield (112) formed on an insulating layer (102) and connected to the transistor through the insulating layer such that the field shield extends over at least a portion of an electrode of the pixel cell (110) or the transistor (106).

2. The pixel cell as recited in claim 1, wherein the thin film field effect transistor (106) includes an organic semiconductor material.

3. The pixel cell as recited in claim 1, wherein the thin film field effect transistor (106) includes an organic interlayer dielectric layer.

4. The pixel cell as recited in claim 1, wherein the thin film field effect transistor (106) selectively connects a column electrode (47) to the pixel pad (110) in accordance with a signal on a row electrode (45).

5. The pixel cell as recited in claim 1, wherein the field shield (112) extends over a portion of the thin film field effect transistor to form a capacitive relationship with the thin film field effect transistor to enhance performance of the transistor.

6. The pixel cell as recited in claim 1, wherein the field shield (112) extends over a portion of the thin film field effect transistor (106) of an adjacent pixel cell to form a capacitive relationship with a thin film field effect transistor of the adjacent pixel cell to enhance performance of that transistor.

7. The pixel cell as recited in claim 1, wherein the field shield (112) extends over a portion of the pixel pad (110) of an adjacent pixel cell to form a capacitive relationship with a pixel pad of the adjacent pixel cell to enhance performance of that pixel pad.
8. A pixel cell for an active matrix display, comprising:
   a pixel pad (110);
   a thin film field effect transistor (106) which selectably couples a signal to activate/deactivate the pixel pad;
   a field shield (112) formed on an insulating layer (102) and connected to the transistor through the insulating layer such that the field shield extends over at least a portion of the transistor (106) to form a second gate (215) which enhances the transistor performance.

9. The pixel cell as recited in claim 8, wherein the thin film field effect transistor (106) includes an organic semiconductor material.

10. The pixel cell as recited in claim 8, wherein the thin film field effect transistor (106) includes an organic interlayer dielectric layer.

11. The pixel cell as recited in claim 8, wherein the thin film field effect transistor (106) selectively connects a column electrode (47) to the pixel pad in accordance with a signal on a row electrode (45).

12. The pixel cell as recited in claim 8, wherein the insulator layer (102) has a different thickness between the field shield and the thin film field effect transistor than between the field shield and other areas of the pixel cell.

13. The pixel cell as recited in claim 8, wherein the insulator layer (102) has a smaller thickness between the field shield and the thin film field effect transistor than between the field shield and other areas the pixel cell.

14. The pixel cell as recited in claim 8, wherein the second gate (215) formed by the field shield (112) increases on-current for the thin film field effect transistor.
15. A method for forming a pixel for active matrix displays, comprising the steps of:
   forming an insulator (102) over a pixel stack (40), the pixel stack including a thin film transistor (106), a pixel pad (110) and addressing lines (45, 47); and
   patterning a conductive layer formed over the insulator to form a field shield (112) which connects to the pixel pad, the field shield connecting to the pixel pad through the insulating layer such that the field shield extends over at least a portion of the thin film transistor to form a second gate (215) which enhances the transistor performance.

16. The method as recited in claim 15, further comprising the step of activating the pixel pad (110) and field shield (112) to increase on-current for the thin film field effect transistor.

17. The method as recited in claim 15, wherein the step of forming an insulator includes setting a thickness of the insulator (102) in accordance with performance criteria for the thin film transistor.

18. The method as recited in claim 15, wherein the step of patterning the conductive layer includes patterning the conductive layer such that the field shield (112) of a first pixel cell extends over a thin film transistor of an adjacent cell.

19. The method as recited in claim 15, wherein the step of patterning the conductive layer includes patterning the conductive layer such that the field shield (112) of a first pixel cell extends over a pixel pad of an adjacent cell.
FIG. 7

FIG. 8A

FIG. 8B