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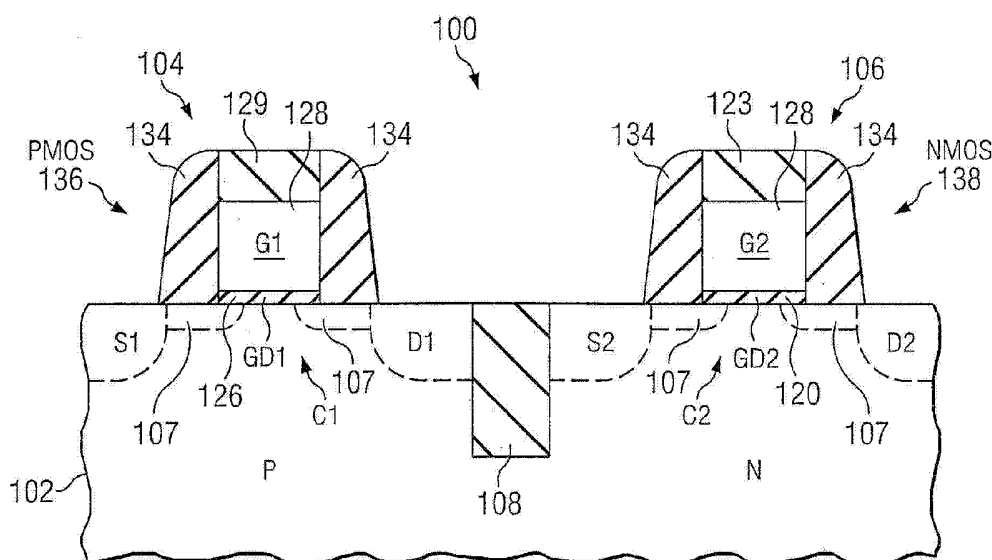
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(54) Title: TRANSISTOR DEVICE AND METHOD OF MANUFACTURE THEREOF



(57) Abstract: A method of forming transistors and structures thereof. A CMOS device includes high k gate dielectric materials. A PMOS device includes a gate that is implanted with an n type dopant. The NMOS device may be doped with either an n type or a p type dopant. The work function of the CMOS device is set by the material selection of the gate dielectric materials. A polysilicon depletion effect is reduced or avoided.

Transistor Device and Method of Manufacture Thereof

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application relates to the following co-pending and commonly assigned patent application: Serial No. 10/870,616, filed on June 17, 2004, entitled, "CMOS Transistor With Dual High-k Gate Dielectric and Method of Manufacture Thereof," which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates generally to semiconductor devices, and more particularly structures for and methods of manufacturing transistors.

BACKGROUND

[0003] Semiconductor devices are used in a variety of electronic applications, such as personal computers, cell phones, digital cameras, and other electronic equipment, as examples. Semiconductor devices are typically fabricated by sequentially depositing insulating (or dielectric) layers, conductive layers, and semiconductive layers of material over a semiconductor substrate, and patterning the various layers using lithography to form circuit components and elements thereon.

[0004] A transistor is an element that is utilized extensively in semiconductor devices. There may be millions of transistors on a single integrated circuit (IC), for example. A common type of transistor used in semiconductor device fabrication is a metal oxide semiconductor field effect transistor (MOSFET).

[0005] Early MOSFET processes used one type of doping to create either positive or negative channel transistors. More recent designs, referred to as complimentary MOS (CMOS) devices, use both positive and negative channel devices, e.g., a positive channel metal oxide semiconductor (PMOS) transistor and a negative channel metal oxide semiconductor (NMOS) transistor, in complimentary configurations. An NMOS device negatively charges so that the transistor is turned on or off by the movement of electrons, whereas a PMOS devices involves the movement of electron vacancies. While the manufacture of CMOS devices requires more manufacturing steps and more transistors, CMOS devices are advantageous because they utilize less power, and the devices may be made smaller and faster.

[0006] The gate dielectric for MOSFET devices has in the past typically comprised silicon dioxide, which has a dielectric constant of about 3.9. However, as devices are scaled down in size, using silicon dioxide for a gate dielectric becomes a problem because of gate leakage current, which can degrade device performance. Therefore, there is a trend in the industry towards the development of the use of high dielectric constant (k) materials for use as the gate dielectric in MOSFET devices. The term "high k materials" as used herein refers to a dielectric material having a dielectric constant of about 4.0 or greater.

[0007] High k gate dielectric development has been identified as one of the future challenges in the 2002 edition of International Technology Roadmap for Semiconductors (ITRS), incorporated herein by reference, which identifies the technological challenges and needs facing the semiconductor industry over the next 15 years. For low power logic (for portable electronic applications, for example), it is important to use devices having low leakage current, in order to extend battery life. Gate leakage current must be controlled in low power applications, as well as sub-threshold leakage, junction leakage, and band-to-band tunneling.

[0008] However, one problem with using high k materials as gate dielectric materials is lower mobility, which is undesirable. Device performance using high k dielectric materials tends to suffer from trapped charge in the dielectric layer, which deteriorates the mobility, making the drive current lower than in transistors having silicon dioxide gate oxides, thus reducing the speed and performance of transistors having high k gate dielectric materials.

[0009] Polysilicon is most often used as a gate material in transistor devices. Another problem of using high k materials as a gate dielectric is that if polysilicon is used as a gate material in conjunction with a high k gate dielectric, poly (polysilicon) depletion can occur between the gate dielectric and the gate. When a CMOS device is operated in an inversion mode, poly depletion causes an increase in the electrical equivalent gate oxide, e.g., by about 4 to 5 Angstroms. It is desirable for the gate capacitance to be relatively high for increased gate control. However, poly depletion decreases the capacitance and lowers the drive current of the CMOS device, which is undesirable.

[0010] What is needed in the art is a transistor design that does not suffer from the poly depletion effect.

[0011] Another problem with using a high-k dielectric material as the gate dielectric of a CMOS transistor is referred to in the art as a "Fermi-pinning" effect, which occurs at the interface of the gate electrode and gate dielectric material. Fermi-pinning is a problem that occurs in CMOS devices having both polysilicon and metal gates. The Fermi-pinning effect causes a threshold voltage shift and low mobility, due to the increased charge caused by the Fermi-pinning effect. Fermi-pinning causes an asymmetric turn-on threshold voltage V_t for the two transistors of a CMOS device, which is undesirable.

[0012] In prior art CMOS transistor designs, shown in Figure 20, typically SiO_2 was used as a gate dielectric material 580, and polysilicon was used as a gate electrode material 582 and 584. A symmetric threshold voltage V_t for the PMOS device and the NMOS device of a prior art CMOS device 500 was easily achieved using SiO_2 as a gate dielectric material 580. The manufacturing steps typically comprised providing a workpiece 502, and forming an n well and p well in the PMOS region and NMOS region, respectively. In some designs, isolation regions 508 were formed between the n well and p well. The gate dielectric 580 was formed over the workpiece 502, and the gate electrode material 582/584 comprising a layer of polysilicon was formed over the gate dielectric 580. The gate electrodes 582 and 584 and gate dielectric 580 were patterned, and the workpiece 502 was lightly doped to form source and drain extensions 507. Spacers 534 were formed over the sidewalls of the gate electrodes 582 and 584 and gate dielectric 580. The workpiece 502 was then more deeply implanted with dopants to form the source and drain regions S and D of the device 500. For the PMOS device, the gate electrode 582 was p type, which was achieved by doping the polysilicon gate with boron (B). For the NMOS device, the gate electrode 584 was n type, which was typically achieved by doping the polysilicon gate with phosphorus (P) or arsenic (As), as examples.

[0013] In electronics, the “work function” is the energy, usually measured in electron volts, needed to remove an electron from the Fermi level to a point an infinite distance away outside the surface. Work function is a material property of any material, whether the material is a conductor, semiconductor, or dielectric. The work function of a semiconductor can be changed by doping the semiconductor material. For example, undoped polysilicon has a work function of about 4.5 eV, whereas polysilicon doped with boron has a work function of about 5.0 eV. The

work function of a semiconductor or conductor directly affects the threshold voltage of a transistor when the material is used as a gate electrode.

[0014] In prior art CMOS devices such as device 500 shown in Figure 20 utilizing SiO_2 or SiON as the gate dielectric material 580, the work function of the CMOS device 500 could be changed or tuned by doping the polysilicon used for the gate electrode material 582/584.

However, high-k gate dielectric materials such as hafnium-based dielectric materials exhibit Fermi-pinning, which is caused by the interaction of the high-k gate dielectric materials with adjacent materials, e.g., the gate material. When used as a gate dielectric, high k gate dielectric materials pin or fix the work function, so that doping the polysilicon gate material does not change the work function. Thus, a symmetric V_t for the NMOS and PMOS transistors of a CMOS device having a high k material for the gate dielectric cannot be achieved by doping polysilicon gate material, as in SiO_2 gate dielectric CMOS devices. A CMOS device having a high k dielectric material for the NMOS and PMOS transistors has an asymmetric V_{tn} and V_{tp} , due to the Fermi-pinning effect of the high k dielectric material. Efforts have been made to improve the quality of high-k dielectric films and resolve the Fermi-pinning problems, but the efforts have resulted in little success.

[0015] Thus, what is needed in the art is a CMOS transistor device design and method of manufacturing thereof that has a high-k gate dielectric material and a symmetric V_t for the p channel metal oxide semiconductor (PMOS) and n channel metal oxide semiconductor (NMOS) transistors of the CMOS device, that does not exhibit a polysilicon depletion effect.

SUMMARY OF THE INVENTION

[0016] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention, which provide transistors and methods of manufacture thereof having a substantially symmetric threshold voltage V_t for the PMOS and NMOS transistors. The gate material of a PMOS transistor is doped with an n type dopant, and the gate of an NMOS transistor is doped with a p type dopant or n type dopant, in a CMOS device. In some embodiments, a different gate dielectric material is used for the PMOS transistor than for the NMOS transistor. Polysilicon depletion effects are reduced or avoided by the novel embodiments of the present invention described herein.

[0017] In accordance with a preferred embodiment of the present invention, a transistor includes a workpiece, the workpiece having a region implanted with a first dopant. A gate dielectric is disposed over the workpiece. A gate is disposed over the gate dielectric, the gate comprising a semiconductive material and being implanted with the first dopant. A source region and a drain region are formed in the region of the workpiece, wherein the source region and the drain region are proximate the gate dielectric.

[0018] In accordance with another preferred embodiment of the present invention, a CMOS device includes a workpiece and a PMOS transistor and NMOS transistor formed in a first region and a second region, respectively, of the workpiece. The PMOS transistor includes a first gate dielectric disposed over the workpiece and a first gate disposed over the first gate dielectric. The first gate comprises a first semiconductive material comprising an n type dopant. The NMOS transistor includes a second gate dielectric disposed over the workpiece and a second gate

disposed over the first gate dielectric. The second gate comprises a second semiconductive material.

[0019] In accordance with yet another preferred embodiment of the present invention, a method of manufacturing a transistor includes providing a workpiece, implanting a first dopant into the workpiece, and forming a gate dielectric over the workpiece. A gate is formed over the gate dielectric, the gate comprising a semiconductive material. The method includes implanting the first dopant into the gate.

[0020] In accordance with another preferred embodiment of the present invention, a method of manufacturing a CMOS device includes providing a workpiece, forming a PMOS transistor in a first region of the workpiece, and forming an NMOS transistor in a second region of the workpiece. The PMOS transistor comprises a first gate dielectric disposed over the workpiece and a first gate disposed over the first gate dielectric, the first gate comprising a first semiconductive material. The method includes implanting an n type dopant into the first semiconductive material of the first gate. The NMOS transistor includes a second gate dielectric disposed over the workpiece and a second gate disposed over the second gate dielectric, the second gate comprising a second semiconductive material.

[0021] Advantages of preferred embodiments of the present invention include providing a method of fabricating a CMOS device and structure thereof, wherein the PMOS transistor and NMOS transistor have a symmetric V_t . The threshold voltage V_t is decreased compared to prior art CMOS devices, and the flat band voltage is easier to tune. Embodiments of the invention may utilize high-k dielectric materials as the gate dielectric, using polysilicon, partially silicided, or fully silicided gate electrodes. Polysilicon depletion and boron penetration effects when the device is operated in an inversion mode are prevented, because the semiconductive material of

the gates function in an accumulation regime, due to the presence of the novel reversal of dopants implanted in the PMOS and NMOS gates. The capacitance effective thickness (CET) of a CMOS device can be decreased in accordance with embodiments of the present invention.

[0022] The foregoing has outlined rather broadly the features and technical advantages of embodiments of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of embodiments of the invention will be described hereinafter, which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0024] Figures 1 through 9 show cross-sectional views of a semiconductor device at various stages of manufacturing in accordance with a preferred embodiment of the present invention, wherein a CMOS device comprises a PMOS transistor having a first gate dielectric material and an NMOS transistor having a second gate dielectric material, wherein the first gate dielectric material and the second gate dielectric material comprise different materials, and wherein the gate of the PMOS transistor is doped with an n type dopant, and the gate of the NMOS transistor is doped with a p type dopant or an n type dopant;

[0025] Figure 10 shows an another preferred embodiment of the present invention, wherein the PMOS transistor gate dielectric comprises a first layer and a second layer, wherein the second layer is adjacent and abuts the PMOS transistor gate electrode, and wherein the second layer comprises a Fermi-pinning material;

[0026] Figures 11 through 17 show cross-sectional views of methods of forming a CMOS device in accordance with other preferred embodiments of the present invention at various stages of manufacturing, wherein the PMOS transistor gate is doped with an n type dopant;

[0027] Figures 18 and 19 show cross-sectional views of a method of forming a CMOS device in accordance with yet another preferred embodiment of the present invention at various stages of manufacturing, wherein the PMOS transistor gate is doped with an n type dopant;

[0028] Figure 20 shows a prior art CMOS device, wherein the gate of the PMOS transistor is doped with a p type dopant, and the gate of the NMOS transistor is doped with an n type dopant;

[0029] Figure 21 shows a cross-sectional view of an embodiment of the present invention, wherein a gate of a PMOS transistor is doped with an n type dopant, and the gate of an NMOS transistor is doped with a p type or n type dopant; and

[0030] Figures 22 and 23 show another embodiment of the present invention, wherein the source and drain regions are formed by etching back the workpiece after patterning the gate and gate dielectric material, and filling the source and drain regions in with an in-situ doped material.

[0031] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0032] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0033] High-k gate dielectrics generally yield orders of magnitude lower gate leakage current than SiO_2 gate dielectrics with the same effective oxide thickness (EOT). For low standby power (LSTP) and high performance (HP) applications, the use of a high-k material for a gate dielectric is a potential solution in the roadmap for the advanced technology nodes. Using high-k materials for gate dielectrics in CMOS devices has resulted in good EOT, lower gate leakage (J_g), mobility and hysteresis parameters, but the devices suffer from lack of V_t controllability. In order to make high-k materials as gate dielectrics useful in CMOS applications, it is desirable that the CMOS device should be manufactured such that V_{tn} and V_{tp} are symmetrical; e.g., $V_{tn}=0.3$ V and $V_{tp}=-0.3$ V, as examples.

[0034] Attempts to use a high-k dielectric material such as HfO_2 have been problematic. In particular, attempts have been made to use HfO_2 , which is a high-k dielectric material having a dielectric constant of about 25, as the gate dielectric for both the PMOS and NMOS FETs of a CMOS device. The work function of a polysilicon gate using a HfO_2 gate dielectric has been found to be pinned, as a result of Fermi-pinning, at a point close to the conduction band of polysilicon, causing the polysilicon gate to function as n type polysilicon, even for the polysilicon gate doped with p type dopant, for the PMOS device. Therefore, the threshold

voltage V_{tp} of the PMOS device was found to be much higher than expected; e.g., V_{tp} was -1.2 V while V_{tn} was 0.4 V, which is very asymmetric. The Fermi-pinning effect is suspected to be related to the Hf-Si bond at the gate electrode to gate dielectric interface, which is almost impossible to avoid with a polysilicon-HfO₂ gate stack structure. Therefore, the Fermi-pinning effect makes the use of polysilicon as a gate electrode incompatible with Hf-based high-k gate dielectric materials in CMOS devices. Fully silicided polysilicon (FUSI) gates have also exhibited Fermi-pinning effects and are undesirable for use as gate electrode materials when a high-k dielectric such as hafnium is used for a gate dielectric.

[0035] Another problem of prior art CMOS devices is a polysilicon depletion effect, which occurs when the device is operated in the inversion regime; e.g., $V > V_{tn}$ in the NMOS transistor or $V < V_{tp}$ in the PMOS transistor. In the inversion regimes, the gate voltage causes the bottom of the gate to become depleted of electrons for the NMOS transistor and to become depleted of holes for the PMOS transistor. The depleted region at the bottom of the gates at the interface of the gates and the gate dielectric materials reduces the total capacitance of the gate stack, and hence, increases the capacitive effective thickness (CET). As a result, the drive current is reduced, which is undesirable.

[0036] Embodiments of the present invention derive technical advantages by disposing a thin layer of a Fermi-pinning material such as Al₂O₃ adjacent and abutting a gate electrode of a PMOS device, disposed over a high-k dielectric material such as HfO₂, while using a single layer of high-k dielectric material as the gate dielectric for the NMOS device. By doing so, polysilicon or FUSI may be used as the gate electrode while still achieving a symmetric V_{tp} and V_{tn} for the CMOS device. In the PMOS portion, a polysilicon to Al₂O₃ interface sets the work function in the p-type regime, and in the NMOS portion, a polysilicon to Hf interface sets the

work function in the n-type regime. The gate of the PMOS device is preferably doped with an n type dopant, and the gate of the NMOS device may be doped with a p type or an n type dopant, to avoid the polysilicon depletion effect.

[0037] The present invention will be described with respect to preferred embodiments in a specific context, namely a CMOS transistor. Embodiments of the present invention may also be applied, however, to other semiconductor device applications where one or more transistors are utilized. Embodiments of the present invention have useful application in single NMOS transistor or single PMOS transistor designs, for example. Note that in the drawings shown, only one PMOS device and one NMOS device are shown; however, there may be many PMOS and NMOS devices formed on a semiconductor workpiece during each of the manufacturing processes described herein.

[0038] Figures 1 through 9 show cross-sectional views of a semiconductor device 100 at various stages of manufacturing in accordance with a preferred embodiment of the present invention. With reference now to Figure 1, there is shown a semiconductor device 100 in a cross-sectional view including a workpiece 102. The workpiece 102 may include a semiconductor substrate comprising silicon or other semiconductor materials covered by an insulating layer, for example. The workpiece 102 may also include other active components or circuits, not shown. The workpiece 102 may comprise silicon oxide over single-crystal silicon, for example. The workpiece 102 may include other conductive layers or other semiconductor elements, e.g., transistors, diodes, etc. Compound semiconductors, GaAs, InP, Si/Ge, or SiC, as examples, may be used in place of silicon. The workpiece 102 may also comprise a silicon-on-insulator (SOI) substrate.

[0039] The workpiece 102 includes a first region 104 and a second region 106. The first region 104 comprises a region where a first transistor comprising a PMOS device or PMOSFET, (indicated by the "P" in the workpiece 102 in the figures) as examples, will be formed. The second region 106 comprises a region where a second transistor comprising an NMOS device or NMOSFET (indicated by the "N" in the workpiece 102 in the figures) will be formed, as examples. The PMOS device and NMOS device are not shown in Figure 1: see Figures 8 and 9 at 136 and 138, respectively.

[0040] The first region 104 and the second region 106 may be separated by an optional shallow trench isolation (STI) region 108 formed in the workpiece 102, as shown. The first region 104 may be doped with n type dopants, e.g., to form an N well, and the second region 106 may be doped with p type dopants, e.g., to form a P well. In general, the workpiece 102 is doped with n or p type dopants depending on whether the junctions of the transistor to be formed will be p or n type, respectively.

[0041] The workpiece 102 is preferably cleaned using a pre-gate clean process to remove contaminants or native oxide from the top surface of the workpiece 102. The pre-gate treatment may comprise a HF, HCl or ozone based cleaning treatment, as examples, although the pre-gate treatment may alternatively comprise other chemistries.

[0042] A hard mask 112 is deposited over the workpiece 102, as shown in Figure 2. The hard mask 112 preferably comprises a first layer 114 and a second layer 116 disposed over the first layer 114, as shown. Alternatively, the hard mask 112 may comprise a single layer of an oxide or a nitride material, for example. In the embodiment shown in Figure 2, the first layer 114 of the hard mask 112 preferably comprises about 300 Angstroms of an oxide material such as tetraethoxysilate (TEOS), although alternatively, the first layer 114 may comprise other

insulating materials deposited in other dimensions, for example. The first layer 114 may be deposited by plasma-enhanced chemical vapor deposition (PECVD) or by other deposition techniques, as examples. The second layer 116 preferably comprises about 1500 Angstroms of a nitride material such as Si_xN_y , for example, although alternatively, the second layer 116 may comprise other insulating materials deposited in other dimensions, for example. The second layer 114 may be deposited by PECVD or by other deposition techniques, as examples.

[0043] A first layer of photoresist 118 is deposited over the second layer 116 of the hard mask 112, as shown in Figure 2. The first layer of photoresist 118 may be patterned with a mask using traditional lithography techniques, although alternatively, the first layer of photoresist 118 may be directly patterned using electron beam lithography (EBL) or other direct etching technique, as examples.

[0044] The first layer of photoresist 118 is used to pattern at least the second layer 116 of the hard mask 112, as shown in Figure 3. For example, exposed portions of the second layer 116 in the second region 106 may be etched using the first layer of photoresist 118 remaining over the first region 104 as a mask. The etch process may be designed to stop when the first layer 114 of the hard mask 112 is reached. The first layer of photoresist 118 is then stripped or removed, and the second layer 116 is then used as a mask to pattern the first layer 114. Alternatively, the first layer of photoresist 118 may be used as a mask to etch both the second layer 116 and the first layer 114 of the hard mask 112, for example. The first layer of photoresist 118 is then stripped or removed.

[0045] A first gate dielectric material 120 is deposited over the patterned hard mask 112 and exposed portions of the workpiece 102, as shown in Figure 3. The first gate dielectric material 120 preferably comprises a high-k dielectric material having a dielectric constant of about 4.0 or

greater, in one embodiment. The first gate dielectric material 120 preferably comprises HfO_2 , HfSiO_x , Al_2O_3 , ZrO_2 , ZrSiO_x , Ta_2O_5 , La_2O_3 , nitrides thereof, Si_xN_y , SiON , HfAlO_x , $\text{HfAlO}_x\text{N}_{1-x-y}$, ZrAlO_x , ZrAlO_xN_y , SiAlO_x , $\text{SiAlO}_x\text{N}_{1-x-y}$, HfSiAlO_x , $\text{HfSiAlO}_x\text{N}_y$, ZrSiAlO_x , $\text{ZrSiAlO}_x\text{N}_y$, combinations thereof, or combinations thereof with SiO_2 , as examples, although alternatively, the first gate dielectric material 120 may comprise other high k insulating materials or other dielectric materials. The first gate dielectric material 120 may comprise a single layer of material, or alternatively, the first gate dielectric material 120 may comprise two or more layers. In one embodiment, one or more of these materials can be included in the first gate dielectric material 120 in different combinations or in stacked layers. The first gate dielectric material 120 may be deposited by chemical vapor deposition (CVD), atomic layer deposition (ALD), metal organic chemical vapor deposition (MOCVD), physical vapor deposition (PVD), or jet vapor deposition (JVD), as examples, although alternatively, the first gate dielectric material 120 may be deposited using other suitable deposition techniques. The first gate dielectric material 120 preferably comprises a thickness of about 10 Å to about 60 Å in one embodiment, although alternatively, the first gate dielectric material 120 may comprise other dimensions, such as about 80 Å or less, as an example.

[0046] A first gate material 122 is deposited over the first gate dielectric material 120, also shown in Figure 3. The first gate material 122 preferably comprises a semiconductive material, such as polysilicon or amorphous silicon, although alternatively, other semiconductive materials may be used for the first gate material 122. In the embodiment shown in Figure 1-9, the first gate material 122 preferably comprises polysilicon or other semiconductor materials.

Alternatively, the first gate material 122 may comprise TiN , HfN , TaN , W , Al , Ru , RuTa , TaSiN , NiSi_x , CoSi_x , TiSi_x , Ir , Y , Pt , Ti , PtTi , Pd , Re , Rh , borides, phosphides, or antimonides of

Ti, Hf, Zr, TiAlN, Mo, MoN, ZrSiN, ZrN, HfN, HfSiN, WN, Ni, Pr, VN, TiW, a partially silicided gate material, a fully silicided gate material (FUSI), other metals, and/or combinations thereof, as examples. If the gate material 122 comprises FUSI, for example, polysilicon may be deposited over the gate dielectric material 120, and a metal such as nickel may be deposited over the polysilicon, although other metals may be used. The workpiece 102 may then be heated to about 600 or 700 degrees C to form a single layer of nickel silicide. The first gate material 122 may comprise a plurality of stacked gate materials, such as a metal underlayer with a polysilicon cap layer disposed over the metal underlayer. The first gate material 122 may be deposited using CVD, PVD, ALD, or other deposition techniques, as examples. The first gate material 122 preferably comprises a thickness of about 1500 Å, although alternatively, the first gate material 122 may comprise about 1000 Å to about 2000 Å, or other dimensions, for example.

[0047] In one embodiment, at this stage of the manufacturing process, in an optional step, the first gate material 122 is implanted with a dopant 190. The dopant 190 may comprise either an n type dopant or a p type dopant. For example, the first gate material 122 may be n doped by doping the first gate material 122 with phosphorus or As. Alternatively, in another embodiment, the first gate material 122 may be p doped by doping the first gate material 122 with B.

Generally, because polysilicon depletion is not as much of a concern in an NMOS transistor as in a PMOS transistor of a CMOS device, in accordance with an embodiment of the present invention, both the PMOS transistor and NMOS transistor gates may be doped with an n type dopant.

[0048] Doping the first gate material 122 makes the semiconductive material conductive or more conductive. Preferably, the work function of the NMOS transistor (see 138 in Figure 9) is set by the material selection for the gate dielectric material 120, rather than by the dopant

implanted into the first gate material 122, in accordance with an embodiment of the present invention.

[0049] After implanting the dopant 190, an optional hard mask 123 may be deposited over the first gate material 122. The optional hard mask 123 protects the first gate material 122 from being implanted with the dopants that are implanted to form the source and drain extension regions and source and drain regions, to be described further herein. If the first gate material 122 is doped with an n type dopant, the hard mask 123 may not be required, because the source and drain regions of the NMOS device are doped with n type, for example. The hard mask 123 also may not be deposited at this stage of the manufacturing process if the gate materials for the PMOS transistor and the NMOS transistor are N doped in a single step, as shown in Figure 7. The hard mask 123 may comprise about 500 Å or less of an oxide or nitride material, as examples. In one embodiment, the hard mask 123 may comprise about 400 Å of TEOS, for example.

[0050] Referring again to Figure 3, after the optional steps of implanting a p or n type dopant into the first gate material 122 and depositing the hard mask 123 over the first gate material 122, a second layer of photoresist 124 is deposited over the optional hard mask 123, as shown in Figure 3, or over the first gate material 122, if the hard mask 123 is not used. The second layer of photoresist 124 may be patterned using a mask, using traditional lithography techniques to remove the second layer of photoresist 124 from over the first region 104 of the workpiece 102, as shown, although alternatively, the second layer of photoresist 124 may be directly patterned.

[0051] The second layer of photoresist 124 is used as a mask to pattern the first gate material 122, the first gate dielectric material 120 and also the hard mask 123, if used, and to

remove the hard mask 112 from the first region 104 of the workpiece 102, as shown in Figure 4. For example, exposed portions of the first gate material 122, first gate dielectric material 120, and hard mask 112 may be etched away from the first region 104 of the workpiece 102 using the second layer of photoresist 124 as a mask. The second layer of photoresist 124 is then stripped or removed from over the second region 106 of the workpiece 102. Any excess first gate material 122, first gate dielectric material 120, and optional hard mask 123 may be removed from over the optional STI region 108 proximate the interface of the first region 104 and second region 106 using a chemical-mechanical polish (CMP) process or an etch process, for example, leaving the structure shown in Figure 4. The exposed surface of the workpiece 102 may be cleaned using a pre-gate clean process.

[0052] Next, a second gate dielectric material 126 is deposited over exposed portions of the workpiece 102 in the first region 104 and over the patterned first gate material 122 and first gate dielectric material 120 in the second region 106, as shown in Figure 5. The second gate dielectric material 126 preferably comprises a different material and/or thickness than the first gate dielectric material 120 in one embodiment of the present invention. Alternatively, the second gate dielectric material 126 may comprise the same material and/or thickness as the first gate dielectric material 120, in one embodiment. The second gate dielectric material 126 preferably comprises a high-k dielectric material having a dielectric constant of about 4.0 or greater, in one embodiment. The second gate dielectric material 126 preferably comprises HfO_2 , HfSiO_x , Al_2O_3 , ZrO_2 , ZrSiO_x , Ta_2O_5 , La_2O_3 , nitrides thereof, Si_xN_y , SiON , HfAlO_x , $\text{HfAlO}_x\text{N}_{1-x-y}$, ZrAlO_x , ZrAlO_xN_y , SiAlO_x , $\text{SiAlO}_x\text{N}_{1-x-y}$, HfSiAlO_x , $\text{HfSiAlO}_x\text{N}_y$, ZrSiAlO_x , $\text{ZrSiAlO}_x\text{N}_y$, combinations thereof, or combinations thereof with SiO_2 , as examples, although alternatively,

the second gate dielectric material 126 may comprise other high k insulating materials or other dielectric materials.

[0053] The second gate dielectric material 126 may comprise a single layer of material, or alternatively, the second gate dielectric material 126 may comprise two or more layers, wherein the top layer comprises a Fermi-pinning material, which will be described further herein with reference to Figure 10. In one embodiment, one or more of these materials can be included in the second gate dielectric material 126 in different combinations or in stacked layers. The second gate dielectric material 126 may be deposited by CVD, ALD, MOCVD, PVD, or JVD, as examples, although alternatively, the second gate dielectric material 126 may be deposited using other suitable deposition techniques. The second gate dielectric material 126 preferably comprises a thickness of about 10 Å to about 60 Å in one embodiment, although alternatively, the second gate dielectric material 126 may comprise other dimensions, such as about 80 Å or less, as an example. The second gate dielectric material 126 preferably comprises a Fermi-pinning material such as an aluminum-containing material disposed at the top surface thereof.

[0054] Next, a second gate material 128 is deposited over the second gate dielectric material 126, also shown in Figure 5. The second gate material 128 preferably comprises a semiconductive material, such as polysilicon or amorphous silicon, although alternatively, other conductive and semiconductive materials may be used for the second gate material 128. In the embodiment shown in Figures 1-9, the second gate material 128 preferably comprises polysilicon or other semiconductor materials. Alternatively, the second gate material 128 may comprise TiN, HfN, TaN, W, Al, Ru, RuTa, TaSiN, NiSi_x, CoSi_x, TiSi_x, Ir, Y, Pt, Ti, PtTi, Pd, Re, Rh, borides, phosphides, or antimonides of Ti, Hf, Zr, TiAlN, Mo, MoN, ZrSiN, ZrN, HfN, HfSiN, WN, Ni, Pr, VN, TiW, a partially silicided gate material, a fully silicided gate material

(FUSI), other metals, and/or combinations thereof, as examples. The second gate material 128 may comprise a plurality of stacked gate materials, such as a metal underlayer with a polysilicon cap layer disposed over the metal underlayer. The second gate material 128 may be deposited using CVD, PVD, ALD, or other deposition techniques, as examples. The second gate material 128 preferably comprises a thickness of about 1500 Å, although alternatively, the second gate material 128 may comprise about 1000 Å to about 2000 Å, or other dimensions, for example. The second gate material 128 may comprise the same material as the first gate material 122, or alternatively, the second gate material 128 may comprise a different material than the first gate material 122, for example.

[0055] In an optional step, the second gate material 128 may be doped at this point in the manufacturing process with an n type dopant 192, e.g., by doping the second gate material 128 with As or phosphorous, for example. Doping the second gate material 128 makes the semiconductive material conductive or more conductive. Preferably, the work function of the PMOS transistor (see 136 in Figure 9) is set by the material selection for the second gate dielectric material 126, rather than by the dopant implanted into the second gate material 128, in accordance with an embodiment of the present invention.

[0056] After implanting the dopant 192, an optional hard mask 129 may be deposited over the second gate material 128. The optional hard mask 129 protects the second gate material 128 from being implanted with the dopants that are implanted to form the source and drain extension regions and source and drain regions, to be described further herein. The hard mask 129 may not be deposited at this stage of the manufacturing process if the gate materials for the PMOS transistor and the NMOS transistor are n doped in a single step, as shown in Figure 7. The hard

mask 129 may comprise about 500 Å or less of an oxide or nitride material, as examples. In one embodiment, the hard mask 129 may comprise about 400 Å of TEOS, for example.

[0057] After the optional steps of implanting the dopant 192 and forming the hard mask 129, a third layer of photoresist 130 is deposited over the second gate material 128, as shown in Figure 5. The third layer of photoresist 130 may be patterned using a mask by traditional lithography techniques to remove the third layer of photoresist 130 from the second region 106 of the workpiece 102, as shown, although alternatively, the third layer of photoresist 130 may be directly patterned.

[0058] The third layer of photoresist 130 is then used as a mask to pattern the second gate material 128, second gate dielectric material 126, and optional hard mask 129, as shown in Figure 6. For example, exposed portions of the second gate material 128, second gate dielectric material 126, and hard mask 129 may be etched away from the second region 106 of the workpiece 102 using the third layer of photoresist 130 as a mask. The third layer of photoresist 130 is then stripped or removed from over the first region 104 of the workpiece 102.

[0059] Any excess second gate material 128, second gate dielectric material 126, and optional hard mask 129 (e.g., as shown at peak 132) may be removed from over the optional STI region 108 proximate the interface of the first region 104 and second region 106 using a chemical-mechanical polish (CMP) process or an etch process, for example (not shown), leaving the structure shown in Figure 7.

[0060] Preferably using a single lithography step, e.g., using a single layer of photoresist and using a single mask to pattern the photoresist, the first gate material 120, the first gate dielectric material 122, the second gate material 126, the second gate dielectric material 128, and optional hard masks 123 and 129, are simultaneously patterned with a desired pattern for a

CMOS device, leaving the structure shown in Figure 8, wherein a gate/gate dielectric stack 126/128/129 of a PMOS transistor 136 is formed in the first region 104, and a gate/gate dielectric stack 120/122/123 of an NMOS transistor 138 is formed in the second region 106.

[0061] Referring again to Figure 7, note that while a vertical portion 160 of the second gate dielectric material 126 formed on the sidewall of the first gate material 122 is left remaining in the structure shown in Figure 7, this is not problematic, because portion 160 is etched away or removed when the first and second gate materials 122 and 128, and first and second gate dielectric materials 120 and 126, are patterned and etched to form PMOS and NMOS transistors 136 and 138, as shown in Figure 8.

[0062] In one embodiment, rather than implanting the first gate material 122 with a dopant 190 as shown in Figure 3 and implanting the second gate material 128 with a dopant 192 as shown in Figure 5 using two separate dopant implantation steps, the first gate material 122 and the second gate material 128 may be simultaneously implanted with a dopant 194, as shown in Figure 7. Preferably, the dopant 194 in this embodiment comprises an n type dopant. In this embodiment, the hard masks 123 and 129 have not been deposited yet, for example. The first gate material 122 and second gate material 128 may simultaneously be n doped by doping the first gate material 122 and second gate material 128 with phosphorous or As. Then a hard mask material 123/129 is deposited over the first gate material 122 and the second gate material 128. Note that in this embodiment, the hard mask 123/129 may comprise a single layer of material, and the vertical portion 160 of the second gate dielectric material 126 does not reside above the top surface of the first and second gate materials 122 and 128. The hard mask 123/129 may comprise about 500 Å or less of an oxide or nitride material, as examples. In one embodiment, the hard mask 129 may comprise about 400 Å of TEOS, for example.

[0063] Again, doping the first gate material 122 and second gate material 128 makes the semiconductive material conductive or more conductive. Preferably, the work function of the NMOS transistor 138 and PMOS transistor 136, shown in Figure 8, is set by the material selection for the gate dielectric materials 120 and 126, rather than by the dopant 194 implanted into the first gate material 122 and second gate material 128, in accordance with an embodiment of the present invention. In particular, the "effective" work function of the NMOS transistor 138 and the PMOS transistor 136 are set by Fermi-pinning, by the interaction between the gate dielectric material 120 and 126 to the gate material 122 and 128, which is a departure from the bulk work function of the semiconductive material used for the gate materials 122 and 128, which effects the V_t .

[0064] Manufacturing of the CMOS device 100 is then continued to complete the fabrication of the CMOS device 100. For example, the exposed portions of the workpiece 102 may be lightly doped to form source and drain extensions 107 in the workpiece 102, as shown in Figure 8. For example, while the second region 106 is masked, p type dopants may be implanted into the first region 104, and while the first region 104 is masked, n type dopants may be implanted into the second region 106. Spacers 134 comprising an insulating material such as an oxide or nitride may be formed on the sidewalls of the gate electrode materials 128 and 122, on the sidewalls of the gate dielectric materials 126 and 120, and on the sidewalls of the hard mask materials 123 and 129, forming the structure shown in Figure 9. Source and drain regions S1 and D1, and S2 and D2 may be formed in exposed surfaces of the PMOS transistor 136 and the NMOS transistor 138, using a deeper implantation step, respectively. For example, the source and drain regions S1 and D1 may be doped with p type dopants to form p-n-p junctions in the N well of the PMOS transistor 136, while the second region 106 is masked. Likewise, the source

and drain regions S2 and D2 may be doped with n type dopants to form n-p-n junctions in the P well of the NMOS transistor 138, while the first region 104 is masked. The workpiece 102 may be annealed to drive the dopants into the workpiece 102 and form the sources S1 and S2 and drains D1 and D2, for example.

[0065] If the first gate material 122 is doped with an n dopant, the hard mask 123 may be removed before implanting the workpiece 102 with an n dopant to form the source and drain extensions 107 and source and drains S2 and D2, for example.

[0066] After the sources S1 and S2 and drains D1 and D2 are formed, the hard mask materials 123 and 129 may be removed from over the top surface of the gates G1 and G2 (not shown in Figure 9; see Figures 10, 17 and 21, as examples). One or more insulating materials (not shown) may be deposited over the PMOS transistor 136 and NMOS transistor 138, and contacts may be formed in the insulating materials in order to make electrical contact with the gates, sources and/or drains. Additional metallization and insulating layers may be formed and patterned over the top surface of the insulating material and contacts. A passivation layer (not shown) may be deposited over the insulating layers or the PMOS transistor 136 and NMOS transistor 138. Bond pads (also not shown) may be formed over contacts, and the semiconductor device 100 may then be singulated or separated into individual die. The bond pads may be connected to leads of an integrated circuit package (not shown) or other die, for example, in order to provide electrical contact to the transistors 136 and 138 of the semiconductor device 100.

[0067] Thus, a novel semiconductor CMOS device 100 comprising a PMOS transistor 136 and an NMOS transistor 138 is formed, as shown in Figure 9, wherein the gate dielectric GD1 of the PMOS transistor 136 comprises a different material and/or thickness than the material of the

gate dielectric GD2 of the NMOS transistor 138. The gate dielectric GD1 of the PMOS transistor 136 preferably comprises a Fermi-pinning material abutting the gate G1. The PMOS transistor 136 includes a source S1 and a drain D1 separated by a first channel region C1. A gate dielectric GD1 is disposed over the first channel region C1, and a gate G1 is disposed over the gate dielectric GD1. The NMOS transistor 138 includes a source S2 and a drain D2 separated by a channel region C2. A gate dielectric GD2 is disposed over the channel region C2, and a gate G2 is disposed over the gate dielectric GD2. A spacer 134 comprising an oxide or nitride, as examples, may be formed on the sidewalls of the gates G1 and G2, and gate dielectrics GD1 and GD2, as shown.

[0068] The gate G1 of the PMOS transistor 136 is doped with an n type dopant, in accordance with a preferred embodiment of the present invention. The gate G2 of the NMOS transistor 138 is preferably doped with either an n or p type dopant.

[0069] The gate and gate dielectric materials for either the PMOS transistor 136 or the NMOS transistor 138 may be deposited first, in accordance with embodiments of the present invention. For example, in the embodiment described herein with reference to Figures 1 through 9, the NMOS transistor 138 gate dielectric and gate materials are deposited first. Alternatively, the PMOS transistor 136 gate dielectric and gate materials may be deposited first.

[0070] Another preferred embodiment of the present invention is shown in Figure 10. Like numerals are used for the various elements that were described in Figures 1 through 9. To avoid repetition, each reference number shown in Figure 10 is not described again in detail herein. Rather, similar materials x02, x04, x06, x08, etc... are preferably used for the various material layers shown as were described for Figures 1 through 9, where x=1 in Figures 1 through 9 and x=2 in Figure 10. As an example, the preferred and alternative materials and dimensions

described for the first and second gate dielectric materials 120 and 126 (GD2 and GD1, respectively) in the description for Figures 1 through 9 are preferably also used for the gate dielectric materials GD1 and GD2 of Figure 10.

[0071] In this embodiment, the PMOS device 236 is shown in the right side of the figure, e.g., in first region 204, indicated by the "P" in the workpiece 202, and the NMOS device 238 is shown on the left side of the figure, e.g., in second region 206, indicated by the "N" in the workpiece 202 (whereas in Figures 1 through 9, the PMOS device 136 was shown on the left side, and the NMOS device was on the right 138). The gate dielectric GD1 in this embodiment may comprise at least two insulating layers: a first insulating layer 250 and a second insulating layer 252 disposed over the first insulating layer 250. The first insulating layer 250 preferably comprises a high-k dielectric material, and may comprise HfO_2 , HfSiO_x , ZrO_2 , ZrSiO_x , Ta_2O_5 , La_2O_3 , nitrides thereof, Si_xN_y , SiON , HfAlO_x , $\text{HfAlO}_x\text{N}_{1-x-y}$, ZrAlO_x , ZrAlO_xN_y , SiAlO_x , $\text{SiAlO}_x\text{N}_{1-x-y}$, HfSiAlO_x , $\text{HfSiAlO}_x\text{N}_y$, ZrSiAlO_x , $\text{ZrSiAlO}_x\text{N}_y$, combinations thereof, or combinations thereof with SiO_2 , as examples, although alternatively, the first insulating layer 250 may comprise other high k insulating materials or other dielectric materials. The first insulating layer 250 preferably comprises a thickness of about 80 Angstroms or less, for example. The second insulating layer 250 preferably comprises about 10 to 60 Angstroms of a Fermi-pinning material. For example, the second insulating layer 250 preferably comprises an aluminum-containing material such as aluminum oxide (Al_xO_y or Al_2O_3) or nitrides thereof, such as $\text{Al}_x\text{O}_y\text{N}_{1-x-y}$, as examples, although alternatively, the second insulating layer 250 may comprise other materials that induce Fermi-pinning of the gate dielectric GD1 to the gate electrode G1 of the PMOS device 236. The second insulating layer 250 may be deposited or may be formed by implanting a Fermi-pinning material such as aluminum, for example. The

gate dielectric GD1 may alternatively comprise a single layer, e.g., comprising a Fermi-pinning material, such as HfAlO_x , HfAlO_xN_y , or Al_2O_3 .

[0072] This embodiment also shows other optional elements that may be included in the CMOS device 200, and in the other CMOS devices 100, 300, 400, 600 and 700 described herein. Before forming spacers 234 over the sidewalls of the gate dielectric GD1 and GD2 and gates G1 and G2, an optional thin insulator 248 may be formed over the top surface of the sources S1 and S2 and drains D1 and D2, the sidewalls of the gate dielectrics GD1 and GD2, and gates G1 and G2, as shown. The spacers 234 are then formed over the thin insulator 248. The thin insulator 248 may comprise an oxide, and the spacers 234 may comprise a nitride, although alternatively, other materials may be used for the thin insulator 248 and the spacers 234, for example.

[0073] The sources S1 and S2 or the drains D1 and D2, or the gates G1 and G2, may include an optional silicide material 244 and 246, respectively, formed at a top surface thereof (often referred to as a salicide because the formation of the silicide may be self-aligning). The silicide 244 and 246 may comprise about 100 Å to 300 Å of TiSi_x , CoSi_x , or NiSi_x , although the silicide 244 and 246 may alternatively comprise other materials and thicknesses, as examples. The sources S1 and S2 and drains D1 and D2 may include lightly doped areas and deeper implantation regions, as shown. The gates G1 and G2 may also be fully silicided, e.g., by heating the workpiece 202 to cause the silicide material 244 and 246 to combine with the underlying gate material, in one embodiment.

[0074] The novel CMOS device of embodiments of the present invention described herein having a PMOS transistor and an NMOS transistor that have gate dielectrics comprising different materials and wherein the PMOS transistor gate is doped with an n dopant, may be manufactured using other methods. Two examples of such other methods are shown Figures 11 through 17,

through 17, and Figures 18 and 19, respectively. Again, like numerals are used for the various elements that were described in Figures 1 through 9 and 10, and to avoid repetition, each reference number shown in Figures 11 through 17, and Figures 18 and 19 is not described again in detail herein. Rather, similar materials x02, x04, x06, x08, etc... are preferably used for the various material layers shown as were described for Figures 1 through 9, where x=1 in Figures 1 through 9, x=2 in Figure 10, x=3 in Figures 11 through 17, and x=4 in Figures 18 and 19.

[0075] Figures 11 through 15 and 17 show cross-sectional views of a method of forming a CMOS device having different gate dielectric materials for the PMOS transistor and NMOS transistor in accordance with another preferred embodiment of the present invention at various stages of manufacturing. In this embodiment, starting with a workpiece such as 102 shown in Figure 1, the second gate dielectric material 326 is deposited over the entire top surface of the workpiece 302. The second gate material 328 is then deposited over the entire surface of the second gate dielectric material 326, as shown in Figure 11. Optionally, the second gate material 328 may be implanted with an n type dopant 392 at this point in the manufacturing process, for example. An optional hard mask 312 may be formed over the second gate material 328, as shown. The second gate material 328, second gate dielectric material 326, and optional hard mask 312 are then removed from over the second region 306 of the workpiece, as shown in Figures 12.

[0076] For example, a layer of photoresist 318 may be deposited over the optional hard mask 312, and the photoresist 318 may be removed from over the second region 306 using lithography techniques, for example, as shown in Figure 11. The photoresist 318 may be used as a mask to pattern the hard mask 312 and second gate material 328 to remove layers 312, 328 and

326 from over the second region 306 of the workpiece 302, and the photoresist 318 may be stripped or ashed, as shown in Figure 12.

[0077] Next, the first gate dielectric material 320 and the first gate material 322 are deposited over the second region 306 of the workpiece 302 and over the second gate material 328 over the first region 304 of the workpiece 302, as shown in Figure 13. The first gate material 322 may optionally be doped with a dopant 390 comprising a p type or n type dopant. An optional hard mask 323 may be formed over the first gate material 322 after the optional doping step, as shown. The first gate dielectric material 320 and the first gate material 322 are then removed from over the first region 304 of the workpiece. For example, a layer of photoresist 324 may be deposited over the workpiece 302, and the photoresist 324 may be patterned to remove the photoresist 324 from over the first region 304 of the workpiece 302, as shown in Figure 13. The photoresist 324 is then used as a mask while the first gate material 322, first gate dielectric material 320, and optional hard mask 323 are removed from the first region 304 of the workpiece.

[0078] The photoresist 324 is then removed, as shown in Figure 14, and the top surface of the first gate material 322 and the second gate material 328 (or optional hard masks 312 and 323, as shown) are then planarized, e.g., using CMP or an etch process, for example, leaving the structure shown in Figure 15. While a vertical portion 362 of the first gate dielectric material 320 formed on the sidewall of the second gate material 322 is left remaining in the structure shown in Figure 16, this is not problematic, because portion 362 will be etched away when the PMOS and NMOS transistors are formed, as shown in Figures 8 through 10. The first gate material 322, the first gate dielectric material 320, the second gate material 328, the second gate dielectric material 326, and optional hard masks 323 and 329, are patterned with a pattern for a

CMOS device, source and drain regions are formed in the workpiece 302, and the hard masks 323 and 329 are removed, leaving the structure shown in Figure 17, wherein a PMOS transistor is formed in the first region 304 of the workpiece 302, and an NMOS transistor is formed in the second region 306 of the workpiece 302. The embodiment shown in Figures 11 through 15 and 17 is advantageous in that one less lithography mask is required, compared to the embodiment shown in Figures 1 through 9.

[0079] Figures 17 and 18 show cross-sectional views of a method of forming a CMOS device 300, wherein rather than separately doping the second gate material 326 with a dopant 392 as shown in Figure 11, and doping the first gate material 322 with a dopant 390 as shown in Figure 13, a single doping step is used to dope the first gate material 322 and the second gate material 328 with a dopant 394, as shown in Figure 16. The dopant 394 is preferably n type in this embodiment. The first gate material 322, the first gate dielectric material 320, the second gate material 328, the second gate dielectric material 326, and optional hard masks 323 and 329, are patterned with a pattern for a CMOS device, source and drain regions are formed in the workpiece 302, and the hard masks 323 and 329 are removed, leaving the structure shown in Figure 17, wherein a PMOS transistor is formed in the first region 304 of the workpiece 302, and an NMOS transistor is formed in the second region 306 of the workpiece 302. The embodiment shown in Figures 16 and 17 is advantageous in that one less doping step and one less hard mask (either 323 or 329) deposition step is required.

[0080] Figures 18 and 19 show yet another preferred embodiment of the present invention. In this embodiment, advantageously, a single layer of gate dielectric material 466 and a single layer of gate material 468 are deposited over the top surface of the workpiece 402. The single layer of gate dielectric material 466 and the single layer of gate material 468 may comprise one

type of material, or may alternatively comprise one or more material layers, for example. The single layer of gate dielectric material 466 is also referred to herein as an insulating layer 466, and the single layer of gate material 468 is also referred to herein as a conductive layer 468, for example.

[0081] The gate dielectric material 466 preferably comprises HfO_2 , HfSiO_x , Al_2O_3 , ZrO_2 , ZrSiO_x , Ta_2O_5 , La_2O_3 , nitrides thereof, Si_xN_y , SiON , combinations thereof, or combinations thereof with SiO_2 , for example, although alternatively, the gate dielectric material 466 may comprise other materials. The gate dielectric material 466 may comprise a thickness of a few hundred Angstroms or less, for example. The gate material 468 may comprise a semiconductor material or a combination of a semiconductor material and a metal, for example. For example, the gate material 468 may comprise polysilicon, other semiconductor materials, TiN , HfN , TaN , W , Al , Ru , RuTa , TaSiN , NiSi_x , CoSi_x , TiSi_x , Ir , Y , Pt , Ti , PtTi , Pd , Re , Rh , borides, phosphides, or antimonides of Ti , Hf , Zr , TiAlN , Mo , MoN , ZrSiN , ZrN , HfN , HfSiN , WN , Ni , Pr , VN , TiW , a partially silicided gate material, a fully silicided gate material (FUSI), other metals, and/or combinations thereof, as examples.

[0082] In this embodiment, in the first region 404 where a PMOS transistor will be formed, a Fermi-pinning material 464 is implanted. Preferably, the Fermi-pinning material 464 is implanted in the first region 404 but not in the second region 406, as shown. For example, the gate material 468 may be covered with photoresist 424 or an insulating material during the implantation process, as shown. Implanting the Fermi-pinning material 464 may comprise implanting aluminum, for example, although alternatively, the Fermi-pinning 464 may comprise other Fermi-pinning materials.

[0083] Preferably, the Fermi-pinning material 464 is implanted into at least the conductive layer 468 over the first region 404 of the workpiece 402, as shown. For example, the Fermi-pinning material 464 is preferably also implanted into a top surface 470 of the insulating layer 466.

[0084] Because the Fermi-pinning material 464 is implanted into the first region 404 and not the second region 406, the gate material and gate dielectric material for the first region 404 and second region 406 are now advantageously different, producing the novel CMOS device having different gate dielectric materials and symmetric V_t for a PMOS transistor and NMOS transistor, as shown in Figures 9 and 10.

[0085] Note that preferably, in accordance with an embodiment of the present invention, the gate material 468 in the first region 404 may be doped with an n type dopant. For example, the gate material 468 in the first region 404 may be doped with the n type dopant while the second region 406 is masked. Alternatively, the gate material 468 in the first region 404 and the second region 406 may be simultaneously doped with the n type dopant, for example. In one embodiment, the gate material 468 in the second region 406 may be doped with a p type dopant while the first region 404 is masked. The gate materials 468 of the first region 404 and the second region 406 may be doped with different amounts of an n type dopant, for example.

[0086] The structure shown in Figure 19 illustrates that the single conductive layer 468, after implanting the Fermi-pinning material 464, forms a first gate material 422 in the second region 406 and a second gate material 428 in the first region 404. Likewise, the single insulating layer 466 forms a first gate dielectric material 420 in the second region 406 and a second gate dielectric material comprising a first insulating layer 450 and a second insulating layer 452 in the first region 404. The device 400 is then patterned and the manufacturing process is continued to

produce a novel CMOS device such as the one shown in a cross-sectional view in Figure 9. The embodiment shown in Figures 18 and 19 is advantageous in that the number of lithography masks required to manufacture the device 400 is further reduced.

[0087] Figure 20 shows a cross-sectional view of a prior art CMOS device 500, wherein the gate 582 of the PMOS device is doped with a p type dopant, and the gate 584 of the NMOS device is doped with an n type dopant. This CMOS device 500 may exhibit the polysilicon depletion effect when operated in the inversion regime.

[0088] Figure 21 shows a cross-sectional view of another embodiment of the present invention. In this embodiment, preferably, the gate 628 of the PMOS device is doped with an n type dopant, and the gate 622 of the NMOS device is doped with either a p type dopant or an n type dopant. In this embodiment, the gate dielectric materials 694 and 696 may be the same material, or may comprise different materials. If the NMOS device comprises a single device, preferably the gate is doped with a p type dopant, in one embodiment.

[0089] Embodiments of the present invention also include single PMOS and/or NMOS transistor devices. Referring only to the left side of Figure 21 (e.g., disregarding the NMOS device in region 606), a single PMOS device such as the one shown in Figure 20 preferably comprises a gate 628 that is doped with an n type dopant. The gate dielectric 696 preferably comprises a high k dielectric material, e.g., having a dielectric constant of about 4.0 or greater. Likewise, referring only to the right side of Figure 21 (e.g., disregarding the PMOS device in region 604), a single NMOS device in accordance with an embodiment of the present invention preferably comprises a gate 622 that is doped with a p type dopant. The gate dielectric 694 of the NMOS device preferably comprises a high k dielectric material, e.g., having a dielectric constant of about 4.0 or greater.

[0090] The CMOS devices 100, 200, 300, 400, 600, and 700 and PMOS and NMOS transistors may include source and drain regions that are formed by implantation, as described herein. Alternatively, the source and drain regions described herein may be formed using other methods. For example, as shown in Figure 22, after patterning the gate materials 722 and 728 and gate dielectric materials 795 and 796, the workpiece 702 may be etched to remove a top portion of the workpiece 702, as shown. For example, an anisotropic etch selective to silicon may be used to remove a few hundred Å, e.g., 200 to 1000 Å of the workpiece. In one embodiment, a top portion of the STI region 708 material may be partially etched or removed during the etchback of the workpiece 702, for example, not shown. The workpiece 702 is then backfilled in the etched areas with a semiconductive material, such as SiGe, SiGeC or other materials. The backfilled semiconductive material may be in-situ doped, using a precursor of the desired dopant for the source and drain regions 798, for example. The first region 704 may be masked while the second region 706 is backfilled, and vice versa. The PMOS transistor source and drain regions 798 may be formed using in-situ B doped SiGe, and the NMOS transistor source and drain regions 798 may be formed using in-situ phosphorous doped SiGe, as examples. After the backfilling step, the hard masks (not shown in Figures 22 and 23) may be removed, and the spacers 734 are formed, as shown in Figure 23.

[0091] Advantages of embodiments of the invention include providing methods of fabricating CMOS devices 100, 200, 300, 400, 600, and 700 and structures thereof wherein the PMOS transistor 136 and 236 and the NMOS transistor 138 and 238 have a substantially symmetric V_t . For example, V_{tn} may be about +0.2 to +5 V, and V_{tp} may be the substantially the same negative value, e.g., about -0.2 to -5 V. The threshold voltages V_t may alternatively comprise other voltage levels, for example. Work function symmetry may be achieved by using

a different dielectric material GD1 and GD2 for the PMOS transistor 136 and 236 and the NMOS transistor 138 and 238, respectively. The threshold voltage V_t is decreased compared to prior art CMOS devices, and the flat band voltage is easier to tune. Embodiments of the invention may utilize high-k dielectric materials as the gate dielectric GD1 and GD2, using semiconductive material or silicided semiconductive material electrodes G1 and G2. In one embodiment, wherein the top layer of the gate dielectric of the PMOS transistor 136 and 236 comprises an aluminum-containing material, the fact that Si-Al pins to p-type and Si-Hf pins to n-type is utilized, to take advantage of the Fermi-pinning effect rather than trying to solve the Fermi-pinning effect or work around it by changing the material of the gate electrode. Polysilicon depletion and boron penetration effects are prevented when the devices 100, 200, 300, 400, 600, and 700 are operated in an inversion mode, because the semiconductive material of the gates function in an accumulation regime, due to the presence of the dopant. The capacitance effective thickness (CET) of a CMOS device can be decreased in accordance with embodiments of the present invention, e.g., by about 4 Angstroms or greater.

[0092] Although embodiments of the present invention and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, it will be readily understood by those skilled in the art that many of the features, functions, processes, and materials described herein may be varied while remaining within the scope of the present invention. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present

invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

- 1 1. A transistor, comprising:
 - 2 a workpiece, the workpiece having a region implanted with a first dopant;
 - 3 a gate dielectric disposed over the workpiece;
 - 4 a gate disposed over the gate dielectric, the gate comprising a semiconductive material
 - 5 and being implanted with the first dopant; and
 - 6 a source region and a drain region formed in the region of the workpiece, wherein the
 - 7 source region and the drain region are proximate the gate dielectric.
- 1 2. The transistor according to Claim 1, wherein the transistor comprises a negative channel
 - 2 metal oxide semiconductor, wherein the first dopant comprises a p type dopant.
- 1 3. The transistor according to Claim 1, wherein the transistor comprises a positive-channel metal
 - 2 oxide semiconductor, wherein the first dopant comprises an n type dopant.
- 1 4. The transistor according to Claim 1, wherein the gate dielectric comprises a dielectric
 - 2 constant of about 4.0 or greater, and wherein the gate dielectric comprises HfO_2 , HfSiO_x , Al_2O_3 ,
 - 3 ZrO_2 , ZrSiO_x , Ta_2O_5 , La_2O_3 , nitrides thereof, Si_xN_y , SiON , HfAlO_x , $\text{HfAlO}_x\text{N}_{1-x-y}$, ZrAlO_x ,
 - 4 ZrAlO_xN_y , SiAlO_x , $\text{SiAlO}_x\text{N}_{1-x-y}$, HfSiAlO_x , $\text{HfSiAlO}_x\text{N}_y$, ZrSiAlO_x , $\text{ZrSiAlO}_x\text{N}_y$, combinations
 - 5 thereof, or combinations thereof with SiO_2 , and wherein the gate comprises polysilicon,
 - 6 amorphous silicon, TiN , HfN , Ta_xN , W , Al , Ru , RuTa , TaSiN , NiSi_x , CoSi_x , TiSi_x , Ir , Y , Pt , Ti ,
 - 7 PtTi , Pd , Re , Rh , borides, phosphides, or antimonides of Ti , Hf , Zr , TiAlN , Mo , MoN , ZrSiN ,
 - 8 ZrN , HfN , HfSiN , WN , Ni , Pr , VN , TiW , a partially silicided gate material, a fully silicided gate
 - 9 material (FUSI), or combinations thereof.

- 1 5. A complimentary metal oxide semiconductor (CMOS) device, comprising:
2 a workpiece;
3 a positive channel metal oxide semiconductor (PMOS) transistor formed in a first region
4 of the workpiece, the PMOS transistor comprising a first gate dielectric disposed over the
5 workpiece and a first gate disposed over the first gate dielectric, the first gate comprising a first
6 semiconductive material comprising an n type dopant; and
7 a negative channel metal oxide semiconductor (NMOS) transistor formed in a second
8 region of the workpiece, the NMOS transistor comprising a second gate dielectric disposed over
9 the workpiece and a second gate disposed over the first gate dielectric, the second gate
10 comprising a second semiconductive material.
- 1 6. The CMOS device according to Claim 5, wherein the second semiconductive material is
2 doped with a p type dopant or an n type dopant.
- 1 7. The CMOS device according to Claim 5, wherein the first gate dielectric comprises a first
2 material, wherein the second gate dielectric comprises a second material, wherein the second
3 material is different from or the same material or thickness as the first material, and wherein the
4 first gate dielectric and the second gate dielectric comprise a dielectric constant of about 4.0 or
5 greater.
- 1 8. The CMOS device according to Claim 7, wherein either the first material or the second
2 material comprises a Fermi-pinning material.
- 1 9. The CMOS device according to Claim 8 wherein the Fermi-pinning material comprises an
2 aluminum-containing material abutting the first gate or the second gate.

1 10. The CMOS device according to Claim 9, wherein the Fermi-pinning material comprises
2 about 10 to 60 Angstroms of Al_xO_y or $\text{Al}_x\text{O}_y\text{N}_{1-x-y}$.

1 11. The CMOS device according to Claim 5, wherein the first gate dielectric and the second gate
2 dielectric comprise HfO_2 , HfSiO_x , Al_2O_3 , ZrO_2 , ZrSiO_x , Ta_2O_5 , La_2O_3 , nitrides thereof, Si_xN_y ,
3 SiON , HfAlO_x , $\text{HfAlO}_x\text{N}_{1-x-y}$, ZrAlO_x , ZrAlO_xN_y , SiAlO_x , $\text{SiAlO}_x\text{N}_{1-x-y}$, HfSiAlO_x , $\text{HfSiAlO}_x\text{N}_y$,
4 ZrSiAlO_x , $\text{ZrSiAlO}_x\text{N}_y$, combinations thereof, or combinations thereof with SiO_2 .

1 12. The CMOS device according to Claim 12, wherein the first gate and the second gate
2 comprise polysilicon, TiN , HfN , TaN , W , Al , Ru , RuTa , TaSiN , NiSi_x , CoSi_x , TiSi_x , Ir , Y , Pt , Ti ,
3 PtTi , Pd , Re , Rh , borides, phosphides, or antimonides of Ti , Hf , Zr , TiAlN , Mo , MoN , ZrSiN ,
4 ZrN , HfN , HfSiN , WN , Ni , Pr , VN , TiW , a partially silicided gate material, a fully silicided gate
5 material (FUSI), or combinations thereof.

1 13. A method of manufacturing a transistor, the method comprising:
2 providing a workpiece;
3 implanting a first dopant into the workpiece;
4 forming a gate dielectric over the workpiece;
5 forming a gate over the gate dielectric, the gate comprising a semiconductive material;
6 and
7 implanting the first dopant into the gate.

1 14. The method according to Claim 13, wherein the transistor comprises a negative channel
2 metal oxide semiconductor, wherein the first dopant comprises a p type dopant, or wherein the
3 transistor comprises a positive channel metal oxide semiconductor, wherein the first dopant
4 comprises an n type dopant.

1 15. The method according to Claim 13, the gate dielectric comprising a dielectric constant of
2 about 4.0 or greater, and wherein the gate dielectric comprises HfO_2 , HfSiO_x , Al_2O_3 , ZrO_2 ,
3 ZrSiO_x , Ta_2O_5 , La_2O_3 , nitrides thereof, Si_xN_y , SiON , HfAlO_x , $\text{HfAlO}_x\text{N}_{1-x-y}$, ZrAlO_x , ZrAlO_xN_y ,
4 SiAlO_x , $\text{SiAlO}_x\text{N}_{1-x-y}$, HfSiAlO_x , $\text{HfSiAlO}_x\text{N}_y$, ZrSiAlO_x , $\text{ZrSiAlO}_x\text{N}_y$, combinations thereof, or
5 combinations thereof with SiO_2 , and wherein the gate comprises polysilicon, amorphous silicon,
6 TiN , HfN , TaN , W , Al , Ru , RuTa , TaSiN , NiSi_x , CoSi_x , TiSi_x , Ir , Y , Pt , Ti , PtTi , Pd , Re , Rh ,
7 borides, phosphides, or antimonides of Ti , Hf , Zr , TiAlN , Mo , MoN , ZrSiN , ZrN , HfN , HfSiN ,
8 WN , Ni , Pr , VN , TiW , a partially silicided gate material, a fully silicided gate material (FUSD),
9 or combinations thereof.

1 16. A method of manufacturing a complimentary metal oxide semiconductor (CMOS) device,
2 the method comprising:
3 providing a workpiece;
4 forming a positive channel metal oxide semiconductor (PMOS) transistor in a first region
5 of the workpiece, the PMOS transistor comprising a first gate dielectric disposed over the
6 workpiece and a first gate disposed over the first gate dielectric, the first gate comprising a first
7 semiconductive material;
8 implanting an n type dopant into the first semiconductive material of the first gate; and
9 forming a negative channel metal oxide semiconductor (NMOS) transistor in a second
10 region of the workpiece, the NMOS transistor comprising a second gate dielectric disposed over
11 the workpiece and a second gate disposed over the second gate dielectric, the second gate
12 comprising a second semiconductive material.

1 17. The method according to Claim 16, further comprising doping the second semiconductive
2 material with a p type dopant or an n type dopant.

1 18. The method according to Claim 16, wherein the work function of the PMOS transistor is set
2 by the first gate dielectric, and wherein the work function of the NMOS transistor is set by the
3 second gate dielectric.

1 19. The method according to Claim 16, wherein the first gate dielectric and the second gate
2 dielectric comprise the same material or different materials or thicknesses, and wherein the first
3 gate dielectric and the second gate dielectric comprise a dielectric constant of about 4.0 or
4 greater.

1 20. The method according to Claim 19, wherein the first gate dielectric and the second gate
2 dielectric comprise HfO_2 , HfSiO_x , Al_2O_3 , ZrO_2 , ZrSiO_x , Ta_2O_5 , La_2O_3 , nitrides thereof, Si_xN_y ,
3 SiON , HfAlO_x , $\text{HfAlO}_x\text{N}_{1-x-y}$, ZrAlO_x , ZrAlO_xN_y , SiAlO_x , $\text{SiAlO}_x\text{N}_{1-x-y}$, HfSiAlO_x , $\text{HfSiAlO}_x\text{N}_y$,
4 ZrSiAlO_x , $\text{ZrSiAlO}_x\text{N}_y$, combinations thereof, or combinations thereof with SiO_2 , and wherein
5 the first gate and the second gate comprise polysilicon, amorphous silicon, TiN , HfN , TaN , W ,
6 Al , Ru , RuTa , TaSiN , NiSi_x , CoSi_x , TiSi_x , Ir , Y , Pt , Ti , PtTi , Pd , Re , Rh , borides, phosphides, or
7 antimonides of Ti , Hf , Zr , TiAlN , Mo , MoN , ZrSiN , ZrN , HfN , HfSiN , WN , Ni , Pr , VN , TiW , a
8 partially silicided gate material, a fully silicided gate material (FUSI), or combinations thereof.

1 21. The method according to Claim 16, wherein forming the PMOS transistor comprises
2 forming a first gate dielectric comprising a Fermi-pinning material abutting the first gate.

1 22. The method according to Claim 21, wherein the Fermi-pinning material comprises about 10
2 to 60 Angstroms of Al_xO_y or $\text{Al}_x\text{O}_y\text{N}_{1-x-y}$.

1 23. The method according to Claim 16, further comprising forming source and drain regions for
2 the PMOS transistor and the NMOS transistor in the workpiece, by implantation or by etching
3 the workpiece and backfilling the workpiece with an in-situ doped semiconductive material.

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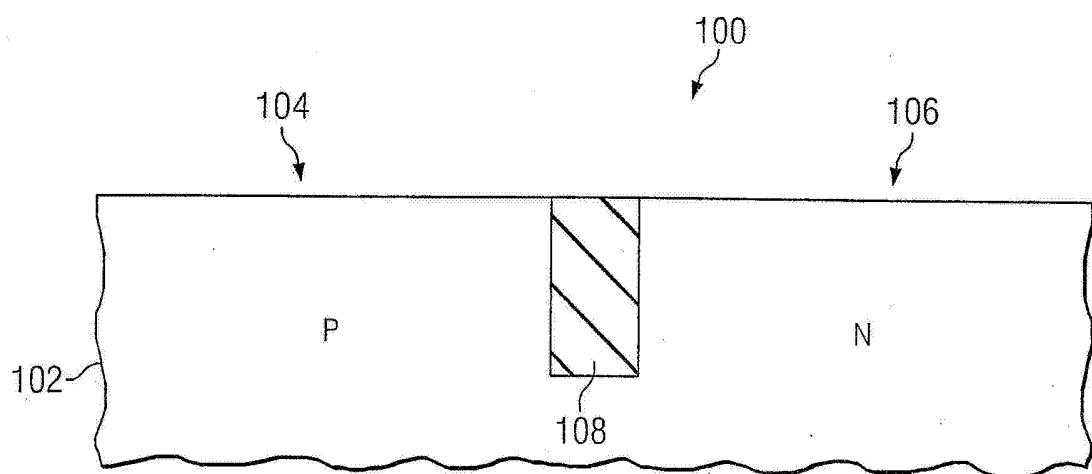


FIG. 1

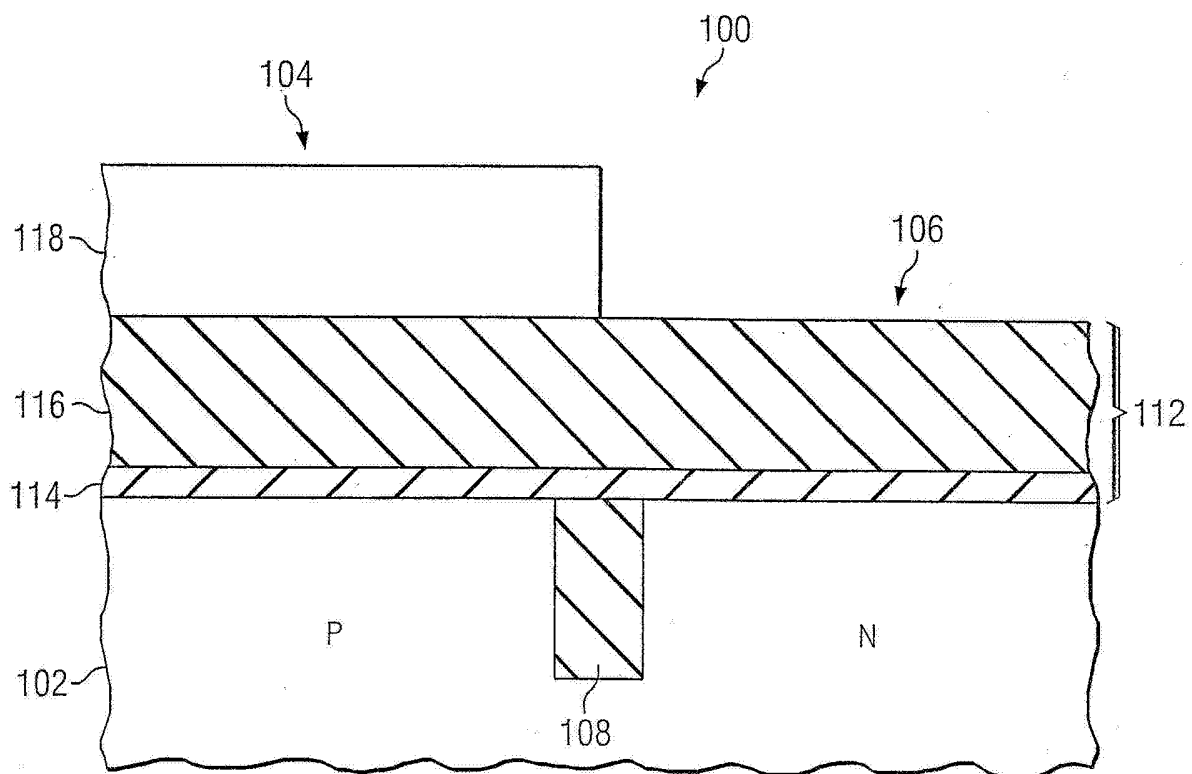


FIG. 2

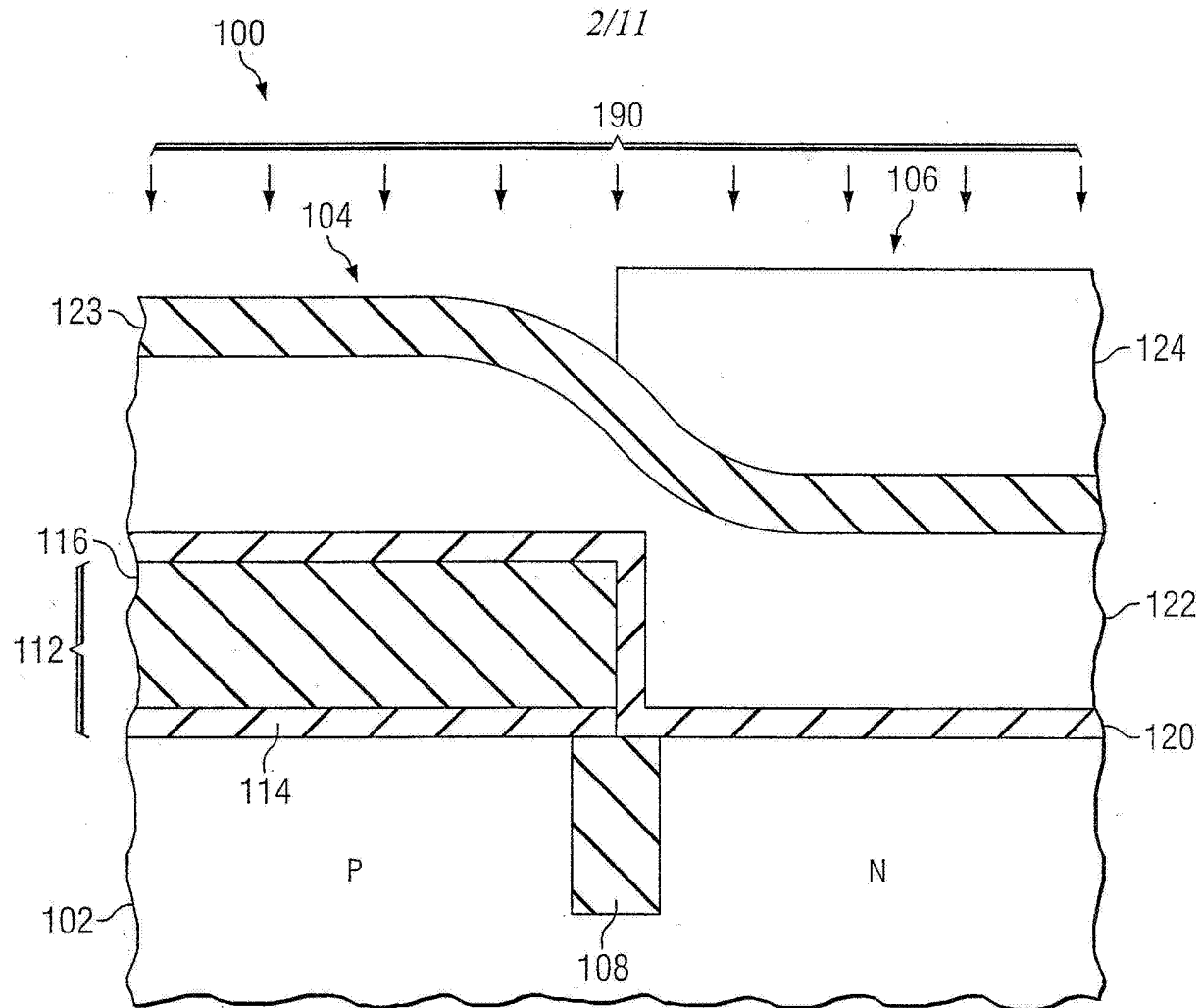


FIG. 3

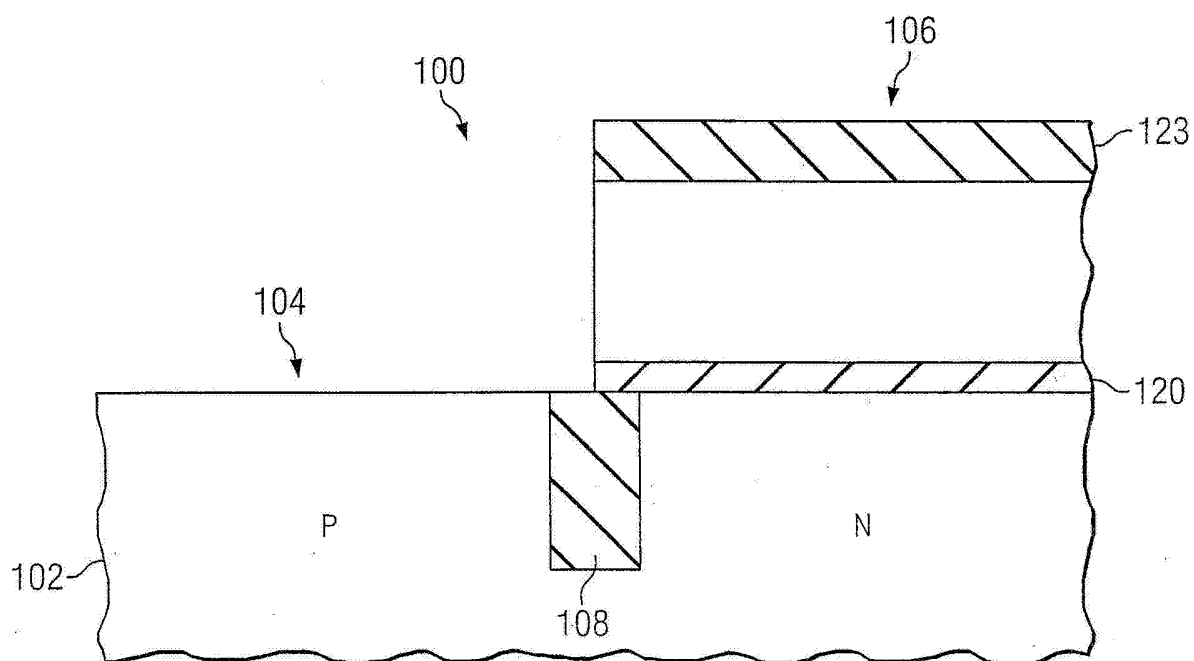


FIG. 4

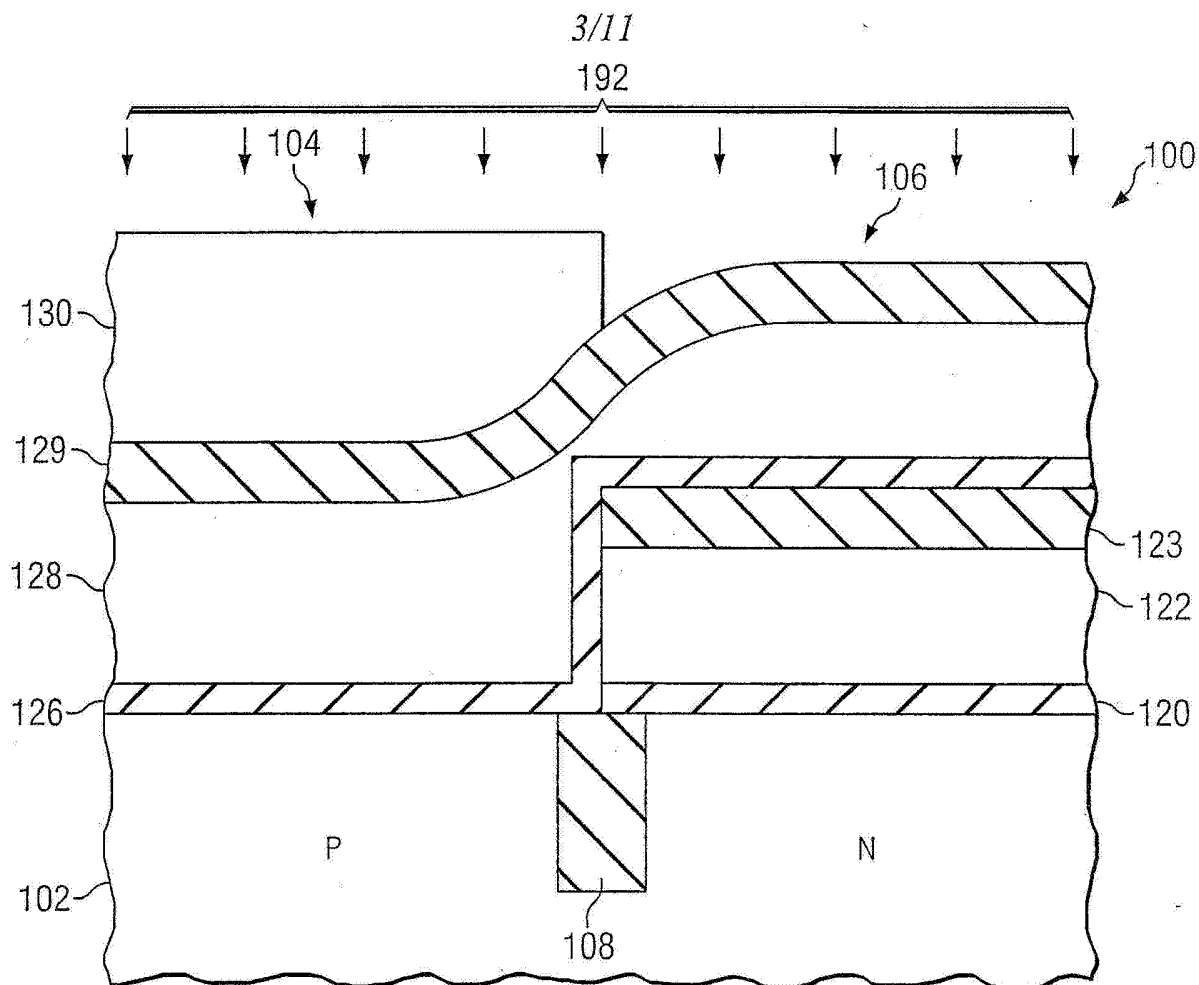


FIG. 5

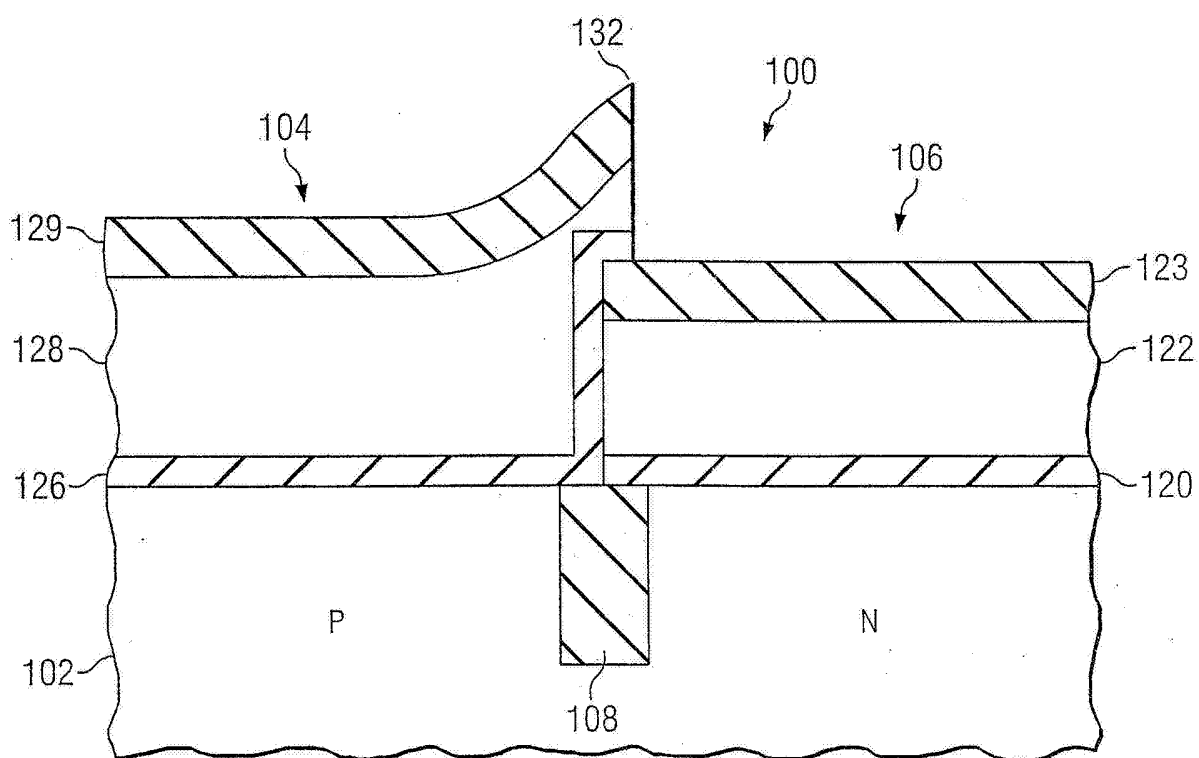


FIG. 6

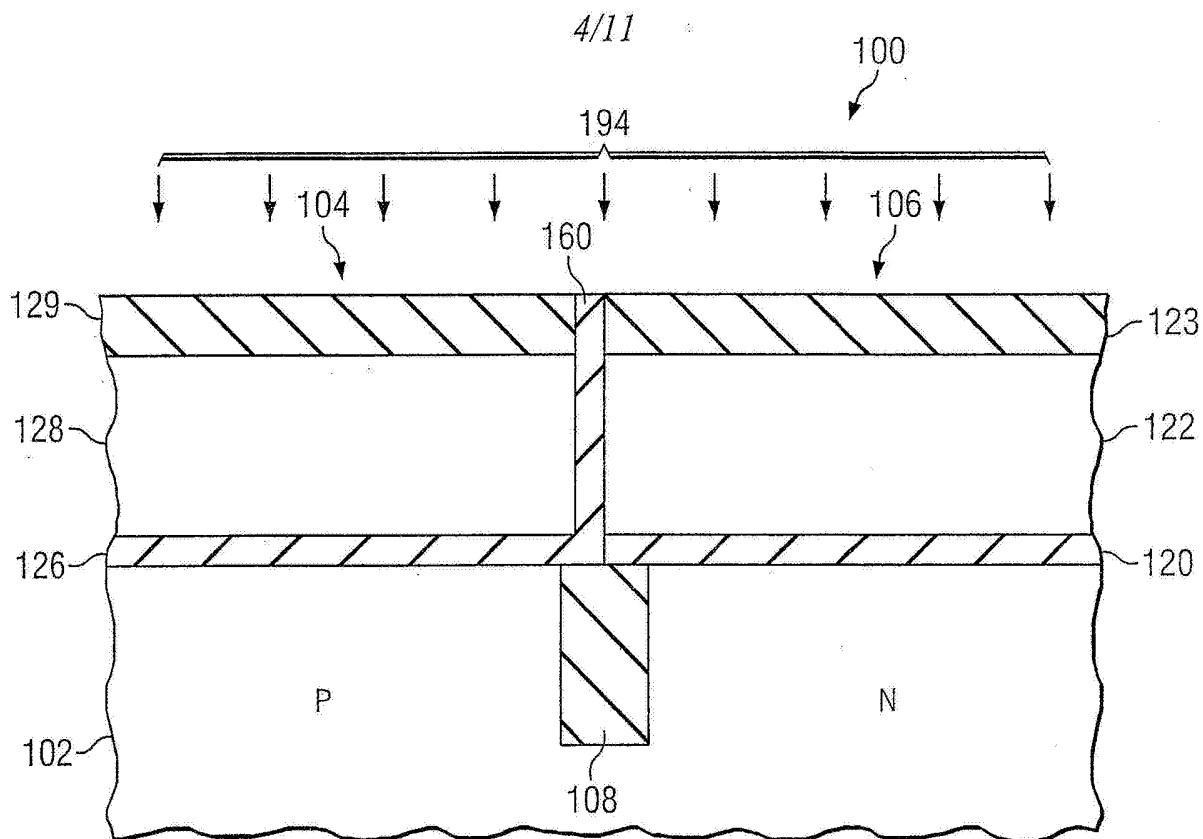


FIG. 7

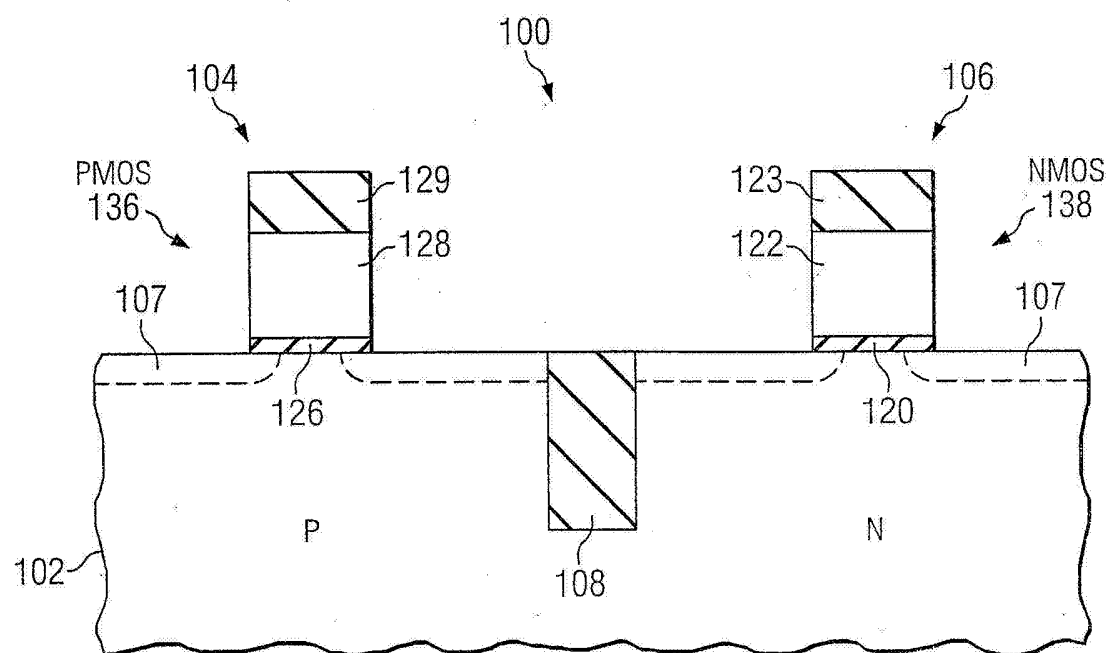


FIG. 8

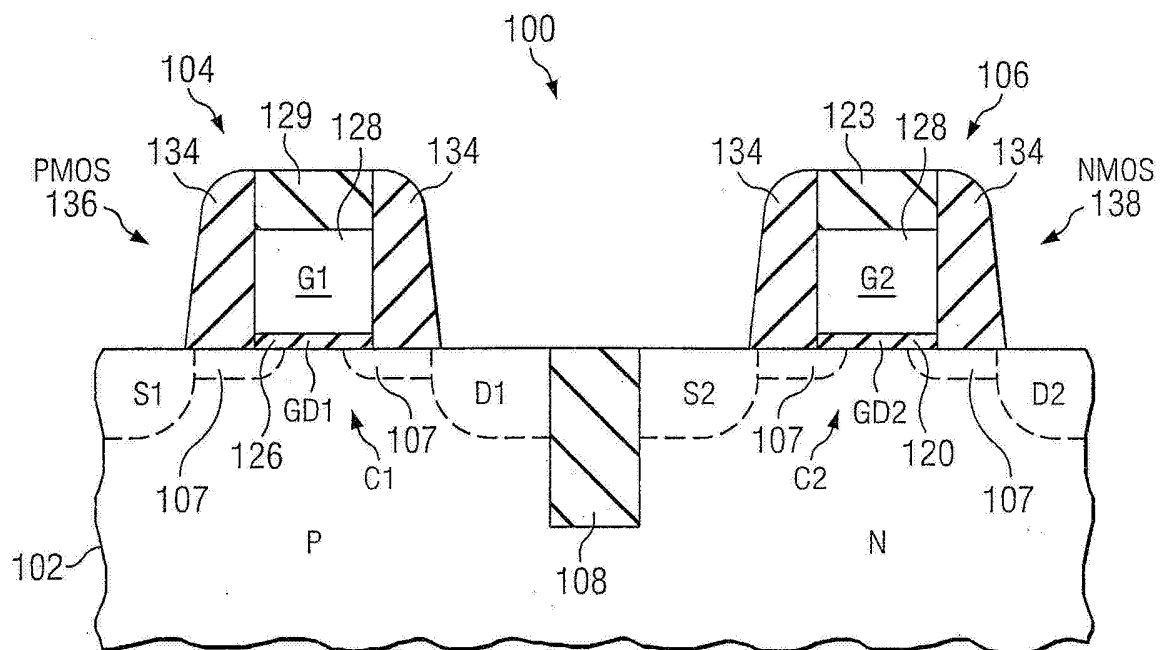


FIG. 9

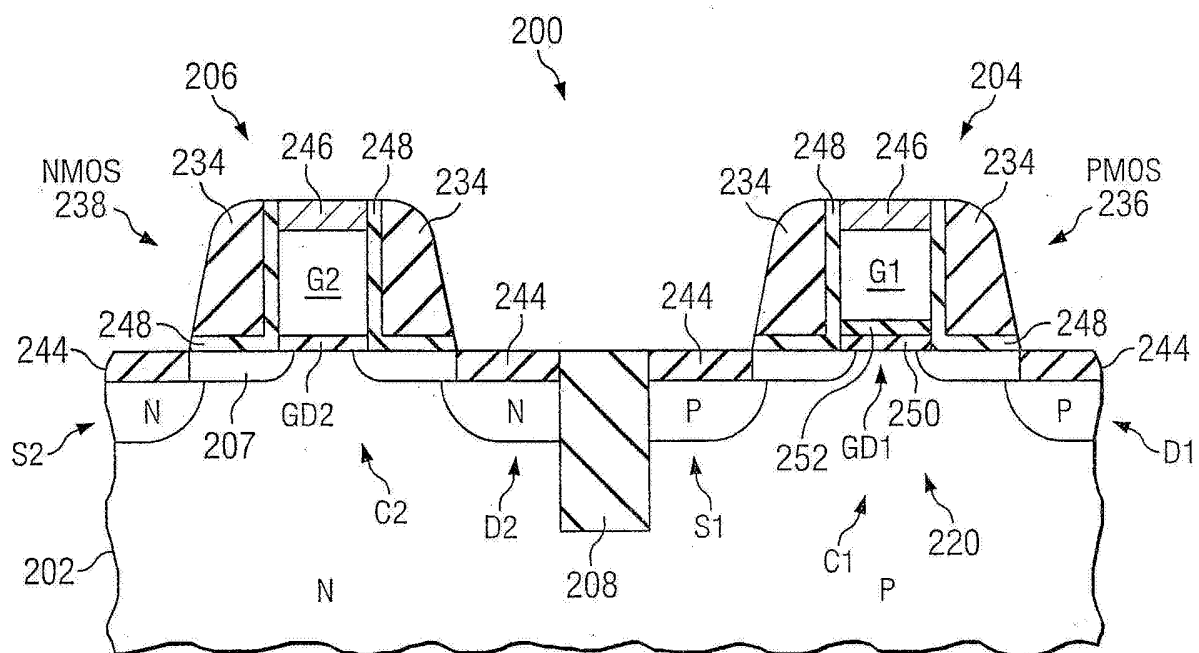


FIG. 10

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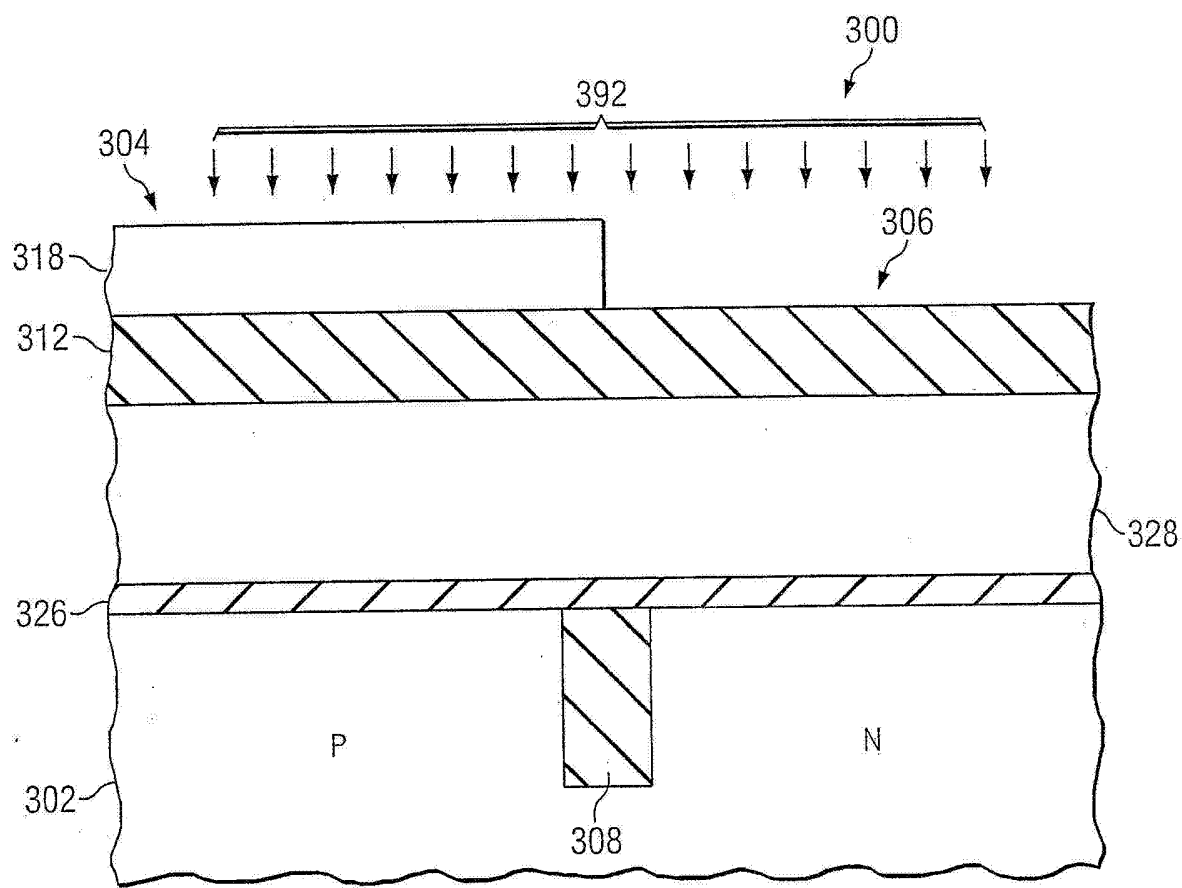


FIG. 11

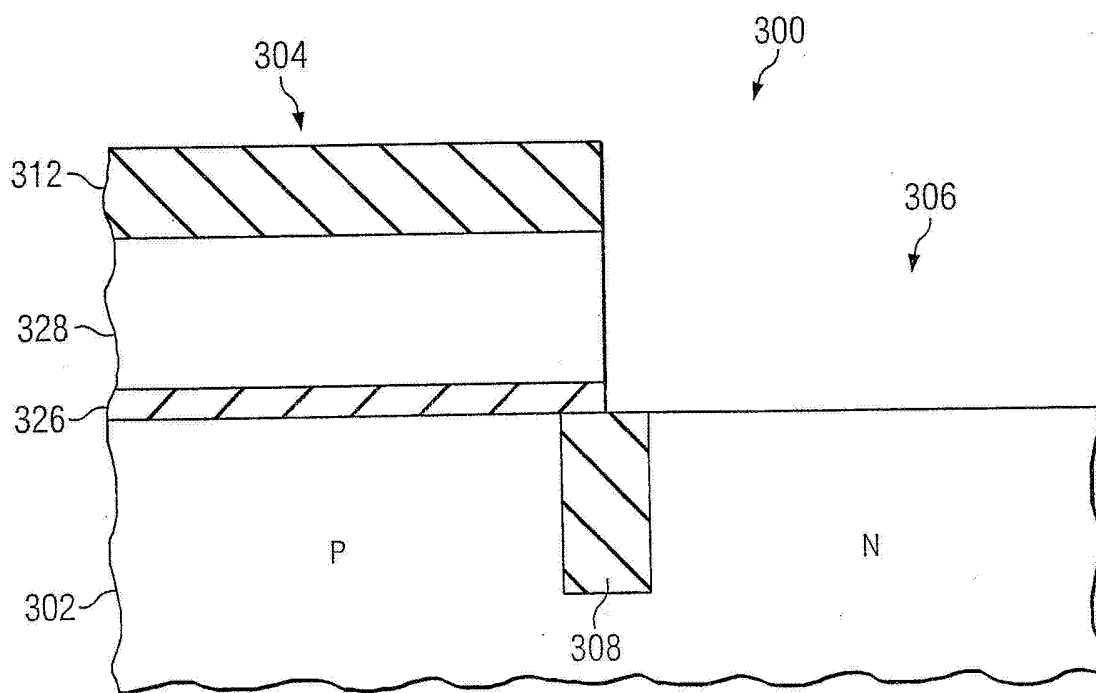


FIG. 12

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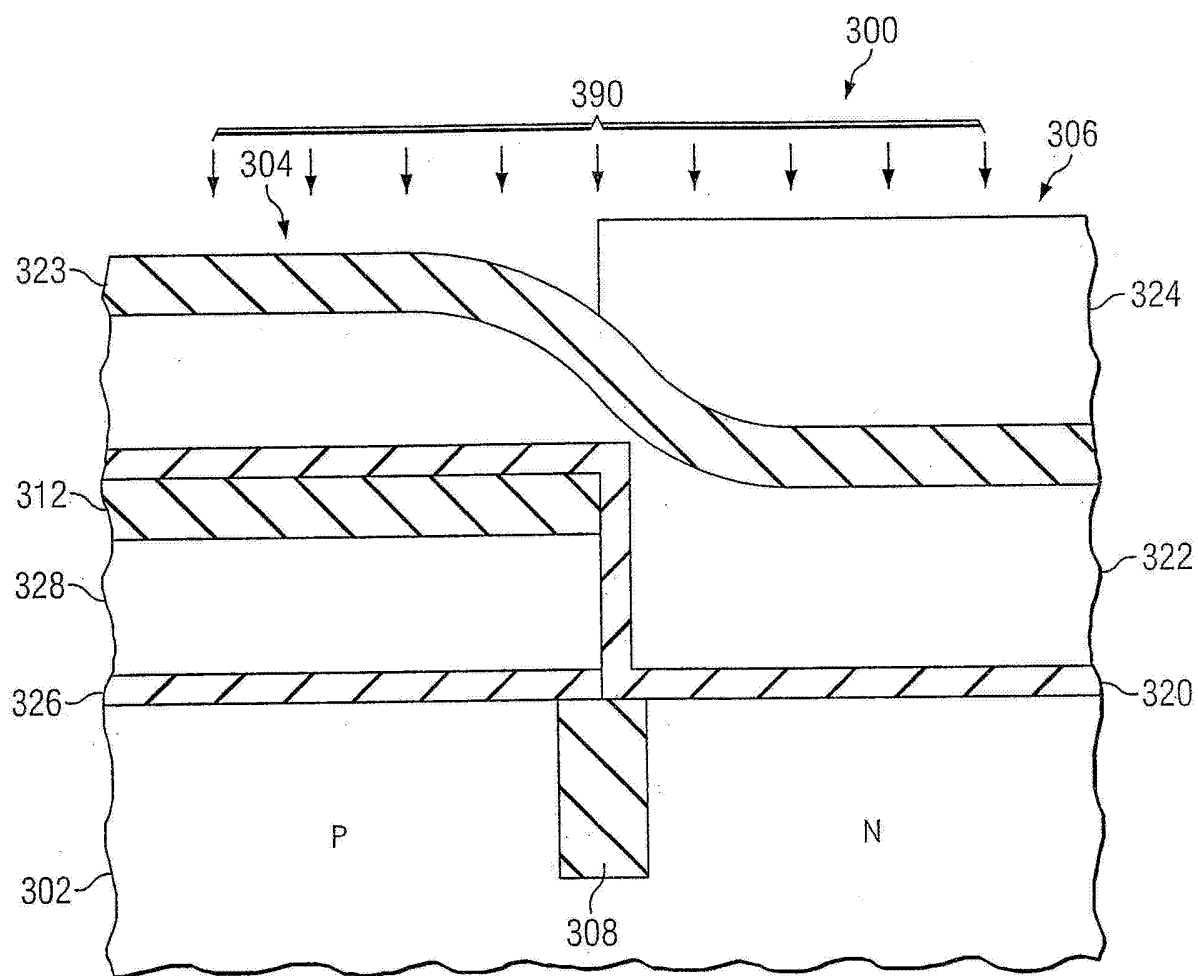


FIG. 13

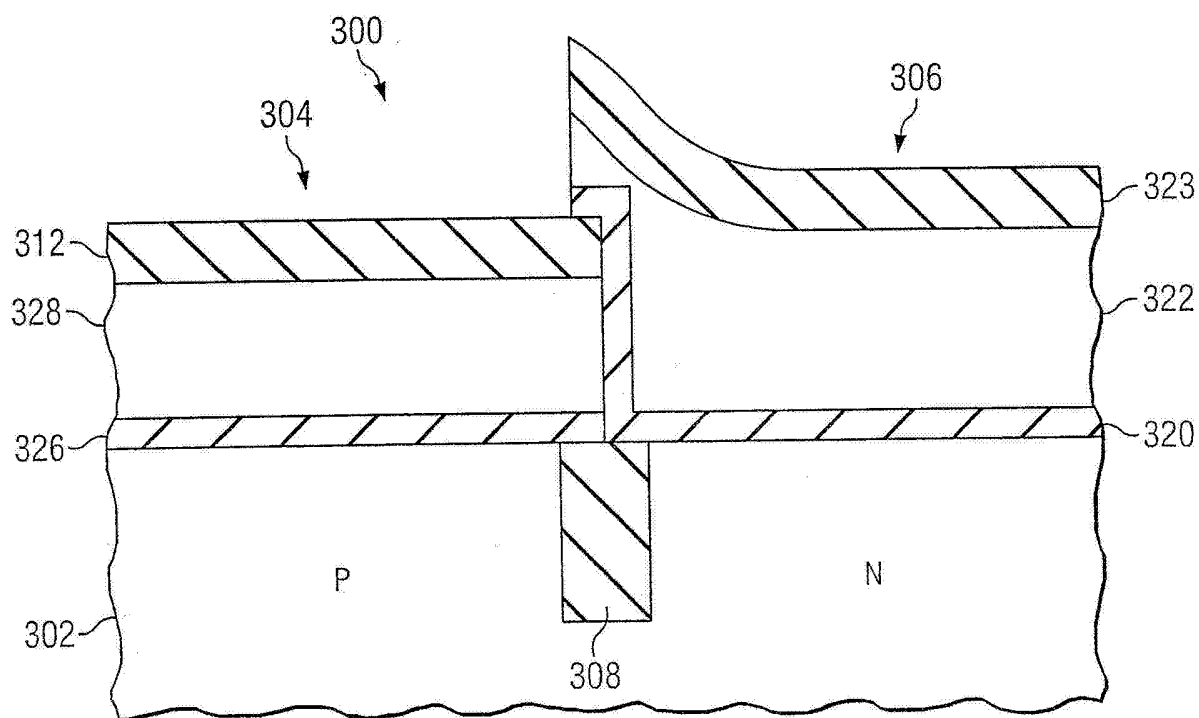


FIG. 14

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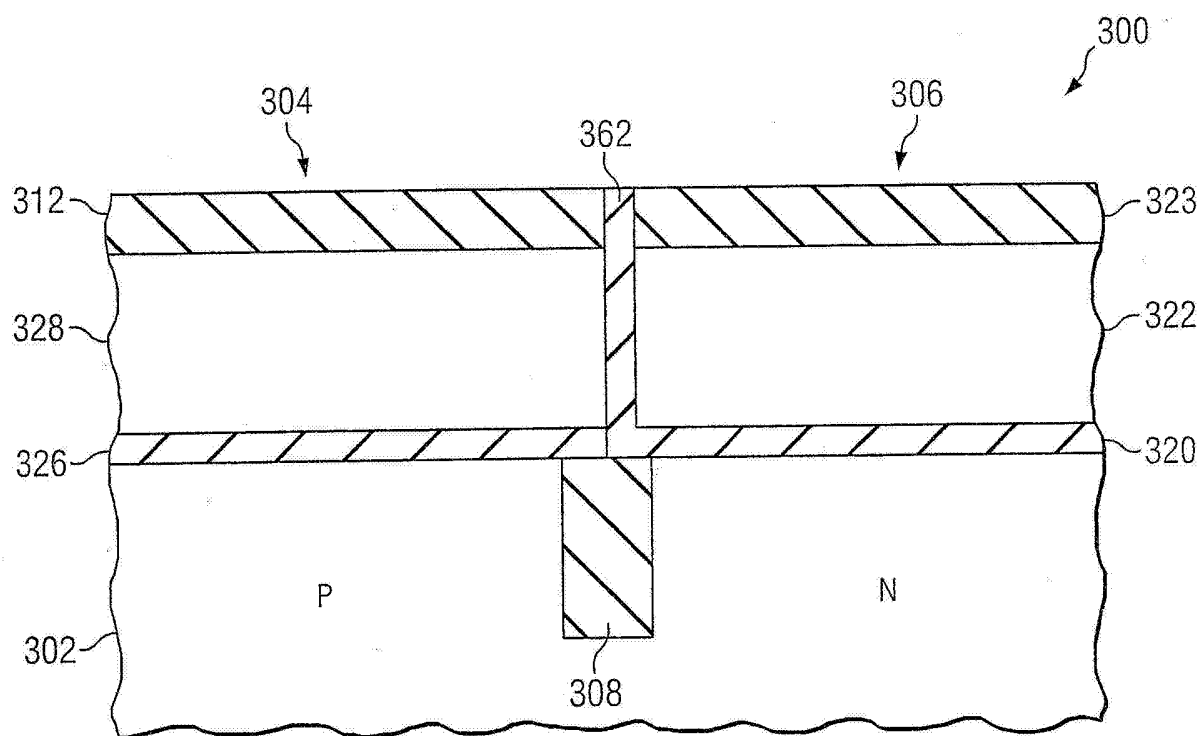


FIG. 15

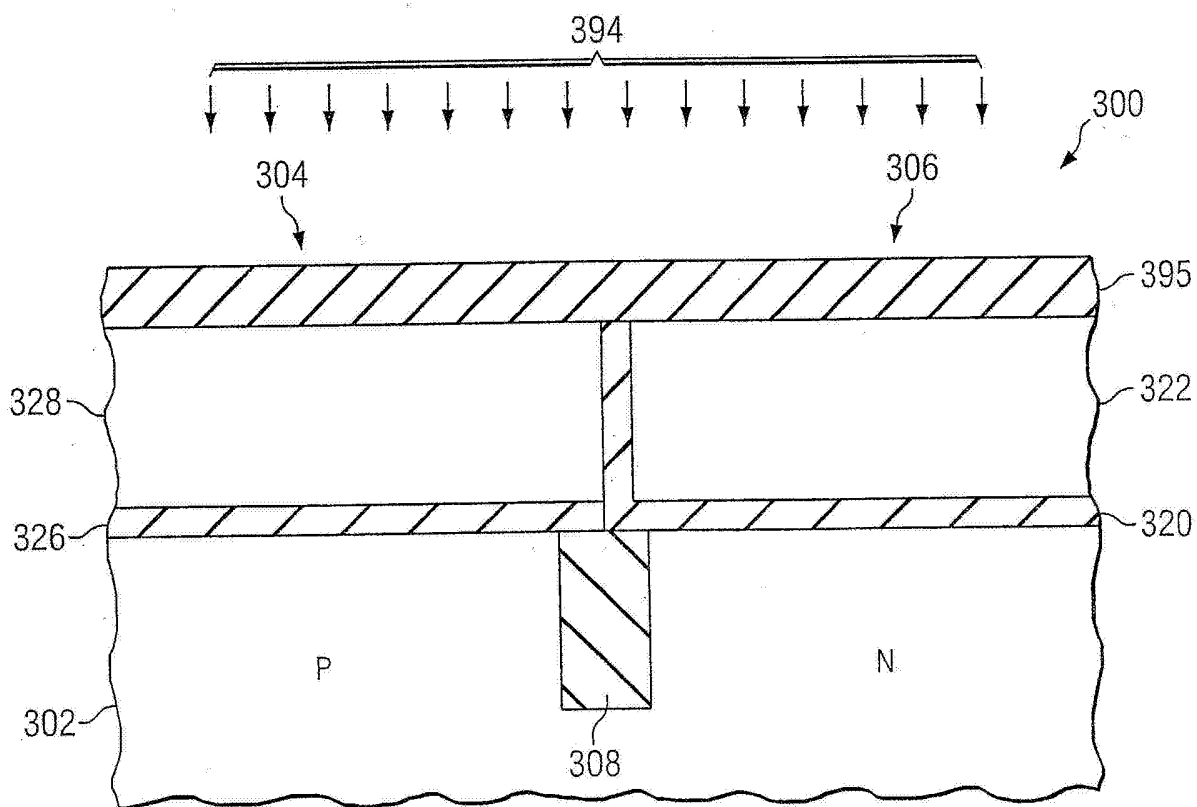


FIG. 16

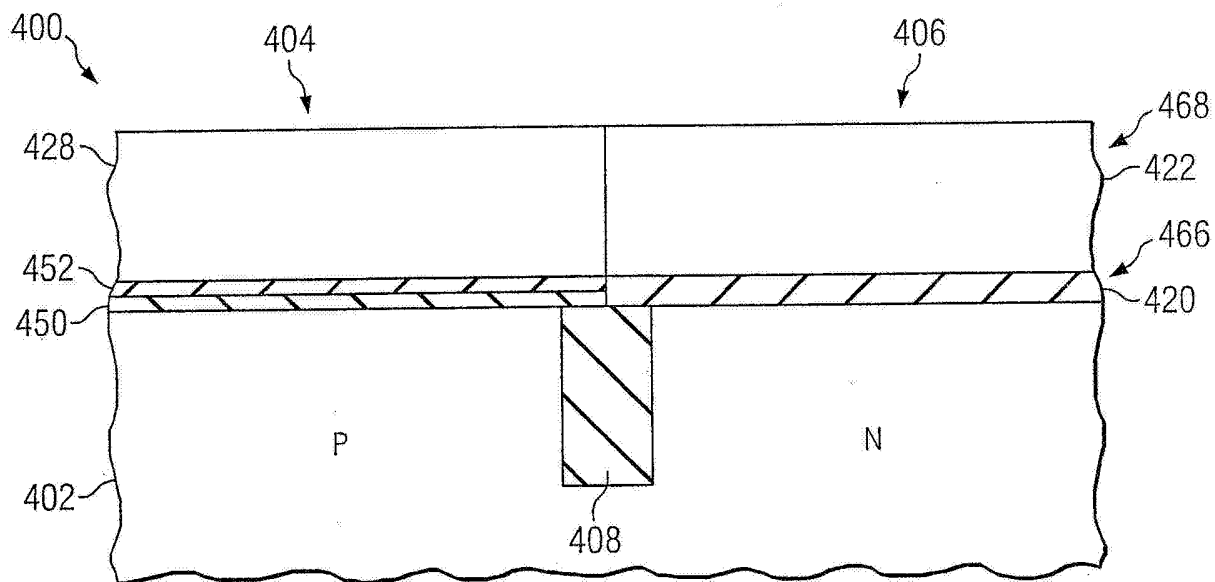


FIG. 19

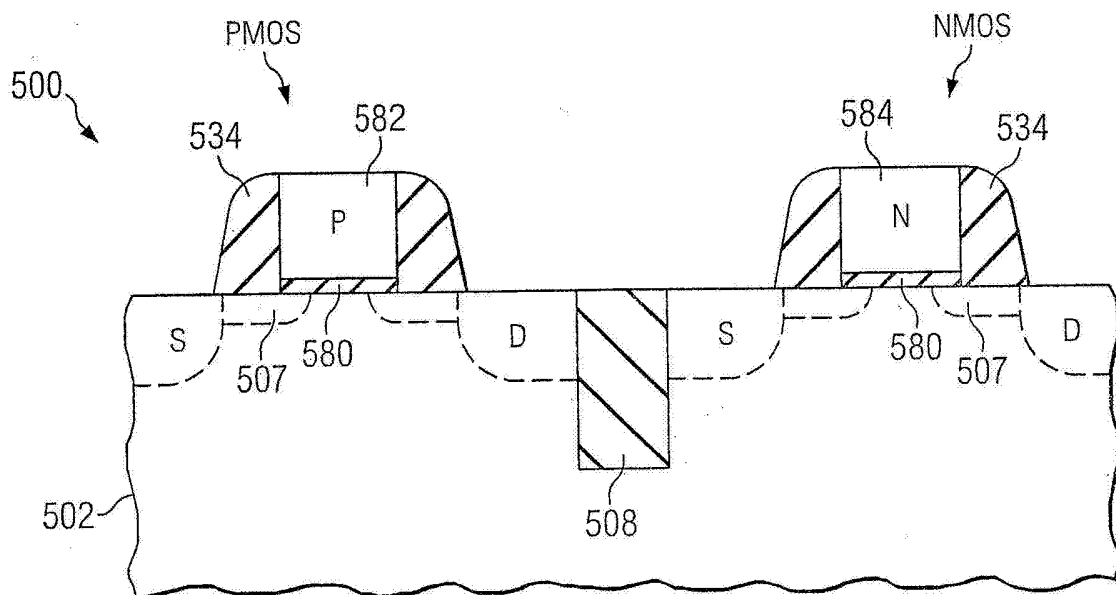


FIG. 20
(PRIOR ART)

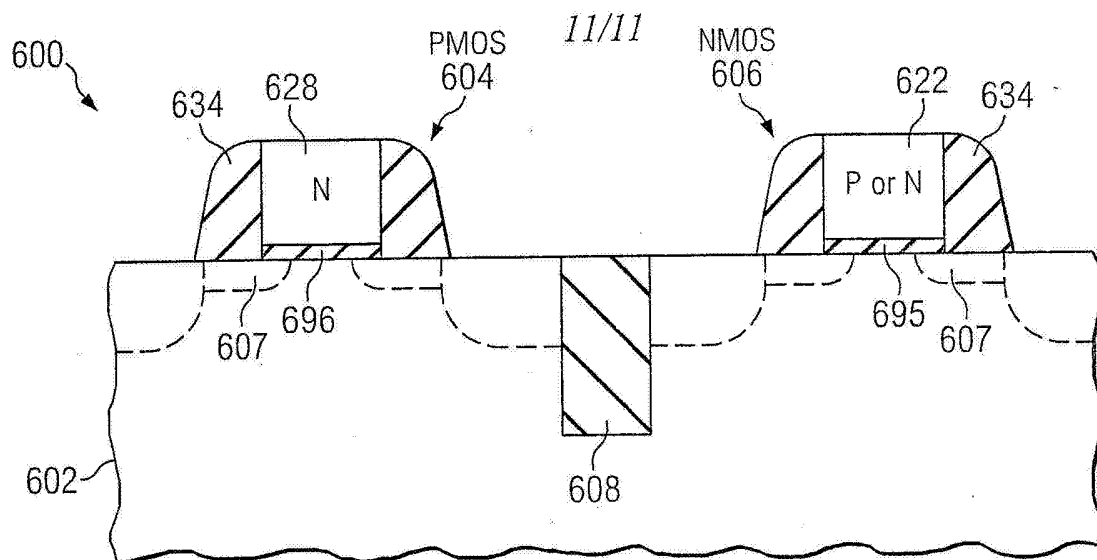


FIG. 21

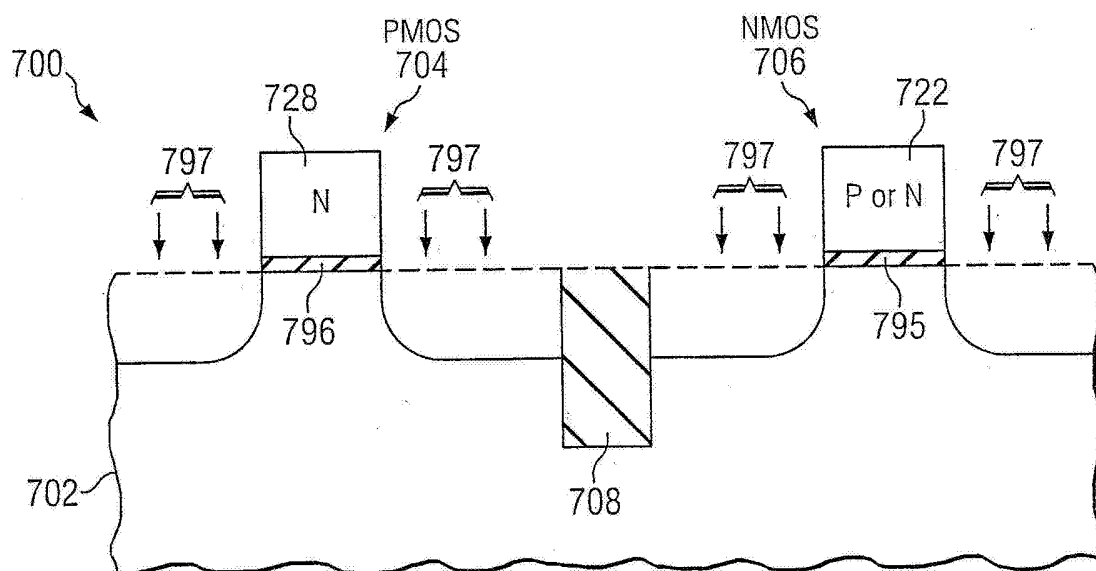


FIG. 22

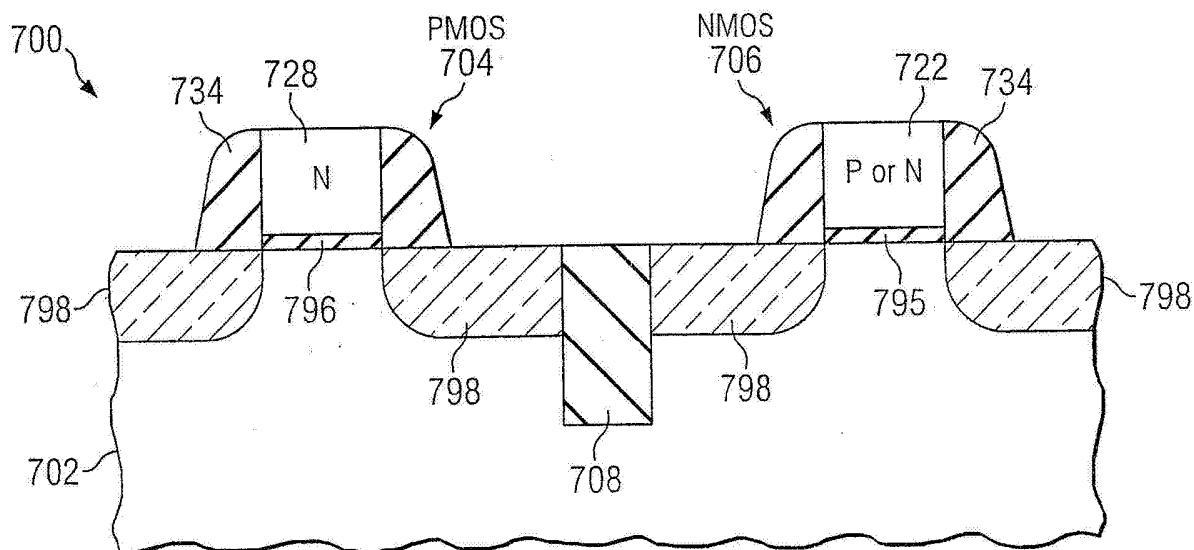


FIG. 23

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2005/056901

A. CLASSIFICATION OF SUBJECT MATTER
H01L27/092 H01L29/51 H01L21/8238

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/135030 A1 (HORIKAWA TSUYOSHI) 26 September 2002 (2002-09-26) paragraphs [0002], [0051] - [0093]	1-3, 5-10, 13, 14, 16-19, 21-23
X	US 6 528 858 B1 (YU BIN ET AL) 4 March 2003 (2003-03-04) column 2, line 34 - column 7, line 10 ----- -/--	1-3, 5-10, 13, 14, 16-19, 21-23

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

G document member of the same patent family

Date of the actual completion of the international search

17 March 2006

Date of mailing of the international search report

28/03/2006

Name and mailing address of the ISA/
European Patent Office, P.B. 5818 Patentlaan 2
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Fax: (+31-70) 340-3016

Authorized officer

Schuitemaker, P

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2005/056901

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>US 5 763 922 A (CHAU ET AL) 9 June 1998 (1998-06-09)</p> <p>column 2, line 45 - column 2, line 57 column 4, line 23 - column 7, line 14</p>	<p>1-3, 5-10,13, 14, 16-19, 21-23</p>
X	<p>US 6 048 769 A (CHAU ET AL) 11 April 2000 (2000-04-11)</p> <p>column 4, line 27 - column 6, line 51</p>	<p>1-3, 5-10,13, 14, 16-19, 21-23</p>

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 4, 11, 12, 15, 20

Present claims 4,11,12,15 and 20 relate to an extremely large number of possible products / methods. Support within the meaning of PCT Article 6 and / or disclosure within the meaning of PCT Article 5 is to be found, however, for only a very small proportion of the compounds / products / apparatus / methods claimed. In the present case, the claims so lack support, and the application so lacks disclosure, that a meaningful search over the whole of the claimed scope is impossible.

Consequently, the search has been carried out for those parts of the claims which appear to be supported and disclosed, namely [indicate precisely what has been covered by the search, e.g. "those compounds/compositions prepared/tested in the examples, and, based on those compounds/based on the compounds present in those compositions, a generalisation of their structural formulae to encompass compounds having the following structural features: (specify exactly these structural features, wherein each individual definition must have a basis in the description or the claims)".

Note: in view of the requirements of PCT Art. 19(2) and 41(2), it is not allowable to make an arbitrary selection.]

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as IPEA is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.5), should the problems which led to the Article 17(2) declaration be overcome.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2005/056901

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 4, 11, 12, 15, 20
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this International application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2005/056901

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002135030 A1	26-09-2002	JP 2002280461 A TW 517378 B	27-09-2002 11-01-2003
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US 5763922 A	09-06-1998	WO 9952151 A1	14-10-1999
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