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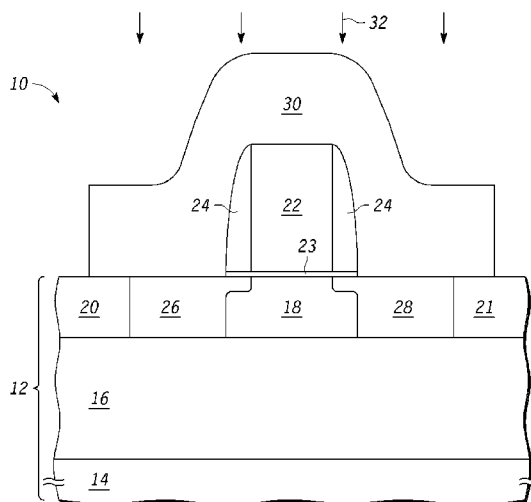
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(54) Title: TRANSFER OF STRESS TO A LAYER



(57) Abstract: A strained semiconductor layer (18) is achieved by a method for transferring stress from a dielectric layer (30) to a semiconductor layer (18). The method comprises providing a substrate (12) having a semiconductor layer (18). A dielectric layer (30) having a stress is formed over the semiconductor layer (18). A radiation anneal (32) is applied over the dielectric layer of a duration not exceeding 10 milliseconds to cause the stress of the dielectric layer (30) to create a stress in the semiconductor layer (18). The dielectric layer (30) may then be removed. At least a portion of the stress in the semiconductor layer (18) remains in the semiconductor layer after the dielectric layer (30) is removed. The radiation anneal can be either by using either a laser beam or a flash tool. The radiation anneal can also be used to activate source/drain regions (26, 28).

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TRANSFER OF STRESS TO A LAYER

Field of the Invention

This invention relates generally to integrated circuits, and more particularly to
5 transferring stress from one layer to another in an integrated circuit.

Related Art

One of the techniques that has been found to enhance transistor performance is to
provide a semiconductor layer that has strain. The strain is effective because it increases
10 carrier mobility. This is typically achieved by forming the strained semiconductor layer by
epitaxial growth over a layer having a different composition. One such example is to grow a
pure silicon layer over a silicon germanium layer. Another example is growing a silicon
germanium layer over a silicon germanium layer with a different percentage of germanium.
Similarly silicon germanium can be grown over silicon. These provide some effectiveness
15 but also increase the semiconductor thickness and are time consuming because of the growth
requirement.

Another approach has been to transfer the stress in an overlying layer, which may be
sacrificial, to underlying amorphous source/drain regions. At the time of changing from
amorphous to crystalline, the underlying source/drain regions become somewhat strained due
20 to the stress of the overlying layer. One problem with this approach is that the amount of
stress transferred to the underlying semiconductor layer is limited. Other issues include
excessive heating and diffusion of source/drain dopants.

Thus, there is a need to provide an improved stress transfer technique.

Brief Description of the Drawings

The present invention is illustrated by way of example, and not by way of limitation,
in the figures of the accompanying drawings and in which like reference numerals refer to
like elements and in which:

FIG. 1 is a cross section of a semiconductor device at a stage in a process according to
30 one embodiment;

FIG. 2 is a cross section of the semiconductor device of FIG. 1 at subsequent stage in
the process;

FIG. 3 is a cross section of the semiconductor device of FIG. 2 at subsequent stage in
the process;

FIG. 4 is a cross section of the semiconductor device of FIG. 3 at subsequent stage in the process;

FIG. 5 is a cross section of a semiconductor device of FIG. 4 at subsequent stage in the process;

5 FIG. 6 is a cross section of a semiconductor device at a stage in a process according to another embodiment;

FIG. 7 is a cross section of the semiconductor device of FIG. 6 at subsequent stage in the process;

10 FIG. 8 is a cross section of the semiconductor device of FIG. 7 at subsequent stage in the process;

FIG. 9 is a cross section of the semiconductor device of FIG. 8 at subsequent stage in the process; and

FIG. 10 is a cross section of the semiconductor device of FIG. 9 at subsequent stage in the process.

15

Description of a Preferred Embodiment

In one aspect, a stressed overlying dielectric layer transfers a resulting strain onto an underlying semiconductor layer. The transfer is effectuated using a directional radiation anneal such as a laser anneal or a flash anneal. The result is that more strain is transferred.

20 The transferred strain also remains after the overlying layer is removed. This is generally important because the overlying layer will typically need to be removed. This has also been found to be effective for underlying semiconductor layers that are not amorphous. This can be beneficial because in such case the underlying semiconductor layer does not have to be converted to amorphous. This is better understood with reference to the FIGs. and the
25 following description.

Shown in FIG. 1 is a semiconductor device 10 formed in and on a substrate 12. Substrate 12 has a supporting layer 14, an insulating layer 16 on supporting layer 14, and a semiconductor layer 18 on insulating layer 16. This is what is generally known as a semiconductor-on-insulator (SOI) substrate. Supporting layer 14 is typically silicon of
30 relatively large thickness that provides physical support. Semiconductor layer 18 is also typically silicon that is comparatively thin, for example 700 Angstroms. Insulating layer 16 is typically oxide. As an alternative, SOI substrate 12 could be replaced by a bulk silicon substrate. On substrate 12 are a gate dielectric 23, a gate 22 on gate dielectric 23, a sidewall spacer 24 around gate 22, a source/drain region 26 substantially aligned to one edge of gate

22, a source/drain 28 aligned to another edge of gate 22. Source/drain regions 26 and 28 are formed in semiconductor layer 18. Also formed in semiconductor layer 18 are trench isolation regions 20 and 21 that are over and adjoin insulating layer 16. Isolation region 20 is adjacent to source/drain region 26. Isolation region 21 is adjacent to source/drain region 28. Gate 22 may be polysilicon or other conductor. Sidewall spacer may be a single a layer or combination of layers and may include a liner. At this stage, source/drain regions 26 and 28 have been implanted and at least portions thereof are amorphous. The amorphization of source/drain regions 26 and 28 may be sufficient from normal source/drain dopants such as boron, arsenic, or phosphorus. If that is not sufficient, an additional implant step using another species such as germanium, silicon, or xenon may be utilized. Also, sidewall spacers could be thinned or even removed to increase the stress transfer effects occurring in subsequent steps to be performed.

Shown in FIG. 2 is semiconductor device 10 after deposition of a dielectric layer 30. Dielectric layer 30 may be silicon nitride or another dielectric material that can be deposited with a desired stress. The thickness of dielectric layer 30 may be about 800 Angstroms and deposited by plasma-enhanced chemical vapor deposition (PECVD). The thickness can vary significantly; a range of 500 to 3000 Angstroms for example. PECVD allows for good control of the stress. PECVD nitride can be either tensile or compressive. But certain desired stresses may also be achieved by other deposition techniques and other dielectrics.

Shown in FIG. 3 is semiconductor device 10 after patterning dielectric layer 30. In this case, dielectric layer 30 is removed outside of trench isolation 20 and trench isolation 21 while being retained between trench isolation 20 and trench isolation 21. Dielectric layer 30 is in direct contact with most of the top surface of source/drain regions 26 and 28 but not with a channel region under gate 22. This is desirable for maximizing stress transfer to source/drain regions 26 and 28, but there may be situations where direct contact is either not feasible or undesirable for some other reason. This patterning may not always be needed. The patterning allows for adding stress to the semiconductor layer for one transistor type and leaving it unchanged for another type. This type of distinction is commonly desirable between P and N channel transistors. The type of stress that increases electron mobility for N channel transistors is normally different than for the stress that increases hole mobility for P channel transistors. There may be situations, however, where such a distinction is not desirable or at least not worth the patterning step.

Shown in FIG. 4 is semiconductor device 10 with an application of a directional radiation anneal 32 of a duration not exceeding 10 milliseconds (ms). Laser and flash

anneal are capable of this. The duration may be shorter, such as 1 ms, and be a peak temperature of 1200 to 1400 Celsius with semiconductor device 10 on a heated chuck. The chuck temperature may preferably be 400 degrees Celsius. A range of 375 to 450 degrees Celsius may also be effective. Although not believed to be necessary in this situation, it may be desirable to deposit an absorber layer for the directional radiation anneal.

Shown in FIG. 5 is semiconductor device 10 after completion of directional radiation anneal, after source/drain regions 26 and 28 have become source/drains 34 and 36, and after the removal of dielectric layer 30. The change to source/drain regions 26 and 28 arises from transferring the stress of dielectric layer 30 and re-crystallizing achieved from directional radiation anneal 32. Source/drains 34 and 36 are activated and stressed. The stress transfer from dielectric layer 30 to source/drains 34 and 36 is measurably better than the stress transfer when using a rapid thermal anneal (RTA). Semiconductor device 10 is now a fully functional transistor. Source/drains 34 and 36 can be either P or N type and the stress of source/drains 34 and 36 can be either tensile or compressive based upon the stress of dielectric layer 30. There may be situations in which dielectric layer 30 may not need to be removed.

Shown in FIG. 6 is semiconductor device 40 comprising a substrate 42 having a supporting layer 44, an insulating layer 46 on supporting layer 44, and a semiconductor layer 48 on insulating layer 46 in which semiconductor layer 48 has formed therein a trench isolation 50 and a trench isolation 52. Substrate 42 is an SOI substrate similar to that of substrate 12. The primary difference is that semiconductor layer 48 is preferably thinner than 700 Angstroms. The thickness of semiconductor layer 48 may be in the range of 100 to 500 Angstroms. Semiconductor layer 48 may be crystalline rather than amorphous. In such case there is no amorphizing step. In some situations it may be desirable to have a portion of semiconductor layer 48 be amorphous even though there is the disadvantage of increased processing due to the amorphization step that would be necessary to achieve that.

Shown in FIG. 7 is semiconductor device 40 after deposition of a dielectric layer 54. Dielectric layer 54 is similar to dielectric layer 30. In this case, however, dielectric layer 54 is preferably significantly thicker than semiconductor layer 48, whereas in the case of dielectric layer 30, it may be nearly the same as semiconductor layer

Shown in FIG. 8 is after patterning dielectric layer 54. In this case, dielectric layer 54 is removed outside of trench isolation 50 and trench isolation 52 while being retained between trench isolation 50 and trench isolation 52. Dielectric layer 54 is shown in direct contact with semiconductor layer 48 between trench isolation 50 and trench isolation 52.

This is desirable for maximizing stress transfer, but there may be situations where direct contact is either not feasible or undesirable for some other reason. This patterning may not always be needed. The patterning allows for adding stress to the semiconductor layer for one transistor type and leaving it unchanged for another type. This type of distinction is commonly desirable between P and N channel transistors. The type of stress that increases electron mobility for N channel transistors is normally different than for the stress that increases hole mobility for P channel transistors. There may be situations, however, where such a distinction is not desirable or at least not worth the patterning step.

Shown in FIG. 9 is semiconductor device 40 with an application of a directional radiation anneal 56 for a duration that is less than 10 milliseconds (ms). Laser and flash anneal are capable of this. The duration may be shorter, such as 1 ms, and be a peak temperature of 1200 to 1400 Celsius with semiconductor device 10 on a heated chuck. The chuck temperature may be in a range of 375 to 450 degrees Celsius. Although not believed to be necessary in this situation of using silicon nitride as dielectric layer 54, it may be desirable to deposit an absorber layer for inhibiting reflection of the directional radiation anneal.

Shown in FIG. 10 is semiconductor device 40 after completion of directional radiation anneal, after semiconductor layer 48 has become semiconductor layer 58, and after the removal of dielectric layer 54. The change to semiconductor layer 48 arises from transferring the stress of dielectric layer 54. The stress transfer from dielectric layer 54 to semiconductor layer 48 is measurably better than the stress transfer when using a rapid thermal anneal (RTA). Semiconductor device 40 now has an active region, semiconductor layer 58 between trench isolation 50 and trench isolation 52. The stress of semiconductor layer 58 can be either tensile or compressive based upon the stress of dielectric layer 54. There may be situations in which dielectric layer 54, or portions thereof, may not need to be removed. As an alternative, the method for the stress transfer to the semiconductor layer as shown in FIGs. 6-10 would be completed prior to the formation of isolation regions 50 and 52.

Semiconductor device 40 of FIG. 10 is now usable for making transistors. One way this could be done is for semiconductor device 40 to be substituted for substrate 12 of FIG. 1. In such case semiconductor layer 18 would have a starting stress that would be altered in the source/drain regions. Although some relaxation is likely to occur in the channel, the channel would retain some of the original stress and the source/drain regions would be altered to achieve the desired source/drain stress. Another alternative is for semiconductor layer 58 of FIG. 10 to be used for one type of transistor, in which case the source/drains and channel

would not necessarily have the stress further changed, and transistors of the other type would undergo the process of FIGs. 1-5 to have the source/drain stress be different from the channel stress.

5 Various changes and modifications to the embodiments herein chosen for purposes of illustration will readily occur to those skilled in the art. For example, different temperature ranges and thicknesses than those described may be found to be effective. To the extent that such modifications and variations do not depart from the spirit of the invention, they are intended to be included within the scope thereof which is assessed only by a fair interpretation of the following claims.

CLAIMS

What is claimed is:

- 5 1. A method, comprising:
 providing a substrate having a semiconductor layer;
 forming a dielectric layer having a stress over the semiconductor layer;
 applying a radiation anneal over the dielectric layer of a duration not
 exceeding 10 milliseconds to cause the stress of the dielectric layer to
10 create a stress in the semiconductor layer; and
 removing the dielectric layer, wherein at least a portion of the stress in the
 semiconductor layer remains in the semiconductor layer after the
 dielectric layer is removed.
- 15 2. The method of claim 1, wherein a portion of the semiconductor layer is made to be
 amorphous prior to applying the radiation anneal.
3. The method of claim 1, wherein a portion of the semiconductor layer is made
 amorphous prior to applying the radiation anneal by implanting one of germanium,
20 silicon, and xenon.
4. The method of claim 1, wherein the semiconductor layer is substantially thinner than
 the dielectric layer.
- 25 5. The method of claim 1, further comprising:
 forming a gate electrode over the semiconductor layer after removing the
 dielectric layer; and
 forming first and second source/drain regions in the semiconductor layer.
- 30 6. The method of claim 1, wherein the dielectric layer comprises nitride, further
 comprising:
 forming a sidewall spacer adjacent to the gate

performing, prior to forming the dielectric layer, one of a group of steps consisting of thinning the sidewall spacer and removing the sidewall spacer.

- 5 7. The method of claim 1, wherein applying the radiation anneal further comprises
applying the radiation using a laser.
8. The method of claim 1, wherein forming the dielectric layer is further comprises
forming the dielectric layer by plasma-enhanced chemical vapor deposition (PECVD).
- 10 9. The method of claim 1, wherein applying the radiation anneal further comprises
applying the radiation anneal to cause a peak temperature of 1200 to 1400 degrees
Celsius in the dielectric layer.
- 15 10. The method of claim 1, further comprising patterning the dielectric layer prior to
applying the radiation anneal.
11. The method of claim 10, further comprising:
forming shallow trench isolation in the semiconductor layer prior to forming
the dielectric layer.
- 20 12. A method, comprising:
providing a substrate having a semiconductor layer;
forming a gate electrode over the semiconductor layer;
forming first and second source/drain regions in the semiconductor layer;
forming a stressed dielectric layer over the semiconductor layer; and
applying a laser anneal to the stressed dielectric layer, wherein the laser anneal
and the stressed dielectric layer impart a first stress to the
semiconductor layer to create a stressed semiconductor layer, and
wherein at least a portion of the first stress will remain in the
semiconductor layer if the stressed dielectric layer is removed from the
stressed semiconductor layer.
- 30

13. The method of claim 12, further comprising removing the stressed dielectric layer.

14. The method of claim 12, wherein applying a laser anneal further comprises applying
5 the laser anneal with a duration not exceeding 10 milliseconds.

15. The method of claim 12, wherein a portion of the semiconductor layer is made to be amorphous prior to applying the radiation anneal.

10 16. The method of claim 12, further comprising:
forming a sidewall spacer adjacent to the gate electrode; and
performing, prior to forming the dielectric layer, one of a group of steps
consisting of thinning the sidewall spacer and removing the sidewall
spacer.

15

17. A method, comprising:
providing a substrate having a semiconductor layer;
forming a first dielectric layer having a first stress over the semiconductor
layer;
20 applying a first radiation anneal over the first dielectric layer of a duration not
exceeding 10 milliseconds to create a semiconductor layer having a
second stress;
removing the first dielectric layer, wherein at least a portion of the second
stress remains in the stressed semiconductor layer after the first
25 dielectric layer is removed;
forming a gate electrode over the semiconductor layer;
forming first and second source/drain regions in the semiconductor layer;
forming a second dielectric layer having a third stress over the semiconductor
layer; and
30 applying a second radiation anneal over the second dielectric layer of a
duration not exceeding 10 milliseconds to create a semiconductor layer
having a fourth stress, wherein at least a portion of the fourth stress
would remain in the semiconductor layer if the second dielectric layer
were removed.

18. The method of claim 17, further comprising forming shallow trench isolation in the semiconductor layer prior to forming the first dielectric layer, wherein a first region is formed on one side of the shallow trench isolation and a second region is formed on another side of the shallow trench isolation, and wherein the first dielectric layer is formed over the first region and the second dielectric layer is formed over the second region.
19. The method of claim 17, wherein a portion of the semiconductor layer is made to be amorphous prior to applying the second radiation anneal.
20. The method of claim 17, wherein applying the first and second radiation anneals further comprises applying the first and second radiation anneals using a laser.

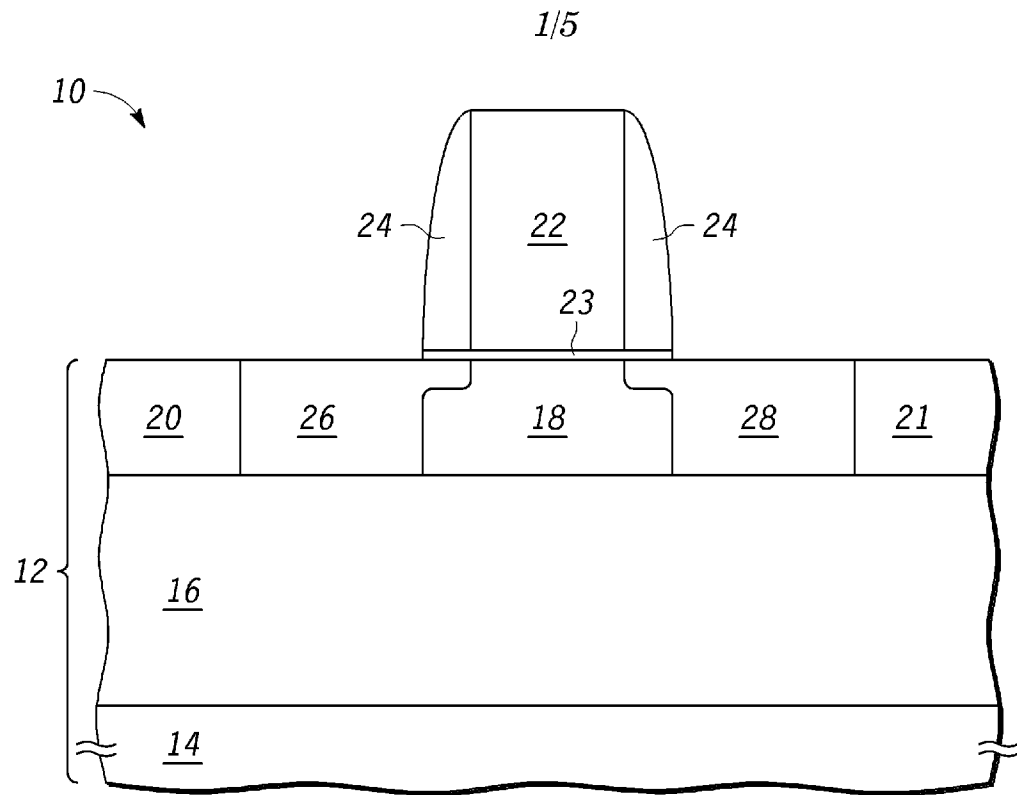


FIG. 1

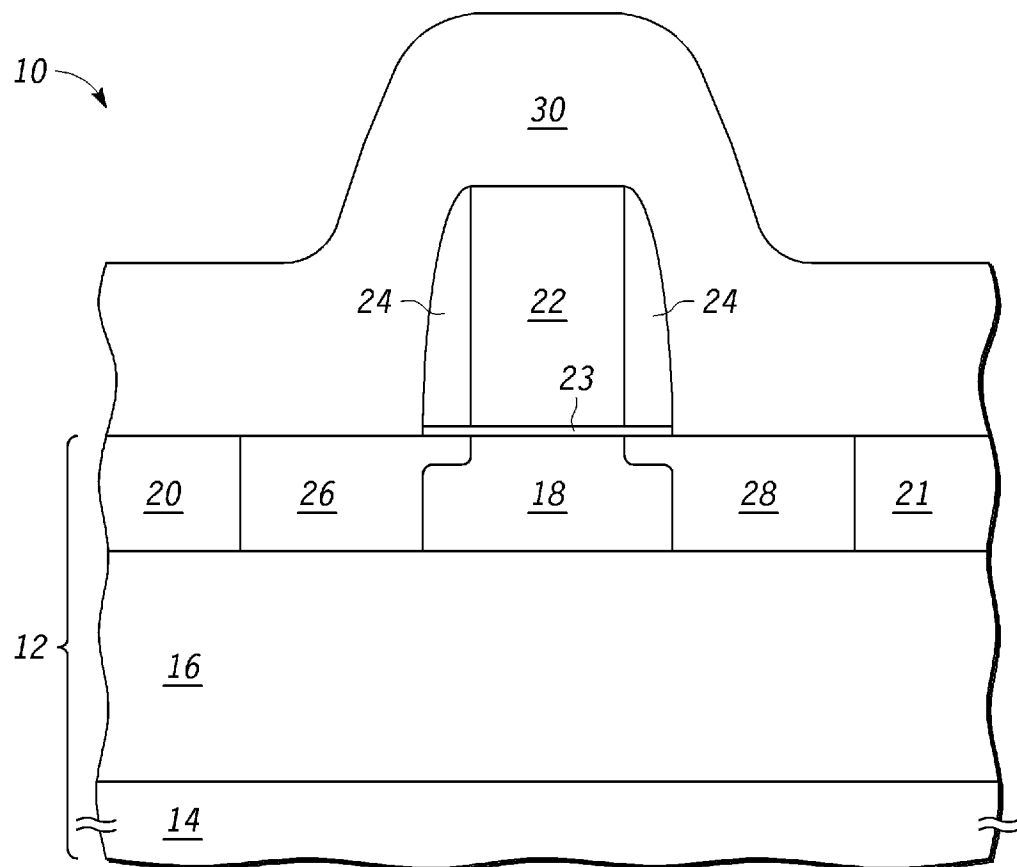


FIG. 2

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FIG. 3

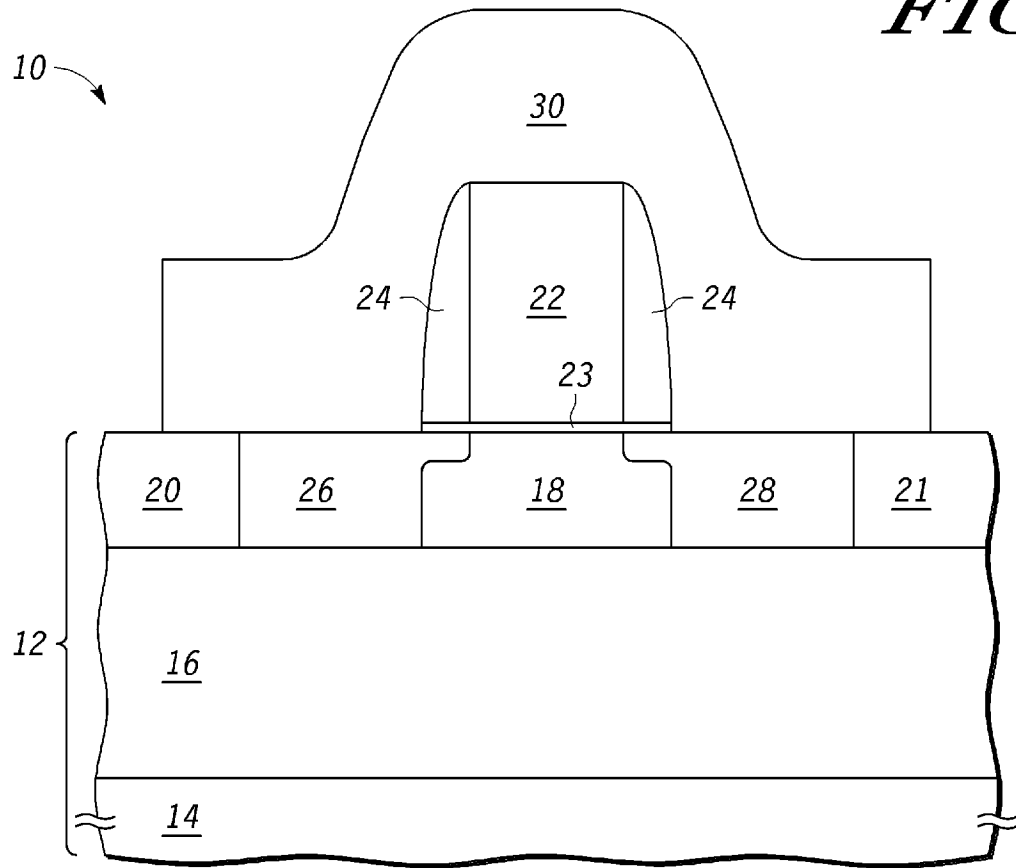
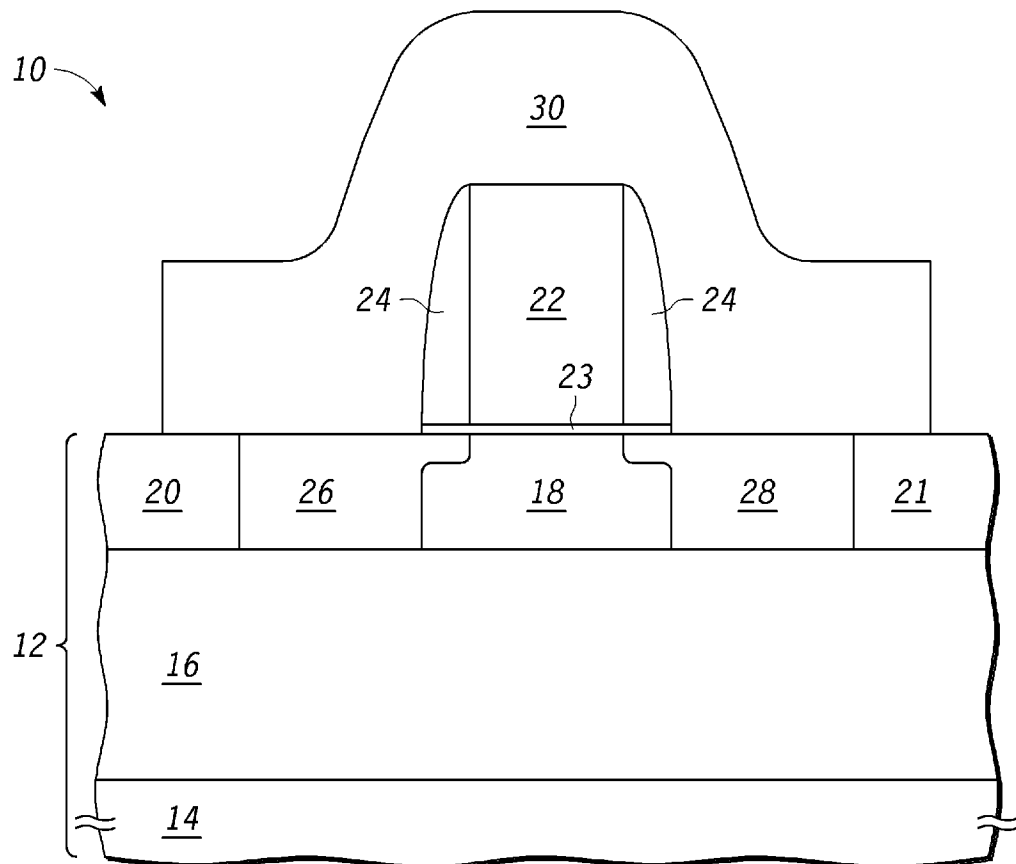


FIG. 4



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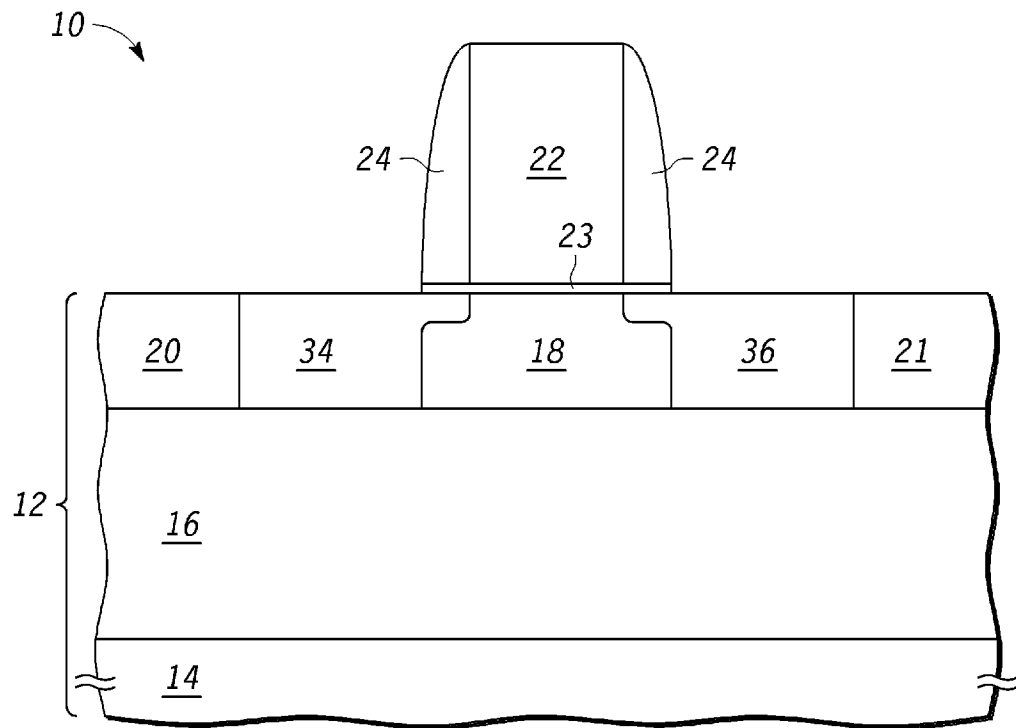


FIG. 5

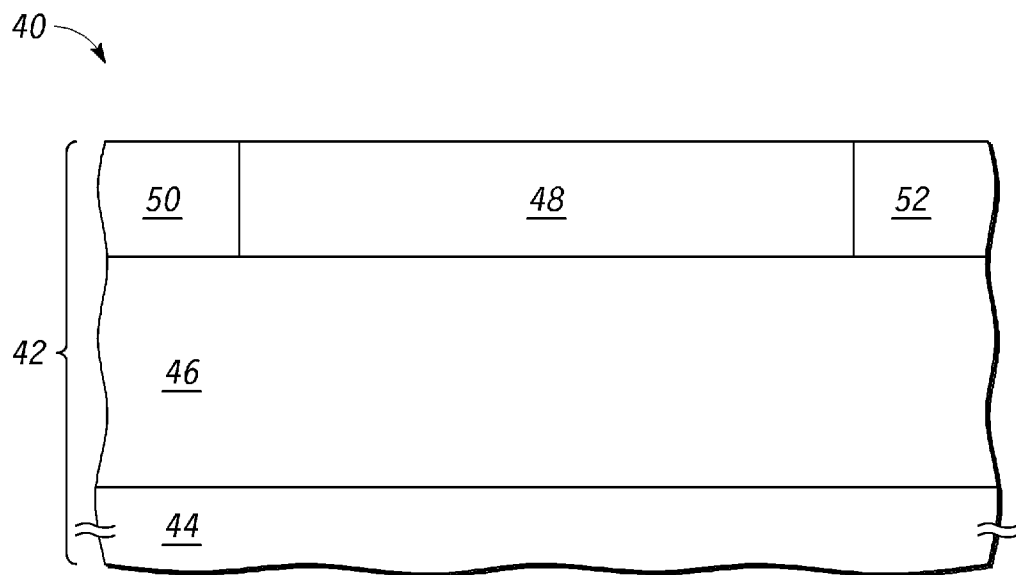


FIG. 6

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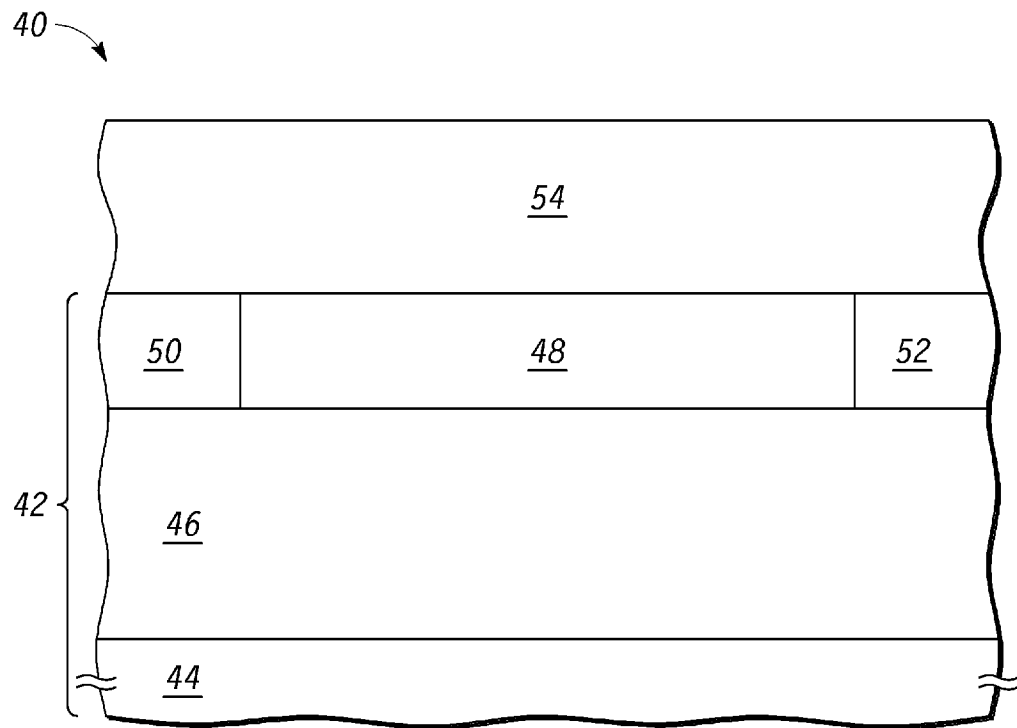


FIG. 7

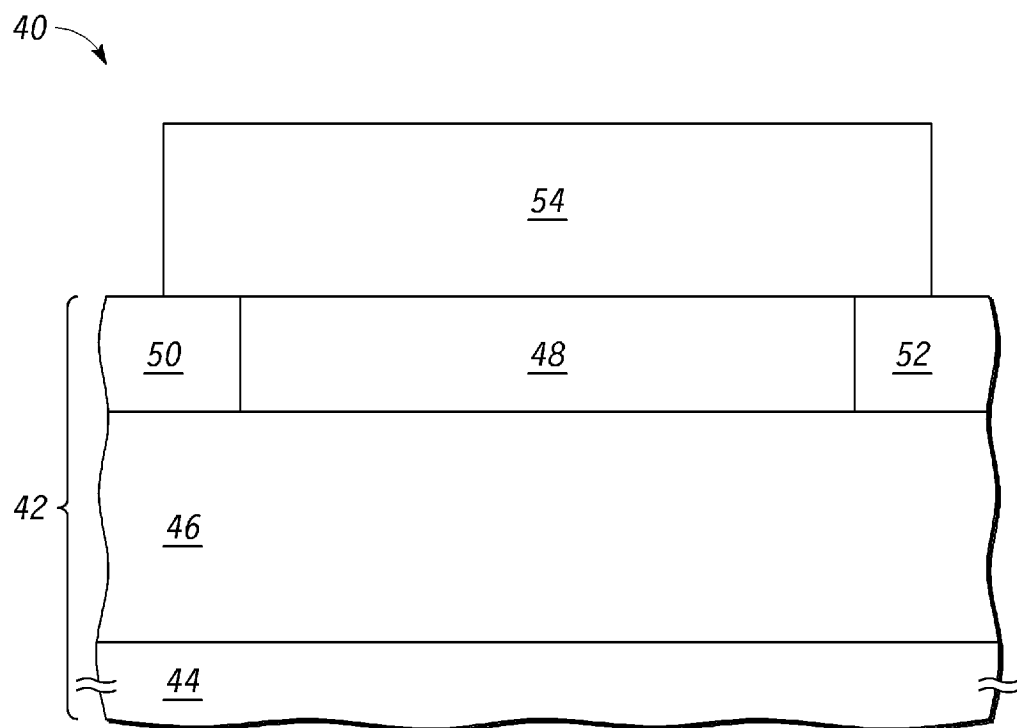
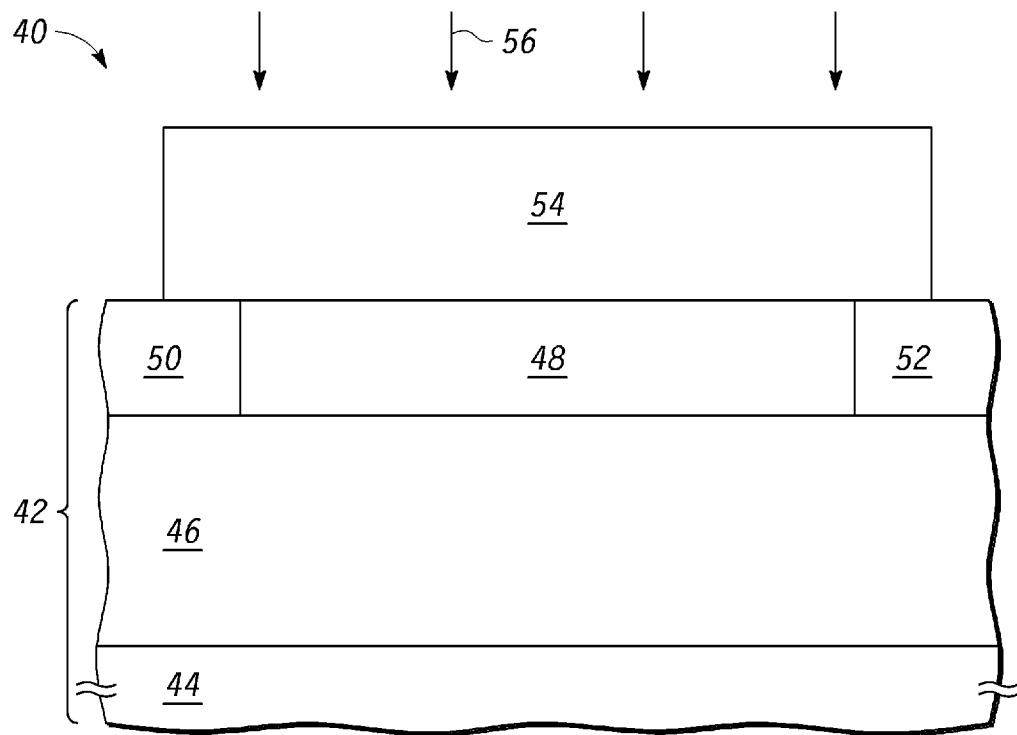
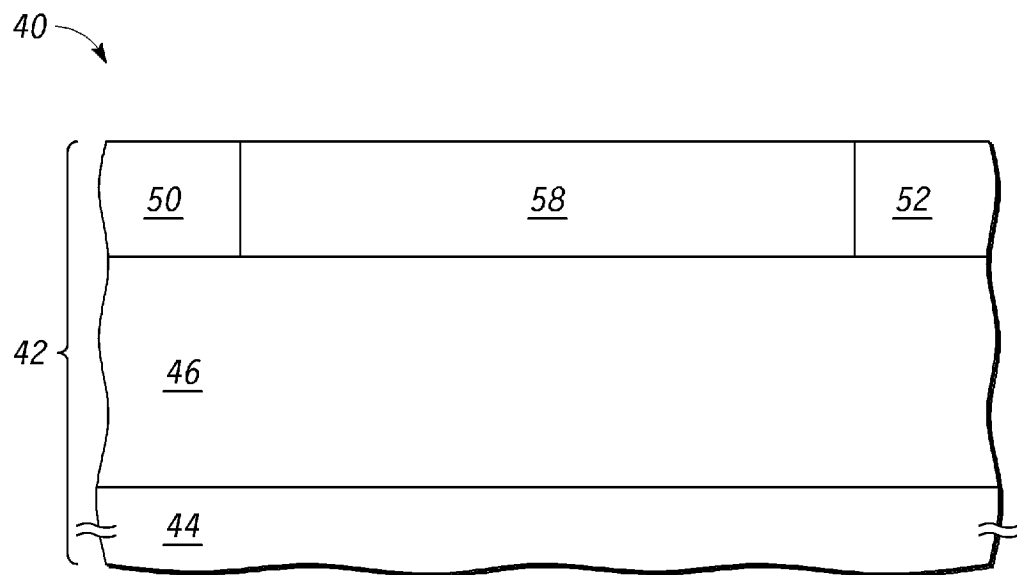


FIG. 8

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*FIG. 9**FIG. 10*

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 07/68098

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 31/117 (2207.01)

USPC - 257/616, 3087, 360; 438/142

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) : H01L 31/117 (2207.01)

USPC : 257/616, 3087, 360; 438/142

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC : 257/616, 3087, 360; 438/142 - search terms below

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWEST, Google Scholar, Google

Search terms:

stress, strain, implantation, amorphous, substrate, laser and anneal, PECVD, dielectric, gate, source, drain, temperature, implant, germanium, millisecond

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/0014366 A1 (Currie et al.) 19 January 2006 (19.01.2006); paras [0003], [0006], [0010], [0014]-[0015], [0019]-[0020], [0023], [0028], [0061]-[0062], [0071]-[0072], [0091], [0095] and [0129].	1-5, 7-15, 17-20
Y		6 and 16
Y	US 2006/0134899 A1 (Wu et al.) 22 June 2006 (22.06.2006); para [0005].	6 and 16

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

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Date of the actual completion of the international search

19 September 2007 (19.09.2007)

Date of mailing of the international search report

29 OCT 2007

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