

[54] **CARDIAC RESUSCITATOR**

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[51] **Int. Cl.**.....**A61n 1/36**

[58] **Field of Search**.....128/2.06 A, 2.06 E, 2.06 F, 128/2.06 R, 2.1 E, 2.1 R, 2.1 Z, 419 D, 419 P, 2.05 P, 2.05 R, 2.05 S, 2.05 T

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[57] **ABSTRACT**

A resuscitator apparatus includes means for detecting and counting the electrical and mechanical output of the heart of a suspected heart attack victim, and means for substantially immediately applying a pacing pulse or a defibrillating pulse, as required. Thus, if both electrical and mechanical outputs have low rates, or are nonexistent, a pacing pulse is automatically applied for stimulating a heart beat in time with such pulse. However, if electrical activity is present while mechanical output is absent, indicative of ventricular fibrillation, a defibrillating pulse is applied to the patient. If both electrical and mechanical activity are present, indicative of substantially normal operation, appropriate indication is given, and no corrective action is taken. The apparatus attaches to the patient for administering the correct electrical stimulation to the patient as soon as possible after the occurrence of the suspected attack.

17 Claims, 14 Drawing Figures

TRUTH TABLE

ECG	ΔZ	D	P
0	0	0	1
1	0	1	0
1	1	0	0

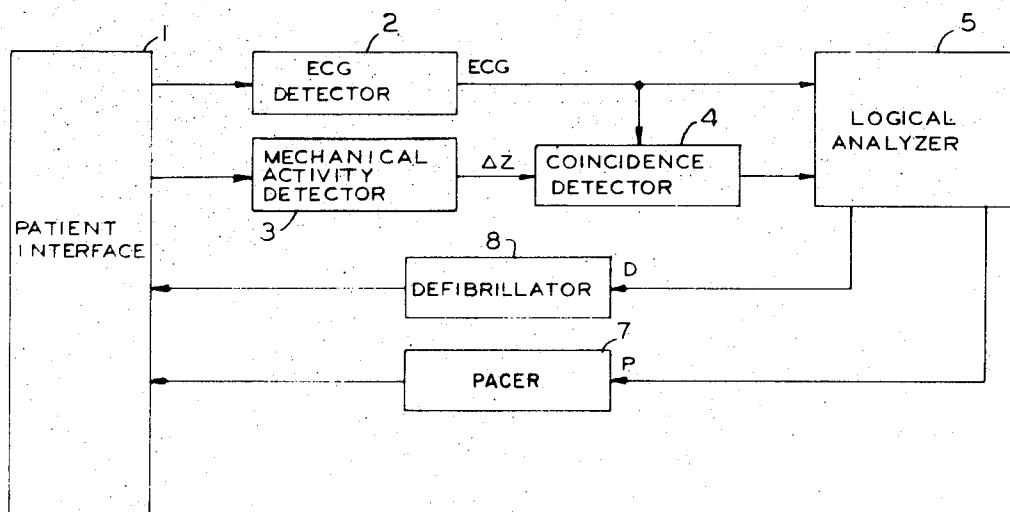


FIG. 1

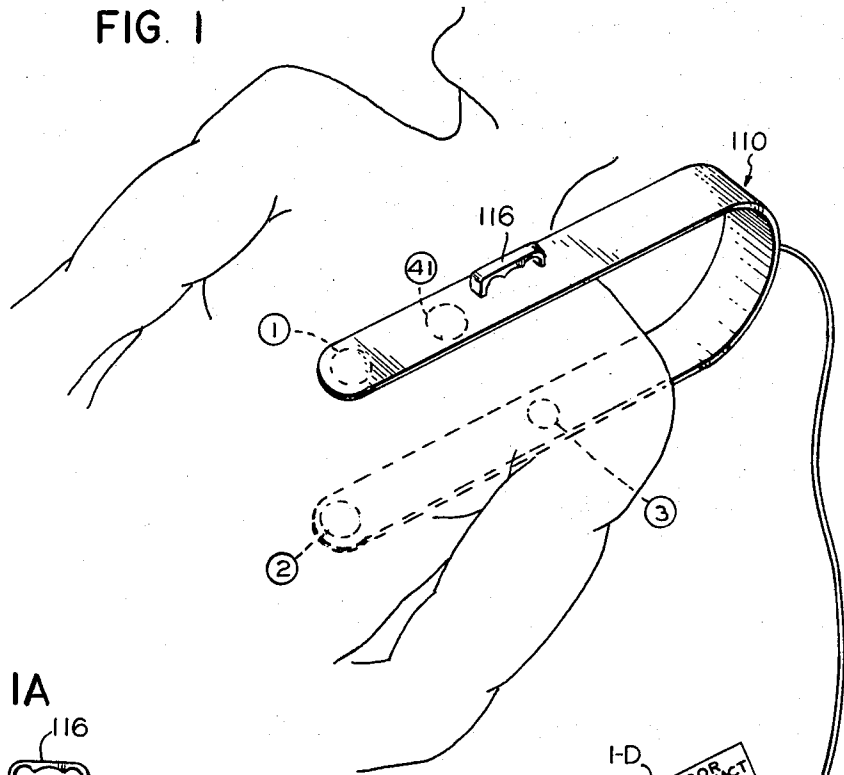
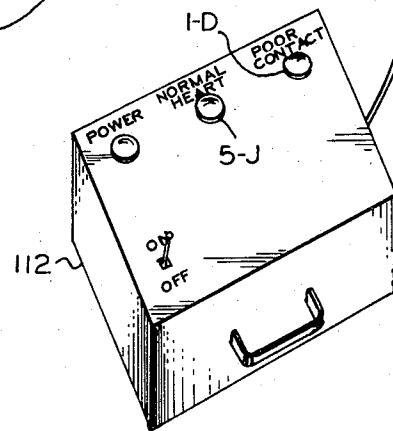
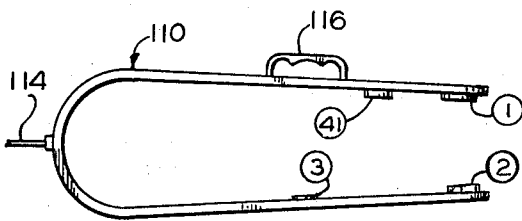


FIG. 1A



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FIG. 2

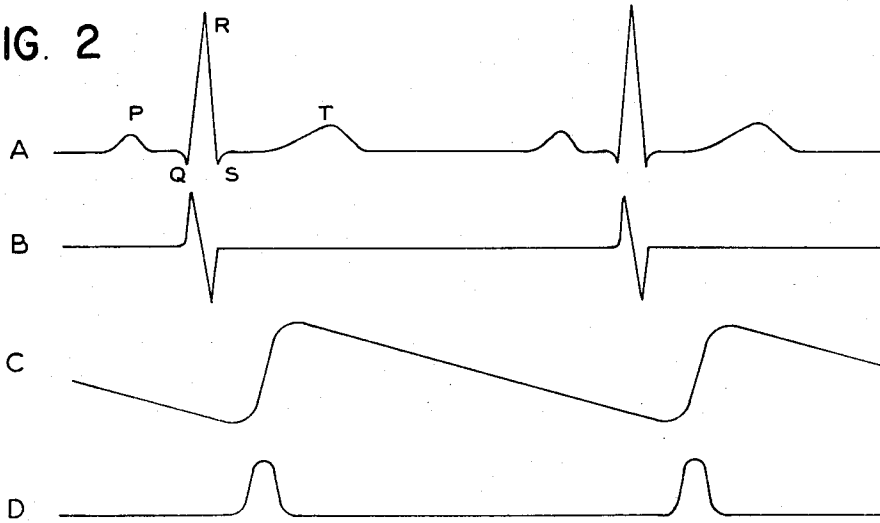
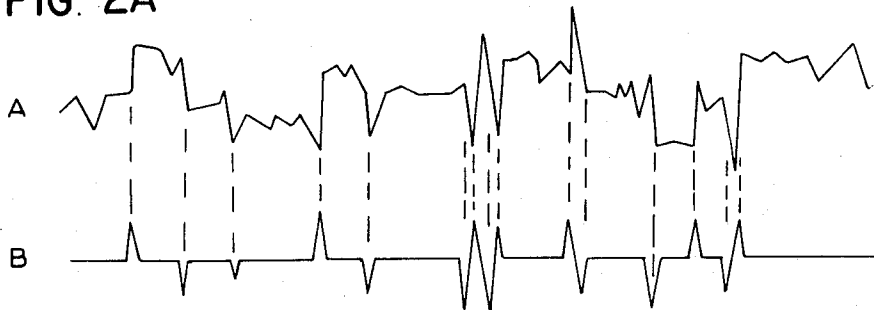


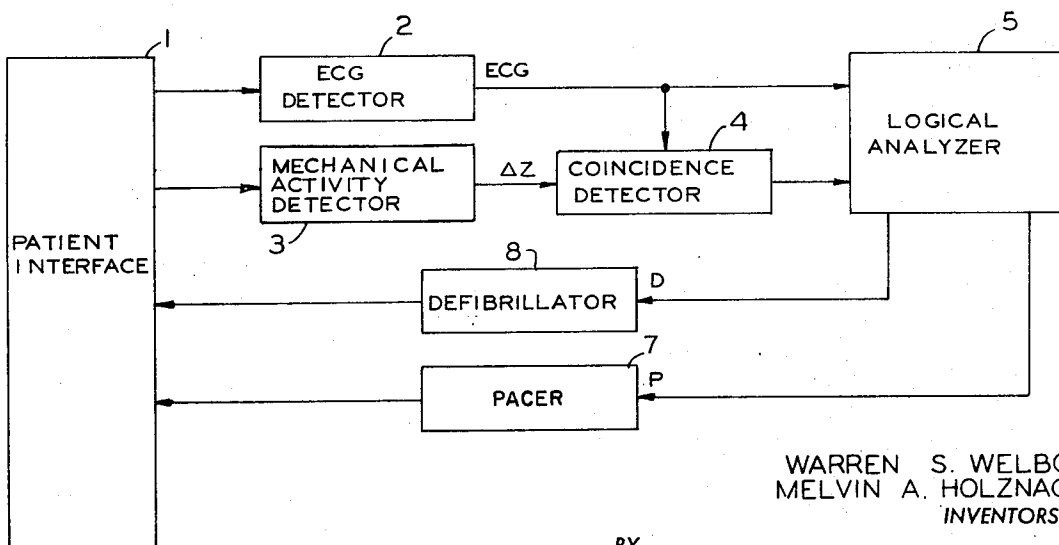
FIG. 2A



TRUTH TABLE

ECG	ΔZ	D	P
0	0	0	1
1	0	1	0
1	1	0	0

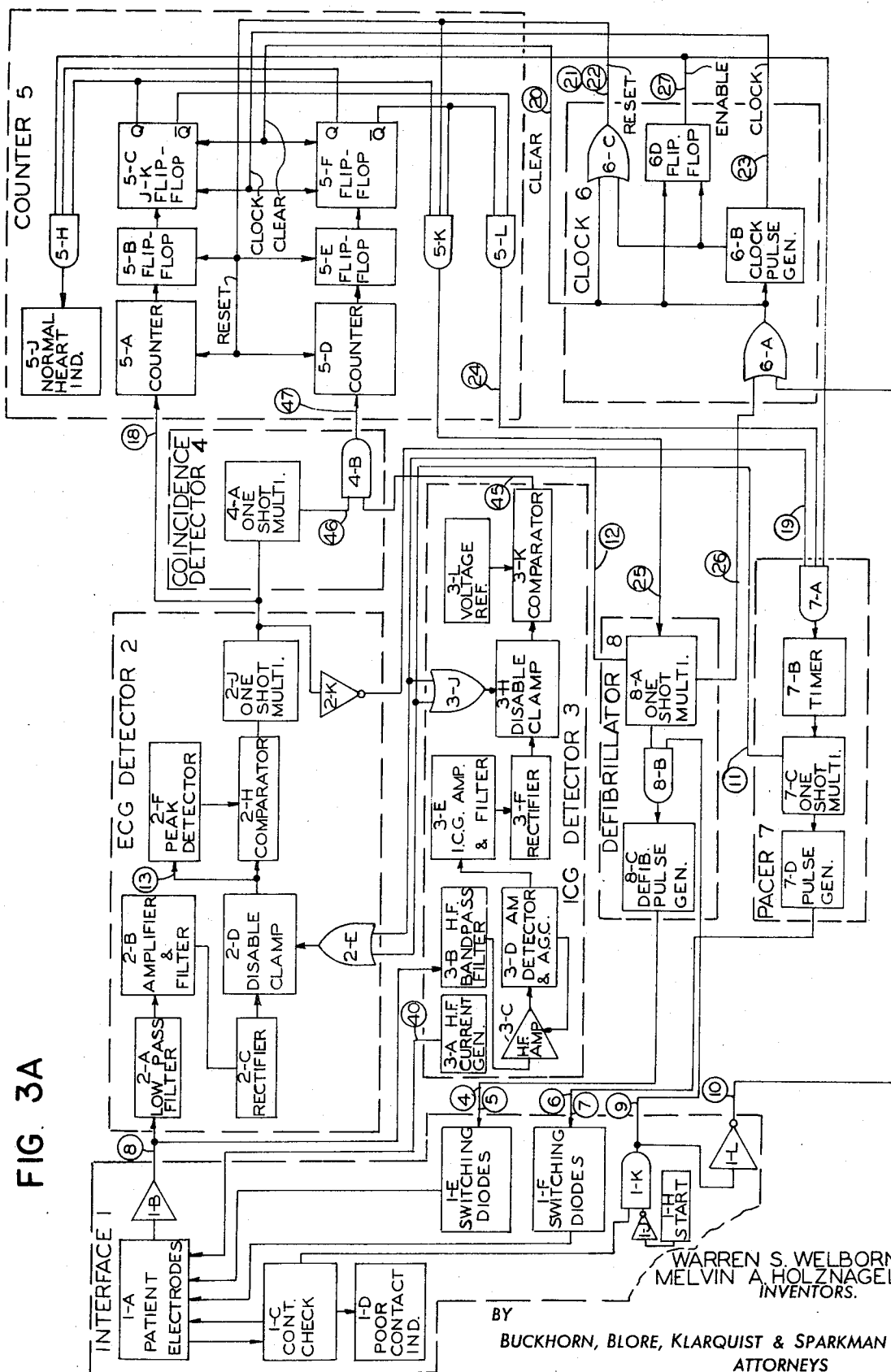
FIG. 3



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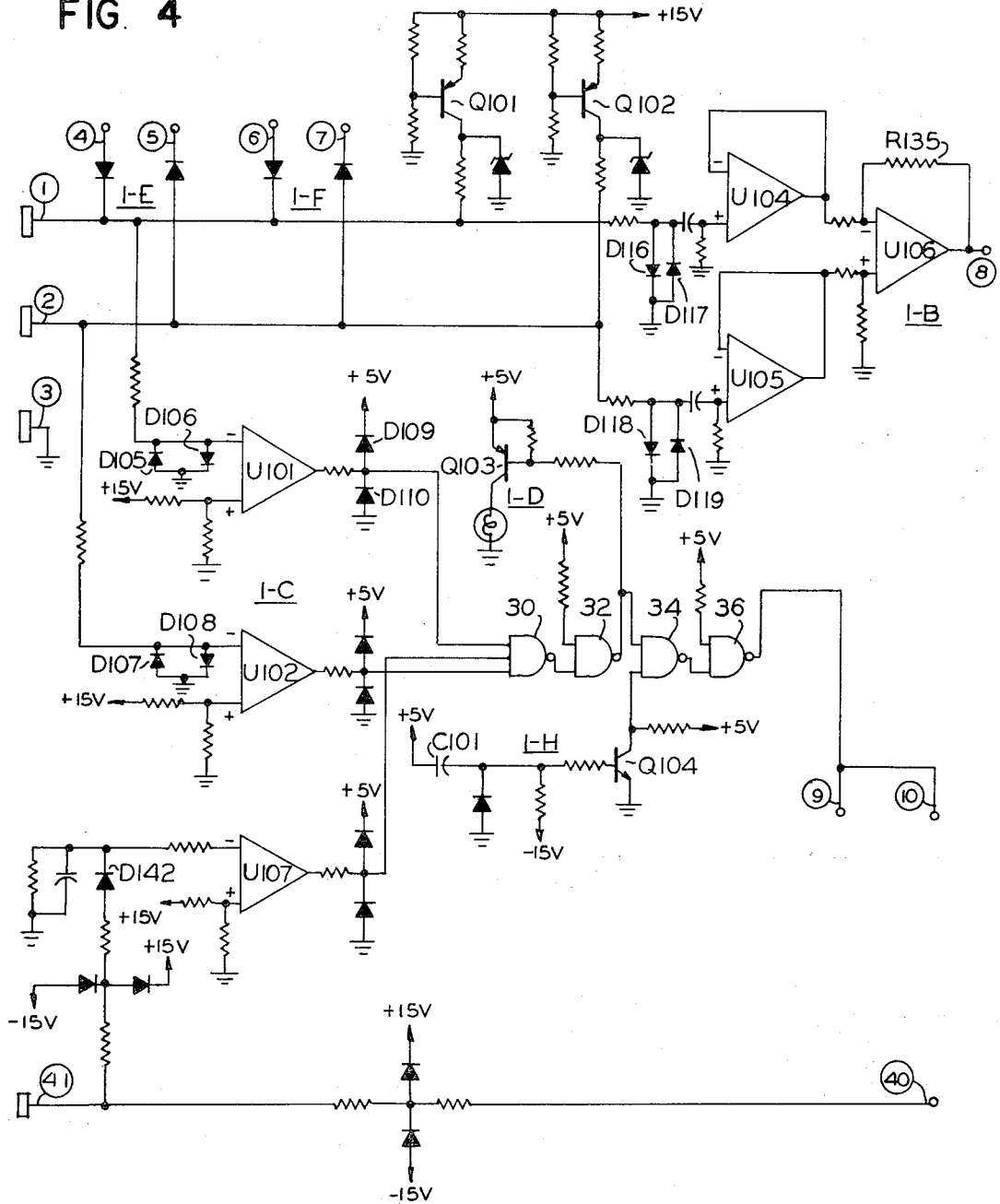
FIG. 3A



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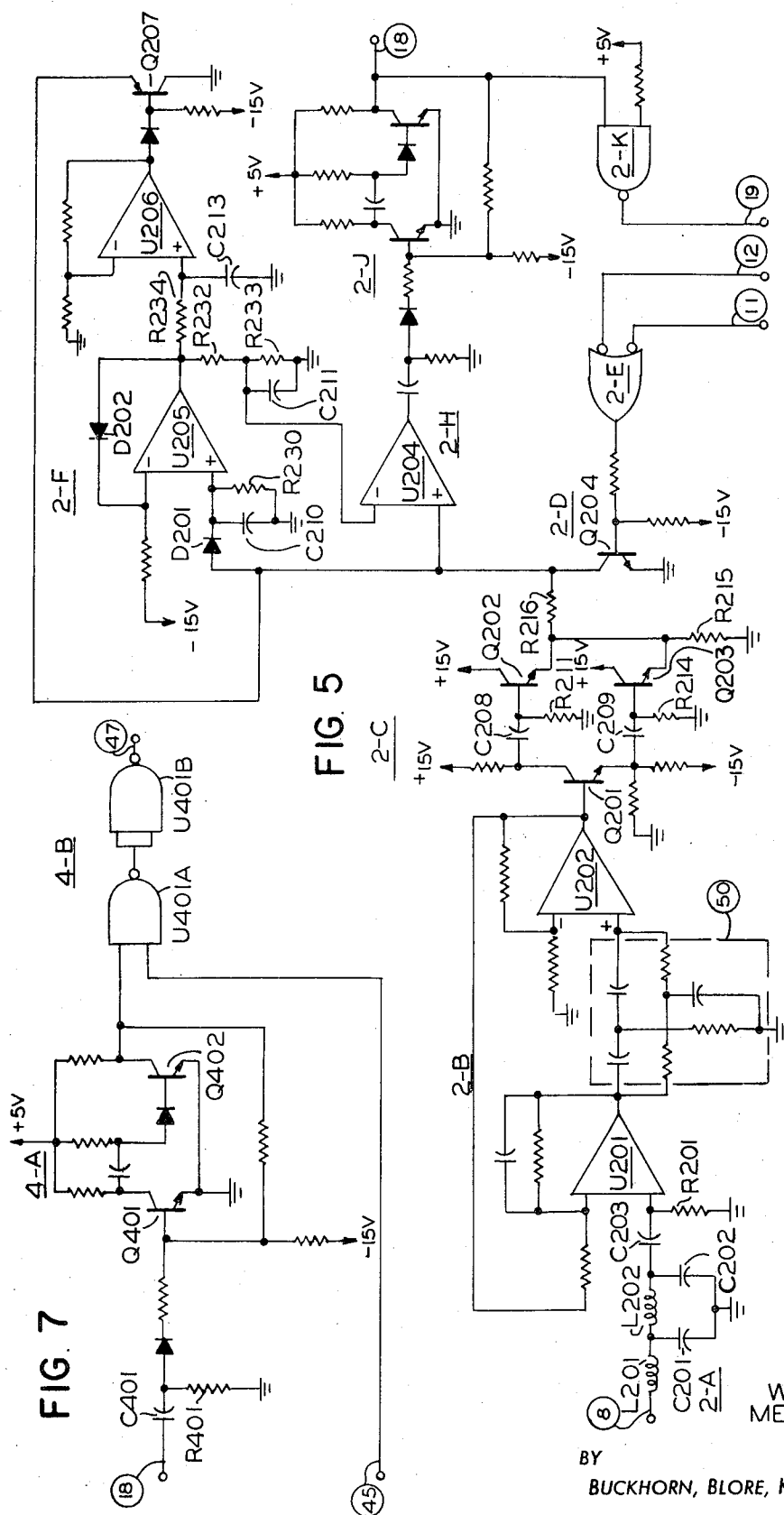
FIG. 4



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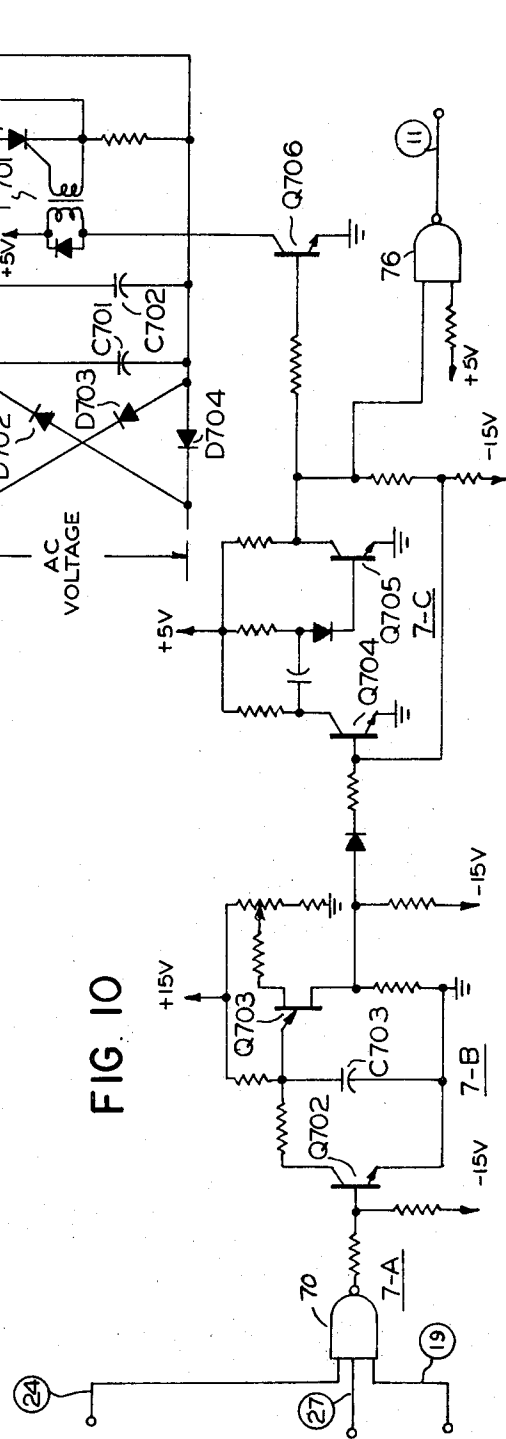
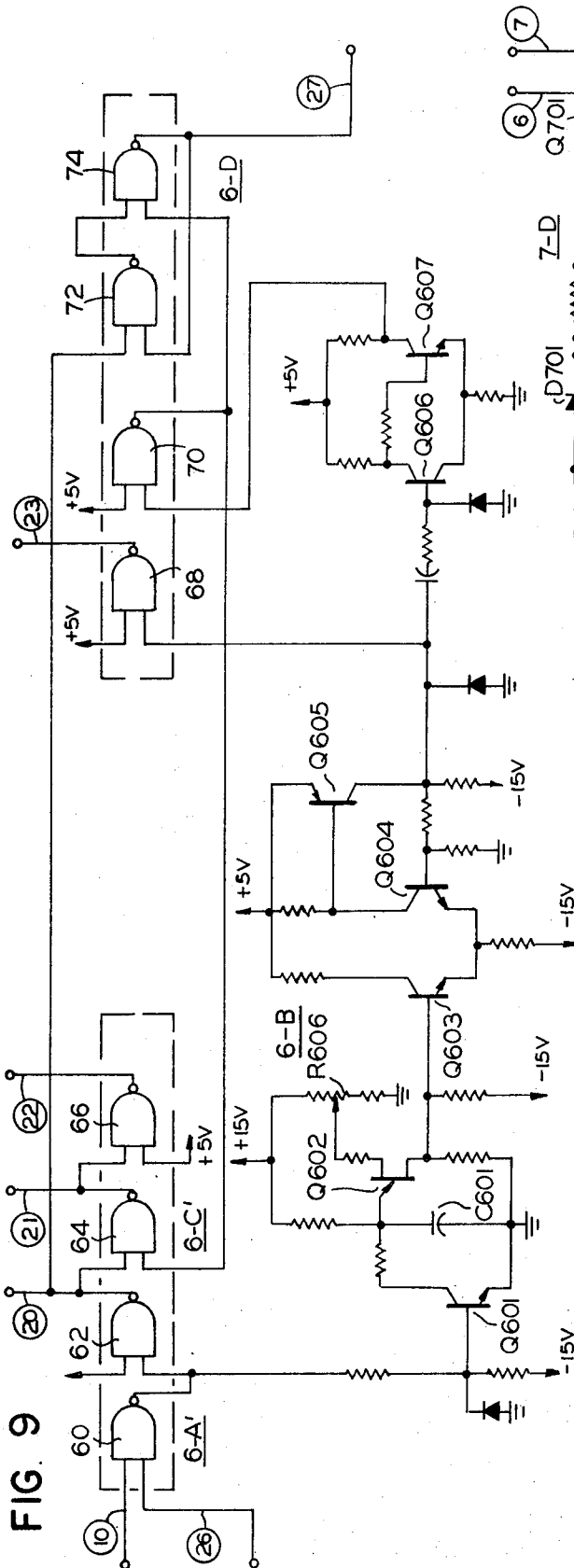


FIG. 10

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FIG. 8

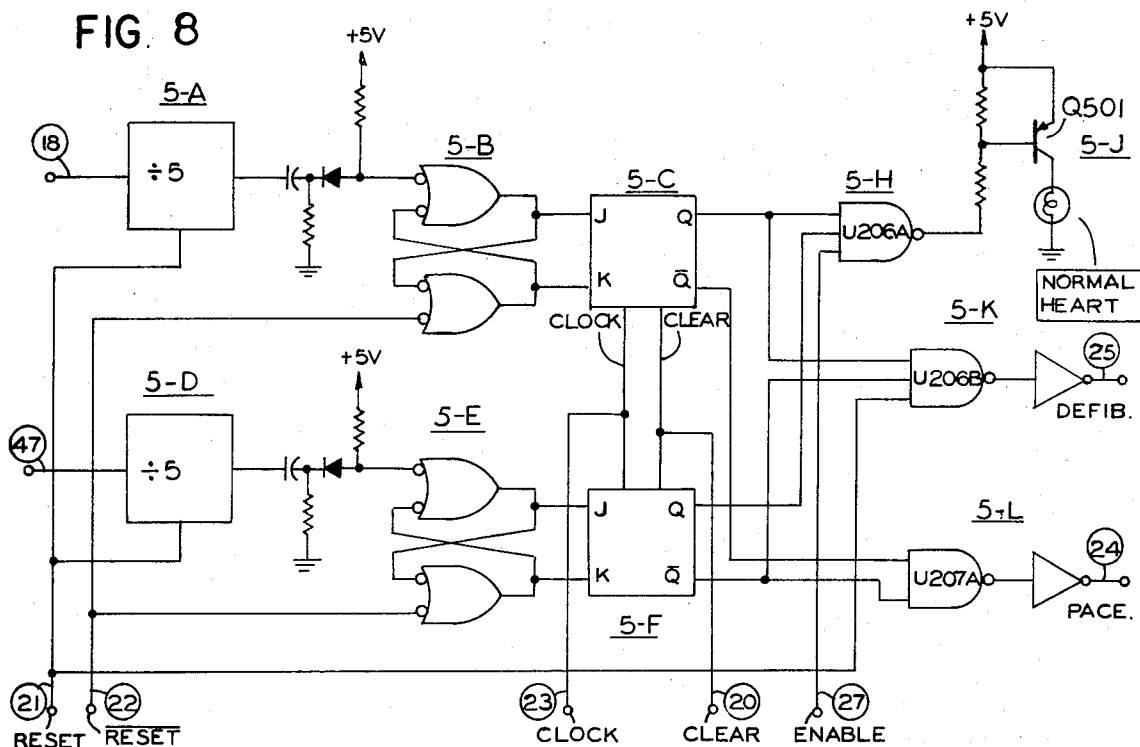
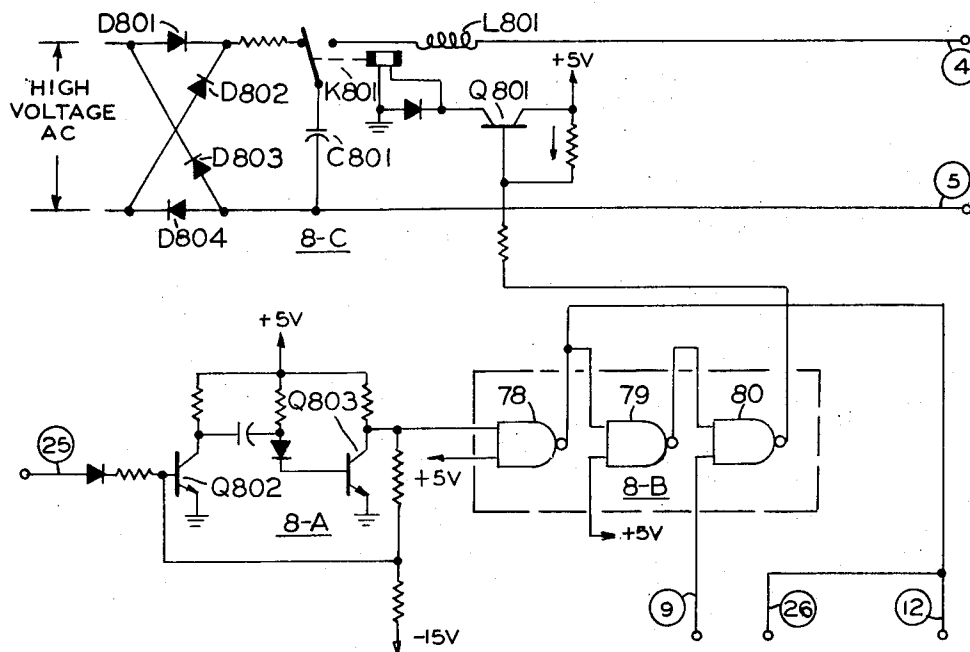


FIG. 11



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CARDIAC RESUSCITATOR**BACKGROUND OF THE INVENTION**

An unusually large number of heart attack victims die each year as a result of delays in providing the intensive care required. A suspected heart attack victim typically must be hospitalized before receiving adequate medical attention. However, a great many patients suffering from a coronary attack never reach the hospital. Cardiac arrests and arrhythmias such as ventricular fibrillation frequently develop within a short time after the onset of the attack, e.g. within the first hour, with fatal results unless remedial steps are taken within minutes. Unless a normal rhythm can be restored to a heart in ventricular fibrillation within minutes, serious brain damage or death will result.

SUMMARY OF THE INVENTION

In accordance with the present invention, a cardiac resuscitator is provided which is compact enough for attachment to a suspected heart attack victim at nearly any location, and which may be operated by comparatively unskilled personnel. The resuscitator may be carried in an ambulance, for example, or may be conveniently stored in an industrial plant, office building, hotel, or the like, for immediate application to the suspected victim of a heart attack. The resuscitator electrode current applicator is applied to the patient, and the apparatus measures the electrical and mechanical output of the patient's heart. If a normal heart beat is detected, an appropriate indication is given. However, if the heart beat is excessively slow or nonexistent indicating substantial cardiac arrest, a pacing pulse is applied to the patient for restoring a normal heart beat. If electrical output is present while mechanical output is absent, indicative of ventricular fibrillation or ventricular tachycardia, an appropriate defibrillating impulse is applied to the patient. The apparatus may remain applied to the patient for detecting possible arrhythmias occurring after the onset of a possible heart attack until adequate hospitalization can be provided.

It is an object of the present invention to provide an improved cardiac resuscitator apparatus which may be applied to a suspected heart attack victim in nearly any location prior to hospitalization.

It is a further object of the present invention to provide an improved cardiac resuscitator apparatus for detecting arrhythmias and providing appropriate corrective action in the absence of a physician.

It is a further object of the present invention to provide an improved cardiac resuscitator apparatus which is substantially portable in nature.

It is a further object of the present invention to provide an improved cardiac resuscitator apparatus which accurately interprets the electrical and mechanical signals from a suspected heart attack victim and applies a corrective impulse in cases of then determined arrhythmias.

It is a further object of the present invention to provide an improved cardiac resuscitator apparatus which is substantially foolproof in operation.

The subject matter which we regard as our invention is particularly pointed out and distinctly claimed in the concluding portion of this specification. The invention, however, both as to organization and method of operation, together with further advantages and objects

thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings wherein like reference characters refer to like elements.

DRAWINGS

FIG. 1 is a perspective view of cardiac resuscitator apparatus according to the present invention, shown applied to a patient;

FIG. 1A is a side view of an electrode current applicator portion of the present resuscitator apparatus;

FIG. 2 illustrates typical electrical signals corresponding to normal cardiac conditions;

FIG. 2A illustrates typical signals corresponding to fibrillation of the patient's heart;

FIG. 3 is a simplified block diagram of cardiac resuscitator apparatus according to the present invention;

FIG. 3A is a more specific block diagram of cardiac resuscitator apparatus according to the present invention;

FIG. 4 is a schematic diagram of interface 1 portion of the apparatus as referenced in the FIG. 3A block diagram;

FIG. 5 is a schematic diagram of the ECG detector 2 portion in the block diagram;

FIG. 6 is a schematic diagram of the ICG detector 3 in the block diagram;

FIG. 7 is a schematic diagram of coincidence detector 4;

FIG. 8 is a schematic diagram of counter 5;

FIG. 9 is a schematic diagram of clock 6;

FIG. 10 is a schematic diagram of pacer 7; and

FIG. 11 is a schematic diagram of the defibrillator 8 portion of the FIG. 3A block diagram.

DETAILED DESCRIPTION

Referring to FIGS. 1 and 1A, illustrating resuscitator apparatus according to the present invention, the apparatus includes a U-shaped electrode current applicator 110 provided with a handle 116 and electrodes ①, ②, ③ and ④ which are individually connected to the control cabinet 112 via cable 114. The applicator is desirably formed of spring plastic or plastic-covered metal electrically insulated from the electrodes. As illustrated in the FIG. 1A, the applicator tends to urge contacts ① and ② toward one another so that when placed on the patient as illustrated in FIG. 1, contacts ①, ②, ③ and ④ make firm contact with the patient's body.

The electrode current applicator is placed over the left shoulder of the patient so that electrodes ① and ② are positioned appropriately above and below the heart, with the patient ordinarily being in a prone position. The patient is desirably stripped to the waist so that such contact may be made with the body or, alternatively, the applicator can be inserted beneath clothing to some extent. Electrode ① is designated the chest electrode, with electrode ② comprising the back electrode. The third electrode ③, termed an indifferent or neutral electrode, makes contact with the patient in the shoulder region. A fourth electrode, ④, located near ①, is called the current source electrode.

The control cabinet 112 suitably contains electronic circuitry for sensing the electrocardiac signal generated by the heart, electronic circuitry for sensing changes in the electrical impedance of the patient's body, and electronic circuitry for making logical decisions based upon the analysis of the electrocardiac (ECG) and impedance (ICG) signals. As hereinafter disclosed, other means may be employed for measuring mechanical activity of the heart in place of circuitry for sensing impedance changes, but the latter is preferred. The control cabinet also contains electronic circuitry for generating defibrillating or pacing pulses in response to the logical decisions and for applying these pulses to the patient electrodes.

FIG. 2 shows typical waveforms which may be present in the cardiac resuscitator when attached to a patient having normal heart operation. Waveform A is the ECG signal as obtained from the patient. The QRS portion of the waveform is associated with contraction of the ventricles and is of great importance in the cardiac resuscitator, while the P and T portions are of no importance in this application. Filtering of waveform A results in waveform B in which the P and T portions are essentially eliminated. Waveform C shows a typical ICG signal which may be obtained by processing a high frequency signal provided at the patient electrodes, and waveform D is a filtered version of waveform C. The voltage peaks of waveform D, which are representative of electrical impedance changes in the patient's chest, occur somewhat later than, but in a definite time relationship with, the peaks of waveform B. The impedance changes are brought about by mechanical movement of the patient's heart, blood flow, or the like. Not shown in FIG. 2 are waveform artifacts which may be present on the ICG waveforms due to patient respiration or externally induced motion. The cardiac resuscitator makes use of the time relationship of the ECG and ICG waveforms to reduce the effects of artifacts by requiring that an ICG pulse, to be valid, must be immediately preceded by an ECG pulse.

FIG. 2A shows waveforms typical of those to be found in the cardiac resuscitator when the patient is in ventricular fibrillation. Waveform A is the ECG waveform as obtained from the patient. Although random in nature, the waveform typically contains fast-rising portions which may be more clearly defined by filtering, to produce waveform B. The same circuitry which converts waveform A to waveform B in FIG. 2 will convert waveform A to waveform B in FIG. 2A. Thus the circuitry is capable of recognizing the presence of electrical activity in a fibrillating heart while rejecting the P and T portions of a normal ECG.

While in fibrillation, the heart muscle fibers contract in a random, uncoordinated manner so that no effective pumping of blood occurs. Thus no significant mechanical changes are present which would bring about body impedance changes, and the ICG pulses are absent. This fact is used to distinguish fibrillation from normal heart operation in the present invention.

The circuitry of the present invention counts the rate of the ECG pulses and the rate of ICG pulses which have been immediately preceded by ECG pulses to determine whether there is substantial electrical activity present and whether there is substantial mechanical activity present.

In order to render the device substantially foolproof, and to prevent improper application of electrical impulses when a proper signal cannot be received, the circuitry according to the present invention is provided with continuity means for determining whether electrodes ①, ②, ③ and ④ are making proper electrical connection with the patient's body. Only after such a determination is the heart rate indication able to bring about the aforementioned pacing or defibrillating impulses. In addition to the inhibition of the device in the absence of proper contact with the patient's body, a poor contact indicator 1-D, suitably comprising a pilot lamp, also warns the operator that proper contact with the patient has not been established. Cabinet 112 additionally includes power supply circuitry and batteries for use in case of portable operation. An off-on switch as well as a pilot lamp indicating the presence of power are suitably also included.

In operation, the electrode current applicator is applied as illustrated in FIG. 1, and the power switch is operated for energizing the apparatus. A normal heart signal may reveal the patient has merely fainted, rather than having suffered a heart attack. However, such a signal may only indicate that arrhythmias have not as yet developed. The device is suitably left applied to the patient until adequate medical attention is provided, and meanwhile the device continuously monitors the heart during the critical period after a possible attack. For example, battery powered apparatus of the present type may be left attached to the patient while he is being transported to a hospital in an ambulance.

The apparatus is relatively compact, and may be transported in an ambulance and easily carried by hand, or conveniently stored in an industrial plant, office building, hotel, or the like, for immediate application to a suspected victim of a heart attack. The apparatus may be operated by comparatively unskilled personnel, without the need of an expert diagnosis, while awaiting conventional medical attention.

FIG. 3 is a simplified block diagram of electronic circuitry according to the present invention. Patient interface 1 collectively includes the various electrodes or other means for receiving information from the patient and applying corrective measures to the patient. Both the ECG detector 2 and mechanical activity detector 3 receive information from the patient, regarding the electrical and mechanical activity of the patient's heart, respectively. The mechanical activity detector suitably comprises an electrical impedance change detector, but may alternatively comprise other means for ascertaining mechanical activity of the heart. For instance, means 3 may alternatively comprise a pressure transducer or microphone for providing a phono-cardiogram signal of heart beat activity, or may comprise ultrasonic or other means for detecting blood flow as understood by those skilled in the art.

The ECG output from detector 2 together with output ΔZ from detector 3 are applied to time coincidence detector 4. The detector 4 supplies an output to logical analyzer 5 only if the output from mechanical activity detector 3 occurs within a predetermined time after an output from ECG detector 2. Logical analyzer 5, which may comprise means for counting pulse inputs within a predetermined period of time, directly receives the ECG output from detector 2, as well as the output from the coincidence detector.

Logical analyzer 5 further comprises means for making a decision on the basis of input supplied thereto, and in consequence thereof delivers an output D, an output P or no output. The possible combinations of ECG activity and ΔZ activity resulting in the D and P outputs are indicated in the truth table accompanying FIG. 3. In each of the ECG and ΔZ columns, a zero is indicative of substantially no activity, or activity below a predetermined minimum threshold level. Thus, if substantially no electrical (ECG) nor mechanical (ΔZ) activity occurs, logical analyzer 5 will provide an output P. If on the other hand, electrical (ECG) activity is present, but no mechanical (ΔZ) activity is present which substantially coincides with electrical activity, logical analyzer 5 will provide an output D. For both, neither an output D nor an input P is supplied.

Output P is applied to pacer 7, which provides a pacing pulse to the patient electrodes in the event that neither electrical nor mechanical activity is detected, i.e. as indicated by the first combination of the truth table. This situation corresponds generally to cardiac arrest. An output D is applied to defibrillator 2 if electrical activity is present, but no mechanical activity or heart beat ensues within a predetermined time immediately following each electrical activity. As a consequence, a defibrillating pulse is applied to the patient. This situation corresponds to the second line of the truth table. The fourth line of the truth table corresponds to normal heart activity, wherein neither a pacing nor defibrillating pulse is needed, while the third combination of mechanical activity without electrical activity will generally not occur.

BLOCK DIAGRAM

FIG. 3A is a more detailed electrical block diagram of the apparatus according to the present invention, principally located within the aforementioned cabinet 112. Referring to FIG. 3A, amplifier 1-B in the interface unit 1 receives the composite electrical signal, comprising a low frequency electrocardiac signal, a high frequency impedance signal, and unwanted noise signals, from the patient electrodes, jointly indicated at 1-A, and applies an amplified version thereof at ⑧ to an ECG detector 2 and to an ICG (impedance cardiogram) detector 3. The latter detects mechanical activity in terms of body impedance. Low pass filter, 2-A, prevents the passage of the high frequency impedance signal to the ECG amplifier. The ECG amplifier and filter, 2-B, amplifies the desired components of the remaining signal while attenuating unwanted signals and noise. In particular, circuit 2-B provides a high degree of rejection of 60 Hz signals which may be present due to the proximity of electrical power lines. The output of circuit 2-B is rectified by rectifier 2-C so that the output of rectifier 2-C comprises pulses of only one polarity. As is hereinafter indicated, disabling claim 2-D operates to inhibit transmission of the ECG signal at times when electrical stimulation is being delivered to the patient.

The output of rectifier 2-C is applied to peak detector 2-F and comparator 2-H. These units comprise detection means of varying sensitivity for detecting or developing peaks from the ECG signal relative to previously stored values of such peaks. The detection means functions over a wide range of input signal amplitude with little or no degradation in performance. Without

such a variable sensitivity feature, the system would be susceptible to noise present on large amplitude signals or would be unable to detect the presence of small amplitude signals, or both. The apparatus also includes means for essentially ignoring the occasional signal of unduly high amplitude, e.g. peaks associated with ectopic beats.

Referring to the drawing, the comparator 2-H provides an output pulse whenever the input signal ⑬ exceeds the reference voltage provided by the peak detector 2-F. The reference voltage represents a proportion of previous signal peaks. The output of the comparator is applied to one-shot multivibrator 2-J which serves to widen the pulse and thus prevent two or more peaks of a QRS complex from producing multiple output pulses at ⑮. One output pulse will be produced at ⑮ for each heart beat. The output at ⑮ is also coupled to inverter 2-K for supplying a resetting signal ⑲ to the pacer as hereinafter more fully described.

The H.F. (high frequency) current generator 3-A supplies an alternating current of constant amplitude at a frequency of approximately 100 KHz to the patient electrode ④. This current produces a high frequency voltage at the patient electrodes, the amplitude of which is a function of the electrical impedance of the patient's body. Thus, the high frequency component of the composite signal at ⑧ is representative of the electrical impedance of the patient's body. The beating of the heart produces a change in the electrical impedance of the body and thus the beating of the heart may be detected by detecting changes in the high frequency component of the signal at ⑧.

The composite electrical signal at ⑧ is applied to H.F. bandpass filter 3-B which rejects all signals except those which contain the ICG (impedance cardiogram) information. The output of 3-B is amplified by H.F. (high frequency) amplifier 3-C which has provision for AGC (automatic gain control). The output of circuit 3-C is applied to the A.M. detector 3-D (and AGC unit) which provides a low frequency output to the ICG amplifier and filter unit 3-E proportional to the changes in electrical impedance occurring in the patient's body. Circuit 3-D also provides an AGC signal to H.F. amplifier 3-C which controls the amplifier gain in such a way as to maintain the average output signal amplitude relatively constant over a wide range of input signal amplitudes. This feature allows the system to operate effectively over a wide range of patient body impedances.

The ICG amplifier and filter 3-E amplifies the desired components of the ICG signal while attenuating unwanted components. In particular, low frequency signals due to patient respiration are attenuated. The output of circuit 3-E is applied to rectifier 3-F which produces output pulses of a single polarity. Disabling clamp 3-H operates to inhibit the transmission of the ICG signal during the delivery of electrical stimulation to the patient, as is hereinafter indicated.

The ICG pulses from circuit 3-H are applied to comparator 3-K which produces an output pulse at ④⑤ which is applied to one input of and-gate 4-B. The second input ④⑥ to and-gate 4-B is provided by one-shot multivibrator 4-A, and is an extended version of the ECG detector output at ⑮. Thus, a pulse is present at ④⑦ if an output pulse from the ICG detector ④⑤ occurs at the time of, or slightly later than, an output from the ECG detector ⑮.

Counter 5-A counts the output pulses of the ECG detector, and after receiving a predetermined number of pulses produces an output which causes flip-flop 5-B to change state. Thus, flip-flop 5-B serves as a temporary storage element, indicating whether or not a predetermined number of pulses have been received at the input of counter 5-A. This information is transferred to J-K flip-flop 5-C upon receipt of a clock pulse. After completion of the clock pulse, a reset pulse is applied to counter 5-A and flip-flop 5-B to reset 5-A and 5-B to the zero state and thus initiate a new counting period. A clear input is provided at J-K flip-flop 5-C to reset flip-flop 5-C to the zero state when power is first applied to the resuscitator or when a defibrillating pulse is applied to the patient, as is hereinafter indicated.

Counter 5-D, flip-flop 5-E and J-K flip-flop 5-F operate in a manner similar to that described above for counter 5-A, flip-flop 5-B and J-K flip-flop 5-C. The input to counter 5-D, however, is the output of the coincidence detector unit 4.

Clock pulses, followed immediately by reset pulses, are supplied at regular intervals. Therefore, the logic levels present at the Q and Q-not outputs of 5-C and 5-F are representative of the number of pulses received at 18 and at 47 during the previous interval between clock pulses.

The interval between clock pulses is desirably 10 seconds, and the dividing ratio of each counter is desirably five to one. Thus a high level at the Q output of circuit 5-C indicates an average ECG rate of at least five pulses per 10 seconds or 30 per minute. Similarly, a high level at the Q output of circuit 5-F indicates that an average rate of at least 30 per minute was attained at the output of the coincidence detector 4 during the previous clock period. The Q outputs of 5-C and 5-F are connected to and-gate 5-H which causes the normal heart indicator to be actuated when the two Q outputs are high and the enable signal 27 is also high. The enable signal is high after the completion of at least one clock period as hereinafter indicated.

The Q output of circuit 5-C and the Q-not output of circuit 5-F are connected to and-gate 5-K. A third input to and-gate 5-K is provided by the reset pulse. Thus, if during a certain clock period at least five ECG pulses are detected but fewer than five ICG pulses which are correlatable to ECG pulses are detected, the reset pulse which occurs at the end of the clock period causes an output pulse from 5-K which, in turn, actuates the defibrillator 8 by an input at 25.

And-gate 5-L receives the Q-not outputs of flip-flops 5-C and 5-F. In the event that fewer than five pulses are present at 18 and fewer than five pulses are present at 47 during a clock period, the output of and-gate 5-L will be high after the completion of the clock period. Therefore the pacer 7 will be actuated by an input at 24.

Clock 6 includes a clock pulse generator 6-B providing pulse outputs at 10-second intervals at 23. If a signal is present at either 26, indicating defibrillator operation, or at 10 indicating faulty interface operation or initial start conditions, the clock pulse generator 6-B is reset from or-gate 6-A. At the same time, the J-K flip-flops 5-C and 5-F are cleared via lead 20, and a reset pulse is provided at 21, 22, via or-gate 6-C. Likewise, flip-flop 6-D is set. After being initially

reset from Or-gate 6-A, clock pulse generator 6-B starts providing clock pulses at 22, at 10-second intervals. At the end of each such clock pulse, a reset is provided or-gate 6-C and flip-flop 6-D. The reset via leads 21 and 22 reset the counters 5-A and 5-D as well as flip-flops 5-B and 5-E for another cycle. At the end of such cycle, the clock pulse at 23 causes the J-K flip-flops to register the condition of flip-flops 5-B and 5-E as hereinbefore described. Flip-flop 6-D provides an output at 27 effective for enabling the pacer and normal heart indicator only after a suitable period of time has elapsed for counter 5 actually to count the heart rate. Otherwise, pacer 7 could be falsely actuated before proper counter operation. Operation of flip-flop 6-D will be further described hereinafter.

In pacer 7, pacemaker timer 7-B generates a series of timing pulses with a period of approximately 0.85 seconds, whenever the output of and-gate 7-A is high. The output of and-gate 7-A is high (1) when the circuitry has operated at least 10 seconds as indicated by a signal at 27, (2) when ECG detector 2 does not detect a present heart beat, and (3) when counter 5 indicates a heart rate of below 30 beats a minute. The output of timer 7-B triggers one-shot multivibrator 7-C which operates pacer pulse generator 7-D. The latter delivers a pacing pulse to the patient electrodes via leads 6, 7, and switching diodes 1-F. The switching diodes 1-F essentially disconnect the pacer from the patient electrodes when the pacer produces no output. During each pacemaker pulse, output 11 of one-shot multivibrator 7-C operates or-gates 2-E and 3-J for disabling the signal paths. If, between pacer pulses, a heart beat is detected, reset signal 19 will reset pacer timer 7-B via and-gate 7-A, restarting the timing of the 0.85 second interval. Thus, the pacer operates on a demand basis and produces no output when spontaneous heart beats are present.

When defibrillator 8 receives an input at 25, one-shot multivibrator 8-A is set in a second state for approximately 100 milliseconds. Output 12 disables the signal paths, and output 26 resets clock 6 as well as counter 5. The third output of multivibrator 8-A operates defibrillator generator 8-C through and-gate 8-B if input 9 is also present. A defibrillating pulse, a high energy electrical pulse, is applied through leads 4, 5, and switching diodes 1-E, to patient electrodes 1-A. Input 9 is present if the patient electrodes make proper contact and certain other conditions are met as hereinafter more fully described. The switching diodes essentially disconnect the defibrillator when the same is not in use. It is observed the defibrillator operation resets clock 6 and counter 5 for successive operations. If, after a defibrillating pulse is applied to the patient, fibrillation or tachycardia persists, defibrillator operation will again be initiated in the same manner as hereinbefore described.

Interface 1 further includes continuity checker 1-C, which determines if the patient electrodes are in proper electrical contact with the patient's body. If not, a poor contact indicator 1-D, suitably comprising a pilot lamp, is energized, and defibrillator and-gate 8-B is disabled via and-gate 1-K and lead 9, thus preventing defibrillator operation and possible patient burns in case of poor electrical contact. Also in such case, clock 6 is reset via lead 10 and inverting gate 1-L, and flip-

flop 6-D is set to prevent operation of the pacer via output 27. When the resuscitator is first started, start circuit 1-H disables and-gate 1-K, thereby disabling defibrillator 8, resetting clock 6 and disabling pacer 7. Pacer 7 is operable when flip-flop 6-D is reset from clock pulse 6-B. The output from the start circuit 1-H is of short duration, and the main purpose thereof is the disabling of the pacer until the counter has time to count.

The individual units of the resuscitator will now be considered in greater detail.

INTERFACE

Referring to FIG. 4, illustrating interface unit 1 in greater detail, transistors Q101 and Q102 provide DC current sources for patient electrodes 1 and 2 to ground via indifferent or neutral patient electrode 3. The DC voltage at electrodes 1 and 2 depends upon the resistance between each electrode and ground, and therefore, if either electrode 1 or 2 is in poor contact with the patient, a comparatively high DC voltage will occur at that electrode. Patient electrode 1 is coupled to the input and an operational amplifier U101, while the patient electrode 2 is coupled to the input of an operational amplifier U102, with diodes D105, D106, D107 and D108 protecting the amplifiers during the application of a pacing or defibrillating pulse. If the voltage at patient electrode 1 is less than about +0.15 volts, then the output of U101 will be about +15 volts, and the voltage at the junction of D109 and D110 will be clamped to about +5.6 volts. However, if the voltage at patient electrode 1 exceeds +0.15 volts, the voltage at the output of U101 will be about -15 volts, and the voltage at the junction of diodes D109 and D110 will be clamped at about -0.6 volts. The output of amplifier U102 is similarly controlled by the voltage at patient electrode 2.

The output of amplifier U107 is controlled by the amplitude of the high frequency AC voltage which exists at electrode 41 due to current supplied at 40. The AC voltage is rectified by diode D142 so that the voltage at the minus input of amplifier U107 is a DC voltage representing the peak value of the AC voltage at 41. Thus if electrode 41 is in poor contact with the patient, the voltage at the minus input of amplifier U107 is relatively high, causing the voltage at the junction of diodes D143 and D144 to be about -0.6 volts.

Nand-gate 30 receives the outputs of the three amplifiers U101, U102 and U107 and drives nand-gate 32, here used as an inverter, which is coupled to transistor Q103 having a poor contact indicator lamp in its collector circuit. Thus, if the output of any of the three amplifiers U101, U102 or U107 drops, indicating poor patient electrode contact, lamp 1-D will light.

Likewise, nand-gate 32 drives nand-gate 34 in conjunction with start circuit 1-H comprising transistor Q104. When power is first turned on, transistor Q104 is momentarily turned on. Capacitor C101 charges so that transistor Q104 cuts off, thereby providing a high input to nand-gate 34. Assuming good contact is made by the patient electrodes, and the power has been applied for a short period of time, both inputs to nand-gate 34 will be up, and the output of nand-gate 36, driven by nand-gate 34, will also be up. The output of nand-gate 36 is applied to leads 9 and 10. Since

nand-gates are employed throughout, no inverting gate is employed in lead 10, nor is an inverting gate required in the output of the start circuit. Both outputs 9 and 10 will be energized so long as continuity is present to the patient's body from the patient electrodes, and so long as power has been applied to the apparatus for at least a short time. Then, the clock and defibrillator are operable.

Switching diodes 1-E and 1-F, from the defibrillator and pacer, respectively, couple these units to the patient electrodes, and essentially decouple these units when neither provides an output pulse. Also, the respective diodes prevent application of a defibrillator pulse to the pacer or a pacer pulse to the defibrillator.

Operational amplifiers U104 and U105 receive signal outputs from patient electrodes 1 and 2, and diodes D116 and D117, D118 and D119 limit the voltage excursion of the inputs of these amplifiers during the occurrence of defibrillator or pacer pulses. Each of the amplifiers U104 and U105 is connected as a voltage follower, so the outputs thereof are the same as those from patient electrodes 1 and 2, respectively, except the DC component has been removed, and the impedance level is greatly reduced. The outputs of amplifiers U104 and U105 are applied as inputs to differential amplifier U106 which has a voltage gain of approximately 10 as determined in part by feed back resistor R135. The output of amplifier U106 at lead 8 is therefore an amplified version of the signal existing between patient electrodes 1 and 2 except that any DC component has been removed.

ECG DETECTOR

Referring to FIG. 5 further illustrating the aforementioned ECG detector 2, a low pass filter 2-A comprises inductors L201 and L202 and capacitors C201 and C202. The cutoff frequency of filter 2-A is such that the 100KHz component of the signal at 8 is severely attenuated, while the low frequency ECG signal is allowed to pass. Capacitor C203 and resistor R201 operate as a differentiating network so the signal at the positive input of amplifier U201 is representative of the rate of change of the ECG signal. Thus the very low frequency components of the signal, including baseline shift and the P and T portions of the normal electrocardiogram, are effectively reduced.

Amplifiers U201 and U202, together with twin-tee filter 50 and other associated components, operate as an active filter which rejects any 60 hertz component which may appear upon the ECG signal due to proximity of electrical power lines or apparatus, while providing amplification of other frequency components. Thus the signal at the base of transistor Q201 is a highly refined version of the signal at 8, with all undesirable components reduced to small amplitude. Rectifier 2-C comprises transistor Q201 operating as a phase inverter so that the signals at the emitter and collector terminals of Q201 are of equal magnitude, but of opposite polarity, the magnitude being nearly equal to the magnitude at the base terminal. The collector of Q201 is coupled through capacitor C208 to the base of transistor Q202 and to one end of resistor R211, which has its opposite end connected to ground. Similarly, the emitter of transistor Q201 is coupled through capacitor C209 to the base of transistor Q203 and to one end of resistor

R214 which has its opposite end connected to ground. The emitter terminals of transistors Q202 and Q203 are connected together and to one end of resistor R215, the other end of which is grounded.

A positive signal at the base of transistor Q201 produces a positive signal at the base of transistor Q203 and a positive signal at the common emitter terminals of transistors Q202 and Q203. A negative signal at the base of transistor Q201 causes a positive signal at the base of transistor Q202 and a positive signal at the common emitter terminals of transistors Q202 and Q203. However, positive signals at the base terminals of transistors Q202 and Q203, which are smaller in amplitude than 0.6 volts, will be severely attenuated because of the nonlinear characteristics of the base-emitter junctions of transistors Q202 and Q203. Therefore, the signal at the common emitter terminal of transistors Q202 and Q203 is a series of positive pulses which occur whenever the signal at the base of transistor Q201 exceeds 0.6 volts in either the positive or negative direction, and which correspond to the fast-rising portions of the ECG component of the signal at (8).

The common emitter terminal of transistors Q202 and Q203 is coupled through resistor R216 to the positive input of amplifier U204 and to the collector of transistor Q204, forming a part of disabling clamp circuit 2-D. The base of transistor Q204 is coupled to the output of gate 2-E employed for causing transistor Q204 to conduct and clamp the signal at its collector terminal to ground whenever either of the inputs, (11) and (12), are low. Clamping occurs during the delivery of defibrillating or pacing pulses to the patient.

Assuming that the disabling clamp circuit 2-D is inactive, the series of positive pulses present at the common emitter terminals of transistors Q202 and Q203 is applied to the positive input of amplifier U204, to the anode of diode D201 and to the emitter of transistor Q207. A positive pulse causes diode D201 to conduct and to charge capacitor C210 to the peak value of the pulse (less the diode voltage). Resistor R230 allows capacitor C210 to discharge at a rate which is slow in comparison with the time between normal heart beats. Therefore capacitor C210 acts as a peak storage capacitor and discharges only slightly between input pulses.

Amplifier U205 is connected as a typical voltage follower except that diode D202 is connected between the output and the inverting input. This diode compensates for the voltage drop which occurs across diode D201 while capacitor C210 is charging, in order to make the output voltage of amplifier U205 more nearly equal to the peak value of the input pulse.

The output of amplifier U205 is applied to amplifier U206 through a delay network comprising resistor R234 and capacitor C213. Thus the input to amplifier U206 does not immediately respond to a change in the output of amplifier U205. Amplifier U206 is connected in a noninverting configuration with a gain of two, so that the output of amplifier U206 is a voltage approximately equal to twice the stored value on capacitor C210. The output of amplifier U206 is coupled to the base of transistor Q207 which operates as a limiter inasmuch as its emitter is coupled to the input line of the peak detector 2-F, i.e. at the anode of diode D201.

Thus, if the input becomes more positive than twice the previously stored value, transistor Q207 conducts, preventing an input pulse of large amplitude but short duration from charging C210 to a voltage more positive than twice the previously stored peak value. This limiting feature prevents a single large pulse, whether originating in the patient as in the case of an ectopic beat, or induced into the patient from an external source, from raising the stored peak value to some value which is entirely unrepresentative of the average signal amplitude. The limiting feature particularly prevents the large voltage peaks associated with ectopic beats from decreasing the sensitivity of the circuit to the point where the next normal QRS heart signal complex would be undetected.

The output of amplifier U205 is also coupled to a divider comprising resistors R232 and R233 which allows approximately one-third of the stored peak value to be coupled to the negative input of comparator amplifier U204 as a reference voltage. Capacitor C211 is connected in shunt with resistor R233 to cause a delay in any change in the reference voltage, so the reference cannot follow the input signal.

Since the reference voltage for the comparator varies with the peak amplitude of the signal, the system is of variable sensitivity, rendering it operable with respect to cardiac signals of different average amplitude values. It is noted that the one-third reference value allows detection of a normal signal after an ectopic beat, the storage of which is restricted to double amplitude.

When an input pulse at the positive input of amplifier U204 exceeds the reference voltage at its negative input, the output of amplifier U204 goes positive, causing a positive voltage spike to be coupled to one-shot multivibrator 2-J, triggering 2-J, and causing a positive pulse of about 5 volts in amplitude and 100 milliseconds in width to occur at (18). During the width of the output pulse at (18), the one-shot multivibrator 2-J cannot respond to further inputs. This prevents the QRS complex of the normal electrocardiac signal, which may comprise several peaks closely adjacent in time, from being registered as multiple pulses.

Nand-gate 2-K, here connected as an inverter, provides an output (19) for resetting the pacer.

ICG DETECTOR

Referring to FIG. 6, further illustrating the ICG detector, high frequency current generator 3-A includes 100 KHz crystal oscillator U301 which is coupled through transformer T301 to high frequency amplifier U302 which also has an automatic gain control (AGC) input, numbered 5. The output of amplifier U302 is coupled through tuned transformer T302 to capacitors C303 and C304 and to the anode of diode D301, the signal at this junction being a sinusoidal voltage symmetrical with respect to ground. The cathode of D301 is coupled to the base of transistor Q301, the emitter of which is connected to the positive input of amplifier U303 and to the parallel combination of resistor R306 and capacitor C305. The time constant of circuit R306, C305 is long with respect to the period of the sinusoidal signal at the anode of diode D301, so that capacitor C305 is maintained at a voltage which is representative of the peak value of the sine wave applied to capacitors C303 and C304.

Amplifier U303 is connected in a noninverting configuration having a feedback resistor R307 connected between output and inverting input, and resistor R308 connected between the inverting input and a +5 volt supply. The output of amplifier U303 is connected to the AGC input of high frequency amplifier U302. Thus a closed-loop feedback system is established which maintains the peak amplitude of the 100 KHz signal, applied to capacitors C303 and C304, at approximately 5 volts.

Capacitor C303 couples the 100 KHz signal to the base of transistor Q302 which is biased so that the base is approximately 14.4 volts DC. The emitter of transistor Q302 is coupled through resistor R302 to the +15 volt supply. Thus, when the sinusoidal signal swings positive, transistor Q302 is cut off, and when the signal swings negative, a half sine wave of current flows to output terminal (40). Similarly capacitor C304 couples the 100 KHz signal to transistor Q303, which conducts a half sine wave of current to the output terminal when the signal at the base swings positive. Thus, a full sine wave of current is supplied at the output terminal (40), the magnitude of the current being approximately 5 milliamperes peak, and independent of load impedance for impedances less than about 1,000 ohms. The output current is coupled to the patient electrodes in order to detect changes in the electrical impedance of the body. A constant current output is required in order to avoid artifacts in the impedance cardiogram (ICG) waveform due to changes in impedance at the electrode-patient interface.

Also, in order to avoid sensing changes in the electrode-patient interface impedance, separate electrode means are used for supplying the constant current and for sensing the voltage which is representative of the body impedance, as hereinbefore described.

The composite signal obtained from the patient, including the 100 KHz ICG signal, the low frequency ECG signal, and superimposed noise, is applied at (8) in FIG. 5. Bandpass filter 3-B, comprising tuned transformer T303, rejects all components of the signal except the 100 KHz component, which is an amplitude modulated signal containing the ICG information. The 100 KHz signal is amplified by high frequency amplifier U304 which has provision for AGC at its terminal 5. The output of amplifier U304 is coupled through tuned transformer T304 to the base of transistor Q305 which has its emitter terminal connected to capacitor C317. The base-emitter junction of transistor Q305 serves as a rectifier, and in conjunction with capacitor C317, as an amplitude modulation detector. Capacitor C317 filters out the 100 KHz component of the signal and the resultant voltage applied to capacitor C320 is therefore a low frequency signal which is proportional to the impedance of the patient's body between electrode (41) and electrodes (1), (2).

The collector terminal of Q305 is connected to ground through resistor R314 in parallel with capacitor C315. The voltage at the collector is an inverted version of the ICG signal at the emitter. This signal is coupled through a filter network comprising resistor R313 and capacitor C316 to the base of transistor Q304. The time constant of the R313, C316 combination is long with respect to the period of a normal heart beat, so that the voltage at the base of transistor Q304 is essen-

tially a DC voltage representative of the average amplitude of the 100 KHz signal at the output of amplifier U304. Transistor Q304 serves as an emitter follower to couple this DC voltage to the AGC input of amplifier U304, thus providing a closed-loop system to maintain the output of amplifier U304 relatively constant. Thus the system is operable over a wide range of body impedance levels with a relatively constant amplitude of ICG signal being obtained.

The low frequency signal at the emitter of Q305 is coupled through the differentiating circuit comprising capacitor C320 and resistor R320 to the inverting input of amplifier U305 which is connected for conventional operation as an inverting amplifier. Capacitor C321 connected in shunt with feedback resistor R321 serves to eliminate any residual high frequency component present on the signal. The signal at the output of amplifier U305 is proportional to the rate of change of the patient's body impedance due to the differentiating action of components C320 and R320.

The output of amplifier U305 is applied to rectifier circuit 3-F which operates in a manner similar to that hereinbefore described in reference to rectifier 2-C. Thus the signal applied at the noninverting input of amplifier U306 is a series of positive pulses, each pulse corresponding to a rapid change in the electrical impedance of the patient's body.

Disabling clamp 3-H, comprising transistor Q309 clamps the signal to ground during times when defibrillating or pacing pulses are being generated. Amplifier U306 here operates as a comparator (3-K) causing a positive rectangular pulse to be applied at output terminal (45) whenever the signal at the noninverting input exceeds the reference voltage supplied by the voltage reference 3-L comprising resistors R333 and R334 and capacitor C324.

Thus a positive rectangular pulse occurs at (45) whenever a rapid change in the patient's body impedance occurs.

COINCIDENCE DETECTOR

Referring to FIG. 7, coincidence detector 4 comprises one-shot multivibrator 4-A and an and-gate 4-B. Rectangular pulses from the ECG detector are applied at input (18) and are differentiated by capacitor C401 and resistor R401. The positive spikes generated at the leading edge of the input pulses trigger the multivibrator, comprising transistors Q401 and Q402, into its quasi-stable state, causing a positive rectangular pulse, approximately 200 milliseconds in width, to be generated at the collector of transistor Q402. The collector of transistor Q402 is connected to one input of nand-gate U401A, the second input of U401A being connected to the output of the ICG detector at (45). The output of gate U401A is connected to the inputs of nand-gate U401B, here employed as an inverter. Thus the output (47) is low except when a high level signal is received at (45) during the first 200 milliseconds after the receipt of a high level input at (18). In essence, this means that in order for an output of the ICG detector to be considered valid, it must be immediately preceded by an output from the ECG detector. This feature reduces the probability that artifacts in the ICG signal can cause a false diagnosis of the patient's condition.

COUNTER

Referring to FIG. 8, counter 5-A receives input pulse at 18 from the ECG detector and after receiving five pulses produces a negative-going voltage step which is differentiated and applied to flip-flop 5-B. Thus, after five pulses are applied at 18, the J input of J-K flip-flop 5-C is high, while the K input is low.

Clock pulses are supplied at 23 at intervals of approximately 10 seconds, the width of the clock pulse being small with respect to the 10-second interval. The clock pulse causes the information present at the J and K inputs of flip-flop 5-C to be stored in such flip-flop and to be registered at the Q and Q-not outputs thereof. Thus, if J is low and K is high at the time of the clock pulse, then Q will be low and Q-not high after the end of the clock pulse. J-K flip-flops are well known to those skilled in the art and need not be described in detail.

Immediately succeeding each clock pulse, high level and low level reset pulses are provided at 21 and 22, respectively, resetting counter 5-A and flip-flop 5-B to their zero states in preparation for a new period of counting.

Clear pulses are supplied at 20 to set the J-K flip-flop 5-C to its zero state under certain conditions hereinafter indicated.

Counter 5-D, flip-flop 5-E and J-K flip-flop 5-F operate in a similar manner to count input pulses presented at 47 during the clock interval and to register the result at the Q and Q-not outputs of flip-flop 5-F. Thus, at any given time, the states of the outputs of flip-flops 5-C and 5-F are representative of the number of pulses received at 18 and 47, respectively during the previous interval between clock pulses. A high level at the Q outputs of both flip-flops 5-C and 5-F indicates that the patient's heart has both significant electrical activity and significant mechanical activity. The two Q outputs are connected to two inputs of nand-gate 5-H. A third input to gate 5-H is supplied at 27 to enable 5-H only after a full clock period has elapsed for counting. Thus the output of gate 5-H is low when significant electrical and mechanical activity is present in the patient and after sufficient time has elapsed for counting, causing the normal heart indicator 5-J including transistor Q501 to be energized. If the Q output of flip-flop 5-C is high while the Q-not output of flip-flop 5-F is high, indicating significant electrical activity but no significant mechanical activity by the patient's heart, i.e. a fibrillation condition, the reset pulse 21 immediately following the clock period in which such determination was made causes the output of nand-gate U206B to be low and the signal at 25 to be high, triggering the defibrillator. If predetermined electrical or mechanical activity of the heart is not present, the two Q-not outputs applied to nand-gate U207A will be high, causing the signal at 24 to be high, activating the pacemaker.

CLOCK

Referring to FIG. 9, gate portions 6-A' and 6-C' perform the functions of or-gates 6-A and 6-C on the block diagram. This structure is conveniently provided as a four-nand-gate integrated circuit including nand-gates 60, 62, 64, and 66, which are consecutively connected. Nand-gate 60 receives inputs 10 from the in-

terface circuit, and 26 from the defibrillator circuit. Providing both these inputs are up, the output of nand-gate 60 is low, and the clock pulse generator 6-B can operate in a normal fashion.

In clock pulse generator 6-B, transistor Q601 receives the output of nand-gate 60 at its base, and its collector-emitter terminals are coupled across capacitor C601 coupled between the emitter and lower base terminals of unijunction transistor Q602. The circuit normally operates as a relaxation oscillator whereby the unijunction transistor periodically discharges capacitor C601 to supply a pulse output at its lower base. If either input 10 or 26 should drop, transistor Q601 would be rendered conducting and short capacitor C601 causing immediate discharge thereof. At the conclusion of such input at 10 or 26, the operation of the oscillator including unijunction transistor Q602 would be restarted.

The normal period of the oscillator is here adjusted to be 10 seconds by means of potentiometer R606, and at the end of conduction of transistor Q601, a new 10-second interval is started. Thus, at the conclusion of a defibrillator pulse, or the conclusion of a period of time during starting, or a period of time when the electrodes are improperly connected to the patient, a new 10-second interval will start.

The output of unijunction transistor Q602 is connected via a Schmitt trigger circuit, comprising transistors Q603, Q604, and Q605, to an input of nand-gate 68, the output of which provides the clock pulse on lead 23. The output of the Schmitt trigger circuit comprising transistors Q603, Q604, and Q605 is also coupled to a second Schmitt trigger circuit comprising transistor Q606 and Q607. The output of the latter trigger circuit is applied to nand-gate 70 and the output of nand-gate 70 is connected to an input of nand-gate 74 which forms flip-flop 6-D together with nand-gate 72. The output of nand-gate 74 is connected to one input of nand-gate 72, and vice versa. Another input of nand-gate 72 is derived from the output of nand-gate 62. As thus appears, flip-flop 6-D will be set upon the operation of nand-gates 60 and 62, and will then be reset upon the occurrence of a clock pulse. The signal at 27 from nand-gate 74 enables the pacemaker at the first clock pulse after power has been applied for a short period, or after any difficulty with respect to continuity has been rectified, or after the occurrence of a defibrillator pulse. Thus, the pacer is disabled until a proper count can be made.

The output of nand-gate 70 drops at the end of a clock pulse, and the output of nand-gate 70 is also applied to nand-gate 64 in conjunction with the output of nand-gate 62. Thus, assuming both signals 10 and 26 are up, a reset is provided by nand-gate 64 on lead 21 at the conclusion of a clock pulse. This signal is inverted by nand-gate 66 to provide the reset signal on lead 22.

It is noted a clear signal is provided on lead 20 at the same time that either input 10 or 26 lowers, and the J-K flip-flops in the counter circuit will be cleared at such time.

PACER

In FIG. 10, nand-gate 70 receives input 24 from the counter, enabling signal 27 from the clock cir-

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cuit, and reset signal 19 from the ECG detector. Input 24 from the counter is the one indicating a slow heart beat and the desirability of applying pacing pulses. Enabling signal 27 indicates that the interface is operating properly and that sufficient time has elapsed for the counter to make a proper count after application of power or application of a defibrillator pulse. The output of gate 7-A, which here comprises a nand-gate, is applied to transistor Q702, and assuming all three of the aforementioned inputs, 19, 24, and 27 are present, the input to transistor Q702 will be low. Therefore, the pacemaker 7-B is operable.

Pacer timer 7-B comprises a unijunction transistor Q703 having a capacitor C703 coupled between its emitter terminal and lower base. This circuit is a relaxation oscillator similar to that described in connection with the clock circuit, except in the present instance the relaxation oscillator suitably has a period of approximately 0.85 seconds. The output of timer 7-B is applied to one-shot multivibrator 7-C including transistors Q704 and Q705. The output at the collector of transistor Q705 is a series of positive pulses, each pulse having a duration of about 100 milliseconds, and this output is connected to the input of nand-gate 76. Nand-gate 76 provides signal 11 applied to the ECG detector and ICG detector for disabling the signal channels when a pacer pulse is being generated. It should be noted that the duration of the output pulse at 11 is considerably longer than the duration of the pacing pulse applied to the patient. This allows time for the amplifier 1-B and other signal circuits to recover from the overdriven condition imposed by the pacing pulse.

The output of one-shot multivibrator circuit 7-C is also applied via transistor Q706 as the input of pulse transformer T701, the secondary of which is coupled to provide the input of thyristor Q701. AC voltage from a power supply is normally applied across a bridge circuit comprising diodes D701, D702, D703 and D704 connected in DC charging relationship to capacitors C701 and C702, with thyristor Q701 being interposed between the positive end of capacitor C702 and connection 6 coupled to the patient electrodes. Thus when transistor Q706 turns on, current flow rapidly increases through the primary winding of pulse transformer T701, and a resultant secondary pulse triggers thyristor Q701 into a conducting state. When thyristor Q701 is turned on, capacitor C702 discharges through diodes 1-F and through the patient's body. As capacitor C702 discharges, the current through thyristor Q701 decreases until the minimum holding current is reached. At this point, thyristor Q701 turns off, and capacitor C702 begins recharging.

If, during the operation of the pacer, spontaneous heart beats occur in the patient, the spontaneous beats are detected by the ECG detector, and a low level pulse 19 is applied to one input of gate 7-A resetting the pacer timer. Another pacing pulse will occur after 0.85 seconds unless another spontaneous beat takes place. Thus, the pacer is of the demand type and produces pacing pulses only in the absence of spontaneous heart beats in the patient.

DEFIBRILLATOR

Referring to FIG. 11, illustrating the defibrillator 8, an input is received at 25 from counter 5 when sig-

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nificant electrical activity in the absence of significant mechanical activity has been detected, indicative of ventricular fibrillation or ventricular tachycardia. The input pulse operates one-shot multivibrator 8-A comprising transistors Q802 and Q803, which in turn applies a lengthened output to gate 8-B, here comprising nand-gates 78, 79 and 80 consecutively connected. The output of nand-gate 78 is connected to leads 26 and 12 which, respectively, disable and recycle the clock, and clamp the input signal channels during the defibrillator pulse. The output of the one-shot multivibrator 8-A is longer than the duration of the defibrillating pulse applied to the patient to allow time for amplifier and other circuits to recover. Signal 9, comprising a disabling input from the interface circuit, is also connected to nand-gate 80, and when this signal drops, indicating improper connection of the patient electrodes or the start of operation, the defibrillator is disabled.

The output of nand-gate 80 is connected to the base of transistor Q801 which has the operating coil of relay K801 serially connected in its collector circuit. The contacts of relay K801 normally connect capacitor C801 to the output of a bridge circuit comprising diodes D801, D802, D803 and D804, receiving a high voltage alternating current input. However, when transistor Q801 conducts, relay K801 connects capacitor C801, theretofore charged through the aforementioned bridge circuit, to leads 4 and 5 via inductance L801. Leads 4 and 5 are coupled through diodes 1-E to the patient electrodes, as hereinbefore mentioned. Capacitor C801, initially charged to a high voltage from the power supply, applies this high voltage across a circuit comprising inductance L801, the switching diodes 1-E, and the body resistance of the patient. Inductance L801 controls the resulting current. At the conclusion of the defibrillation pulse, clock 6 is recycled as the output at 26 rises. Thus, the clock circuit begins a new 10-second period, and signals are allowed to pass through the disabling clamp 2-B so that monitoring of the electrocardiac signal is resumed.

OPERATION

In general operation, the device is applied to the suspected heart attack patient as illustrated in FIG. 1, with the patient electrodes in direct contact with his body. Thus, patient electrodes 1 and 41 are positioned in good contact with the patient's chest, and patient electrodes 2 and 3 are positioned in direct contact with the patient's back. The device is turned on to operate the apparatus power supplies, and if proper contact is not made with the patient, indicator 1-D will light, and moreover, operation of the instrument is prevented. Normally, counter 5 will cycle under the control of clock 6 for the first 10-second period, and if a normal condition exists, normal heart indicator 5-J will light. However, if a cardiac arrest has taken place, or the heart rate is extremely low, pacer 7 will operate through switching diodes 1-F, and the patient electrodes, to provide a pacing pulse to the patient as long as required. Should a normal heart beat resume without the aid of the pacer, the pacer will be disabled via input 19 of and-gate 7-A. If, on the other hand, electrical activity is present, while mechanical activity is absent, indicating ventricular fibrillation, defibrillator 8 will be energized to provide a defibrillating pulse to the patient

via switching diodes 1-E. The apparatus will then be recycled to take another measurement of the heart rate, and appropriate corrective action will again be taken.

Since the corrective action taken by the resuscitator may be accomplished as soon as or even before an ambulance team or first aid personnel have reached the patient, the chances for survival are materially increased as compared with the chances for survival when treatment must await telemetry or transport of a heart patient to a hospital.

While we have shown and described a preferred embodiment of our invention, it will be apparent to those skilled in the art that many changes and modifications may be made without departing from our invention in its broader aspects. We therefore intend the appended claims to cover all such changes and modifications as fall within the true spirit and scope of our invention.

What is claimed is:

1. A cardiac resuscitator comprising:
means for detecting electrical activity of a patient's heart,
means for detecting mechanical activity of a patient's heart,
and means for applying a defibrillating pulse to said patient in the presence of electrical activity accompanied by the absence of mechanical activity as compared with predetermined activity levels.
2. The apparatus according to claim 1 including means for rendering said means for detecting mechanical activity effective only immediately following detected electrical activity.
3. The apparatus according to claim 1 wherein said means for detecting mechanical activity comprises means for detecting impedance changes in a patient's body.
4. Cardiac resuscitator apparatus comprising:
first means for detecting an electrocardiac signal generated by a patient's heart including the QRS wave of the electrocardiac complex,
second means responsive to mechanical movement in the patient's body indicative of a patient's heart beat,
means for applying a pacing pulse at a predetermined rate to the patient in response to the absence of both electrical and mechanical activity of the patient's heart as indicated by failure of both said first and second means to produce outputs above predetermined limits,
and means for applying a defibrillating pulse to the patient in response to the presence of an electrical activity indicating output above a predetermined limit from said first means and the absence of a mechanical activity indicating output above a predetermined limit from said second means.
5. The apparatus according to claim 4 wherein said means for detecting mechanical activity comprises means for applying a signal to the patient, and means for detecting a change in voltage drop produced by said signal for detecting changes in body impedance caused by mechanical heart activity.
6. The apparatus according to claim 5 wherein said means for applying a signal to a patient includes a first electrode connected to the means for applying a signal, a second electrode for application to the patient, and

means connecting the second electrode to the means for detecting a change in voltage drop.

7. The apparatus according to claim 6 wherein at least one of said electrodes is also coupled to said first means for detecting the electrocardiac signal.

8. A cardiac resuscitator comprising:

electrode means for application to a patient suffering from possible heart attack,

first means coupled to said electrode means for detecting the electrocardiac signal generated by the patient's heart including the QRS wave of the electrocardiac complex, if present,

second means coupled to said electrode means for detecting impedance changes in the patient's body,

logical means coupled to receive outputs from said first and second means and for determining when said first and second means produce output rates respectively indicative of acceptable electrical and mechanical activity of the patient's heart, as the pulse rate detected by each of said first and second means exceeds predetermined levels,

pacer means coupled to said logical means and responsive to the absence of both electrical and mechanical activity, as indicated by failure of the outputs of either said first and second means to exceed predetermined levels, for providing an output comprising periodic pacing pulses at a predetermined rate, means coupling the last mentioned output to said electrode means,

and defibrillator means coupled to said electrode means and responsive to said logical means, as the output of said first means above a predetermined level indicates electrical activity of the patient's heart, while the output of the second means fails to exceed a predetermined level indicating absence of acceptable mechanical activity of the patient's heart, for applying a defibrillating pulse to said electrode means.

9. The apparatus according to claim 8 including indicating means responsive to said logical means when both said first and second means produce outputs above predetermined limits for indicating normal heart activity.

10. The apparatus according to claim 8 including a coincidence detector for receiving the outputs of both said first and second means and providing the output of said second means to said logical means only in the event that the output of said second means occurs within predetermined time limits of the output of said first means such that mechanical activity will only be detected in each instance substantially immediately following a detection of electrical activity of a patient's heart.

11. The apparatus according to claim 8 wherein said logical means comprises means for counting the outputs of said first means and said second means within predetermined time periods and producing logical outputs in accordance with the count of said outputs as they exceed predetermined lower activity levels.

12. The apparatus according to claim 8 wherein said means for detecting impedance changes of the patient's body comprises means for generating a high frequency alternating current for application to said patient's body via said electrode means, and means responsive to

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the signal received at other electrode means for detecting changes in said signal.

13. The apparatus according to claim 8 including means for decoupling said detecting means from said electrode means during an output from said pacemaker means or said defibrillator means.

14. The apparatus according to claim 8 including means for determining the continuity of connection of said electrode means with the patient's body, and means for inhibiting the pacing pulse and defibrillating pulse application of said resuscitator apparatus, in response to a lack of such continuity.

15. The apparatus according to claim 8 wherein said first detecting means includes a variable sensitivity signal channel, having means for receiving and coupling the electrocardiac signal and means for storing previous peak values detected, the signal channel being coupled to the means for storing for changing the sensitivity of said signal channel in response to the previous level of peak values stored for causing said

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first detecting means to be responsive to signals exceeding at least a predetermined proportion of said peak values.

16. The apparatus according to claim 15 further including means for limiting the level stored by said storing means to a predetermined multiple of said peak values stored theretofore.

17. The apparatus according to claim 8 including a U-shaped applicator wherein said electrode means are carried by said U-shaped applicator positionable for yieldably urging said electrode means into firm contact with the patient's body, at least one of said electrode means being mounted from an upper leg of said applicator for location against the patient's chest over the heart area, and a second electrode means being mounted upon a lower leg of said applicator for positioning against the patient's back opposite the first mentioned electrode means.

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