(12) STANDARD PATENT (11) Application No. **AU 2007261054 B2**
(19) AUSTRALIAN PATENT OFFICE

(54) Title
Silicon carbide and related wide-bandgap transistors on semi insulating epitaxy

(51) International Patent Classification(s)
H01L 29/15 (2006.01)

(21) Application No: **2007261054** (22) Date of Filing: **2007.06.19**

(87) WIPO No: **WO07/149849**

(30) Priority Data

(31) Number	(32) Date	(33) Country
60/805,139	**2006.06.19**	**US**
11/764,593	**2007.06.18**	**US**

(43) Publication Date: **2007.12.27**
(44) Accepted Journal Date: **2013.09.26**

(71) Applicant(s)
Power Integrations, Inc.

(72) Inventor(s)
Mazzola, Michael S.

(74) Agent / Attorney
A J PARK, L 11 60 Marcus Clarke ST, Canberra, ACT, 2601

(56) Related Art
US 7009209 B2
US 6303475 B1

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 December 2007 (27.12.2007)

PCT

(10) International Publication Number
WO 2007/149849 A1

(51) International Patent Classification:
H01L 29/15 (2006.01)

(21) International Application Number:
PCT/US2007/071549

(22) International Filing Date: 19 June 2007 (19.06.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/805,139	19 June 2006 (19.06.2006)	US
11/764,593	18 June 2007 (18.06.2007)	US

(71) Applicant (*for all designated States except US*): **SEMISOUTH LABORATORIES, INC.** [US/US]; 201 Research Boulevard, Starkville, MS 39759 (US).

(72) Inventor; and
(75) Inventor/Applicant (*for US only*): **MAZZOLA, Michael, S.** [US/US]; 1877 Highway 12 West, Starkville, MS 39759 (US).

(74) Agents: **HEINTZ, James, M.** et al.; Patent Group, DLA Piper US LLP, 1200 Nineteenth Street, NW, Washington, DC 20036-2412 (US).

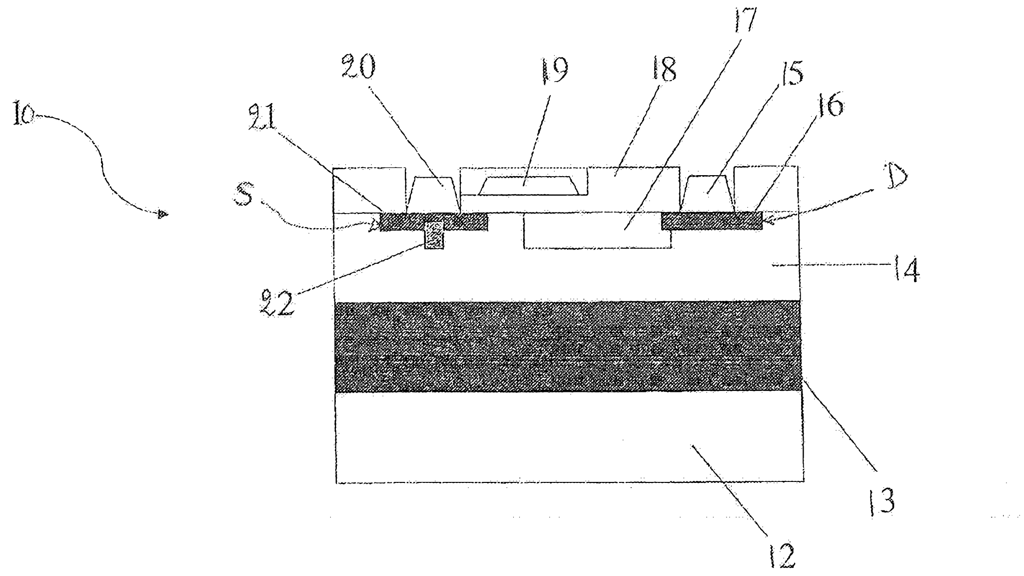
(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SILICON CARBIDE AND RELATED WIDE-BANDGAP TRANSISTORS ON SEMI INSULATING EPITAXY



(57) Abstract: A method of making a semi-insulating epitaxial layer includes implanting a substrate or a first epitaxial layer formed on the substrate with boron ions to form a boron implanted region on a surface of the substrate or on a surface of the first epitaxial layer, and growing a second epitaxial layer on the boron implanted region of the substrate or on the boron implanted region of the first epitaxial layer to form a semi-insulating epitaxial layer.

WO 2007/149849 A1

TITLE:

SILICON CARBIDE AND RELATED WIDE-BANDGAP TRANSISTORS ON SEMI INSULATING EPITAXY

CROSS REFERENCE TO RELATED APPLICATIONS

[001] This application is based on, and claims priority to, U.S. Provisional Application Serial No. 60/805,139, filed June 19, 2006, the entire contents of which are hereby incorporated by reference.

Field

[002] The present invention relates generally semiconductor devices and method of fabrication and more particularly to semiconductor devices employing a silicon carbide semi-insulating layer.

BRIEF SUMMARY

[002a] The present invention provides a method of making a semi-insulation epitaxial layer, the method comprising implanting a substrate or a first epitaxial layer formed on the substrate with boron ions to form a boron implanted region on a surface of the substrate or on a surface of the first epitaxial layer and growing a second epitaxial layer on the boron implanted region of the substrate or on the boron implanted region of the first epitaxial layer and diffusing the boron ions from the first epitaxial layer into the second epitaxial layer to form a semi-insulation epitaxial layer in at least part of the second epitaxial layer.

[002b] The present invention further provides a microelectronic device comprising a substrate and a lightly n-doped silicon carbide epitaxial layer formed above the substrate, the lightly n-doped silicon carbide epitaxial layer having a semi-insulating region formed therein, wherein the semi-insulating region comprises boron-related D-center defects that compensate for the light n-doping, wherein the boron-related D-center defects are distributed in the semi-insulating region consistent with diffusion of the boron into the semi-insulating region.

[003] There is described herein a method of making a semi-insulating epitaxial layer. The method includes implanting a substrate or a first epitaxial layer formed on the substrate with boron ions to form a boron implanted region on a surface of the substrate or on a surface of the first epitaxial layer; and growing a second epitaxial layer on the boron implanted region of the substrate or on the boron implanted region of the first epitaxial layer to form a semi-insulating epitaxial layer.

[004] There is also described herein a microelectronic device. The device includes a substrate, a semi-insulating silicon carbide epitaxial layer formed on the substrate. The semi-insulating silicon carbide epitaxial layer comprises boron and boron-related D-center defects. The microelectronic device also includes a first semiconductor device formed on the semi-insulating silicon carbide layer. The semi-insulated epitaxial silicon carbide layer is formed by implanting the substrate or a first epitaxial layer formed on the substrate with boron ions to form a boron implanted region on a surface of the substrate or on a surface of the first epitaxial layer, and growing a second epitaxial layer on the boron implanted region of the substrate or on the boron implanted region of the first epitaxial layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[005] FIGURE 1 is a schematic representation of a cross-section of a SiC MOSFET device, according to an embodiment of the present invention;

[006] FIGURE 2 is a schematic representation of a cross-section of a first semiconductor device and a second semiconductor device formed on a same SiC chip, according to an embodiment of the present invention;

[007] FIGURE 3A-3C depict the various steps for forming a semi-insulating epitaxial layer in which a substrate is utilized as a boron source, according to an embodiment of the present invention.

[008] FIGURE 4A-4D depict the various steps for forming a semi-insulating epitaxial layer in which an epitaxial layer formed on a substrate is utilized as a boron source, according to another embodiment of the present invention.

[009] FIGURES 5A-5D depict the various steps for forming a semi-insulating epitaxial layer in which an epitaxial layer formed on a substrate is utlilized as a boron source, according to an alternative embodiment of the present invention.

[010] FIGURES 6A-6D depict the various steps for forming a semi-insulating (SI) epitaxial layer in which an epitaxial layer formed on a substrate is a utilized as a boron source and which a mask material is applied on a surface of epitaxial layer, according to another embodiment of the present invention; and

[011] FIGURES 7A-7E depict the various steps for forming a semi-insulating (SI) epitaxial layer in which an epitaxial layer formed on a substrate is utilized as a boron source and a mask material is applied on a boron implanted region.

[011a] In the description in this specification reference may be made to subject matter which is not within the scope of the appended claims. That subject matter should be readily identifiable by a person skilled in the art and may assist in putting into practice the invention as defined in the presently appended claims.

DETAILED DESCRIPTION OF SOME PREFERRED EMBODIMENTS

[011b] The present invention will now be described, by way of non-limiting example only, with reference to the accompanying drawings, in which:

[012] FIGURE 1 is a schematic representation of a cross-section of a SiC MOSFET device, according to an embodiment of the invention. The device 10 includes a substrate 12 (e.g., n^+ 611 silicon carbide), upon which is formed, such as by epitaxial growth, a semi-insulating silicon carbide epitaxial layer 13. A p^- silicon carbide layer 14 is formed on the semi-insulating (SI) silicon carbide epitaxial layer 13. The p^- silicon carbide layer 14 includes a graded implant region 17, such as an n-type drift region.

[013] A source/body S, including, for example, a n+ source region, with contact area 20, a n+ source well 21, and a p+ body contact 22, as well as a drain D, including, for example, a n+ drain region, with contact area 15, and a n+ drain well 16, are formed on the p-silicon carbide layer 14. A silicon oxide layer 18 is also formed on the p- silicon carbide layer 14, along with a gate and contact area 19.

[014] In one embodiment, all layers of the MOSFET device 10 are grown epitaxially. In one embodiment, the SI SiC layer 13 is created by one of a plurality of methods that will be described in detail in the following paragraphs.

[015] FIGURE 2 is a schematic representation of a cross-section of a first semiconductor device 44 and a second semiconductor device 49 formed on a same SiC chip 40, according to an embodiment of the invention. As shown in FIGURE 2, SiC chip 40 includes a substrate 41, such as an n+ substrate, a SI layer 42, such as an epitaxial layer. An optional shallow trench isolation (STI) 43 is provided, as appropriate, for example, for device formation, to separate the first semiconductor device 44 and the second semiconductor device 49 (e.g., for electrical isolation).

[016] In one embodiment, the first semiconductor device 44 is a vertical bipolar junction transistor (BJT) and the second semiconductor device 49 is a vertical junction field effect transistor (JFET). The BJT device 44 includes various features, such as a n- collector 45, a n+ subcollector 46, a p- base 47, and a n+ emitter 48. The vertical JFET 49 includes various features, such as a source layer 50. The source layer 50 can be, for example, a n+ layer. The vertical JFET 49 also includes gate regions 51 and 52 which can be p+ layers, and a drain region 53, which can be a n+ layer. A contact 54 is provided in the drain region 53.

[017] Each of the devices 44 and 49 of FIGURE 2 are intended to be merely illustrative of devices that may be formed on the SI layer 42. With SI epitaxy, these vertical power devices are capable of being integrated on the same chip as lateral power devices or lateral control circuitry, which forms the basis for a complex, multi-function (e.g., power conditioning, control, amplification) monolithic circuit in SiC, also known as a "Smart Power IC." A detailed description of various devices can be found in U.S. Patent No. 7,009,209 to Casady et al. entitled “Silicon Carbide and Related Wide-Bandgap Transistors on Semi-Insulating Epitaxy for High Speed, High Power Applications,” the contents of which are incorporated herein by reference.

[018] First, electrical isolation between devices can be achieved. Technical performance and affordability are both enhanced by growing a semi-insulating epitaxial layer on a much higher quality and less expensive conducting 4H SiC substrate. Second, high power density integrated circuits can be better achieved using SiC rather than Silicon-on-Insulator (SOI) because the thermal conductivity of the semi-insulating SiC epitaxial layer is much higher than the thermal conductivity of SiO2 used in SOI. Therefore, waste heat can be removed far more efficiently. For example, based on the ratio of their thermal conductivities, a SI SiC buffer layer is able to thermally conduct up to 231 times as much heat on a per unit area basis as compared to the typical silicon-dioxide buffer layer used in SOI.

[019] Various methods for growing SI SiC epitaxial films are described herein in the following paragraphs. A method includes using boron related D-center to compensate shallow nitrogen donors during growth of SiC epitaxial layers. The D-center, approximately 0.7 eV above the valence band in SiC, has been detected in all polytypes of SiC studied. The boron related D-center, also known as a "point defect," is related to the boron atom occupying a silicon substitution site in the SiC crystal.

[020] The different polytypes of silicon carbide (e.g., 6H SiC and 4H SiC) can produce different characteristics in a semiconductor device, and thus can be used in various applications. One difference between 6H SiC and 4H SiC, for example, is the bandgap of these polytypes: the bandgap of 6H SiC is about 2.9 eV, while that of 4H SiC is about 3.2 eV. The 0.3 eV difference between these polytypes makes each typically suitable for different applications. For example, 4H SiC is often preferable for high voltage or high power applications, to take advantage of the larger bandgap, while 6H SiC is preferable, for example, for use in some applications because of its common commercial use in light emitting diodes. The present invention has been observed to work well in all SiC polytypes.

[021] Many different solid sources of boron can be used to form the compensated epitaxial layer containing a boron-related D-center. In addition to the solid doping sources, the solid source of boron may also reside in the substrate, in another adjacent epitaxial layer, or in the epitaxial layer itself. In one embodiment, the transport of boron into the compensated epitaxial layer is by diffusion. Diffusion of the boron and the consequential formation of desirable D-center defects could occur during growth of the compensated epitaxial layer onto either the substrate or an adjacent conducting epitaxial layer first grown on the substrate.

[022] A precondition for the diffusion is to implant boron into a surface of the substrate and/or the first conducting epitaxial layer. Damage in the crystalline structure of the implanted material facilitates anomalously fast diffusion of boron and a higher efficiency of D-center formation.

[023] In one embodiment, a homogeneous method of implanting the boron directly into the targeted epitaxial layer itself may be utilized. In another embodiment, a heterogeneous method of solid source doping in an adjacent SiC material may be utilized. If the epitaxial layer is grown first, and boron is then implanted into that layer, boron will, in a subsequent thermal annealing step, redistribute and form D-centers. Either the heterogeneous or homogeneous embodiments will result in a device containing an epitaxially grown semi-insulating thin film of silicon carbide.

[024] FIGURE 3A-3C depict the various steps for forming the semi-insulating (SI) epitaxial layer, according to an embodiment of the present invention. In this embodiment, the substrate may be utilized as a boron source. First, a substrate 60 is provided as depicted in FIGURE 3A. The substrate 60 may comprise silicon carbide. The substrate can be, for example, a p-type SiC substrate. A surface of the substrate 60 is bombarded with boron ions to form a boron implanted region 61 in the substrate 60, as depicted in FIGURE 3B. Following the formation of the boron implanted region 61, an epitaxial layer is grown on the boron implanted region 61. In one embodiment, the growth of the epitaxial layer is conducted at temperatures between about 1,500 °C and 1,700 °C, for example, at a temperature of approximately 1,600 °C during a time period between about 1 hour to about 3 hours, for example during a time period of approximately 1 hour. In one embodiment, the epitaxial layer 62 is a n-type epitaxial layer. During the growth of the epitaxial layer 62, the boron in the boron region 61 diffuses into the epitaxial layer 62 to form the semi-insulating epitaxial layer 62, as shown in FIGURE 3C. The boron implanted region 61 acts as a source

of boron and the boron in the boron implanted region 61 diffuses into the epitaxial layer grown on the boron implanted region 61. The diffusion of boron into the epitaxial layer 62 forms the boron-related D-centers that compensate the shallow donors. While the material close to the surface of the grown epitaxial layer 62 is n-type, a profile closer to the interface with the boron-implanted substrate reveals a clear transition to p-type.

[025] FIGURE 4A-4D depict the various steps for forming a semi-insulating (SI) epitaxial layer, according to another embodiment of the present invention. In this embodiment, an epitaxial layer is formed on a substrate, i.e., an epitaxial layer adjacent to the substrate, may be utilized as a boron source. A substrate 70 is provided as depicted in FIGURE 4A. The substrate 70 may comprise silicon carbide. The substrate can be of any type, for example, a p-type SiC substrate. A first epitaxial layer 71 is formed on the substrate 70, as depicted in FIGURE 4B. In one embodiment, the first epitaxial layer 71 is a n-type epitaxial layer. Following the formation of the first epitaxial layer 71, a surface of the first epitaxial layer 71 is bombarded with boron ions to form a boron implanted region 72 in the first epitaxial layer 71, as depicted in FIGURE 4C. Following the formation of the boron implanted region 72, a second epitaxial layer 74 is grown on the boron implanted region 72. In one embodiment, the growth of the second epitaxial layer 74 is conducted at temperatures between about 1,500 °C and 1,700 °C, for example, at a temperature of approximately 1,600 °C during a time period between about 1 hour to about 3 hours, for example during a time period of approximately 1 hour. In one embodiment, the second epitaxial layer 74 is a n-type epitaxial layer. During the growth of the second epitaxial layer 74, the boron in the boron region 72 diffuses into the first epitaxial layer 71 to form the semi-insulating layer 73 and diffuses into the second epitaxial layer 74 to form the semi-insulating epitaxial layer 74, as shown in FIGURE 4D. The boron implanted region 72 acts as a source of boron and diffuses into the first and the second epitaxial layers. The diffusion of boron into the first and second epitaxial layers 71, 74 forms the boron-related D-centers in both the first epitaxial layer and the second epitaxial layer. The result is the formation of SI layers 73 and 74, respectively, below and above the boron implanted region 72.

[026] FIGURES 5A-5D depict the various steps for forming a semi-insulating (SI) epitaxial layer, according to further embodiment of the present invention. FIGURES 5A-5D illustrate an embodiment which is a homogenous alternative to the embodiments depicted in FIGURES 3A-3C and 4A-4D. In this embodiment, similar to the embodiment depicted in FIGURES 4A-4D an epitaxial layer formed on a substrate, i.e., an epitaxial layer adjacent to the substrate, may be utilized as a boron source. A substrate 80 is provided as depicted in FIGURE 5A. The substrate 80 may comprise silicon carbide. The substrate can be of any type, for example, a p-type SiC substrate. An epitaxial layer 81 is formed on the substrate 80, as depicted in FIGURE 5B. In one embodiment, the epitaxial layer 81 is a n-type epitaxial layer. Following the formation of the first epitaxial layer 81, a surface of the epitaxial layer 81 is bombarded with boron ions to form a boron implanted region 82 in the epitaxial layer 81, as depicted in FIGURE 5C. In one embodiment, the growth of the epitaxial layer is conducted at temperatures between about 1,500 °C and 1,700 °C, for example, at a temperature of approximately 1,600 °C during a time period between about 1 hour to about 3 hours, for example during a time period of approximately 1 hour. The boron in the boron region 82 diffuses into the epitaxial layer 81 to form the semi-insulating layer 83, as shown in FIGURE 5D. The boron implanted region 82 acts as a source of boron and diffuses into the epitaxial layer 81 formed on the substrate 80. The diffusion of boron into the epitaxial layer forms the boron-related D-centers in the epitaxial layer 81 to obtain SI layer 83. Optionally, after forming the SI layer 83, the residual boron implanted region 82 can be removed using, for example, any etching technique known in the art. The obtained SI layer is specified to be p-type which is to say that it must be doped more heavily p-type than the underlying substrate.

[027] FIGURES 6A-6D depict the various steps for forming a semi-insulating (SI) epitaxial layer, according to another embodiment of the present invention. FIGURES 6A-6D illustrate an embodiment which is a variation of the method illustrated in FIGURES 5A-5D. In this embodiment, similar to the embodiment depicted in FIGURES 5A-5D an epitaxial layer formed on a substrate, i.e., an epitaxial layer adjacent to the substrate, may be utilized as a boron source. However, in this embodiment, a mask material is applied on a surface of the epitaxial layer. Specifically, a substrate 90 is provided as depicted in FIGURE 6A. The substrate 90 may comprise silicon carbide. The substrate 90 can be of any type, for example, a n+-type SiC substrate. An epitaxial layer 91 is formed on the substrate 90, as depicted in FIGURE 6A. In one embodiment, the epitaxial layer 91 is a n-type epitaxial layer. Following the formation of the first epitaxial layer 91, a mask material 92 is applied on a surface of the epitaxial layer 91 so as to form masked areas and unmasked areas on the surface of the epitaxial layer 91. After applying the mask material 92 on a surface of the epitaxial layer 91, trenches 93 are formed, for example by etching the unmasked (unprotected) areas of the epitaxial layer 91, as depicted in FIGURE 6B. After forming the trenches 93, the surface of the epitaxial layer 91 on which the mask material 92 is deposited is bombarded with boron ions. In addition to being a mask for selective etching for forming trenches 93, the mask material 92 can also be selected to prevent implantation underneath masked areas of the epitaxial layer 91. In this way, the mask material 92 can also be used as "a dopant mask" to implant doping material in selective areas of the epitaxial layer. However, if the mask material 92 is not a dopant mask, the mask material 92 can be removed and another mask material suitable as a dopant mask can be applied on a surface of the epitaxial layer 91. The boron ions impinge unprotected areas of the epitaxial layer 91

including a bottom of the trench 93 and sidewall(s) of the trench 93. As a result, a boron implanted region 94 is formed in trench 93 of the epitaxial layer 91, as depicted in FIGURE 6C. After forming the boron implanted region 94, the mask material 94 is removed, as shown in FIGURE 6D, and a high temperature anneal process is applied resulting in the diffusion of boron deeper into the epitaxial layer 91. In one embodiment, the anneal process is performed at a temperature between about 1,500°C and about 1,700°C during a time period between about 1 hour and about 3 hours. In one example, the anneal process is performed at a temperature of about 1,600°C during a time period of about 1 hour. The diffusion of boron into the epitaxial layer 91, in turn, results in the creation of D-centers to produce the semi-insulating epitaxial layer 95. The implantation of boron in the sidewall(s) of the trench 93, which is a phenomenon that is associated with implantation in trenches, assists in a lateral diffusion of boron into the channel formed by the trenches 93. Examples using the above method can be found in U.S. Patent No. 6,767,783 to Casady et al., entitled "Self-Aligned Transistor and Diode Topologies in Silicon Carbide Through the Use of Selective Epitaxy or Selective implantation," the entire contents of which are incorporated herein by reference. The dimensions of the channel should be consistent with the expected diffusion length of boron and the range of creation of boron-related D-centers, which is of the order of a few micrometers.

[028] A variation of the above method can use a lightly n-type epitaxial layer 91 that is thicker than an expected diffusion depth of boron which also determines the depth of D-center compensation and thus determines the thickness of the formed semi-insulating epitaxial layer 95. As a result, the remainder of the semiconductor between the substrate 90 and the semi-insulating epitaxial layer 95 is occupied by the residual n-type epitaxial layer 91.

[029] FIGURES 7A-7E depict the various steps for forming a semi-insulating (SI) epitaxial layer, according to another embodiment of the present invention. FIGURES 7A-7D illustrate an embodiment which is a variation of the method illustrated in FIGURES 4A-4D. In this embodiment, similar to the embodiment depicted in FIGURES 4A-4D an epitaxial layer formed on a substrate, i.e., an epitaxial layer adjacent to the substrate, may be utilized as a boron source. However, in this embodiment, a mask material is applied on a surface of a boron implanted region. Specifically, a substrate 100 is provided, as depicted in FIGURE 7A. The substrate 100 may comprise silicon carbide. The substrate 100 can be of any type, for example, a n+-type SiC substrate. An epitaxial layer 101 is formed on the substrate 100, as depicted in FIGURE 6A. In one embodiment, the epitaxial layer 101 is a n-type epitaxial layer. Following the formation of the epitaxial layer 101, a surface of the epitaxial layer 101 is bombarded with boron ions to form boron implanted region 102, as shown in FIGURE 7B. A mask material 103 is applied on the boron implanted region 102 of the epitaxial layer 101 so as to define masked areas and unmasked areas on the surface of the epitaxial layer 101. After applying the mask material 103, trenches 104 are formed, for example by etching the unmasked (unprotected) areas of the epitaxial layer 101 and the unmasked areas of the boron implanted region 102, as depicted in FIGURE 7C.

[030] After forming the trenches 104, the mask material 103 is removed and another epitaxial layer 105 is grown on the epitaxial layer 101 and on the boron implanted region 102, as depicted in FIGURE 7D. This is performed using a process that fills the trenches 104 and self-planarizes above the trenches 104. During the growth of the epitaxial layer 105, boron in boron implanted region 102 diffuses into both epitaxial layers 101 and 105 and create D-centers to produce a semi-insulating epitaxial layer 106, as depicted in FIGURE 7E.

[031] The above method can be used in the fabrication of various devices, examples of which can be found in U.S. Patent Application No. 11/198,298 of Lin Cheng and Michael

S. Mazzola, entitled "Vertical-Trench Junction Field-Effect Transistor Having Epitaxially Grown Drift, Buried Gate and Guard Rings, Self-Planarized Channel and Source Regions in Silicon Carbide," filed on August 8, 2005, the entire contents of which are incorporated herein by reference. The dimensions of the channel should be consistent with the expected diffusion length of boron and the range of creation of boron-related D-centers, which is of the order of a few micrometers.

[032] A variation of the above method uses a lightly n-type epitaxial layer 101 that is thicker than an expected diffusion depth of boron, which also determines the depth of D-center compensation and thus the thickness of the resulting semi-insulating epitaxial layer 106. As a result, the remainder of the semiconductor between the substrate 100 and the semi-insulating epitaxial layer 106 is occupied by the residual n-type epitaxial layer 101.

[033] In one embodiment, in order to implant boron in the substrate or an adjacent epitaxial layer, the substrate or the adjacent epitaxial layer is bombared with boron ions having an energy between about 80 keV and 160 KeV. In one embodiment, a three-energy (80 keV, 115 keV, and 160 keV) boron implantation scheme with a total dose of 1.23 x 1015 cm-2 was applied to form a boron-rich near-surface layer.

[034] Various embodiments of the present invention can be used for application in compact, solid-state television and radar transmitters operating from very high frequency (VHF) to above X-band (10 GHz). Various embodiments of the present invention can also be used for military applications, for example in airborne radar systems on in advanced military aircraft. Commercial applications include use of embodiments of the present invention in television transmitter stations, cellular telephone base stations, and satellite communication links for telephony, audio, and image transmission. Furthermore, efficient power switching utilizing compact direct current to direct current (DC--DC) converters and motor drive control circuitry can also take advantage of embodiments of the present invention in, for example, hybrid-electric vehicles and fluorescent lighting ballasts.

[035] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example, and not limitation. It will be apparent to persons skilled in the relevant art(s) that various changes in form and detail can be made therein without departing from the spirit and scope of the present invention. In fact, after reading the above description, it will be apparent to one skilled in the relevant art(s) how to implement the invention in alternative embodiments. Thus, the present invention should not be limited by any of the above-described exemplary embodiments.

[036] Moreover, the method and apparatus of the present invention, like related apparatus and methods used in the semiconductor arts are complex in nature, are often best practiced by empirically determining the appropriate values of the operating parameters, or by conducting computer simulations to arrive at best design for a given application. Accordingly, all suitable modifications, combinations and equivalents should be considered as falling within the spirit and scope of the invention.

[037] In addition, it should be understood that the figures, are presented for example purposes only. The method and devices of the present invention are sufficiently flexible and configurable, such that it may be utilized in ways other than that shown in the accompanying figures.

[038] Further, the purpose of the Abstract of the Disclosure is to enable the U.S. Patent and Trademark Office and the public generally, and especially the scientists, engineers and practitioners in the art who are not familiar with patent or legal terms or phraseology, to determine quickly from a cursory inspection the nature and essence of the technical disclosure of the application. The Abstract of the Disclosure is not intended to be limiting as to the scope of the present invention in any way.

[039] The term ‘comprising’ as used in this specification and claims means ‘consisting at least in part of’. When interpreting statements in this specification and claims which include the term ‘comprising’, other features besides the features prefaced by this term in each statement can also be present. Related terms such as ‘comprise’ and ‘comprised’ are to be interpreted in similar manner.

[040] In this specification where reference has been made to patent specifications, other external documents, or other sources of information, this is generally for the purpose of providing a context for discussing the features of the invention. Unless specifically stated otherwise, reference to such external documents is not to be construed as an admission that such documents, or such sources of information, in any jurisdiction, are prior art, or form part of the common general knowledge in the art.

2007261054 02 Sep 2013

Claims:

1. A method of making a semi-insulating epitaxial layer, the method comprising:

implanting a substrate or a first epitaxial layer formed on the substrate with boron ions to form a boron implanted region on a surface of the substrate or on a surface of the first epitaxial layer; and

growing a second epitaxial layer on the boron implanted region of the substrate or on the boron implanted region of the first epitaxial layer and diffusing the boron ions from the first epitaxial layer into the second epitaxial layer to form a semi-insulating epitaxial layer in at least part of the second epitaxial layer.

2. The method of claim 1, wherein implanting the substrate or the first epitaxial layer comprises bombarding with boron ions having an energy between 80 KeV and 160 KeV.

3. The method of claim 1, wherein implanting the substrate comprises implanting a p-type silicon carbide substrate.

4. The method of claim 1, wherein implanting the first epitaxial layer comprises implanting a n-type silicon carbide epitaxial layer.

5. The method of claim 1, wherein growing the second epitaxial layer comprises growing the second epitaxial layer at temperatures between 1500 °C and 1700 °C.

6. The method of claim 1, wherein growing the second epitaxial layer comprises growing the second epitaxial layer during a time period between 1 hour and 3 hours.

7. The method of claim 1, wherein growing the second epitaxial layer comprises growing a n-type second epitaxial layer.

8. The method of claim 1, wherein boron in the boron implanted region diffuses into the second epitaxial layer grown on the boron implanted region to form D-centers in the second epitaxial layer.

9. The method of claim 1, further comprising removing the boron implanted region after forming the semi-insulating epitaxial layer.

10. The method of claim 1, further comprising applying a mask material on a surface of the first epitaxial layer.

11. The method of claim 10, further comprising:

forming trenches in the first epitaxial layer;

wherein implanting the first epitaxial layer comprises implanting the first epitaxial layer after forming the trenches in the first epitaxial layer to form a boron implanted region in the trenches.

12. The method of claim 11, further comprising applying a high temperature anneal process so that the boron diffuses deeper into the first epitaxial layer.

13. The method of claim 1, further comprising applying a mask material on the boron implanted region to define masked areas and unmasked areas on a surface of the first epitaxial layer.

14. The method of claim 13, further comprising forming trenches in the unmasked areas of the first epitaxial layer and in the unmasked areas of the boron implanted regions.

15. The method of claim 14, further comprising removing the mask material and growing the second epitaxial layer on the first epitaxial layer and on the boron implanted region.

16. The method of claim 15, wherein growing the second epitaxial layer on the first epitaxial layer and on the boron implanted region comprises filling the trenches and planarizing the second epitaxial layer above the trenches.

17. The method of claim 15, wherein boron in the boron implanted region diffuses into the first and the second epitaxial layers during the growing of the second epitaxial layer on the first epitaxial layer to form the semi-insulating epitaxial layer.

18. A microelectronic device comprising:

a substrate;

a lightly n-doped silicon carbide epitaxial layer formed above the substrate, the lightly n-doped silicon carbide epitaxial layer having a semi-insulating region formed therein, wherein the semi-insulating region comprises boron-related D-center defects that compensate for the light n-doping, wherein the boron-related D-center defects are distributed in the semi-insulating region consistent with diffusion of the boron into the semi-insulating region.

19. The device of claim 18, wherein:

the substrate is a conductor; and

the boron related D-centers are distributed in the silicon carbide epitaxial layer consistent with diffusion of boron from a source below the lower surface up into the silicon carbide epitaxial layer.

20. The device of claim 18, wherein:

2007261054 02 Sep 2013

the substrate includes a p-type substrate; and

the boron related D-centers are distributed in the silicon carbide epitaxial layer consistent with diffusion of boron from a source below the lower surface up into the silicon carbide epitaxial layer.

21. The device of claim 18, wherein:

the first semiconductor device comprises a metal oxide field effect transistor, a bipolar junction transistor, or a junction field effect transistor; and

the silicon carbide epitaxial layer is lightly n-doped with shallow nitrogen donors.

22. The device of claim 18, further comprising a second semiconductor device formed on the semi-insulating silicon carbide layer.

23. The device of claim 22, wherein the second semiconductor device is physically and electrically isolated from the first semiconductor device.

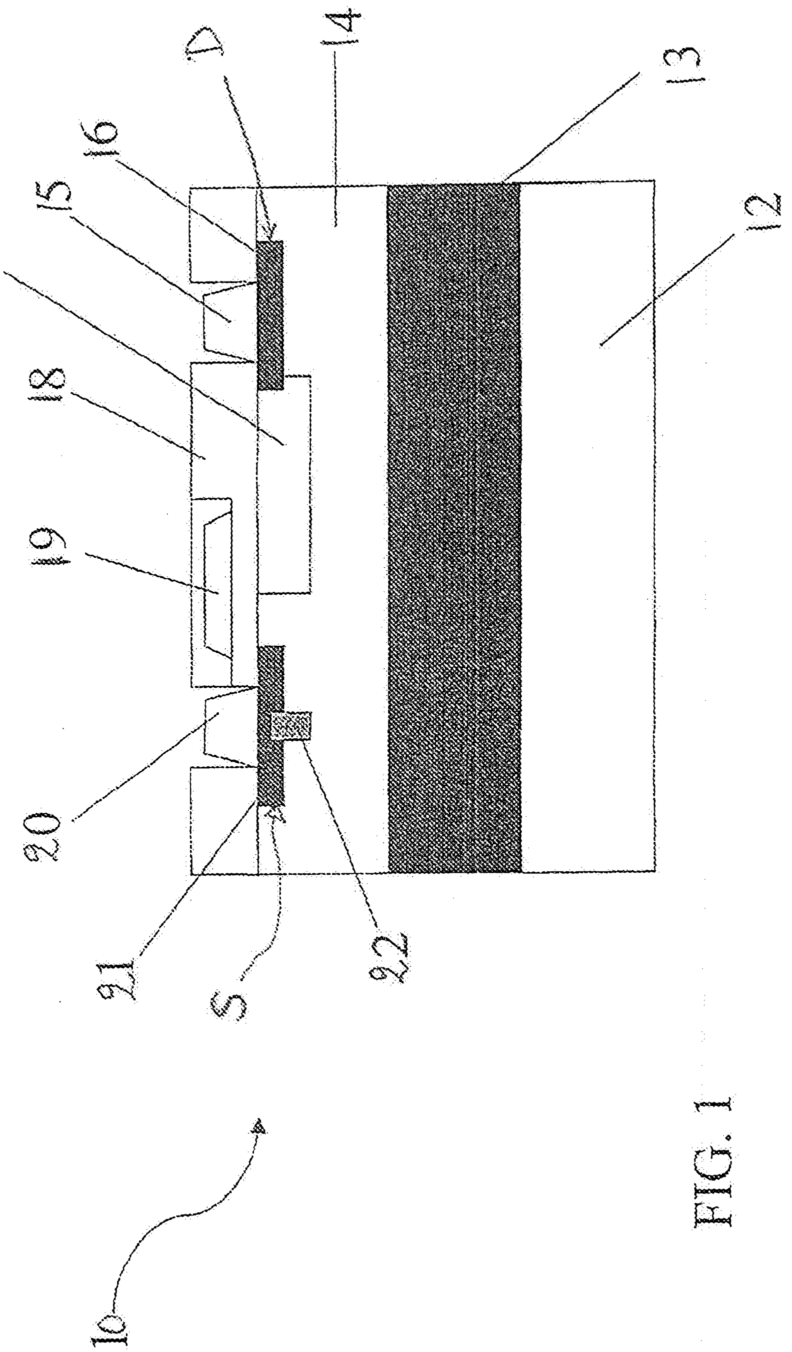


FIG. 1

FIG. 2

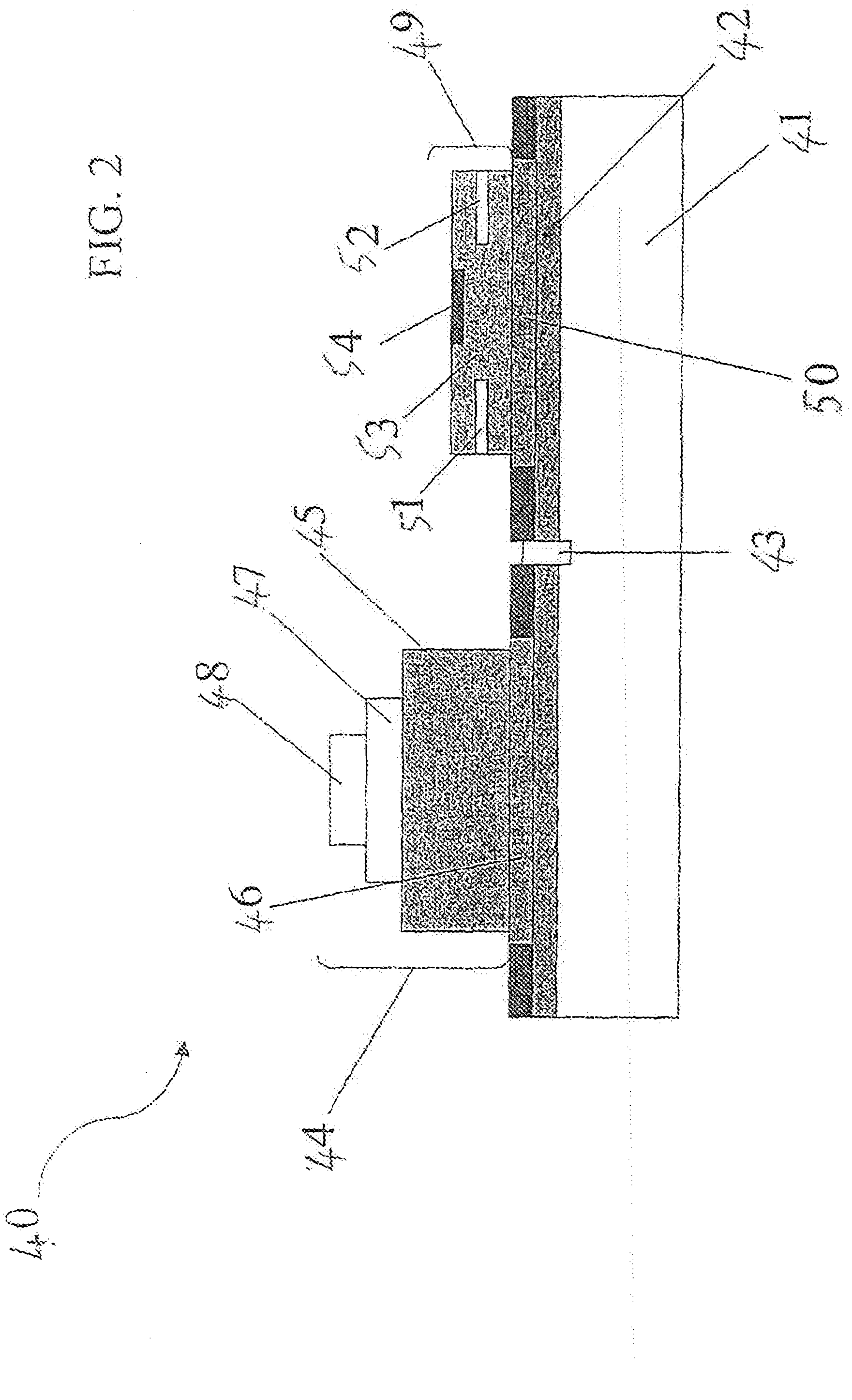


FIG. 3A

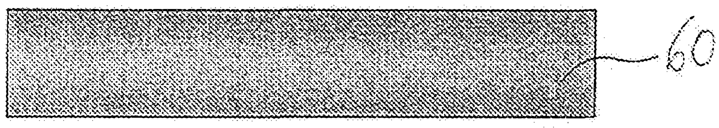


FIG. 3B

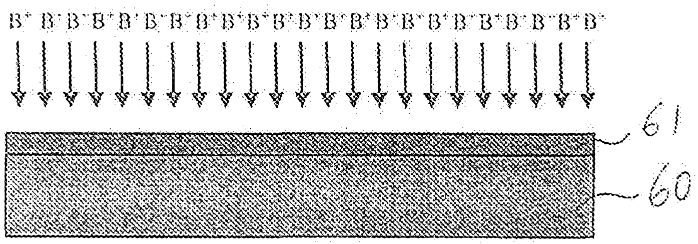


FIG. 3C

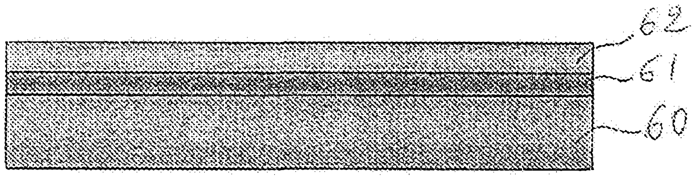


FIG. 4A

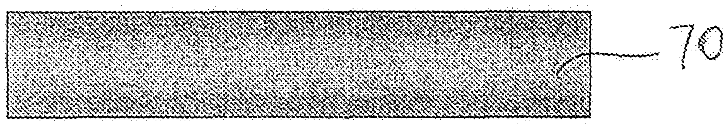


FIG. 4B

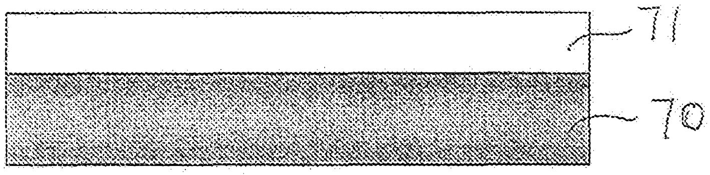


FIG. 4C

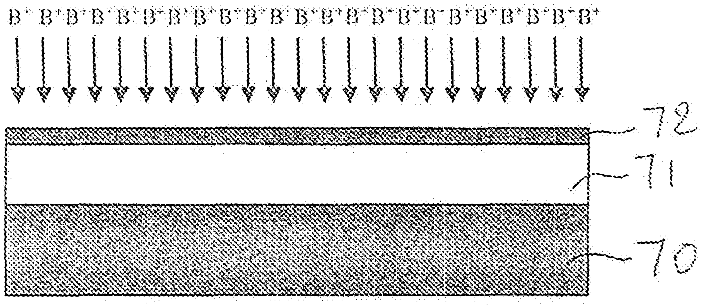


FIG. 4D

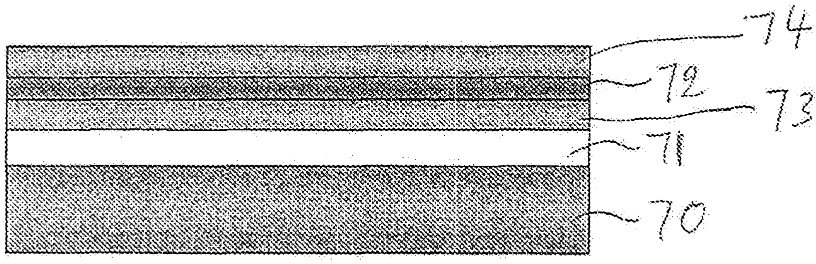


FIG. 5A

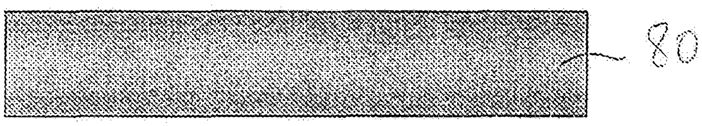


FIG. 5B

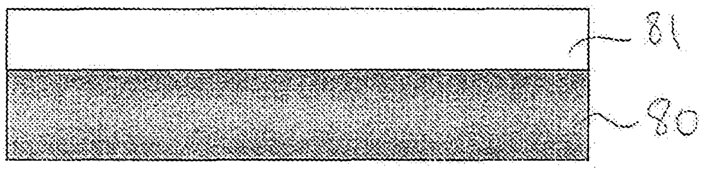


FIG. 5C

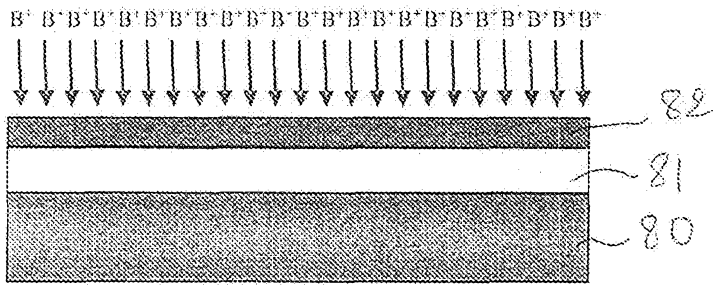


FIG. 5D

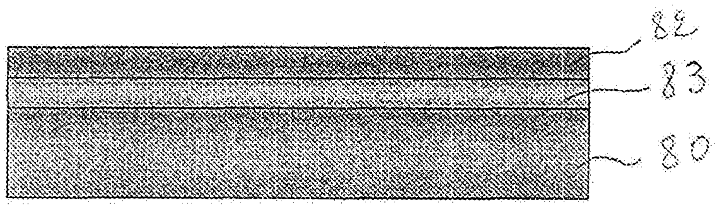


FIG. 6A

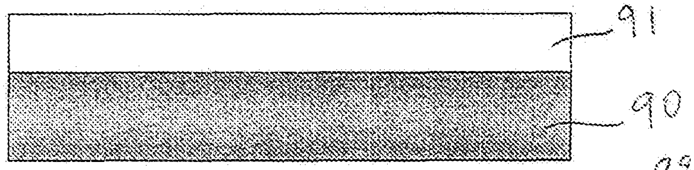


FIG. 6B

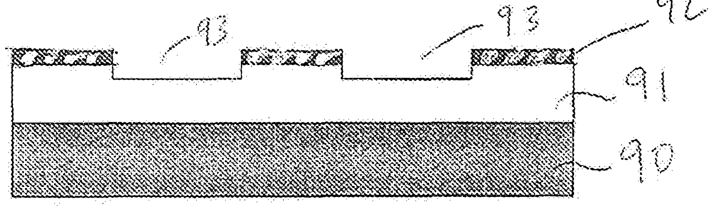


FIG. 6C

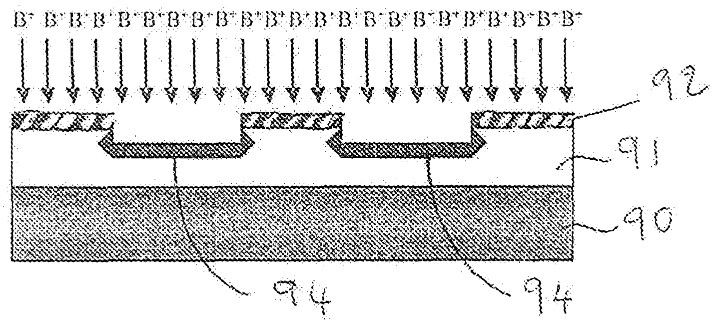


FIG. 6D

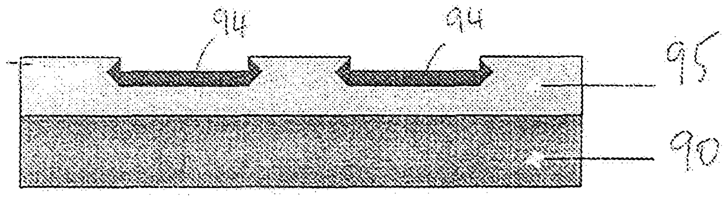


FIG. 7A

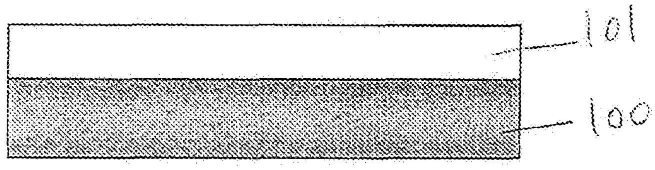


FIG. 7B

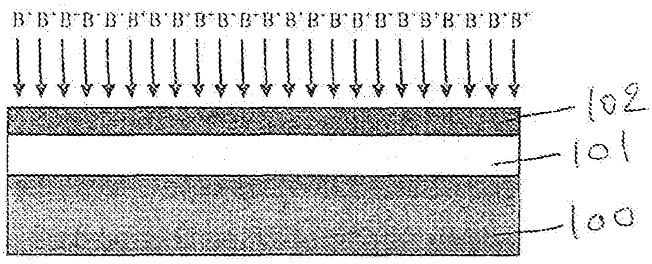


FIG. 7C

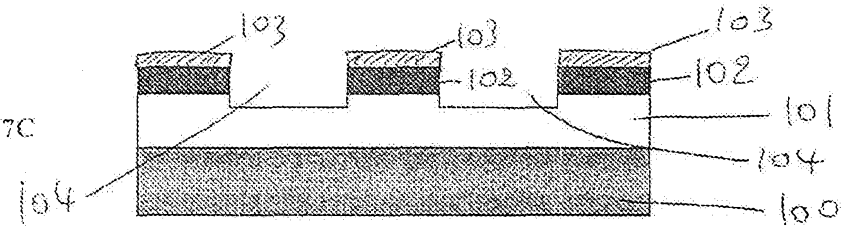


FIG. 7D

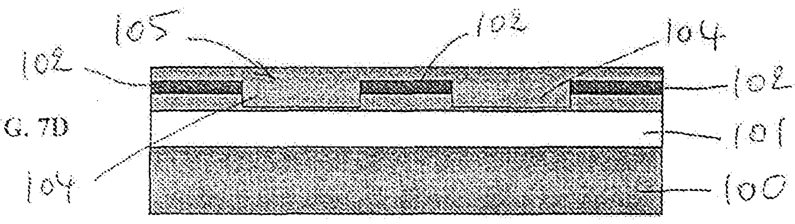


FIG. 7E