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(54) Title: METHOD FOR INTEGRATION OF CIRCUIT COMPONENTS INTO THE BUILD-UP LAYERS OF A PRINTED WIRING BOARD

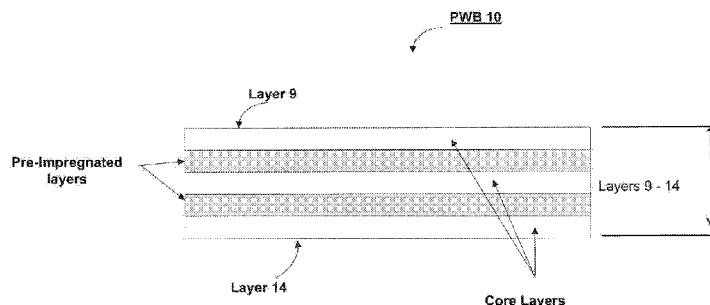


FIGURE 1

(57) Abstract: The present invention provides a printed wiring board assembly having active and passive components embedded between the printed wiring board layers and associated fabrication method so as to complete a multilayer printed wiring board to improve the flexibility of circuit layout.

METHOD FOR INTEGRATION OF CIRCUIT COMPONENTS INTO THE BUILD-UP LAYERS OF A PRINTED WIRING BOARD

Field of the Invention

[0001] The invention relates to a multilayer printed wiring board and provides a technique related to a multilayer printed wiring board capable of having improved electrical characteristics and reliability, decreased overall size, weight and cost and increased surface real estate for additional components on the printed wiring board.

Description of the Related Art

[0002] As electronic products are being made smaller and lighter, represented by the trends of smaller, thinner, higher-density, packaged, and portable products, so also is the multilayer printed circuit board (PCB) undergoing a trend towards finer patterns and smaller and packaged products. Accordingly, along with changes in the raw materials for forming fine patterns on the multilayer printed circuit board (PCB) and for improving reliability and design density (the number of chips mounted on a single circuit board or substrate), there is a change towards integrating the layer composition of circuits. Components are also undergoing a change from DIP (dual in-line package) types to SMT (surface mount technology) types, so that the mounting density is also being increased.

[0003] Generally, a method of packaging semiconductor chips on PCBs may include one or more of the following features. For example, a semiconductor chip may be stacked on the PCB, bonded and connected by a metal wire, or connected to the PCB using various direct mounting techniques that are well-known, including for example, flip-chip mounting (FC), direct chip attach (DCA), direct die attach (DDA), and flip chip on board (FCOB). These

techniques usually involve the fixing of a semiconductor die to a build-up PWB substrate.

[0004] Meanwhile, as functionality required by the electronic devices increases, an increased number of functional chips must be packaged on a limited space (or "real estate") of the PCB. This demand may suffer from a problem of causing the fabricated chip modules to be bulky as the thickness of the PCB is increased by thickness of semiconductor chips packaged to the PCB.

[0005] To solve or obviate these problems, chip embedded PCB technology has been researched where the semiconductor chips are embedded inside the PCB for integration there between. However, such embedding techniques bring about the following problems.

[0006] Difficulty in depositing high temperature fired high permittivity (dielectric constant) material on chip embedded PCBs. In other words, when the high temperature fired high permittivity material is deposited on a copper clad, co fired and deposited with polymer, a treatment problem occurs because the fabricating process is performed on the copper clad, and a bending problem is generated by differences of coefficient of thermal expansion with high permittivity material during high temperature firing.

[0007] Chips are embedded through a build-up process using a substrate as a core for fabricating the chip-embedded PCBs, and in case of coreless substrate, it is difficult to manufacture the PCBs and to embed chips inside a two-layered substrate without core.

[0008] In case of many functional chips being embedded inside the PCB, a metal plated heat sink must be additionally formed to radiate the heat generated in the course of product use. Adhesive is used to adhere a plated heat sink to the substrate in manufacturing of conventional chip embedded PCBs during which substrates may be seriously compromised by generation of air bubbles, and the

yield from manufacture of substrates may decrease significantly, thereby resulting in incurrence of additional manufacturing cost.

SUMMARY OF THE INVENTION

[0009] In view of the above prior art disadvantages, the object of the present invention is to provide a printed wiring circuit board (PWB) having active semiconductor devices and passive surface mount (SMT) chips embedded between PWB layers and fabricating method thereof, whereby increased surface real estate for additional components on electronic assemblies is achieved.

[00010] Another object of the present invention is to provide a printed wiring board (PWB) having active semiconductor devices and passive SMT chips embedded between PWB layers and fabricating method thereof, so as to decrease the overall size, weight and costs of electronic assemblies.

[00011] Another object of the present invention is to provide a printed wiring circuit board (PWB) having active semiconductor devices and passive SMT chips embedded between PWB layers and fabricating method thereof, so as to increase the electrical functions and electrical performance of electronic assemblies.

[00012] To achieve the above objects, a printed wiring circuit board (PWB) having active semiconductor devices and passive SMT chips embedded between PWB layers in the present invention includes: a first circuit board panel consisting of one or more layers, where the embedded components are installed using regular component assembly processes; additional "partially cured or pre-impregnated" panel layer(s) with openings used to create cavities; additional "solid or core" circuit board panel layers with openings used to create cavities can also be used. The openings in this layer(s) provide clearance for the components installed on the above "first circuit board panel". The openings can

be any shape and can provide clearance for one or more components; a second circuit board panel consisting of one or more layers. This second panel is used to cover the embedded components cavities; components, that will be embedded inside the final circuit board; and solder used for installing the embedded components using well known SMT Assembly processes.

[00013] The present invention also discloses a method of fabricating a printed wiring board having active semiconductor devices and passive SMT chips embedded therein contains the following steps: providing a carrier board comprised of a plurality of core and pre-impregnated layers; installing one or more embedded components onto a support layer; building up cavities around the one or more installed embedded components using additional core and pre-impregnated layers; installing further core and pre-impregnated layers above the built up cavities to form a PWB assembly; and laminating the PWB assembly thereby causing the cavities to backfill with lamination.

[00014] The above method further comprises processing all layers under heat, pressure and vacuum.

[00015] The present invention discloses a printed wiring board structure having active semiconductor devices and passive surface mount (SMT) chips embedded between PWB layers and fabricating method thereof further comprise embedding surface mount structures thereto, so as to complete a multilayer circuit board, to improve the flexibility of circuit layout.

[00016] Moreover, in the present invention, the circuit board having capacitors embedded therein and fabricating method thereof can avoid alignment errors during drilling and lamination in the conventional method. Therefore, quality of products is advanced, and fabricating method is simplified to decrease the production cost.

[00017] Other objects, advantages, and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[00018] These and other objects, features and advantages of the invention will be apparent from a consideration of the following Detailed Description Of The Invention considered in conjunction with the drawing Figures, in which:

[00019] **Figure 1** is a process diagram showing the manufacturing method of the multilayer printed wiring board according to the first embodiment.

[00020] **Figure 2** is a process diagram showing the manufacturing method of the multilayer printed wiring board according to the first embodiment.

[00021] **Figure 3** is a process diagram showing the manufacturing method of the multilayer printed wiring board according to the first embodiment.

[00022] **Figure 4** is a process diagram showing the manufacturing method of the multilayer printed wiring board according to the first embodiment.

[00023] **Figure 5** is a process diagram showing the manufacturing method of the multilayer printed wiring board according to the first embodiment.

[00024] **Figure 6** is a process diagram showing the manufacturing method of the multilayer printed wiring board according to the first embodiment.

DETAILED DESCRIPTION OF THE INVENTION

[00025] Because of the specific embodiments illustrating the practice of the present invention, a person having ordinary skill in the art can easily understand

other advantages and efficiency of the present invention through the content disclosed therein. The present invention can also be practiced or applied by other variant embodiments. Many other possible modifications and variations of any detail in the present specification based on different outlooks and applications can be made without departing from the spirit of the invention.

[00026] The drawings of the embodiments in the present invention are all simplified charts, and only reveal elements relative to the present invention. The elements revealed in the drawings are not aspects of the practice, and quantity and shape thereof are optionally designed. Further, the design aspect of the elements can be more complex.

[00027] Now, exemplary implementations of the present inventive disclosure will be described in detail with reference to the accompanying drawings.

[00028] FIGS. 1 to 6 are cross-sectional views illustrating a fabricating method of passive SMT chip and semiconductor device embedded printed wiring board 10 according to one embodiment of the invention.

[00029] Referring to FIGS. 1 to 6, a partial lamination of layers 9-14 of a build-up substrate, i.e., PWB 10, is shown. PWB 10 preferably comprises a core substrate and a resin insulation layer laminated on the core substrate. Build-up PWB substrates typically include a central constraining layer or "core" to which comparatively thin dielectric layers are attached. The thin dielectric layers include fine circuit features and narrow diameter plated vias. A core can be constructed using a glass fiber based dielectric material possessing physical characteristics similar to those of glass fiber based dielectric materials used in the construction of the type of PWB on which an integrated circuit (i.e., a packaged semiconductor device) would be surface mounted. To distinguish between PWBs on which ICs are mounted and PWB substrates, the former are referred to as conventional PWBs. The thin dielectric layers in build-up PWB substrates are constructed from a class of materials that are typically not used in

the construction of conventional PWBs. Specialized processing techniques are used to bond the core and the thin dielectric layers and to form the fine circuit traces and narrow diameter plated vias.

[00030] Preferably, all PWB layers in the fabricating method are of a standard panel size, 12 x 18, however, the present invention is not so restricted. A panel size of 12 x 18 is preferred because of its compatibility with standard PCB lamination and assembly equipment.

[00031] At a first stage of the fabricating method, one or more embedded components (e.g., active semiconductor devices and passive surface mount (SMT) chips) 21, 23, are successively fixed to support layer 9 of a build-up PWB substrate 10, as shown in FIG. 2. Two components 21, 23 are shown by way of example only. In one embodiment, the embedded components 21, 23 are fixed to support layer 9 using a flip-chip bonding method. Although an implementation using flip-chip bonding method for packaging the embedded components 21, 23 onto support layer 9 has been exemplified, other various methods such as, for example, wire bonding method and ACF (Anisotropic Conductive Film) method may be employed. In addition, other SMT components such as, for example, resistor, capacitors, inductors, etc. can also be installed using regular SMT assembly processes. The reader will now be aware of still other SMT components contemplated by the invention, including future and envisioned components, suitable for use with the invention.

[00032] Next, cavities are built up around the components 21, 23 in order to prevent the embedded components 21, 23 from becoming damaged, as shown in Fig. 3. The cavities are built up using core and prepregged layers 7-8. These layers are typically formed of a half-hardened pre-impregnated. The pre-impregnated layers are typically made of glass fiber hardened by a predetermined heat and pressure and thermosetting resin. Openings are cut into these layers 7-8 to create mechanical clearance around the embedded components 21, 23. The openings can be any shape and can provide clearance

for the embedded components 21, 23 when the regular production layers 1-6 are stacked above layer 7 to cover the embedded components 21, 23.

[00033] Next, regular production layers 1-6 are stacked above layer 7 to cover the embedded components 21, 23, as shown in Fig. 4. Layers 1-6 can be individual layers or layers 1-6 can be pre-laminated as a lamina before being stacked above layer 7.

[00034] Fig. 5 shows a final lamination process during which epoxy from pre-pregnated layers backfill the cavities. During this step all layers 1-14 are permanently bonded using regular production processing conditions for FR4 core and pre-pregnated layers. A vacuum is used to pull air from the cavities which cause the cavities to become filled with residual resin/materials from pre-pregnated layers to avoid voids, gaps, bubbles which are common defects in printed circuit boards.

[00035] Fig. 6 shows a completed PWB 10 according to embodiments of the present invention. All layers 1-14, i.e., core and dielectric (e.g., pre-impregnated) layers 1-14 have been laminated and bonded. Signal plane assemblies may also be formed using other dielectric layers other than a pre-impregnated dielectric layer and still be within the scope of the present invention.

[00036] It should be understood that the embodiment described above is exemplary and that the layers are numbered for reference only. According to the invention, the number of layers required to build up the cavities is dependent upon the clearance required for embedding components and the thickness of these layers. A minimum number of layers to build up the cavities is one and a maximum number of layers is dependent upon the cavity thickness and layer thickness.

[00037] According to the instant inventive concept, a printed wiring circuit board (PWB) having active semiconductor devices and passive SMT chips embedded between PWB layers is provided.

[00038] The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments, not explicitly defined in the detailed description.

WHAT IS CLAIMED IS:

1. A manufacturing method of a printed wiring board assembly, the method comprising:
providing a carrier board comprising a plurality of core and pre-impregnated layers;
installing one or more components onto a support layer of said carrier board, wherein the one or more components are electrically coupled to the carrier board;
building up cavities around the one or more installed components using at least a first set of additional core and pre-impregnated layers;
installing at least a second set of additional layers above the built up cavities to embed said one or more components to form a printed wiring board assembly; and
laminating the printed wiring board assembly thereby causing the cavities to backfill with lamination.
2. A method according to claim 1, wherein the plurality of core and pre-impregnated layers of said carrier board are juxtaposed in an alternating sequence.
3. A method according to claim 1, wherein the first set of additional layers comprise a plurality of core and pre-impregnated layers.
4. A method according to claim 3, wherein the core and pre-impregnated layers comprising said first set of additional layers are juxtaposed in an alternating sequence.

5. A method according to claim 1, wherein the second set of additional layers are laminated as a lamina prior to being installed onto said support layer of said carrier board.

6. A method according to claim 3, wherein the core and pre-impregnated layers are juxtaposed in said lamina in an alternating sequence.

7. A method according to claim 1, wherein the second set of additional layers are a combination of core and pre-impregnated layers.

8. A method according to claim 1, wherein the step of building up cavities around the one or more installed components using said first set of additional layers, further comprises:

- (i) creating openings in the first set of additional layers; and
- (ii) installing said first set of additional layers including said created openings onto said support layer.

9. A method according to claim 1, wherein said components comprise active semiconductor devices.

10. A method according to claim 1, wherein said components comprise passive surface mount chips.

11. A method according to claim 1, wherein said step of laminating the printed wiring board assembly thereby causing the cavities to backfill with lamination further comprises: using a vacuum to pull air from said cavities to cause said cavities to become filled with residual resin/material from said pre-impregnated layers.

12. A printed wiring board assembly, comprising:
a plurality of core and pre-impregnated layers;
one or more components installed onto a support layer of said
printed
wiring board assembly, wherein the one or more components are
electrically coupled to the printed wiring board assembly; and
wherein the one or more components are situated inside cavities
internal to
the printed wiring board assembly.
13. A printed wiring board according to claim 12, wherein the printed
wiring
board is laminated.
14. A printed wiring board assembly according to claim 12, wherein the
core
and pre-impregnated layers are juxtaposed in an alternating sequence.
15. A printed wiring board assembly according to claim 12 comprising
at least
one core layer and at least two pre-impregnated layers.
16. A printed wiring board assembly wherein the printed wiring board
comprises:
a first set of layers comprising core and pre-impregnated layers;
a second set of layers comprising core and pre-impregnated
layers including cavities to accommodate one or more components;
a third set of layers comprising core and pre-impregnated layers for
encapsulating said cavities.
17. A printed wiring board assembly according to claim 16 wherein the
first,

second and third set of layers collectively comprise at least one core layer and at least two pre-impregnated layers.

18. A printed wiring board assembly according to claim 16, wherein the core and pre-impregnated layers of said first, second and third layers are juxtaposed in an alternating sequence.

19. A printed wiring board assembly according to claim 16, wherein the first set of layers are pre-constructed as a lamina.

20. A printed wiring board according to claim 16, wherein the printed wiring board is laminated.

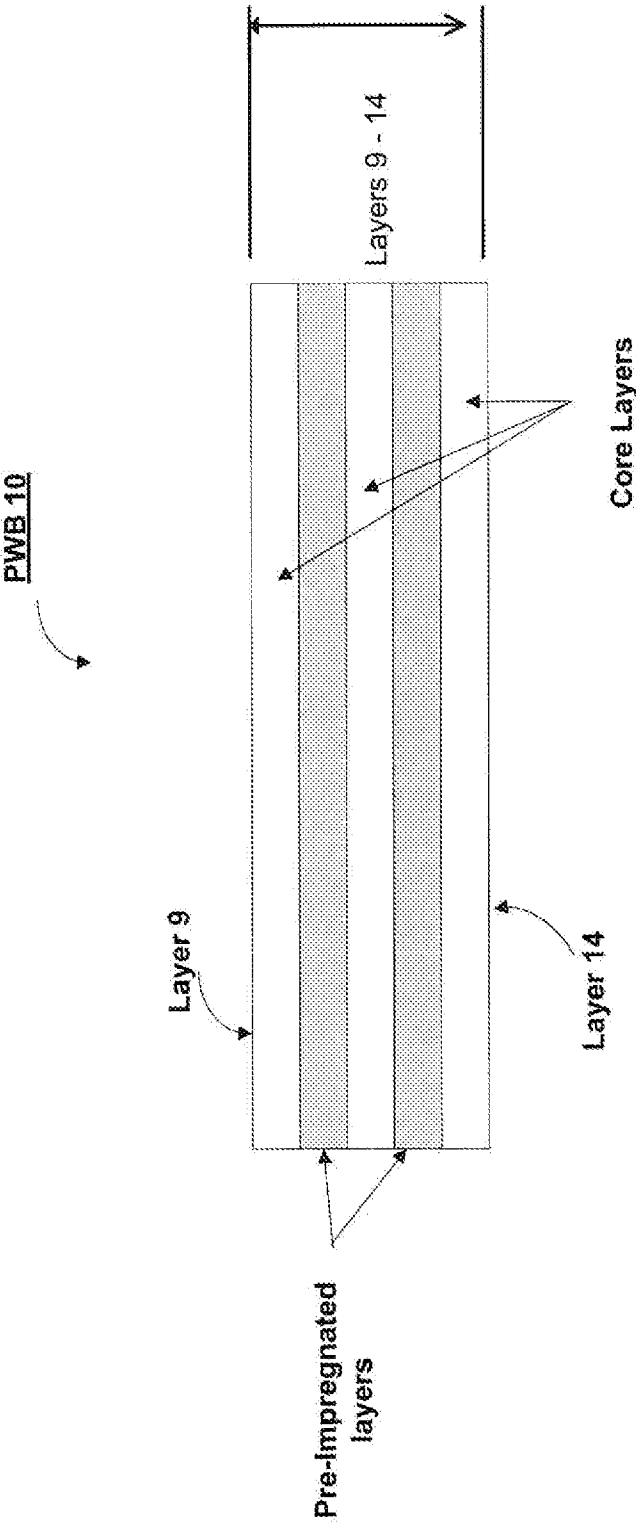


FIGURE 1

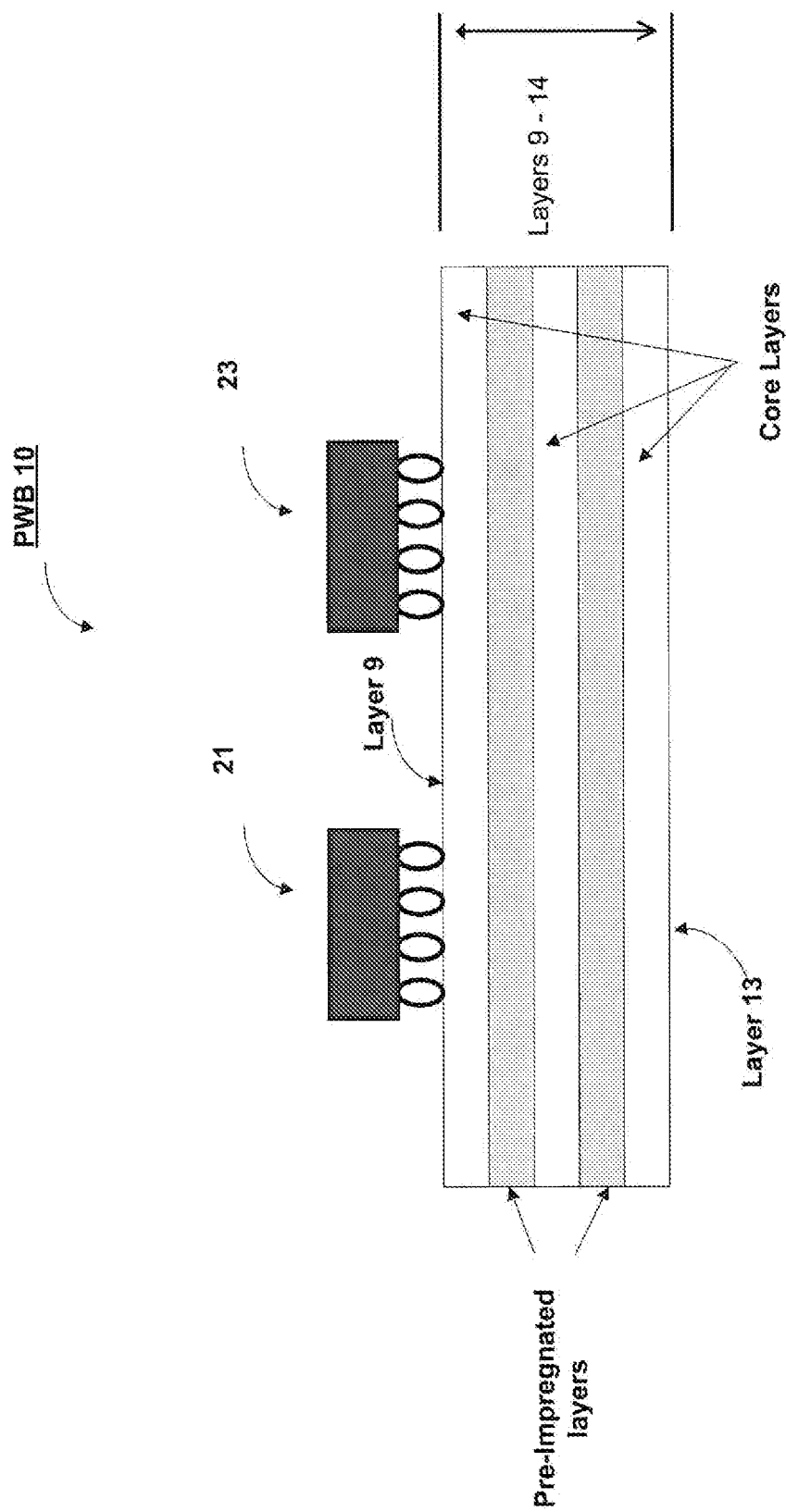


FIGURE 2

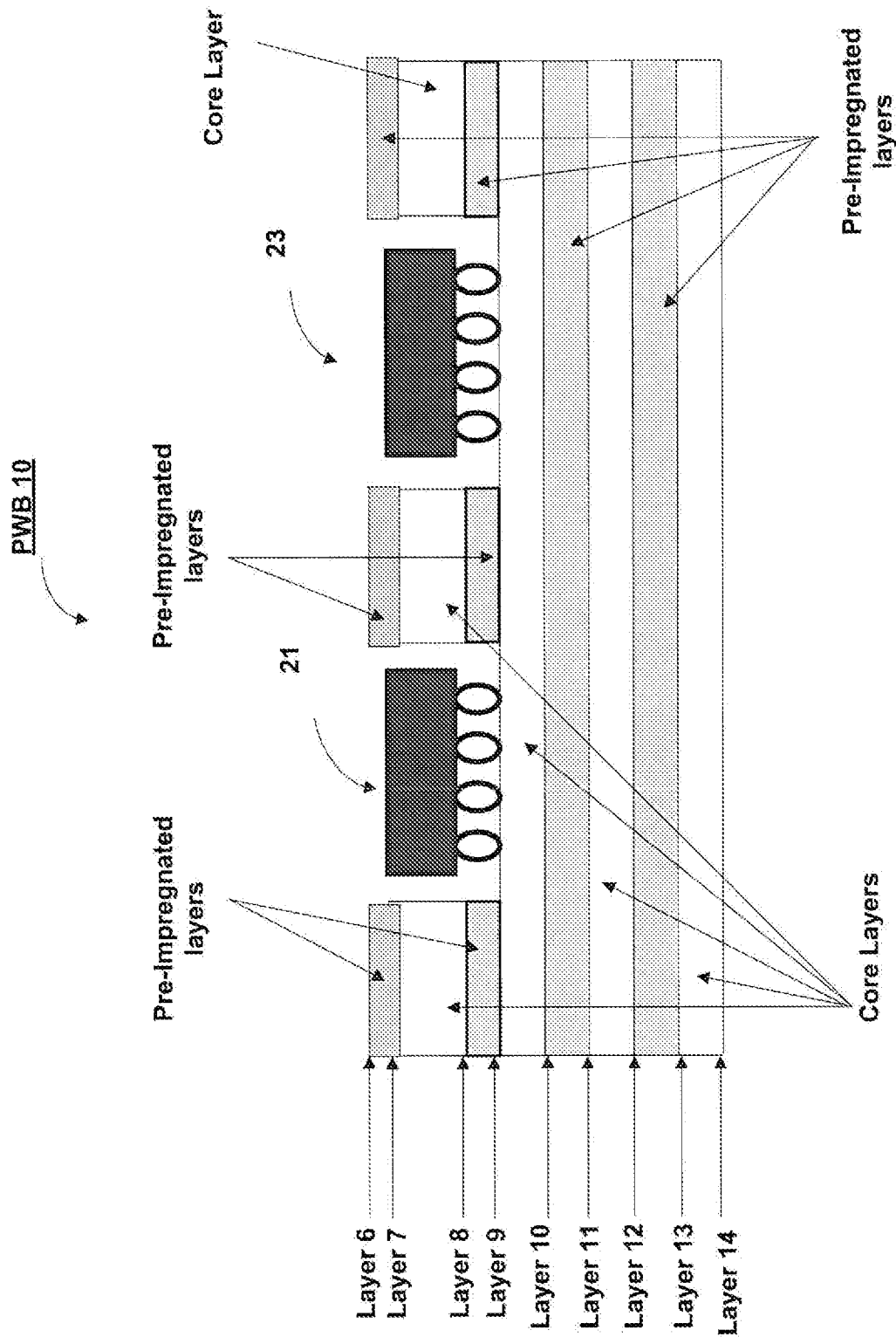


FIGURE 3

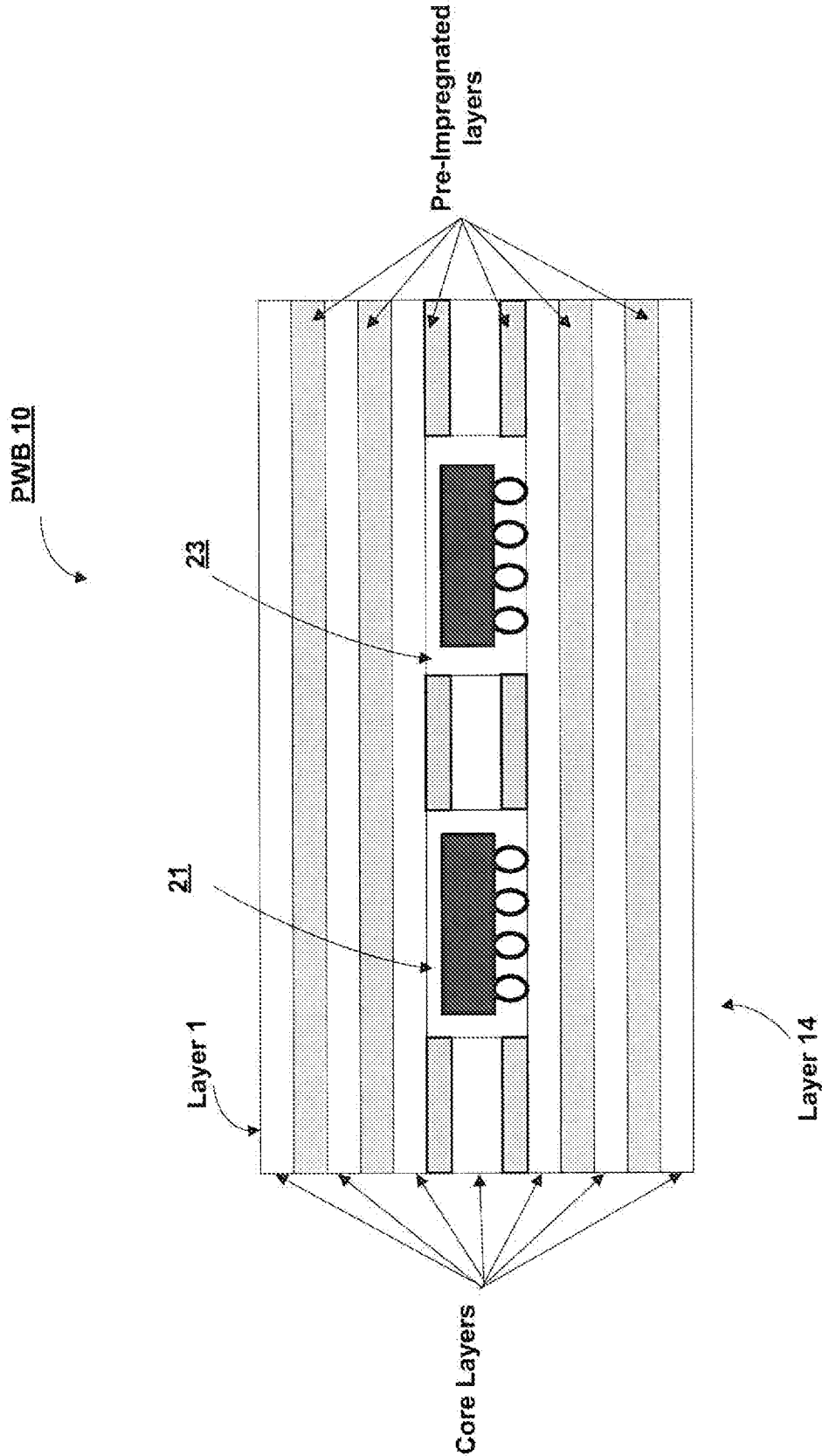


FIGURE 4

PWB 10

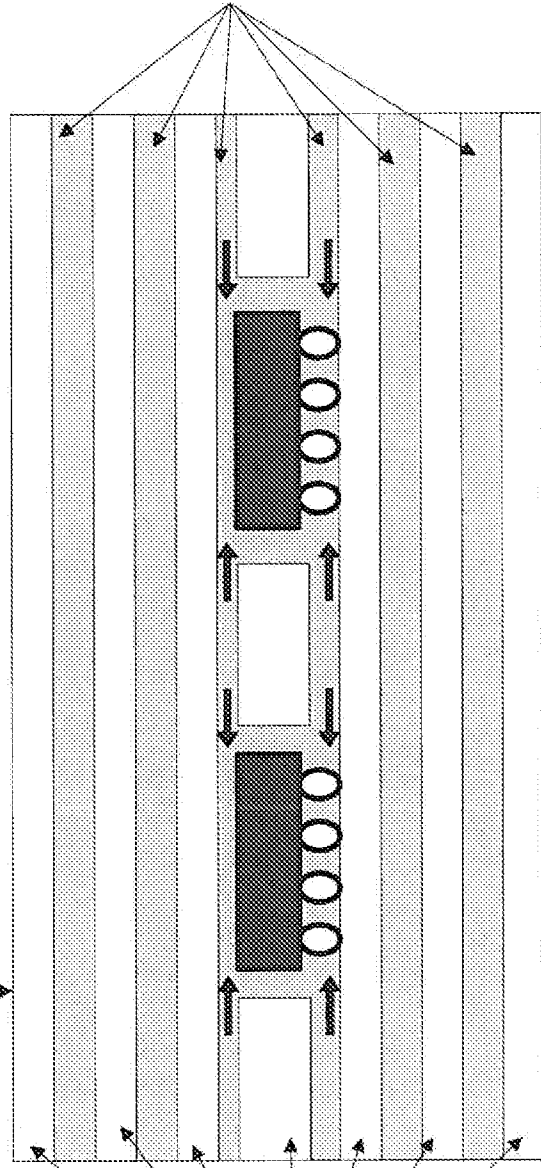
Layer 1

Layer 14

5/6
Pre-Impregnated
layers

Core Layers

FIGURE 5



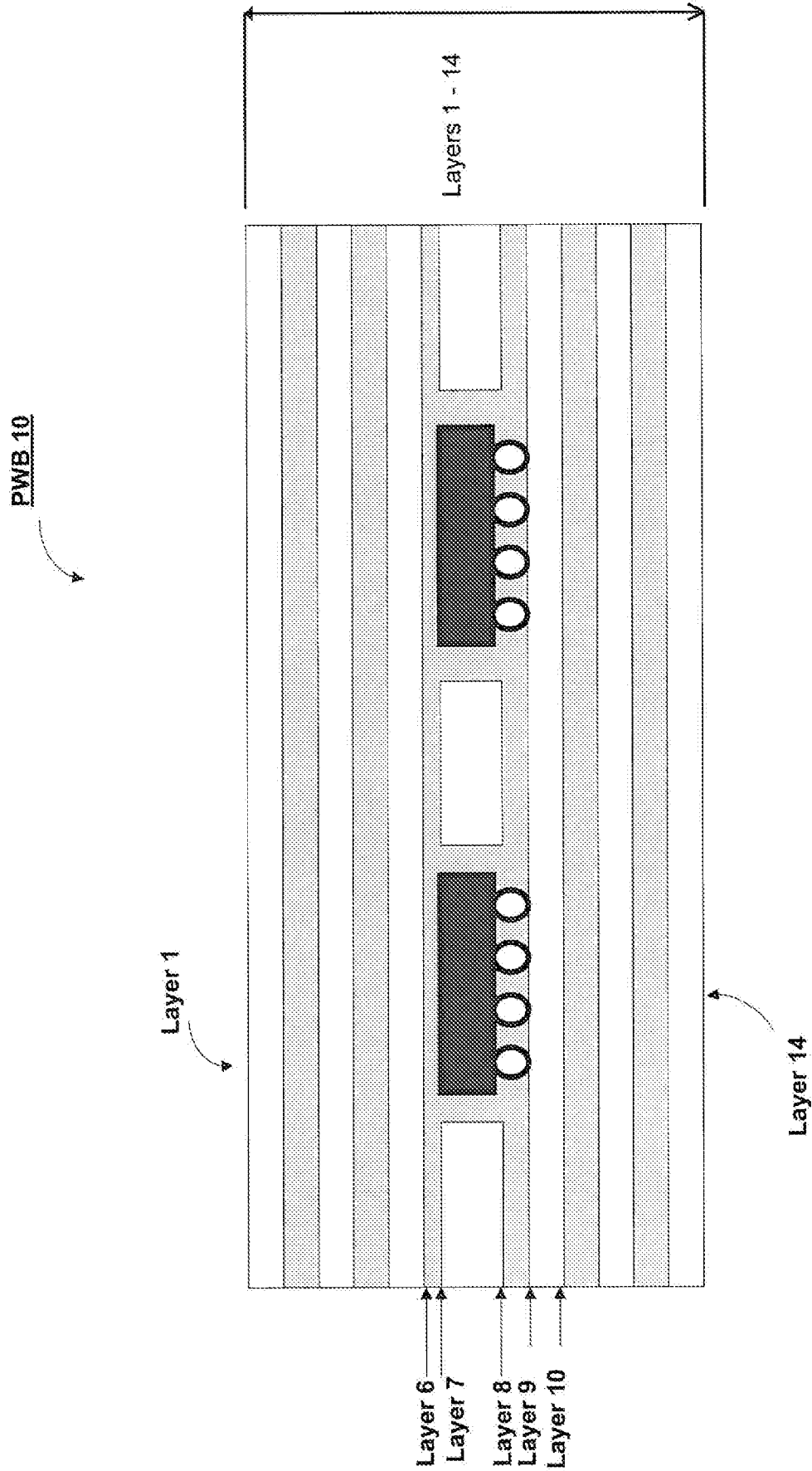


FIGURE 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2010/033682

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H05K 3/46 (2010.01)

USPC - 427/96.2

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - H05K 3/46 (2010.01)

USPC - 216/18; 257/E21.244, E21.275, E21.279, E21.293, E21.548; 427/96.2, 97.2

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatBase; Google Patents

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,429,132 B1 (HASKELL et al) 06 August 2002 (06.08.2002) entire document	1-20
A	US 5,629,242 A (NAGASHIMA et al) 13 May 1997 (13.05.1997) entire document	1-20
A	US 5,837,155 A (INAGAKI et al) 17 November 1998 (17.11.1998) entire document	1-20
A	US 5,837,427 A (HWANG et al) 17 November 1998 (17.11.1998) entire document	1-20

☐ Further documents are listed in the continuation of Box C.


* Special categories of cited documents:

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09 June 2010

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