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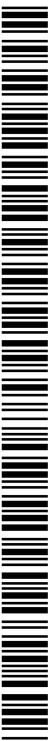

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(54) Title: UNIDIRECTIONAL METAL ON LAYER WITH EBEAM

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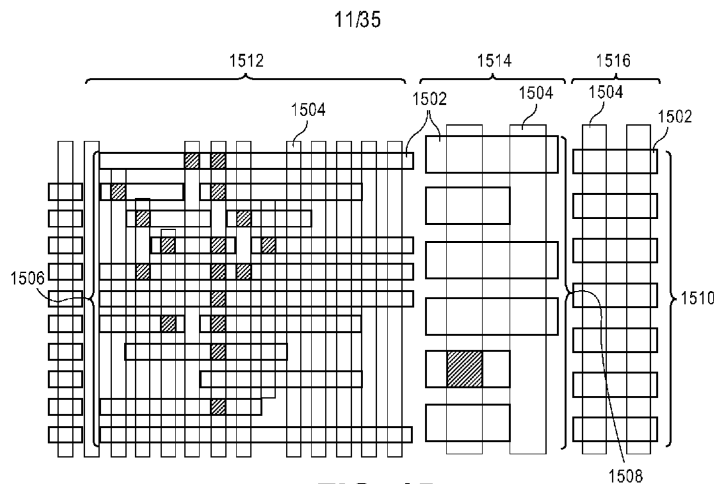


FIG. 15

(57) Abstract: Lithographic apparatuses suitable for, and methodologies involving, complementary e-beam lithography (CEBL) are described. In an example, a layout for a metallization layer of an integrated circuit includes a first region having a plurality of uni - directional lines of a first width and a first pitch and parallel with a first direction. The layout also includes a second region having a plurality of unidirectional lines of a second width and a second pitch and parallel with the first direction, the second width and the second pitch different than the first width and the first pitch, respectively. The layout also includes a third region having a plurality of unidirectional lines of a third width and a third pitch and parallel with the first direction, the third width and the third pitch differ - ent than the first and second widths and different than the first and second pitches.

UNIDIRECTIONAL METAL ON LAYER WITH EBEAM

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 62/012,220, filed on June 13, 2014, the entire contents of which are hereby incorporated by reference herein.

TECHNICAL FIELD

[0002] Embodiments of the invention are in the field of lithography and, in particular, lithography involving complementary e-beam lithography (CEBL).

BACKGROUND

[0003] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips.

[0004] Integrated circuits commonly include electrically conductive microelectronic structures, which are known in the art as vias. Vias can be used to electrically connect metal lines above the vias to metal lines below the vias. Vias are typically formed by a lithographic process. Representatively, a photoresist layer may be spin coated above a dielectric layer, the photoresist layer may be exposed to patterned actinic radiation through a patterned mask, and then the exposed layer may be developed in order to form an opening in the photoresist layer. Next, an opening for the via may be etched in the dielectric layer by using the opening in the photoresist layer as an etch mask. This opening is referred to as a via opening. Finally, the via opening may be filled with one or more metals or other conductive materials to form the via.

[0005] In the past, the sizes and the spacing of vias has progressively decreased, and it is expected that in the future the sizes and the spacing of the vias will continue to progressively decrease, for at least some types of integrated circuits (e.g., advanced microprocessors, chipset components, graphics chips, etc.). One measure of the size of the vias is the critical dimension of the via opening. One

measure of the spacing of the vias is the via pitch. Via pitch represents the center-to-center distance between the closest adjacent vias. When patterning extremely small vias with extremely small pitches by such lithographic processes, several challenges present themselves.

5 **[0006]** One such challenge is that the overlay between the vias and the overlying metal lines, and the overlay between the vias and the underlying metal lines, generally needs to be controlled to high tolerances on the order of a quarter of the via pitch. As via pitches scale ever smaller over time, the overlay tolerances tend to scale with them at an even greater rate than lithographic equipment is able to 10 scale with.

[0007] Another such challenge is that the critical dimensions of the via openings generally tend to scale faster than the resolution capabilities of lithographic scanners. Shrink technologies exist to shrink the critical dimensions of the via openings. However, the shrink amount tends to be limited by the minimum via 15 pitch, as well as by the ability of the shrink process to be sufficiently optical proximity correction (OPC) neutral, and to not significantly compromise line width roughness (LWR) and/or critical dimension uniformity (CDU).

[0008] Yet another such challenge is that the LWR and/or CDU characteristics of photoresists generally need to improve as the critical dimensions 20 of the via openings decrease in order to maintain the same overall fraction of the critical dimension budget. However, currently the LWR and/or CDU characteristics of most photoresists are not improving as rapidly as the critical dimensions of the via openings are decreasing. A further such challenge is that the extremely small via pitches generally tend to be below the resolution capabilities of even extreme 25 ultraviolet (EUV) lithographic scanners. As a result, commonly two, three, or more different lithographic masks may have to be used, which tends to increase the fabrication costs. At some point, if pitches continue to decrease, it may not be possible, even with multiple masks, to print via openings for these extremely small pitches using conventional scanners.

30 **[0009]** In the same vein, the fabrication of cuts (i.e., disruptions) in the metal line structures associated with metal vias is faced with similar scaling issues.

[0010] Thus, improvements are needed in the area of lithographic processing technologies and capabilities.

BRIEF DESCRIPTION OF THE DRAWINGS

5 **[0011]** Figure 1A illustrates a cross-sectional view of a starting structure following deposition, but prior to patterning, of a hardmask material layer formed on an interlayer dielectric (ILD) layer.

[0012] Figure 1B illustrates a cross-sectional view of the structure of Figure 1A following patterning of the hardmask layer by pitch halving.

10 **[0013]** Figure 2 illustrates cross-sectional views in a spacer-based-sextuple-patterning (SBSP) processing scheme which involves pitch division by a factor of six.

[0014] Figure 3 illustrates cross-sectional views in a spacer-based-nonuple-patterning (SBNP) processing scheme which involves pitch division by a factor of
15 nine.

[0015] Figure 4 is a cross-sectional schematic representation of an ebeam column of an electron beam lithography apparatus.

[0016] Figure 5 is a schematic demonstrating an optical scanner overlay limited by its ability to model in plane grid distortions (IPGD).

20 **[0017]** Figure 6 is a schematic demonstrating distorted grid information using an align on the fly approach, in accordance with an embodiment of the present invention.

[0018] Figure 7 provides a sample calculation showing the information to be transferred to pattern a general/conventional layout at 50% density on a 300 mm
25 wafer in contrast to a via pattern at 5% density, in accordance with an embodiment of the present invention.

[0019] Figure 8 illustrates a gridded layout approach for simplified design rule locations for vias, and cut start/stop, in accordance with an embodiment of the present invention.

30 **[0020]** Figure 9 illustrates the allowable placement of cuts, in accordance with an embodiment of the present invention.

[0021] Figure 10 illustrates a via layout among lines A and B, in accordance with an embodiment of the present invention.

[0022] Figure 11 illustrates a cut layout among lines A-E, in accordance with an embodiment of the present invention.

5 **[0023]** Figure 12 illustrates a wafer having a plurality of die locations thereon and an overlying dashed box representing a wafer field of a single column, in accordance with an embodiment of the present invention.

[0024] Figure 13 illustrates a wafer having a plurality of die locations thereon and an overlying actual target wafer field of a single column and increased 10 peripheral area for on the fly correction, in accordance with an embodiment of the present invention.

[0025] Figure 14 demonstrates the effect of a few degree wafer rotation on the area to be printed (inner dark, thin dashed) against the original target area (inner light, thick dashed), in accordance with an embodiment of the present invention.

15 **[0026]** Figure 15 illustrates a plan view of horizontal metal lines as represented overlaying vertical metal lines in the previous metallization layer, in accordance with an embodiment of the present invention.

[0027] Figure 16 illustrates a plan view of horizontal metal lines as represented overlaying vertical metal lines in the previous metallization layer, where 20 metal lines of differing width/pitch overlap in a vertical direction, in accordance with an embodiment of the present invention.

[0028] Figure 17 illustrates a plan view of conventional metal lines as represented overlaying vertical metal lines in the previous metallization layer.

[0029] Figure 18 illustrates an aperture (left) of a BAA relative to a line 25 (right) to be cut or to have vias placed in targeted locations while the line is scanned under the aperture.

[0030] Figure 19 illustrates two non-staggered apertures (left) of a BAA relative to two lines (right) to be cut or to have vias placed in targeted locations while the lines are scanned under the apertures.

30 **[0031]** Figure 20 illustrates two columns of staggered apertures (left) of a BAA relative to a plurality of lines (right) to be cut or to have vias placed in targeted

locations while the lines are scanned under the apertures, with scanning direction shown by the arrow, in accordance with an embodiment of the present invention.

[0032] Figure 21A illustrates two columns of staggered apertures (left) of a BAA relative to a plurality of lines (right) having cuts (breaks in the horizontal lines) or vias (filled-in boxes) patterned using the staggered BAA, with scanning direction shown by the arrow, in accordance with an embodiment of the present invention.

[0033] Figure 21B illustrates a cross-sectional view of a stack of metallization layers in an integrated circuit based on metal line layouts of the type illustrated in Figure 21A, in accordance with an embodiment of the present invention.

[0034] Figure 22 illustrates apertures of a BAA having a layout of three different staggered arrays, in accordance with an embodiment of the present invention.

[0035] Figure 23 illustrates apertures of a BAA having a layout of three different staggered arrays, where the ebeam covers only one of the arrays, in accordance with an embodiment of the present invention.

[0036] Figure 24A includes a cross-sectional schematic representation of an ebeam column of an electron beam lithography apparatus having a deflector to shift the beam, in accordance with an embodiment of the present invention.

[0037] Figure 24B illustrates a three (or up to n) pitch array for a BAA 2450 having pitch #1, cut #1, a pitch # 2, cut # 2 and a pitch # N, cut # N, in accordance with an embodiment of the present invention.

[0038] Figure 24C illustrates a zoom in slit for inclusion on an ebeam column, in accordance with an embodiment of the present invention.

[0039] Figure 25 illustrates apertures of a BAA having a layout of three different pitch staggered arrays, where the ebeam covers all of the arrays, in accordance with an embodiment of the present invention.

[0040] Figure 26 illustrates a three beam staggered aperture array (left) of a BAA relative to a plurality of large lines (right) having cuts (breaks in the horizontal lines) or vias (filled-in boxes) patterned using the BAA, with scanning direction shown by the arrow, in accordance with an embodiment of the present invention.

[0041] Figure 27 illustrates a three beam staggered aperture array (left) of a BAA relative to a plurality of medium sized lines (right) having cuts (breaks in the horizontal lines) or vias (filled-in boxes) patterned using the BAA, with scanning direction shown by the arrow, in accordance with an embodiment of the present invention.

[0042] Figure 28 illustrates a three beam staggered aperture array (left) of a BAA relative to a plurality of small lines (right) having cuts (breaks in the horizontal lines) or vias (filled-in boxes) patterned using the BAA, with scanning direction shown by the arrow, in accordance with an embodiment of the present invention.

[0043] Figure 29A illustrates a three beam staggered aperture array (left) of a BAA relative to a plurality of lines of varying size (right) having cuts (breaks in the horizontal lines) or vias (filled-in boxes) patterned using the BAA, with scanning direction shown by the arrow, in accordance with an embodiment of the present invention.

[0044] Figure 29B illustrates a cross-sectional view of a stack of metallization layers in an integrated circuit based on metal line layouts of the type illustrated in Figure 29A, in accordance with an embodiment of the present invention.

[0045] Figure 30 illustrates a three beam staggered aperture array (left) of a BAA relative to a plurality of lines of varying size (right) having cuts (breaks in the horizontal lines) or vias (filled-in boxes) patterned using the BAA, with scanning direction shown by the arrow, in accordance with an embodiment of the present invention.

[0046] Figure 31 illustrates three sets of lines of differing pitch with overlying corresponding apertures on each line, in accordance with an embodiment of the present invention.

[0047] Figure 32 illustrates a plurality of different sized lines (right) including one very large line, and a beam aperture arrays vertical pitch layout (three arrays) on a common grid, in accordance with an embodiment of the present invention.

[0048] Figure 33 illustrates a plurality of different sized lines (right), and a universal cutter pitch array (left), in accordance with an embodiment of the present invention.

[0049] Figure 34 demonstrates the 2* EPE rule for a universal cutter (left) as referenced against two lines (right), in accordance with an embodiment of the present invention.

[0050] Figure 35 illustrates a plan view and corresponding cross-sectional view of a previous layer metallization structure, in accordance with an embodiment of the present invention.

[0051] Figure 36A illustrates a cross-sectional view of a non-planar semiconductor device having fins, in accordance with an embodiment of the present invention.

[0052] Figure 36B illustrates a plan view taken along the a-a' axis of the semiconductor device of Figure 36A, in accordance with an embodiment of the present invention.

[0053] Figure 37 illustrates a computing device in accordance with one implementation of the invention.

[0054] Figure 38 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present invention.

[0055] Figure 39 is an interposer implementing one or more embodiments of the invention.

[0056] Figure 40 is a computing device built in accordance with an embodiment of the invention.

DESCRIPTION OF THE EMBODIMENTS

[0057] Lithographic apparatuses suitable for, and methodologies involving, complementary e-beam lithography (CEBL) are described. In the following description, numerous specific details are set forth, such as specific tooling, integration and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as single or dual damascene

processing, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale. In some cases, various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0058] One or more embodiments described herein are directed to lithographic approaches and tooling involving or suitable for complementary e-beam lithography (CEBL), including semiconductor processing considerations when implementing such approaches and tooling.

[0059] Complementary lithography draws on the strengths of two lithography technologies, working hand-in-hand, to lower the cost of patterning critical layers in logic devices at 20nm half-pitch and below, in high-volume manufacturing (HVM). The most cost-effective way to implement complementary lithography is to combine optical lithography with e-beam lithography (EBL). The process of transferring integrated circuit (IC) designs to the wafer entails the following: optical lithography to print unidirectional lines (either strictly unidirectional or predominantly unidirectional) in a pre-defined pitch, pitch division techniques to increase line density, and EBL to “cut” the lines. EBL is also used to pattern other critical layers, notably contact and via holes. Optical lithography can be used alone to pattern other layers. When used to complement optical lithography, EBL is referred to as CEBL, or complementary EBL. CEBL is directed to cutting lines and holes. By not attempting to pattern all layers, CEBL plays a complementary but crucial role in meeting the industry’s patterning needs at advanced (smaller) technology nodes (e.g., 10nm or smaller such as 7nm or 5nm technology nodes). CEBL also extends the use of current optical lithography technology, tools and infrastructure.

[0060] As mentioned above, pitch division techniques can be used to increase a line density prior to using EBL to cut such lines. In a first example, pitch halving can be implemented to double the line density of a fabricated grating

structure. Figure 1A illustrates a cross-sectional view of a starting structure following deposition, but prior to patterning, of a hardmask material layer formed on an interlayer dielectric (ILD) layer. Figure 1B illustrates a cross-sectional view of the structure of Figure 1A following patterning of the hardmask layer by pitch halving.

[0061] Referring to Figure 1A, a starting structure 100 has a hardmask material layer 104 formed on an interlayer dielectric (ILD) layer 102. A patterned mask 106 is disposed above the hardmask material layer 104. The patterned mask 106 has spacers 108 formed along sidewalls of features (lines) thereof, on the hardmask material layer 104.

[0062] Referring to Figure 1B, the hardmask material layer 104 is patterned in a pitch halving approach. Specifically, the patterned mask 106 is first removed. The resulting pattern of the spacers 108 has double the density, or half the pitch or the features of the mask 106. The pattern of the spacers 108 is transferred, e.g., by an etch process, to the hardmask material layer 104 to form a patterned hardmask 110, as is depicted in Figure 1B. In one such embodiment, the patterned hardmask 110 is formed with a grating pattern having unidirectional lines. The grating pattern of the patterned hardmask 110 may be a tight pitch grating structure. For example, the tight pitch may not be achievable directly through conventional lithography techniques. Even further, although not shown, the original pitch may be quartered by a second round of spacer mask patterning. Accordingly, the grating-like pattern of the patterned hardmask 110 of Figure 1B may have hardmask lines spaced at a constant pitch and having a constant width relative to one another. The dimensions achieved may be far smaller than the critical dimension of the lithographic technique employed.

[0063] Accordingly, as a first portion of a CEBL integration scheme, a blanket film may be patterned using lithography and etch processing which may involve, e.g., spacer-based-double-patterning (SBDP) or pitch halving, or spacer-based-quadruple-patterning (SBQP) or pitch quartering. It is to be appreciated that other pitch division approaches may also be implemented.

[0064] For example, Figure 2 illustrates cross-sectional views in a spacer-based-sextuple-patterning (SBSP) processing scheme which involves pitch division

by a factor of six. Referring to Figure 2, at operation (a), a sacrificial pattern X is shown following litho, slim and etch processing. At operation (b), spacers A and B are shown following deposition and etching. At operation (c), the pattern of operation (b) is shown following spacer A removal. At operation (d), the pattern of operation (c) is shown following spacer C deposition. At operation (e), the pattern of operation (d) is shown following spacer C etch. At operation (f), a pitch/6 pattern is achieved following sacrificial pattern X removal and spacer B removal.

[0065] In another example, Figure 3 illustrates cross-sectional views in a spacer-based-nonuple-patterning (SBNP) processing scheme which involves pitch division by a factor of nine. Referring to Figure 3, at operation (a), a sacrificial pattern X is shown following litho, slim and etch processing. At operation (b), spacers A and B are shown following deposition and etching. At operation (c), the pattern of operation (b) is shown following spacer A removal. At operation (d), the pattern of operation (c) is shown following spacer C and D deposition and etch. At operation (e), a pitch/9 pattern is achieved following spacer C removal.

[0066] In any case, in an embodiment, complementary lithography as described herein involves first fabricating a gridded layout by conventional or state-of the-art lithography, such as 193nm immersion lithography (193i). Pitch division may be implemented to increase the density of lines in the gridded layout by a factor of n. Gridded layout formation with 193i lithography plus pitch division by a factor of n can be designated as 193i + P/n Pitch Division. Patterning of the pitch divided gridded layout may then be patterned using electron beam direct write (EBDW) "cuts," as is described in greater detail below. In one such embodiment, 193nm immersion scaling can be extended for many generations with cost effective pitch division. Complementary EBL is used to break gratings continuity and to pattern vias.

[0067] More specifically, embodiments described herein are directed to patterning features during the fabrication of an integrated circuit. In one embodiment, CEBL is used to pattern openings for forming vias. Vias are metal structures used to electrically connect metal lines above the vias to metal lines below the vias. In another embodiment, CEBL is used to form non-conductive spaces or interruptions along the metal lines. Conventionally, such interruptions have been

referred to as "cuts" since the process involved removal or cutting away of portions of the metal lines. However, in a damascene approach, the interruptions may be referred to as "plugs" which are regions along a metal line trajectory that are actually not metal at any stage of the fabrication scheme, but are rather preserved regions
5 where metal cannot be formed. In either case, however, use of the terms cuts or plugs may be done so interchangeably. Via opening and metal line cut or plug formation is commonly referred to as back end of line (BEOL) processing for an integrated circuit. In another embodiment, CEBL is used for front end of line (FEOL) processing. For example, the scaling of active region dimensions (such as
10 fin dimensions) and/or associated gate structures can be performed using CEBL techniques as described herein.

[0068] As described above, electron beam (ebeam) lithography may be implemented to complement standard lithographic techniques in order to achieved desired scaling of features for integrated circuit fabrication. An electron beam
15 lithography tool may be used to perform the ebeam lithography. In an exemplary embodiment, Figure 4 is a cross-sectional schematic representation of an ebeam column of an electron beam lithography apparatus.

[0069] Referring to Figure 4, an ebeam column 400 includes an electron source 402 for providing a beam of electrons 404. The beam of electrons 404 is
20 passed through a limiting aperture 406 and, subsequently, through high aspect ratio illumination optics 408. The outgoing beam 410 is then passed through a slit 412 and may be controlled by a slim lens 414, e.g., which may be magnetic. Ultimately, the beam 404 is passed through a shaping aperture 416 (which may be a one-dimensional (1-D) shaping aperture) and then through a blanker aperture array
25 (BAA) 418. The BAA 418 includes a plurality of physical apertures therein, such as openings formed in a thin slice of silicon. It may be the case that only a portion of the BAA 418 is exposed to the ebeam at a given time. Alternatively, or in conjunction, only a portion 420 of the ebeam 404 that passes through the BAA 418 is allowed to pass through a final aperture 422 (e.g., beam portion 421 is shown as
30 blocked) and, possibly, a stage feedback deflector 424.

[0070] Referring again to Figure 4, the resulting ebeam 426 ultimately impinges as a spot 428 on a surface of a wafer 430, such as a silicon wafer used in

IC manufacture. Specifically, the resulting ebeam may impinge on a photo-resist layer on the wafer, but embodiments are not so limited. A stage scan 432 moves the wafer 430 relative to the beam 426 along the direction of the arrow 434 shown in Figure 4. It is to be appreciated that an ebeam tool in its entirely may include numerous columns 400 of the type depicted in Figure 4. Also, as described in some embodiments below, the ebeam tool may have an associated base computer, and each column may further have a corresponding column computer.

[0071] One drawback of state-of-the-art e-beam lithography is that it is not readily adoptable into a high volume manufacturing (HVM) environment for advanced integrated circuit manufacturing. Today's e-beam tooling and associated methodology has proven to be too slow with respect to throughput requirements for HVM wafer processing. Embodiments described herein are directed to enabling the use of EBL in an HVM environment. In particular, many embodiments described herein enable improved throughput in an EBL tool to allow for the use of EBL in an HVM environment.

[0072] Described below are seven different aspects of embodiments that can improve EBL beyond its current capabilities. It is to be appreciated that, although broken out as seven distinct aspects of embodiments, embodiments described below may be used independently or in any suitable combination to achieve improvements in EBL throughput for an HVM environment. As described in greater detail below, in a first aspect, alignment considerations for a wafer subjected to ebeam patterning on an ebeam tool are addressed. In a second aspect, data compression or data reduction for ebeam tool simplification is described. In a third aspect, the implementation of regions of uniform metal or other grating pattern density for an integrated circuit layout is described. In a fourth aspect, a staggered blanker aperture array (BAA) for an ebeam tool is described. In a fifth aspect, a three beam aperture array for an ebeam tool is described. In a sixth aspect, a non-universal cutter for an ebeam tool is described. In a seventh aspect, a universal cutter for an ebeam tool is described.

[0073] For all aspects, in an embodiment, when referring below to openings or apertures in a blanker aperture array (BAA), all or some of the openings or apertures of the BAA can be switched open or "closed" (e.g., by beam deflecting) as

the wafer/die moves underneath along a wafer travel or scan direction. In one embodiment, the BAA can be independently controlled as to whether each opening passes the ebeam through to the sample or deflects the beam into, e.g., a Faraday cup or blanking aperture. The ebeam column or apparatus including such a BAA may be built to deflect the overall beam coverage to just a portion of the BAA, and then individual openings in the BAA are electrically configured to pass the ebeam ("on") or not pass ("off"). For example, un-deflected electrons pass through to the wafer and expose a resist layer, while deflected electrons are caught in the Faraday cup or blanking aperture. It is to be appreciated that reference to "openings" or "opening heights" refers to the spot size impinged on the receiving wafer and not to the physical opening in the BAA since the physical openings are substantially larger (e.g., micron scale) than the spot size (e.g., nanometer scale) ultimately generated from the BAA. Thus, when described herein as the pitch of a BAA or column of openings in a BAA being said to "correspond" to the pitch of metal lines, such description actually refers to the relationship between pitch of the impinging spots as generated from the BAA and the pitch of the lines being cut. As an example provided below, the spots generated from the BAA 2110 have a pitch the same as the pitch of the lines 2100 (when both columns of BAA openings are considered together). Meanwhile, the spots generated from only one column of the staggered array of the BAA 2110 have twice the pitch as the pitch of the lines 2100.

[0074] For all aspects, it is also to be appreciated that, in some embodiments, an ebeam column as described above may also include other features in addition to those described in association with Figure 4. For example, in an embodiment, the sample stage can be rotated by 90 degrees to accommodate alternating metallization layers which may be printed orthogonally to one another (e.g., rotated between X and Y scanning directions). In another embodiment, an e-beam tool is capable of rotating a wafer by 90 degrees prior to loading the wafer on the stage. Other additional embodiments are described below in association with Figures 24A-24C.

[0075] In a first aspect of embodiments of the present invention, alignment considerations for a wafer subjected to ebeam patterning on an ebeam tool are addressed.

[0076] Approaches described below may be implemented to overcome excessive contribution to edge placement error (EPE) from layer to layer physical overlay when a layer is patterned by an imaging tool (e.g., an optical scanner). In an embodiment, the approaches described below are applicable for an imaging tool that otherwise uses preselected sampling of wafer coordinate system markers (i.e., alignment marks) to estimate wafer processing induced in-plane grid distortion parameters on a processed wafer. The collected alignment information (e.g., sampled wafer in plane grid distortion) is typically fit to a predefined order polynomial. The fit is then typically used as a representation of a distorted grid to adjust various scanner printing parameters and to achieve the best possible overlay between underlying and printed layers.

[0077] Instead, in an embodiment, use of an ebeam for patterning allows for collection of alignment information during a write at any point on the pattern ("align on the fly") containing underlying layer features, and not only on every die. For example, an electron detector is placed at the ebeam column bottom in order to collect backscattered electrons from alignment marks or other underlying patterned feature. A straight forward linear model allows for collection of such information hundreds of time within every die as an ebeam column writes (and the detector detects) while the stage is scanning underneath the column during die exposure. In one such embodiment, there is no need for fitting polynominal and estimating complex correction parameters of higher orders. Rather, only simple linear corrections can be used.

[0078] In an embodiment, in practice, multiple (hundreds) time positions of the ebeam can and will be registered against alignment marks patterned on a previous layer in scribe lines as well as inside active areas of the dies. The registering may be performed using drop in cells usually present for the purpose of characterizing patterning characteristics of a layer pattern to be exposed without loss of tool throughput of COO (cost of ownership).

[0079] In the case that on-the-fly alignment is not implemented, the alternative is to use higher order polynomials, as described above. However, alignment based on higher order polynomials is used to fit relatively sparse alignment information (e.g., only 10-15% of dies locations to be patterned are used

to collect in-plane grid distortions on the wafer), whereas un-modeled (residual) fit errors constitute about 50% of maximum total overlay predicted errors. Collecting much more dense alignment information and using even higher order polynominal for fit and patterning correction might improve overlay somewhat yet this will be
5 achieved at significant throughput and cost of ownership loss.

[0080] To provide context, wafer processing induced in-plane grid distortion occurs from multiple sources, including but not limited to backscatter/field displacement errors due to metal/other layers underneath the pattern being printed, wafer bowing/localized incremental wafer expansion due to pattern writing heat
10 effects, and other additional effects that contribute greatly to EPE. If corrections are not made, the likelihood of patterning a wafer with localized gross patterning misalignment is very high.

[0081] Figure 5 is a schematic demonstrating an optical scanner overlay limited by its ability to model in plane grid distortions (IPGD). Referring to the left-
15 hand portion 502 of Figure 5, a die grid 504 on a wafer 506 is distorted by wafer processing. Vectors indicate corners displacement of every die versus the initial positioning (e.g., first layer print). Referring to the right-hand portion 510 of Figure 5, a conventional stepper will collect relatively sparse distorted grid information on this layer, as represented by the dots 512. Accordingly, using higher order
20 polynomials allows fitting of relatively sparse alignment information. The number of locations is optimized for "acceptable" residuals after the model fits to grid representation obtained from grid coordinate information in the sampled locations. Overhead time is needed to collect this information.

[0082] In contrast to the relatively sparse distorted grid information collected
25 as represented in Figure 5, Figure 6 is a schematic demonstrating distorted grid information using an align on the fly approach, in accordance with an embodiment of the present invention. Referring to Figure 6, as an ebeam writes every die, the detector at the column bottom collects information about positional coordinated of an underlying layer. Necessary adjustment to writing position can be performed
30 through stage position control in real time everywhere on the wafer at no or minimal overhead time increase or throughput loss. In particular, Figure 6 illustrates the

same plot 602 as provided in Figure 5. A zoomed-in exemplary die region 604 illustrates the scanning directions 606 within the die region 604.

[0083] In a second aspect of embodiments of the present invention, data compression or data reduction for ebeam tool simplification is described.

5 **[0084]** Approaches described herein involve restricting data to allow massive compression of data, reducing a data path and ultimately providing for a much simpler ebeam writing tool. More particularly, embodiments described enable significant reduction in the amount of data that must be passed to an ebeam column of an ebeam tool. A practical approach is provided for allowing a sufficient amount
10 of data to write the column field and adjust the column field for field edge placement error, while keeping within the electrical bandwidth limits of the physical hardware. Without implementing such embodiments, the required bandwidth is approximately 100 times that possible by today's electronics. In an embodiment, data reduction or compression approaches described herein can be implemented to
15 substantially increase throughput capabilities of an EBL tool. By increasing the throughput capabilities, EBL can more readily be adopted in an HVM environment, such as into an integrated circuit manufacturing environment.

[0085] Figure 7 provides a sample calculation showing the information to be transferred to pattern a general/conventional layout at 50% density on a 300 mm
20 wafer in contrast to a via pattern at 5% density, in accordance with an embodiment of the present invention. Referring to Figure 7, information to be transferred is according to equation (A). Information transfer is according to equation (B) with information loss due to edge placement error (EPE) uncertainty (Ap) is minimal resolved feature, and ΔPV is equal to 2EPE. Assuming EBDW tool resolution of
25 AP is equal to 10nm and EPE is equal to 2.5 nm, the information volume to be transferred by such a general purpose imaging system in $1m^2$ (assuming 50% pattern density) will be according to equation (C). A 300 mm wafer area is $706cm^2$ which is $0.0706m^2$. Correspondingly, to pattern a general layout at 50% density on a 300mm wafer, the number of bytes needed to be transferred is according to equation
30 (D). The result is 70TB to be transferred in 6 minutes assuming 10wph TPT for a transfer rate of 194.4 GB/s. In accordance with an embodiment of the present invention, an EBDW tool that is designed to print vias (and/or cuts) at a pattern

density of approximately 10% will require correspondingly smaller information to be transferred, e.g., at a realistic 40GB/s transfer rate. In a specific embodiment, an EBDW tool is designed to print vias (and/or cuts) at a pattern density of approximately 5% and requires correspondingly smaller information to be transferred, e.g., 7TB at a realistic 20GB/s transfer rate.

[0086] With reference again to Figure 7, the information transfer is reduced to a relative (integerized) distance instead of transferring absolute 64bit coordinates. By using an ebeam tool to pattern only vias at less than approximately 10% density, and even as low as 5% density, versus a general layout pattern at 50% density, for example, a reduction in the amount of data transfer from 70+TB in 6 minutes to less than 7TB in 6 minutes can be realized, allowing the ebeam apparatus to achieve the manufacturing throughput needed for high volume production.

[0087] In an embodiment, one or more of the following four approaches is implemented for data reduction: (1) all design rules for vias and cuts are simplified to reduce the number of positions that a via can occupy, and where the start and stop of a line cut is possibly located; (2) encryption of placement of cut starts and stops, as well as distances between vias, is encrypted as n*min distance (this removes the need to send 64 bit address for each start and stop location for a cut, as well as for via locations); (3) for each column in the tool, only the data required to make the cuts and vias that fall within this section of the wafer are forwarded to the column computer (each column receives only the data needed, in a form encrypted as in part 2); and/or (4) for each column in the tool, the area that is transmitted is increased by n lines at top, bottom and additional breadth in x is also allowed (accordingly, the associated column computer can adjust on the fly for changes in wafer temperature and alignment without having the entire wafer data transmitted). In an embodiment, implementation of one or more such data reduction approaches enables simplification of an ebeam tool at least to some extent. For example, a dedicated computer or processor normally associated with a single dedicated column in a multi-column ebeam tool may be simplified or even altogether eliminated. That is, a single column equipped with on-board dedicated logic capability may be simplified to move the logic capability off-board or to reduce to amount of on-board logic capability required for each individual column of the ebeam tool.

[0088] With respect to approach (1) above, Figure 8 illustrates a gridded layout approach for simplified design rule locations for vias, and cut start/stop, in accordance with an embodiment of the present invention. A horizontal grid 800 includes a regular arrangement of line positions, with solid lines 802 representing actual lines and dashed lines 804 representing unoccupied line positions. The key to this technique is that vias (filled-in boxes 806) are on a regular grid (shown as the vertical grid 808 in Figure 8) and are printed in the scan direction 810 parallel with the metal lines (horizontal rectangles with solid outline) that are below the vias. The requirement for this design system is that via locations 806 are formed only in alignment with the vertical grid 808.

[0089] With respect to cuts, cuts are made with a grid that is finer than the via grid. Figure 9 illustrates the allowable placement of cuts, in accordance with an embodiment of the present invention. Referring to Figure 9, an array of lines 902 has vias 904 positioned therein according to grid 906. The allowable placement of cuts (e.g., labeled cuts 908, 910 and 912) is indicated by the vertical dashed lines 914, with the via locations continuing as vertical solid lines 906. The cuts always start, and stop, exactly on the grid 914, which is key to reducing the amount of data transferred from the base computer down to the column computer. It is to be appreciated, however, that the position of the dashed vertical lines 914 appears to be a regular grid, but that is not a requirement. Instead, the pair of lines centered around the via cut lines is the known distance of –xn and +xn relative to the via location. The via locations are a regular grid that is spaced every m units along the cut direction.

[0090] With respect to approach (2) above, distance-based encryption of cuts and vias may be used to eliminate the need to send 64 bit full addresses. For example, rather than sending absolute 64 bit (or 128 bit) addresses for x, and y positions, the distance along the direction of travel from the left edge (for wafer lines printing in direction moving to right) or from the right edge (for wafer lines printing in the direction moving to the left) is encrypted. The pair of lines centered around the via lines is the known distance of –xn and +xn relative to the via location, and the via locations are a regular grid that is spaced every m units along the cut direction. Any via print location can thus be encrypted as a distance from

zero to the numbered via location (spaced m units apart). This significantly reduces the amount of positioning data that must be transmitted.

[0091] The amount of information can be further reduced by providing the machine with the relative count of vias from the previous via. Figure 10 illustrates a via layout among lines A and B, in accordance with an embodiment of the present invention. Referring to Figure 10, the two lines as shown can be reduced as follows: line A: via 1002 spacing +1,+4,+1,+2; line B: via 1004 spacing +9. The via 1002/1004 spacing is according to grid 1006. It is to be appreciated that additional communication theory of assignment of most likely terms could be further performed to reduce the data space. Even so, even ignoring such further reduction yields an excellent improvement using straight forward compression to reduce 4 vias of 64 bits position, to just a handful of bits.

[0092] Similarly, the start and stop of cuts can be reduced to eliminate the need to send 64 bits (or 128 bits) of positional information for each cut. Like a light switch, starting a cut means the next data point is the end of cut, and similarly the next location is the start of the next cut. Since it is known that cuts end +xn in the direction of travel from via locations (and similarly start at –xn), depending upon cut start/stop, the via location can be encoded and the local column computer can be instructed reapply the offset from the via location. Figure 11 illustrates a cut layout among lines A-E, in accordance with an embodiment of the present invention. Referring to Figure 11, a substantial decrease over sending absolute 64 (or 128) bit locations results: spacing from previous cut: A: +5 (shown as space 1102), +1; B: x <no cuts> (whatever x is encrypted as—no cuts for distance); C: +1 (the stopping point of the cut at the left), +4 (the start of the large cut aligned vertically with the start of cut 1102) +3 (the end of the large cut); D: +3, +4; E: +3, +2, +1, +4.

[0093] With respect to approach (3) above, for each column, the data transmitted for cuts and vias is restricted to just that required for the wafer field that falls under the given column. In an example, Figure 12 illustrates a wafer 1200 having a plurality of die locations 1202 thereon and an overlying dashed box 1204 representing a wafer field of a single column, in accordance with an embodiment of the present invention. Referring to Figure 12, the data transmitted to the local

column computer is limited to only the lines that occur in the printed region shown in dotted lines of box 1204.

[0094] With respect to approach (4) above, since correction for wafer bow, heating, and chuck misalignment by an angle theta must be done on the fly, the actual region transmitted to the column computer is a few lines larger top and bottom, as well as additional data to the left and right. Figure 13 illustrates a wafer 1300 having a plurality of die locations 1302 thereon and an overlying actual target wafer field 1304 of a single column. As shown in Figure 13, an increased peripheral area 1306 is provided to account for on the fly correction, in accordance with an embodiment of the present invention. Referring to Figure 13, while the increased peripheral area 1306 slightly increases the amount of data transmitted to the column computer, it also allows the column printing to correct for wafer misalignment resulting from a myriad of issues by allowing the column to print outside its normal region. Such issues may include wafer alignment issues or local heating issues, etc.

[0095] Figure 14 demonstrates the effect of a few degree wafer rotation on the area to be printed (inner dark, thin dashed box 1402) against the original target area (inner light, thick dashed box 1304) from Figure 13, in accordance with an embodiment of the present invention. Referring to Figure 14, the column computer is able to use the additional transmitted data to make the necessary printing changes without requiring a complex rotational chuck on the machine (which would otherwise limit the speed of the printing).

[0096] In a third aspect of embodiments of the present invention, the implementation of regions of uniform metal or other grating pattern density for an integrated circuit layout is described.

[0097] In an embodiment, in order to improve throughput of an ebeam apparatus, design rules for interconnect layers are simplified to enable a fixed set of pitches that can be used for logic, SRAM, and Analog/IO regions on the die. In one such embodiment, the metal layout further requires that the wires be unidirectional with no jogs, orthogonal direction wires, or hooks on the ends, as is currently used to enable via landings in conventional, non-ebeam lithography processes.

[0098] In a particular embodiment, three different wire widths of unidirectional wire are permitted within each metallization layer. Gaps in the wires

are cut precisely, and all to the vias are self-aligned to a maximum allowed size. The latter is an advantage in minimizing via resistance for extremely fine pitch wiring. The approach described herein permits an efficient ebeam line cut and via printing with ebeam that achieves orders of magnitude improvement over existing 5 ebeam solutions.

[0099] Figure 15 illustrates a plan view of horizontal metal lines 1502 as represented overlaying vertical metal lines 1504 in the previous metallization layer, in accordance with an embodiment of the present invention. Referring to Figure 15, three different pitch/widths 1506, 1508 and 1510 of wires are permitted. The 10 different line types may be segregated into chip regions 1512, 1514 and 1516, respectively, as shown. It is to be appreciated that regions are generally larger than shown, but to draw to scale would make the detail on the wires comparatively small. Such regions on the same layer may be fabricated first using conventional lithography techniques.

15 **[00100]** The advances described in embodiments herein permit precise wire trimming and fully self-aligned vias between layers. It is to be appreciated that trims occur as needed with no trim-trim (plug) rules required as in current litho-based processes. Furthermore, in an embodiment, via-via rules are significantly removed. Vias of the density and relationship shown would be difficult or impossible to print 20 using current optical proximity correction (OPC)-enabled lithography capability. Similarly, the plug/cut rules that would otherwise preclude some of the cuts shown are removed through use of this technique. As such, the interconnect/via layers are less limiting to the design of circuits.

[00101] Referring again to Figure 15, in the vertical direction, lines of 25 different pitches and widths are not overlapping, i.e., each region is segregated in a vertical direction. By contrast, Figure 16 illustrates a plan view of horizontal metal lines 1602 as represented overlaying vertical metal lines 1604 in the previous metallization layer, where metal lines of differing width/pitch overlap in a vertical direction, in accordance with an embodiment of the present invention. For example, 30 lines pair 1606 overlap in the vertical direction, and lines pair 1608 overlap in the vertical direction. Referring again to Figure 16, the regions may be fully overlapping. The wires of all three sizes may be interdigitated, if enabled by the

lines fabrication method, yet cuts and vias continue to be fully enabled by a universal cutter, as described below in association with another aspect of embodiments of the present invention.

[00102] To provide context, Figure 17 illustrates a plan view of conventional metal lines 1702 as represented overlaying vertical metal lines in the previous metallization layer. Referring to Figure 17, in contrast to the layouts of Figures 15 and 16, bi-directional wires are used conventionally. Such wiring adds orthogonal wiring in the form of long orthogonal wires, short jogs between tracks to change lanes, and “hooks” at the ends of wires to place a via such that line pullback does not encroach the vias. Examples of such constructs are shown at the X positions in Figure 17. It could be argued that allowance of such orthogonal constructs provides some small density advantage (particularly the track jog at the upper X), but these significantly add design rule complexity/design rule checking as well as preclude a tool such as the ebeam methodology from achieving needed throughput. Referring again to Figure 17, it is to be appreciated that conventional OPC/lithography would preclude some of the vias shown on the left hand side from actually being fabricated.

[00103] In a fourth aspect of embodiments of the present invention, a staggered blanker aperture array (BAA) for an ebeam tool is described.

[00104] In an embodiment, a staggered beam aperture array is implemented to solve throughput of an ebeam machine while also enabling minimum wire pitch. With no stagger, consideration of edge placement error (EPE) means that a minimum pitch that is twice the wire width cannot be cut since there is no possibility of stacking vertically in a single stack. For example, Figure 18 illustrates an aperture 1800 of a BAA relative to a line 1802 to be cut or to have vias placed in targeted locations while the line is scanned along the direction of the arrow 1804 under the aperture 1800. Referring to Figure 18, for a given line 1802 to be cut or vias to be placed, the EPE 1806 of the cutter opening (aperture) results in a rectangular opening in the BAA grid that is the pitch of the line.

[00105] Figure 19 illustrates two non-staggered apertures 1900 and 1902 of a BAA relative to two lines 1904 and 1906, respectively, to be cut or to have vias placed in targeted locations while the lines are scanned along the direction of the

arrow 1908 under the apertures 1900 and 1902. Referring to Figure 19, when the rectangular opening 1800 of Figure 18 is placed in a vertical single column with other such rectangular openings (e.g., now as 1900 and 1902), the allowed pitch of the lines to be cut is limited by 2x EPE 1910 plus the distance requirement 1912
5 between the BAA opens 1900 and 1902 plus the width of one wire 1904 or 1906. The resulting spacing 1914 is shown by the arrow on the far right of Figure 19. Such a linear array would severely limit the pitch of the wiring to be substantially greater than 3-4x of the width of the wires, which may be unacceptable. Another unacceptable alternative would be to cut tighter pitch wires in two (or more) passes
10 with slightly offset wire locations; this approach could severely limit the throughput of the ebeam machine.

[00106] By contrast to Figure 19, Figure 20 illustrates two columns 2002 and 2004 of staggered apertures 2006 of a BAA 2000 relative to a plurality of lines 2008 to be cut or to have vias placed in targeted locations while the lines 2008 are
15 scanned along the direction 2010 under the apertures 2006, with scanning direction shown by the arrow, in accordance with an embodiment of the present invention. Referring to Figure 19, a staggered BAA 2000 includes two linear arrays 2002 and 2004, staggered spatially as shown. The two staggered arrays 2002 and 2004 cut (or place vias at) alternate lines 2008. The lines 2008 are, in one embodiment, placed
20 on a tight grid at twice the wire width. As used throughout the present disclosure, the term staggered array can refer to a staggering of openings 2006 that stagger in one direction (e.g., the vertical direction) and either have no overlap or have some overlap when viewed as scanning in the orthogonal direction (e.g., the horizontal direction). In the latter case, the effective overlap provides for tolerance in
25 misalignment.

[00107] It is to be appreciated that, although a staggered array is shown herein as two vertical columns for simplicity, the openings or apertures of a single "column" need not be columnar in the vertical direction. For example, in an embodiment, so long as a first array collectively has a pitch in the vertical direction,
30 and a second array staggered in the scan direction from the first array collectively has the pitch in the vertical direction, the a staggered array is achieved. Thus, reference to or depiction of a vertical column herein can actually be made up of one

or more columns unless specified as being a single column of openings or apertures. In one embodiment, in the case that a "column" of openings is not a single column of openings, any offset within the "column" can be compensated with strobe timing. In an embodiment, the critical point is that the openings or apertures of a staggered array of a BAA lie on a specific pitch in the first direction, but are offset in the second direction to allow them to place cuts or vias without any gap between cuts or vias in the first direction.

[00108] Thus, one or more embodiments are directed to a staggered beam aperture array where openings are staggered to allow meeting EPE cuts and/or via requirements as opposed to an inline arrangement that cannot accommodate for EPE technology needs. By contrast, with no stagger, the problem of edge placement error (EPE) means that a minimum pitch that is twice the wire width cannot be cut since there is no possibility of stacking vertically in single stack. Instead, in an embodiment, use of a staggered BAA enables much greater than 4000 times faster than individually ebeam writing each wire location. Furthermore, a staggered array allows a wire pitch to be twice the wire width. In a particular embodiment, an array has 4096 staggered openings over two columns such that EPE for each of the cut and via locations can be made. It is to be appreciated that a staggered array, as contemplated herein, may include two or more columns of staggered openings.

[00109] In an embodiment, use of a staggered array leaves space for including metal around the apertures of the BAA which contain one or two electrodes for passing or steering the ebeam to the wafer or steering to a Faraday cup or blanking aperture. That is, each opening may be separately controlled by electrodes to pass or deflect the ebeam. In one embodiment, the BAA has 4096 openings, and the ebeam apparatus covers the entire array of 4096 openings, with each opening electrically controlled. Throughput improvements are enabled by sweeping the wafer under the opening as shown by the thick black arrows.

[00110] In a particular embodiment, a staggered BAA has two rows of staggered BAA openings. Such an array permits tight pitch wires, where wire pitch can be 2x the wire width. Furthermore, all wires can be cut in a single pass (or vias can be made in a single pass), thereby enabling throughput on the ebeam machine. Figure 21A illustrates two columns of staggered apertures (left) of a BAA relative to

a plurality of lines (right) having cuts (breaks in the horizontal lines) or vias (filled-in boxes) patterned using the staggered BAA, with scanning direction shown by the arrow, in accordance with an embodiment of the present invention.

[00111] Referring to Figure 21A, the line result from a single staggered array could be as depicted, where lines are of single pitch, with cuts and vias patterned. In particular, Figure 21A depicts a plurality of lines 2100 or open line positions 2102 where no lines exist. Vias 2104 and cuts 2106 may be formed along lines 2100. The lines 2100 are shown relative to a BAA 2110 having a scanning direction 2112. Thus, Figure 21A may be viewed as a typical pattern produced by a single staggered array. Dotted lines show where cuts occurred in the patterned lines (including total cut to remove a full line or line portion). The via locations 2104 are patterning vias that land on top of the wires 2100.

[00112] In an embodiment, all or some of the openings or apertures of the BAA 2110 can be switched open or "closed" (e.g., beam deflecting) as the wafer/die moves underneath along the wafer travel direction 2112. In an embodiment, the BAA can be independently controlled as to whether each opening passes the ebeam through to the sample or deflects the beam into, e.g., a Faraday cup or blanking aperture. The apparatus may be built to deflect the overall beam coverage to just a portion of the BAA, and then individual openings in the BAA are electrically configured to pass the ebeam ("on") or not pass ("off"). It is to be appreciated that reference to "openings" or "opening heights" refers to the spot size impinged on the receiving wafer and not to the physical opening in the BAA since the physical openings are substantially larger (e.g., micron scale) than the spot size (e.g., nanometer scale) ultimately generated from the BAA. Thus, when described herein as the pitch of a BAA or column of openings in a BAA being said to "correspond" to the pitch of metal lines, such description actually refers to the relationship between pitch of the impinging spots as generated from the BAA and the pitch of the lines being cut. As an example, the spots generated from the BAA 2110 have a pitch the same as the pitch of the lines 2100 (when both columns of BAA openings are considered together). Meanwhile, the spots generated from only one column of the staggered array of the BAA 2110 have twice the pitch as the pitch of the lines 2100.

[00113] It is also to be appreciated that an ebeam column that includes a staggered beam aperture array (staggered BAA) as described above may also include other features in addition to those described in association with Figure 4, some examples of which are further described in greater detail below in association with Figures 24A-24C. For example, in an embodiment, the sample stage can be rotated by 90 degrees to accommodate alternating metallization layers which may be printed orthogonally to one another (e.g., rotated between X and Y scanning directions). In another embodiment, an e-beam tool is capable of rotating a wafer by 90 degrees prior to loading the wafer on the stage.

[00114] Figure 21B illustrates a cross-sectional view of a stack 2150 of metallization layers 2152 in an integrated circuit based on metal line layouts of the type illustrated in Figure 21A, in accordance with an embodiment of the present invention. Referring to Figure 21B, in an exemplary embodiment, a metal cross-section for an interconnect stack 2150 is derived from a single BAA array for the lower eight matched metal layers 2154, 2156, 2158, 2160, 2162, 2164, 2166 and 2168. It is to be appreciated that upper thicker/wider metal lines 2170 and 2172 would not be made with the single BAA. Via locations 2174 are depicted as connecting the lower eight matched metal layers 2154, 2156, 2158, 2160, 2162, 2164, 2166 and 2168.

[00115] In a fifth aspect of embodiments of the present invention, a three beam aperture array for an ebeam tool is described.

[00116] In an embodiment, a beam aperture array is implemented to solve throughput of an ebeam machine while also enabling minimum wire pitch. As described above, with no stagger, the problem of edge placement error (EPE) means that a minimum pitch that is twice the wire width cannot be cut since there is no possibility of stacking vertically in single stack. Embodiments described below extend the staggered BAA concept to permit three separate pitches to be exposed on a wafer, either through three passes, or by illuminating/controlling all three beam aperture arrays simultaneously in a single pass. The latter approach may be preferable for achieving the best throughput.

[00117] In some implementations, a three staggered beam aperture array is used instead of a single beam aperture array. The pitches of the three different

arrays may either be related (e.g., 10-20-30) or unrelated pitches. The three pitches can be used in three separate regions on the target die, or the three pitches may occur simultaneously in the same localized region.

[00118] To provide context, the use of two or more single arrays would require a separate ebeam apparatus, or a change out of the beam aperture array for each different hole size/wire pitch. The result would otherwise be a throughput limiter and/or a cost of ownership issue. Instead, embodiments described herein are directed to BAAs having more than one (e.g., three) staggered array. In one such embodiment (in the case of including three arrays on one BAA), three different arrays of pitches can be patterned on a wafer without loss of throughput. Furthermore, the beam pattern may be steered to cover one of the three arrays. An extension of this technique can be used to pattern any mixture of different pitches by turning on and off the blanker holes in all three arrays as needed.

[00119] As an example, Figure 22 illustrates apertures of a BAA 2200 having a layout of three different staggered arrays, in accordance with an embodiment of the present invention. Referring to Figure 22, a three-column 2202, 2204 and 2206 blanker aperture array 2200 can be used for three different line pitches for cutting or making vias by all or some of the apertures 2208 which are switched open or "closed" (beam deflecting) as the wafer/die moves underneath along the wafer travel direction 2210. In one such embodiment, multiple pitches can be patterned without changing the BAA plate in the device. Furthermore, in a particular embodiment, multiple pitches can be printed at the same time. Both techniques allow many spots to be printed during a continuous pass of the wafer under the BAA. It is to be appreciated that while the focus of the description is on three separate columns of different pitches, embodiments can be extended to include any number of pitches that can fit within the apparatus, e.g., 1, 2, 3, 4, 5, etc.

[00120] In an embodiment, the BAA can be independently controlled as to whether each opening passes the ebeam or deflects the beam into a Faraday cup or blanking aperture. The apparatus may be built to deflect the overall beam coverage to just a single pitch column, and then individual openings in the pitch column are electrically configured to pass the ebeam ("on") or not pass ("off"). As an example, Figure 23 illustrates apertures 2308 of a BAA 2300 having a layout of three different

staggered arrays 2302, 2304 and 2306, where the ebeam covers only one of the arrays (e.g., array 2304), in accordance with an embodiment of the present invention. In such an apparatus configuration, throughput could be gained for specific areas on a die that contain only a single pitch. The direction of travel of the
5 underlying wafer is indicated by arrow 2310.

[00121] In one embodiment, in order to switch between pitch arrays, a deflector can be added to the ebeam column to allow the ebeam to be steerable onto the BAA pitch array. As an example, Figure 24A includes a cross-sectional schematic representation of an ebeam column of an electron beam lithography
10 apparatus having a deflector to shift the beam, in accordance with an embodiment of the present invention. Referring to Figure 24A, an ebeam column 2400, such as described in association with Figure 4, includes a deflector 2402. The deflector can be used to shift the beam onto an appropriate pitch/cut row in a shaping aperture corresponding to an appropriate array of a BAA 2404 having multiple pitch arrays.
15 As an example, Figure 24B illustrates a three (or up to n) pitch array for a BAA 2450 having pitch #1, cut #1 (2452), a pitch # 2, cut # 2 (2454) and a pitch # N, cut # N (2456). It is to be appreciated that the height of cut#n is not equal to the height of cut#n+m.

[00122] Other features may also be included in the ebeam column 2400. For
20 example, further referring to Figure 24A, in an embodiment, the stage can be rotated by 90 degrees to accommodate alternating metallization layers which may be printed orthogonally to one another (e.g., rotated between X and Y scanning directions). In another embodiment, an e-beam tool is capable of rotating a wafer by 90 degrees prior to loading the wafer on the stage. In yet another example, Figure 24C
25 illustrates a zoom in slit 2460 for inclusion on an ebeam column. The positioning of such a zoom in slit 2460 on column 2400 is shown in Figure 24A. The zoom in slit 2460 may be included to keep efficiency for different cut heights. It is to be appreciated that one or more of the above described features may be included in a single ebeam column.

30 **[00123]** In another embodiment, the ebeam fully illuminates multiple or all columns of pitches on the BAA. In such a configuration, all of the illuminated BAA openings would be electrically controlled to be "open" to pass the ebeam to the die,

or "off" to prevent the ebeam from reaching the die. The advantage of such an arrangement is that any combination of holes could be used to print line cuts or via locations without reducing throughput. While the arrangement described in association with Figures 23 and 24A-24C could also be used to produce a similar result, a separate pass across the wafer/die for each of the pitch arrays would be required (which would reduce throughput by a factor of 1/n, where n is the number of pitch arrays on the BAA that require printing).

[00124] Figure 25 illustrates apertures of a BAA having a layout of three different pitch staggered arrays, where the ebeam covers all of the arrays, in accordance with an embodiment of the present invention. Referring to Figure 25, apertures 2508 of a BAA 2500 having a layout of three different staggered arrays 2502, 2504 and 2506, where the ebeam can cover all of the arrays (e.g., covers arrays 2502, 2504 and 2506), in accordance with an embodiment of the present invention. The direction of travel of the underlying wafer is indicated by arrow 2510.

[00125] In either the case of Figure 23 or Figure 25, having three pitches of openings permits the cutting or via creation for three different line or wire widths. However, the lines must be in alignment with the apertures of the corresponding pitch array (by contrast, a universal cutter is disclosed below). Figure 26 illustrates a three beam staggered aperture array 2600 of a BAA relative to a plurality of large lines 2602 having cuts (e.g., breaks 2604 in the horizontal lines) or vias (filled-in boxes 2606) patterned using the BAA, with scanning direction shown by the arrow 2608, in accordance with an embodiment of the present invention. Referring to Figure 26, all the lines in a local region are of the same size (in this case, corresponding to the largest apertures 2610 on the right side of the BAA). Thus, Figure 26 illustrates a typical pattern produced by one of three staggered beam aperture arrays. Dotted lines show where cuts occurred in patterned lines. Dark rectangles are patterning vias that land on top of the lines/wires 2602. In this case, only the largest blanker array is enabled.

[00126] Figure 27 illustrates a three beam staggered aperture array 2700 of a BAA relative to a plurality of medium sized lines 2702 having cuts (e.g., breaks 2704 in the horizontal lines) or vias (filled-in boxes 2706) patterned using the BAA,

with scanning direction shown by the arrow 2708, in accordance with an embodiment of the present invention. Referring to Figure 27, all the lines in a local region are of the same size (in this case, corresponding to the medium sized apertures 2710 in the middle of the BAA). Thus, Figure 27 illustrates a typical pattern produced by one of three staggered beam aperture arrays. Dotted lines show where cuts occurred in patterned lines. Dark rectangles are patterning vias that land on top of the lines/wires 2702. In this case, only the medium blanker array is enabled.

[00127] Figure 28 illustrates a three beam staggered aperture array 2800 of a BAA relative to a plurality of small lines 2802 having cuts (e.g., breaks 2804 in the horizontal lines) or vias (filled-in boxes 2806) patterned using the BAA, with scanning direction shown by the arrow 2808, in accordance with an embodiment of the present invention. Referring to Figure 28, all the lines in a local region are of the same size (in this case, corresponding to the smallest apertures 2810 on the left side of the BAA). Thus, Figure 28 illustrates a typical pattern produced by one of three staggered beam aperture arrays. Dotted lines show where cuts occurred in patterned lines. Dark rectangles are patterning vias that land on top of the lines/wires 2802. In this case, only the small blanker array is enabled.

[00128] In another embodiment, combinations of the three pitches can be patterned, where the aperture alignment is possible against the lines already in these positions. Figure 29A illustrates a three beam staggered aperture array 2900 of a BAA relative to a plurality of lines 2902 of varying size having cuts (e.g., breaks 2904 in the horizontal lines) or vias (filled-in boxes 2906) patterned using the BAA, with scanning direction shown by the arrow 2908, in accordance with an embodiment of the present invention. Referring to Figure 29A, as many as three different metal widths can be patterned on the fixed grids 2950 that occur on the three-staggered BAA. The dark colored apertures 2910 of the BAA are being turned on/off during they scan. The light colored BAA apertures 2912 remain off. Thus, Figure 29A illustrates a typical pattern produced by simultaneous use of all three staggered beam aperture arrays. Dotted lines show where cuts occurred in patterned lines. Dark rectangles are patterning vias that land on top of the lines/wires 2902.

In this case, the small blanker array, the medium blanker array and the large blanker array are all enabled.

[00129] Figure 29B illustrates a cross-sectional view of a stack 2960 of metallization layers in an integrated circuit based on metal line layouts of the type illustrated in Figure 29A, in accordance with an embodiment of the present invention. Referring to Figure 29B, in an exemplary embodiment, a metal cross-section for an interconnect stack is derived from three BAA pitch arrays of 1x, 1.5x and 3x pitch/width for the lower eight matched levels 2962, 2964, 2966, 2968, 2970, 2972, 2974 and 2976. For example, in level 2962, exemplary lines 2980 of 1x, an exemplary line 2982 of 1.5x, and an exemplary line 2984 of 3x are called out. It is to be appreciated that the varying width for the metals can only be seen for those layers with lines coming out of the page. All metals in the same layer are the same thickness regardless of metal width. It is to be appreciated that upper thicker/wider metals would not be made with the same three pitch BAA.

[00130] In another embodiment, different lines within the array can change width. Figure 30 illustrates a three beam staggered aperture array 3000 of a BAA relative to a plurality of lines 3002 of varying size having cuts (e.g., breaks 3004 in the horizontal lines) or vias (filled-in boxes 3006) patterned using the BAA, with scanning direction shown by the arrow 3008, in accordance with an embodiment of the present invention. Referring to Figure 30, the third horizontal line 3050 from the bottom of the array of lines 3002 has a wide line 3052 on a same grid line 3056 as a narrow line 3054. The corresponding different sized, but horizontally aligned, apertures 3060 and 3062 used to cut or make vias in the different sized lines are highlighted and horizontally centered with the two lines 3052 and 3054. Thus, Figure 30 illustrates a scenario with the additional possibility to change line widths during patterning, as well as within different regions.

[00131] In a sixth aspect of embodiments of the present invention, a non-universal cutter for an ebeam tool is described.

[00132] In an embodiment, the cutting of multiple pitches of wires in the same region is made possible. In a particular implementation, high throughput ebeam processing is used to define cuts with two BAA arrays each with opening heights equal to predetermined values. As an illustrative example, N(20nm-minimal

layout pitch) and M(30nm) can cut multiple pitch layouts (N[20], M[30], N*2[40], N*3 or M*2[60], N*4[80], M*3[90]nm) etc. with required EPE tolerance of minimum pitch/4 (N/4) provided that cut/plug tracks are placed on grids.

[00133] Figure 31 illustrates three sets of lines 3102, 3104 and 3106 of differing pitch with overlying corresponding apertures 3100 on each line, in accordance with an embodiment of the present invention. Referring to Figure 31, a 40nm, 30nm and 20nm arrays vertical pitch is shown. For the 40nm pitch lines 3102, a staggered BAA (e.g., having 2048 openings) is available for cutting the lines. For the 30nm pitch lines 3104, a staggered BAA (e.g., having 2730 openings) is available for cutting the lines. For the 20nm pitch lines 3106, a staggered BAA (e.g., having 4096 openings) is available for cutting the lines. In this exemplary case, parallel lines drawn on a 10 nm step unidirectional grid 3150 with pitches 20nm, 30nm and 40nm need to be cut. The BAA has three pitches (i.e., three sub-arrays) and is axially aligned with drawn tracks 3160, as depicted in Figure 31.

[00134] Provided each aperture on each of the three sub-arrays of Figure 31 has its own driver, cutting of complex layouts with tracks on a layout consistent with the depicted unidirectional grid can be performed with tool throughput independent of number and mix of pitches present in the layout. The result is that multiple cuts, multiple simultaneous cuts of different widths, and cuts of widths that are greater than any single pitch are made possible. The design may be referred to as pitch agnostic throughput. To provide context, such a result is not possible where multiple passes of the wafer are required for each pitch. It is to be appreciated that such an implementation is not restricted to three BAA opening sizes. Additional combinations could be produced as long as there is a common grid relationship between the various BAA pitches.

[00135] Furthermore, in an embodiment, multiple cuts made at the same time are possible with multiple pitches, and wider lines are accommodated by combinations of different openings that completely cover the cut distance. For example, Figure 32 illustrates a plurality of different sized lines 3202 including one very large line 3204, and a beam aperture arrays vertical pitch layout 3206 (three arrays 3208, 3210 and 3212) on a common grid 3214, in accordance with an embodiment of the present invention. The very wide line 3204 is cut by a

combination of three large apertures 3216 which are additive in the vertical direction. It is to be appreciated in viewing Figure 32, the wires 3202 are shown as being cut by various openings which are shown as dashed boxes (e.g., dashed boxes 3218 corresponding to apertures 3216).

5 **[00136]** In a seventh aspect of embodiments of the present invention, a universal cutter for an ebeam tool is described.

[00137] In an embodiment, high throughput ebeam processing is enabled by defining cuts such that a single (universal) BAA having opening heights equal to predetermined values can be used for a variety of line pitches/widths. In one such

10 embodiment, the opening heights are targeted at half of the minimal pitch layout. It is to be appreciated that reference to “opening heights” refers to the spot size impinged on the receiving wafer and not to the physical opening in the BAA since the physical openings are substantially larger (e.g., micron scale) than the spot size (e.g., nanometer scale) ultimately generated from the BAA. In a particular example,

15 the height of the openings is 10nm for a minimal layout pitch of N=20nm). In such a case, multiple pitch layouts (e.g., N[20], M[30], N*2[40], N*3 or M*2[60], N*4[80], M*3[90]nm) etc. can be cut. The cuts can be performed with a required EPE tolerance of minimum pitch/4 (N/4) provided cut/plug tracks are placed on a predetermined grid where tracks axes are aligned on a predetermined one-

20 dimensional (1D) grid coincidental with the middle between two BAA openings. Each metal track adjacency is interrupted by exposing two openings at the minimum to satisfy an EPE requirement = pitch/4.

[00138] In an example, Figure 33 illustrates a plurality of different sized lines 3302, and a universal cutter pitch array 3304, in accordance with an embodiment of

25 the present invention. Referring to Figure 33, in a particular embodiment, a BAA having a 10nm pitch array 3304 with, e.g., 8192 openings (only a few of which are shown) is used as a universal cutter. It is to be appreciated that although shown on a common grid 3306, in one embodiment, the lines need not actually be aligned to a grid at all. In that embodiment, spacing is differentiated by the cutter openings.

30 **[00139]** More generally, referring again to Figure 33, a beam aperture array 3304 includes an array of staggered square beam openings 3308 (e.g., 8192 staggered square beam openings) that can be implemented to cut any width line/wire

3302 by using one or more of the openings in conjunction in the vertical direction while the scan is performed along the horizontal direction 3310. The only restriction is that adjacent wires be 2*EPE for cutting any individual wire. In one embodiment, the wires are cut by combinations of universal cutter openings 3308 chosen on the fly from the BAA 3304. As an example, line 3312 is cut by three openings 3314 from the BAA 3304. In another example, line 3316 is cut by 11 openings 3318 from the BAA 3304.

[00140] For comparison to a non-universal cutter, a grouping of arrays 3320 is illustrated in Figure 33. It is to be appreciated that the grouping of arrays 3320 is not present in the universal cutter, but are shown for comparison of the universal cutter to a non-universal cutter based on the grouping of arrays 3320.

[00141] To provide context, other beam aperture array arrangements require openings that are specifically aligned on the centerline of the lines to be cut. Instead, in accordance with an embodiment herein, a universal aperture array technique allows universal cutting of any width line/wire on non-aligned line centerlines. Furthermore, changes in line widths (and spacings) that would otherwise be fixed by the BAA of other techniques are accommodated by the universal cutter. Accordingly, late changes to a fabrication process, or lines/wires specifically tailored to the RC needs of an individual circuit may be permitted.

[00142] It is to be appreciated that as long as the EPE coverage requirement of pitch/4 is met, the various lines/wires do not have to be exactly aligned in a universal cutter scenario. The only restrictions is that sufficient enough space is provided between lines to have EPE/2 distance between lines with the cutter lining up at EPE/4 as follows. Figure 34 demonstrates the 2* EPE rule for a universal cutter 3400 as referenced against two lines 3402 and 3404, in accordance with an embodiment of the present invention. Referring to Figure 34, the EPE 3406 of the top line and the EPE 3408 of the bottom line provide the 2*EPE width which corresponds to the pitch of the universal cutter holes 3410. Thus, the rule for opening pitch corresponds to the minimum space between two lines. If the distance is greater than this, the cutter will cut any arbitrary width line. Note that the minimum hole size and pitch is exactly equal to 2*EPE for lines.

[00143] In an embodiment, by using a universal cutter, the resulting structures can have random wire widths and placement in an ebeam-produced semiconductor sample. The random placement, however, is still described as unidirectional since no orthogonal lines or hooks are fabricated in this approach. A universal cutter can be implemented for cutting many different pitches and widths, e.g., whatever can be fabricated by patterning prior to ebeam patterning used for cuts and vias. As a comparison, the above described staggered array and three-staggered array BAAs are associated with fixed locations for the pitches.

[00144] More generally, referring to all of the above aspects of embodiments of the present invention, it is to be appreciated that a metallization layer having lines with line cuts (or plugs) and having associated vias may be fabricated above a substrate and, in one embodiment, may be fabricated above a previous metallization layer. As an example, Figure 35 illustrates a plan view and corresponding cross-sectional view of a previous layer metallization structure, in accordance with an embodiment of the present invention. Referring to Figure 35, a starting structure 3500 includes a pattern of metal lines 3502 and interlayer dielectric (ILD) lines 3504. The starting structure 3500 may be patterned in a grating-like pattern with metal lines spaced at a constant pitch and having a constant width, as is depicted in Figure 35. Although not shown, the lines 3502 may have interruptions (i.e., cuts or plugs) at various locations along the lines. The pattern, for example, may be fabricated by a pitch halving or pitch quartering approach, as described above. Some of the lines may be associated with underlying vias, such as line 3502' shown as an example in the cross-sectional view.

[00145] In an embodiment, fabrication of a metallization layer on the previous metallization structure of Figure 35 begins with formation of an interlayer dielectric (ILD) material above the structure 3500. A hardmask material layer may then be formed on the ILD layer. The hardmask material layer may be patterned to form a grating of unidirectional lines orthogonal to the lines 3502 of 3500. In one embodiment, the grating of unidirectional hardmask lines is fabricated using conventional lithography (e.g., photoresist and other associated layers) and may have a line density defined by a pitch-halving, pitch-quartering etc. approach as described above. The grating of hardmask lines leaves exposed a grating region of

the underlying ILD layer. It is these exposed portions of the ILD layer that are ultimately patterned for metal line formation, via formation, and plug formation. For example, in an embodiment, via locations are patterned in regions of the exposed ILD using EBL as described above. The patterning may involve formation of a resist layer and patterning of the resist layer by EBL to provide via opening locations which may be etched into the ILD regions. The lines of overlying hardmask can be used to confine the vias to only regions of the exposed ILD, with overlap accommodated by the hardmask lines which can effectively be used as an etch stop. Plug (or cut) locations may also be patterned in exposed regions of the ILD, as confined by the overlying hardmask lines, in a separate EBL processing operation. The fabrication of cuts or plugs effectively preserve regions of ILD that will ultimately interrupt metal lines fabricated therein. Metal lines may then be fabricated using a damascene approach, where exposed portions of the ILD (those portions between the hardmask lines and not protected by a plug preservation layer, such as a resist layer patterned during “cutting”) are partially recessed. The recessing may further extend the via locations to open metal lines from the underlying metallization structure. The partially recessed ILD regions are then filled with metal (a process which may also involve filling the via locations), e.g., by plating and CMP processing, to provide metal lines between the overlying hardmask lines. The hardmask lines may ultimately be removed for completion of a metallization structure. It is to be appreciated that the above ordering of line cuts, via formation, and ultimate line formation is provided only as an example. A variety of processing schemes may be accommodated using EBL cuts and vias, as described herein.

[00146] In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example,

chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

[00147] In an embodiment, as is also used throughout the present description, interconnect material is composed of one or more metal or other conductive
5 structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The interconnect lines are also
10 sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect.

[00148] In an embodiment, as is also used throughout the present description, hardmask materials are composed of dielectric materials different from the interlayer dielectric material. In some embodiments, a hardmask layer includes a layer of a
15 nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials. In another embodiment, a hardmask material includes a metal species. For example, a hardmask or other overlying material may include a layer of a nitride of titanium or another metal (e.g., titanium nitride). Potentially lesser amounts of other
20 materials, such as oxygen, may be included in one or more of these layers. Alternatively, other hardmask layers known in the arts may be used depending upon the particular implementation. The hardmask layers maybe formed by CVD, PVD, or by other deposition methods.

[00149] It is to be appreciated that the layers and materials described in
25 association with Figure 35 are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another
30 semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The

semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, the structure depicted in Figure 35
5 may be fabricated on underlying lower level interconnect layers.

[00150] In another embodiment, EBL cuts may be used to fabricate semiconductor devices, such as PMOS or NMOS devices of an integrated circuit. In one such embodiment, EBL cuts are used to pattern a grating of active regions that are ultimately used to form fin-based or trigate structures. In another such
10 embodiment, EBL cuts are used to pattern a gate layer, such as a poly layer, ultimately used for gate electrode fabrication. As an example of a completed device, Figures 36A and 36B illustrate a cross-sectional view and a plan view (taken along the a-a' axis of the cross-sectional view), respectively, of a non-planar semiconductor device having a plurality of fins, in accordance with an embodiment
15 of the present invention.

[00151] Referring to Figure 36A, a semiconductor structure or device 3600 includes a non-planar active region (e.g., a fin structure including protruding fin portion 3604 and sub-fin region 3605) formed from substrate 3602, and within isolation region 3606. A gate line 3608 is disposed over the protruding portions
20 3604 of the non-planar active region as well as over a portion of the isolation region 3606. As shown, gate line 3608 includes a gate electrode 3650 and a gate dielectric layer 3652. In one embodiment, gate line 3608 may also include a dielectric cap layer 3654. A gate contact 3614, and overlying gate contact via 3616 are also seen from this perspective, along with an overlying metal interconnect 3660, all of which
25 are disposed in inter-layer dielectric stacks or layers 3670. Also seen from the perspective of Figure 36A, the gate contact 3614 is, in one embodiment, disposed over isolation region 3606, but not over the non-planar active regions.

[00152] Referring to Figure 36B, the gate line 3608 is shown as disposed over the protruding fin portions 3604. Source and drain regions 3604A and 3604B of the
30 protruding fin portions 3604 can be seen from this perspective. In one embodiment, the source and drain regions 3604A and 3604B are doped portions of original material of the protruding fin portions 3604. In another embodiment, the material of

the protruding fin portions 3604 is removed and replaced with another semiconductor material, e.g., by epitaxial deposition. In either case, the source and drain regions 3604A and 3604B may extend below the height of dielectric layer 3606, i.e., into the sub-fin region 3605.

5 **[00153]** In an embodiment, the semiconductor structure or device 3600 is a non-planar device such as, but not limited to, a fin-FET or a tri-gate device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate electrode stacks of gate lines 3608 surround at least a top surface and a pair of sidewalls of the
10 three-dimensional body.

[00154] Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-
15 controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other
20 components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

[00155] Figure 37 illustrates a computing device 3700 in accordance with one implementation of the invention. The computing device 3700 houses a board 3702.
25 The board 3702 may include a number of components, including but not limited to a processor 3704 and at least one communication chip 3706. The processor 3704 is physically and electrically coupled to the board 3702. In some implementations the at least one communication chip 3706 is also physically and electrically coupled to the board 3702. In further implementations, the communication chip 3706 is part of
30 the processor 3704.

[00156] Depending on its applications, computing device 3700 may include other components that may or may not be physically and electrically coupled to the

board 3702. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[00157] The communication chip 3706 enables wireless communications for the transfer of data to and from the computing device 3700. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 3706 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 3700 may include a plurality of communication chips 3706. For instance, a first communication chip 3706 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 3706 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[00158] The processor 3704 of the computing device 3700 includes an integrated circuit die packaged within the processor 3704. In some implementations of the invention, the integrated circuit die of the processor includes one or more structures fabricated using CEBL, in accordance with implementations of embodiments of the invention. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to

transform that electronic data into other electronic data that may be stored in registers and/or memory.

[00159] The communication chip 3706 also includes an integrated circuit die packaged within the communication chip 3706. In accordance with another implementation of embodiments of the invention, the integrated circuit die of the communication chip includes one or more structures fabricated using CEBL, in accordance with implementations of embodiments of the invention.

[00160] In further implementations, another component housed within the computing device 3700 may contain an integrated circuit die that includes one or more structures fabricated using CEBL, in accordance with implementations of embodiments of the invention.

[00161] In various implementations, the computing device 3700 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 3700 may be any other electronic device that processes data.

[00162] Embodiments of the present invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present invention. In one embodiment, the computer system is coupled with an ebeam tool such as described in association with Figure 4 and/or Figures 24A-24C. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory (“ROM”), random access memory (“RAM”), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

[00163] Figure 38 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 3800 within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein (such as end-point detection), may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term "machine" shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

[00164] The exemplary computer system 3800 includes a processor 3802, a main memory 3804 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 3806 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 3818 (e.g., a data storage device), which communicate with each other via a bus 3830.

[00165] Processor 3802 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 3802 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 3802 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor

3802 is configured to execute the processing logic 3826 for performing the operations described herein.

[00166] The computer system 3800 may further include a network interface device 3808. The computer system 3800 also may include a video display unit 3810 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 3812 (e.g., a keyboard), a cursor control device 3814 (e.g., a mouse), and a signal generation device 3816 (e.g., a speaker).

[00167] The secondary memory 3818 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 3832 on which is stored one or more sets of instructions (e.g., software 3822) embodying any one or more of the methodologies or functions described herein. The software 3822 may also reside, completely or at least partially, within the main memory 3804 and/or within the processor 3802 during execution thereof by the computer system 3800, the main memory 3804 and the processor 3802 also constituting machine-readable storage media. The software 3822 may further be transmitted or received over a network 3820 via the network interface device 3808.

[00168] While the machine-accessible storage medium 3832 is shown in an exemplary embodiment to be a single medium, the term "machine-readable storage medium" should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term "machine-readable storage medium" shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term "machine-readable storage medium" shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

[00169] Implementations of embodiments of the invention may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or

may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

[00170] A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the invention, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the invention may also be carried out using nonplanar transistors.

[00171] Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[00172] The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal,

depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer.

5 **[00173]** For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate
10 electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

15 **[00174]** In some implementations, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially
20 parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the invention, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or
25 more planar, non-U-shaped layers.

[00175] In some implementations of the invention, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride.
30 Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a

plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[00176] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[00177] One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[00178] Figure 39 illustrates an interposer 3900 that includes one or more embodiments of the invention. The interposer 3900 is an intervening substrate used to bridge a first substrate 3902 to a second substrate 3904. The first substrate 3902 may be, for instance, an integrated circuit die. The second substrate 3904 may be,

for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 3900 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 3900 may couple an integrated circuit die to a ball grid array (BGA) 3906
5 that can subsequently be coupled to the second substrate 3904. In some embodiments, the first and second substrates 3902/3904 are attached to opposing sides of the interposer 3900. In other embodiments, the first and second substrates 3902/3904 are attached to the same side of the interposer 3900. And in further embodiments, three or more substrates are interconnected by way of the interposer
10 3900.

[00179] The interposer 3900 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a
15 semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[00180] The interposer may include metal interconnects 3908 and vias 3910, including but not limited to through-silicon vias (TSVs) 3912. The interposer 3900 may further include embedded devices 3914, including both passive and active
20 devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 3900.

25 **[00181]** In accordance with embodiments of the invention, apparatuses or processes disclosed herein may be used in the fabrication of interposer 3900.

[00182] Figure 40 illustrates a computing device 4000 in accordance with one embodiment of the invention. The computing device 4000 may include a number of components. In one embodiment, these components are attached to one or more
30 motherboards. In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in the computing device 4000 include, but are not limited to, an integrated circuit die

4002 and at least one communication chip 4008. In some implementations the communication chip 4008 is fabricated as part of the integrated circuit die 4002. The integrated circuit die 4002 may include a CPU 4004 as well as on-die memory 4006, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

[00183] Computing device 4000 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 4010 (e.g., DRAM), non-volatile memory 4012 (e.g., ROM or flash memory), a graphics processing unit 4014 (GPU), a digital signal processor 4016, a crypto processor 4042 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 4020, an antenna 4022, a display or a touchscreen display 4024, a touchscreen controller 4026, a battery 4029 or other power source, a power amplifier (not shown), a global positioning system (GPS) device 4028, a compass 4030, a motion coprocessor or sensors 4032 (that may include an accelerometer, a gyroscope, and a compass), a speaker 4034, a camera 4036, user input devices 4038 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 4040 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[00184] The communications chip 4008 enables wireless communications for the transfer of data to and from the computing device 4000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 4008 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device

4000 may include a plurality of communication chips 4008. For instance, a first communication chip 4008 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 4008 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[00185] The processor 4004 of the computing device 4000 includes one or more structures fabricated using CEBL, in accordance with implementations of embodiments of the invention. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[00186] The communication chip 4008 may also include one or more structures fabricated using CEBL, in accordance with implementations of embodiments of the invention.

[00187] In further embodiments, another component housed within the computing device 4000 may contain one or more structures fabricated using CEBL, in accordance with implementations of embodiments of the invention.

[00188] In various embodiments, the computing device 4000 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 4000 may be any other electronic device that processes data.

[00189] The above description of illustrated implementations of embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

[00190] These modifications may be made to the invention in light of the above detailed description. The terms used in the following claims should not be

construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

5 **[00191]** In an embodiment, a layout for a metallization layer of an integrated circuit includes a first region having a plurality of unidirectional lines of a first width and a first pitch and parallel with a first direction. The layout also includes a second region having a plurality of unidirectional lines of a second width and a second pitch and parallel with the first direction, the second width and the second 10 pitch different than the first width and the first pitch, respectively. The layout also includes a third region having a plurality of unidirectional lines of a third width and a third pitch and parallel with the first direction, the third width and the third pitch different than the first and second widths and different than the first and second pitches.

15 **[00192]** In one embodiment, in a second direction orthogonal to the first direction, the plurality of unidirectional lines of the second region do not overlap with the plurality of unidirectional lines of the first region, and the plurality of unidirectional lines of the third region do not overlap with the plurality of unidirectional lines of the first region or with the plurality of unidirectional lines of 20 the second region.

[00193] In one embodiment, in a second direction orthogonal to the first direction, a portion of the plurality of unidirectional lines of the second region overlap with the plurality of unidirectional lines of the first region.

[00194] In one embodiment, the plurality of unidirectional lines of the second 25 region is interdigitated with the plurality of unidirectional lines of the first region.

[00195] In one embodiment, the second width is 1.5 times the first width and the second pitch is 1.5 times the first pitch, and the third width is 3 times the first width and the third pitch is 3 times the first pitch.

[00196] In one embodiment, the first region is a logic region, the second 30 region is an analog/IO region, and the third region is an SRAM region.

[00197] In one embodiment, none of the first, second or third regions the layout includes lines having jogs, orthogonal direction lines, or hooks.

[00198] In an embodiment, a metallization layer of an integrated circuit includes a first region having a plurality of unidirectional wires of a first width and a first pitch and parallel with a first direction. The metallization layer also includes a second region having a plurality of unidirectional wires of a second width and a second pitch and parallel with the first direction, the second width and the second pitch different than the first width and the first pitch, respectively. The metallization layer also includes a third region having a plurality of unidirectional wires of a third width and a third pitch and parallel with the first direction, the third width and the third pitch different than the first and second widths and different than the first and second pitches.

[00199] In one embodiment, in a second direction orthogonal to the first direction, the plurality of unidirectional wires of the second region do not overlap with the plurality of unidirectional wires of the first region, and the plurality of unidirectional wires of the third region do not overlap with the plurality of unidirectional wires of the first region or with the plurality of unidirectional wires of the second region.

[00200] In one embodiment, in a second direction orthogonal to the first direction, a portion of the plurality of unidirectional wires of the second region overlap with the plurality of unidirectional wires of the first region.

[00201] In one embodiment, the plurality of unidirectional wires of the second region is interdigitated with the plurality of unidirectional wires of the first region.

[00202] In one embodiment, the second width is 1.5 times the first width and the second pitch is 1.5 times the first pitch, and the third width is 3 times the first width and the third pitch is 3 times the first pitch.

[00203] In one embodiment, the first region is a logic region, the second region is an analog/IO region, and the third region is an SRAM region.

[00204] In one embodiment, none of the first, second or third regions the layout includes wires having jogs, orthogonal direction wires, or hooks.

[00205] In an embodiment, a method of forming a pattern for a semiconductor structure involves forming a pattern of lines above a substrate. The pattern of lines includes a first region having a plurality of unidirectional lines of a

first width and a first pitch and parallel with a first direction. The pattern of lines also includes a second region having a plurality of unidirectional lines of a second width and a second pitch and parallel with the first direction, the second width and the second pitch different than the first width and the first pitch, respectively. The pattern of lines also includes a third region having a plurality of unidirectional lines of a third width and a third pitch and parallel with the first direction, the third width and the third pitch different than the first and second widths and different than the first and second pitches. The method also involves aligning the substrate in an e-beam tool to provide the pattern of lines parallel with a scan direction of the e-beam tool, the scan direction orthogonal to the first direction. The method also involves forming a pattern of cuts in or above the pattern of lines to provide line breaks for the pattern of lines by scanning the substrate along the scan direction.

[00206] In one embodiment, forming the pattern of cuts involves using a three beam staggered blanker aperture array.

[00207] In one embodiment, forming the pattern of cuts involves using a universal cutter blanker aperture array.

[00208] In one embodiment, forming the pattern of cuts involves using a non-universal cutter blanker aperture array.

[00209] In one embodiment, forming the pattern of lines involves using a pitch halving or pitch quartering technique.

[00210] In one embodiment, forming the pattern of cuts involves exposing regions of a layer of photo-resist material.

CLAIMS

What is claimed is:

1. A layout for a metallization layer of an integrated circuit, the layout comprising:
5 a first region having a plurality of unidirectional lines of a first width and a first pitch and parallel with a first direction;
a second region having a plurality of unidirectional lines of a second width and a second pitch and parallel with the first direction, the second width and the second pitch different than the first width and the first pitch, respectively;
10 and
a third region having a plurality of unidirectional lines of a third width and a third pitch and parallel with the first direction, the third width and the third pitch different than the first and second widths and different than the first and second pitches.

15

2. The layout of claim 1, wherein, in a second direction orthogonal to the first direction, the plurality of unidirectional lines of the second region do not overlap with the plurality of unidirectional lines of the first region, and the plurality of unidirectional lines of the third region do not overlap with the plurality of
20 unidirectional lines of the first region or with the plurality of unidirectional lines of the second region.

3. The layout of claim 1, wherein, in a second direction orthogonal to the first direction, a portion of the plurality of unidirectional lines of the second region
25 overlap with the plurality of unidirectional lines of the first region.

4. The layout of claim 3, wherein the plurality of unidirectional lines of the second region is interdigitated with the plurality of unidirectional lines of the first region.

30 5. The layout of claim 1, wherein the second width is 1.5 times the first width and the second pitch is 1.5 times the first pitch, and wherein the third width is 3 times the first width and the third pitch is 3 times the first pitch.

6. The layout of claim 1, wherein the first region is a logic region, the second region is an analog/IO region, and the third region is an SRAM region.

5 7. The layout of claim 1, wherein none of the first, second or third regions the layout includes lines having jogs, orthogonal direction lines, or hooks.

8. A metallization layer of an integrated circuit, the metallization layer comprising:

a first region having a plurality of unidirectional wires of a first width and a first
10 pitch and parallel with a first direction;

a second region having a plurality of unidirectional wires of a second width and a second pitch and parallel with the first direction, the second width and the second pitch different than the first width and the first pitch, respectively; and

15 a third region having a plurality of unidirectional wires of a third width and a third pitch and parallel with the first direction, the third width and the third pitch different than the first and second widths and different than the first and second pitches.

20 9. The metallization layer of claim 8, wherein, in a second direction orthogonal to the first direction, the plurality of unidirectional wires of the second region do not overlap with the plurality of unidirectional wires of the first region, and the plurality of unidirectional wires of the third region do not overlap with the plurality of unidirectional wires of the first region or with the plurality of unidirectional wires of
25 the second region.

10. The metallization layer of claim 8, wherein, in a second direction orthogonal to the first direction, a portion of the plurality of unidirectional wires of the second region overlap with the plurality of unidirectional wires of the first region.

30

11. The metallization layer of claim 10, wherein the plurality of unidirectional wires of the second region is interdigitated with the plurality of unidirectional wires of the first region.

5 12. The metallization layer of claim 8, wherein the second width is 1.5 times the first width and the second pitch is 1.5 times the first pitch, and wherein the third width is 3 times the first width and the third pitch is 3 times the first pitch.

13. The metallization layer of claim 8, wherein the first region is a logic region, the
10 second region is an analog/IO region, and the third region is an SRAM region.

14. The metallization layer of claim 8, wherein none of the first, second or third regions the layout includes wires having jogs, orthogonal direction wires, or hooks.

15 15. A method of forming a pattern for a semiconductor structure, the method comprising:

forming a pattern of lines above a substrate, the pattern of lines comprising:

a first region having a plurality of unidirectional lines of a first width and a first pitch and parallel with a first direction;

20 a second region having a plurality of unidirectional lines of a second width and a second pitch and parallel with the first direction, the second width and the second pitch different than the first width and the first pitch, respectively; and

a third region having a plurality of unidirectional lines of a third width
25 and a third pitch and parallel with the first direction, the third width and the third pitch different than the first and second widths and different than the first and second pitches;

aligning the substrate in an e-beam tool to provide the pattern of lines parallel with a scan direction of the e-beam tool, the scan direction orthogonal to the
30 first direction; and

forming a pattern of cuts in or above the pattern of lines to provide line breaks for the pattern of lines by scanning the substrate along the scan direction.

16. The method of claim 15, wherein forming the pattern of cuts comprises using a three beam staggered blanker aperture array.

5 17. The method of claim 15, wherein forming the pattern of cuts comprises using a universal cutter blanker aperture array.

18. The method of claim 15, wherein forming the pattern of cuts comprises using a non-universal cutter blanker aperture array.

10

19. The method of claim 15, wherein forming the pattern of lines comprises using a pitch halving or pitch quartering technique.

20. The method of claim 15, wherein forming the pattern of cuts comprises

15 exposing regions of a layer of photo-resist material.

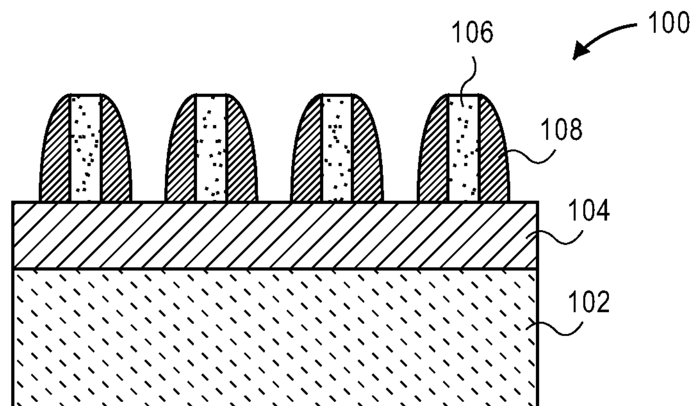


FIG. 1A

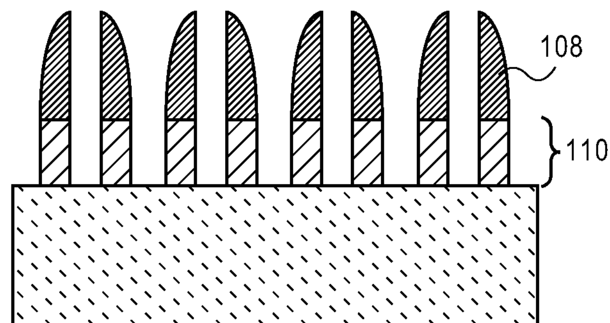


FIG. 1B

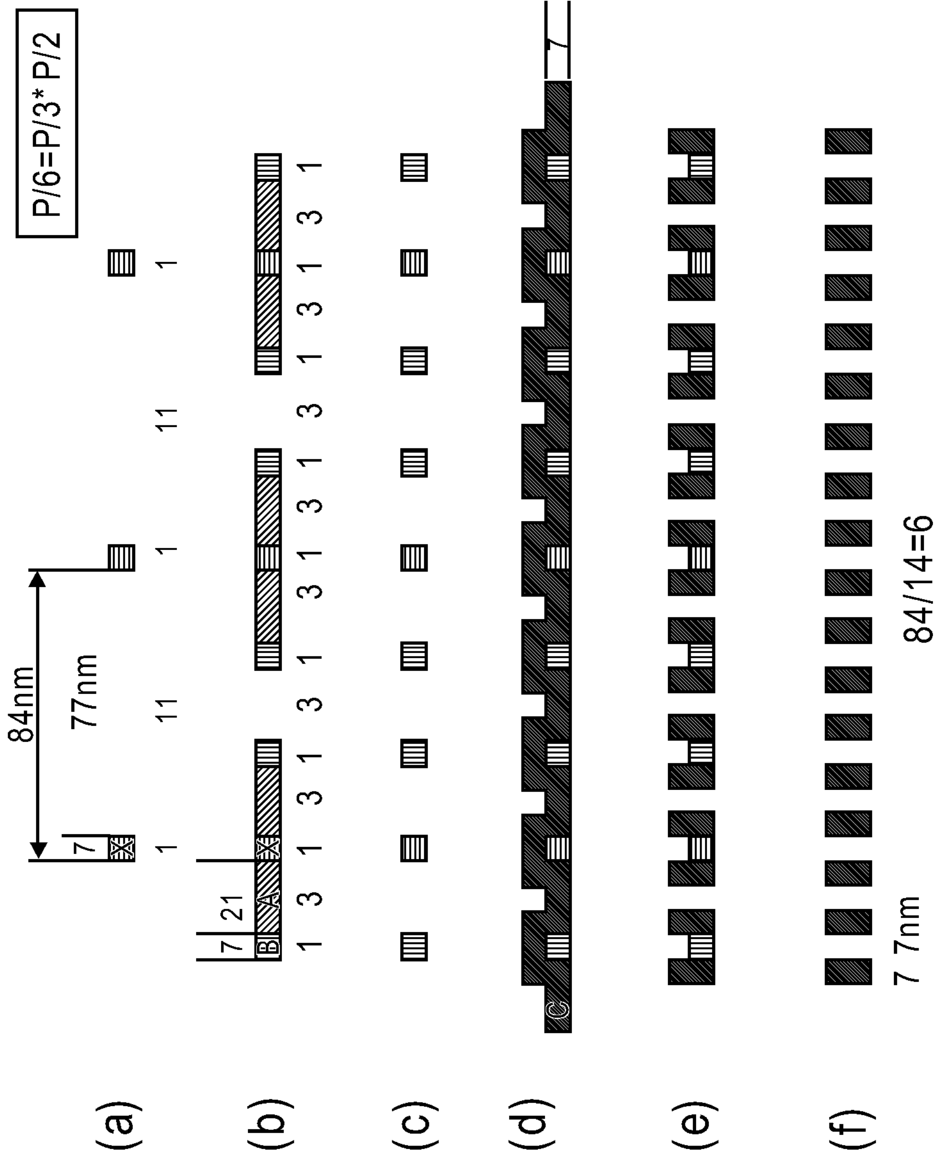


FIG. 2

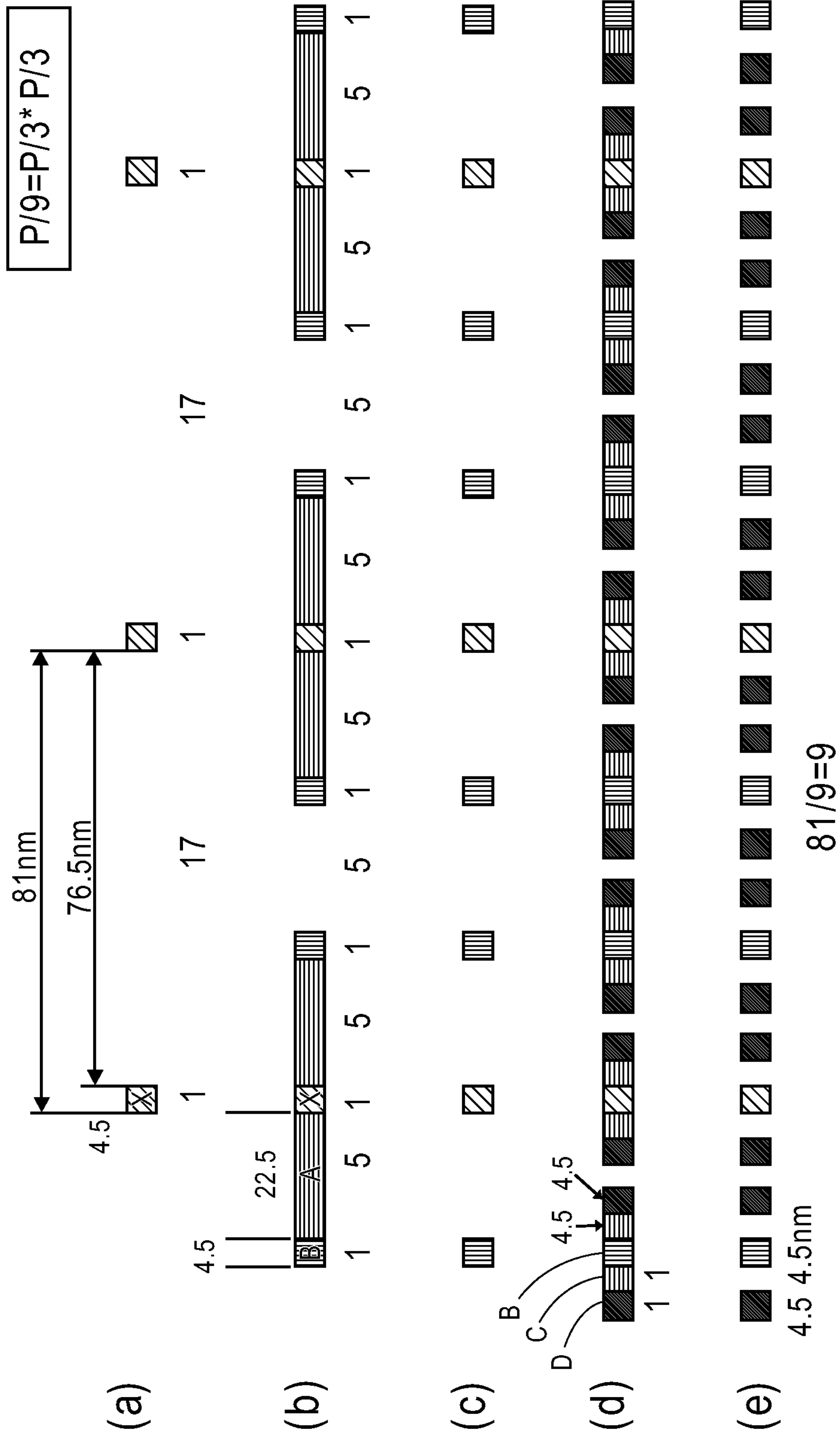


FIG. 3

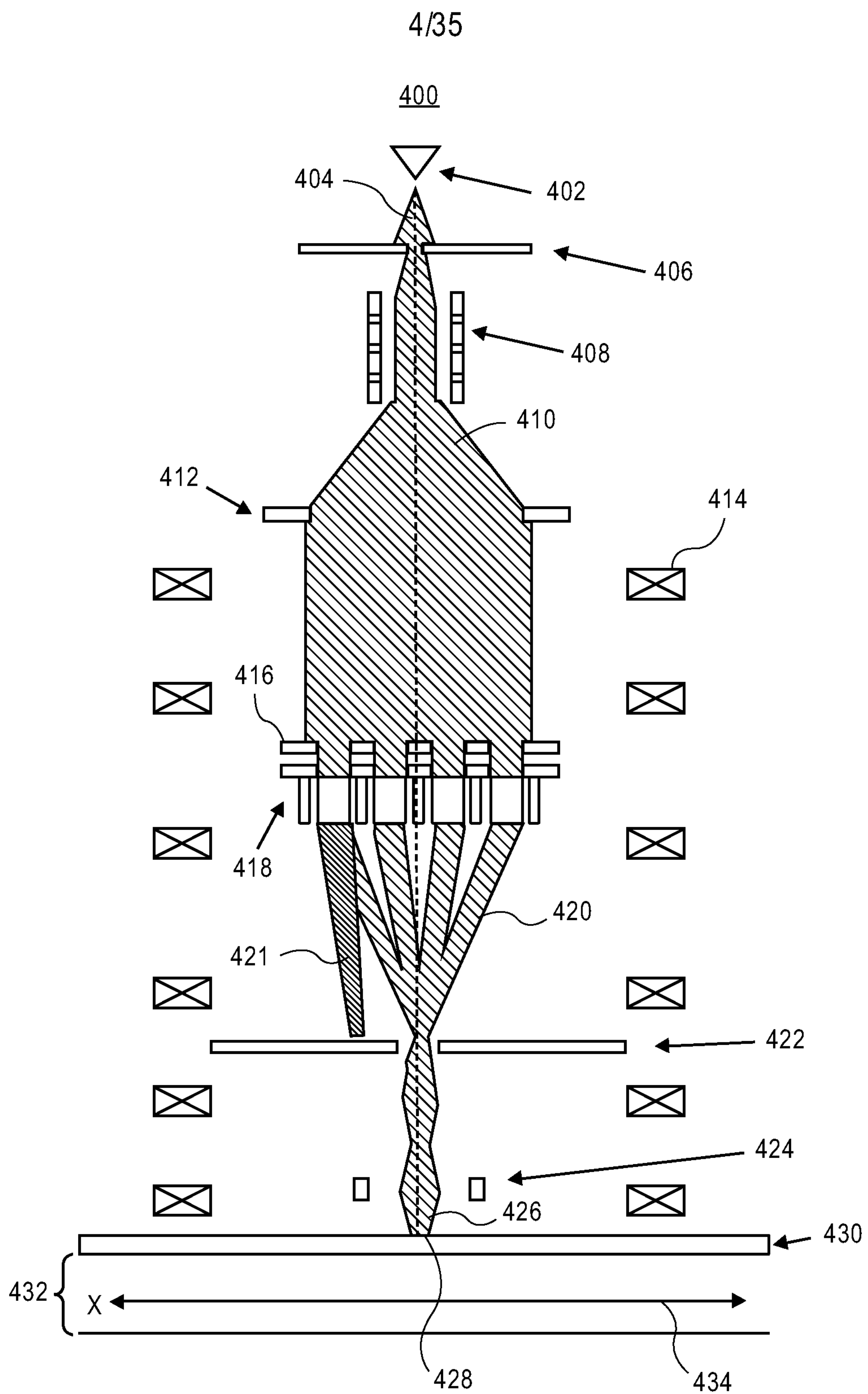


FIG. 4

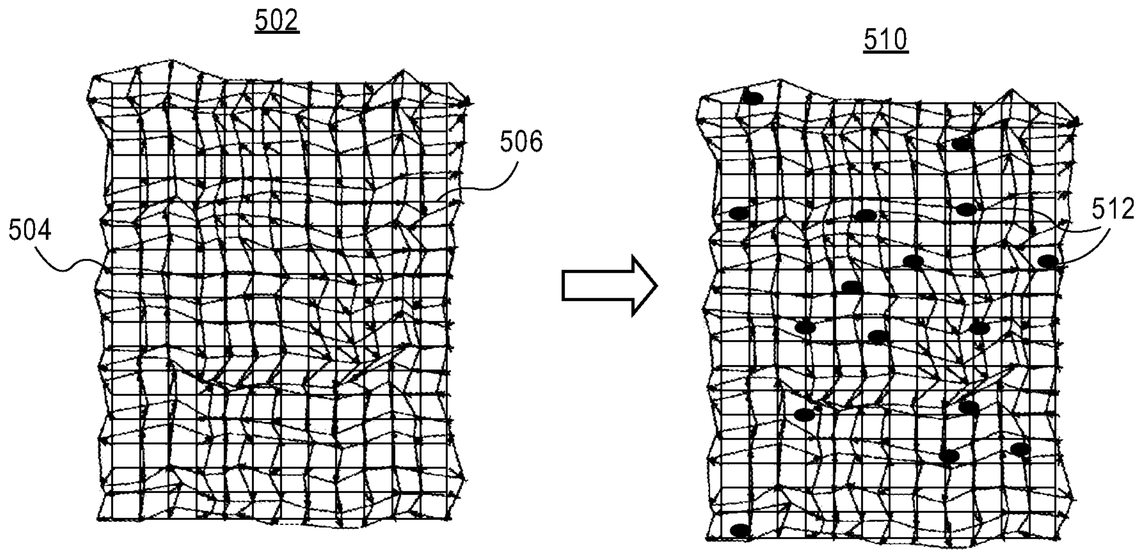


FIG. 5

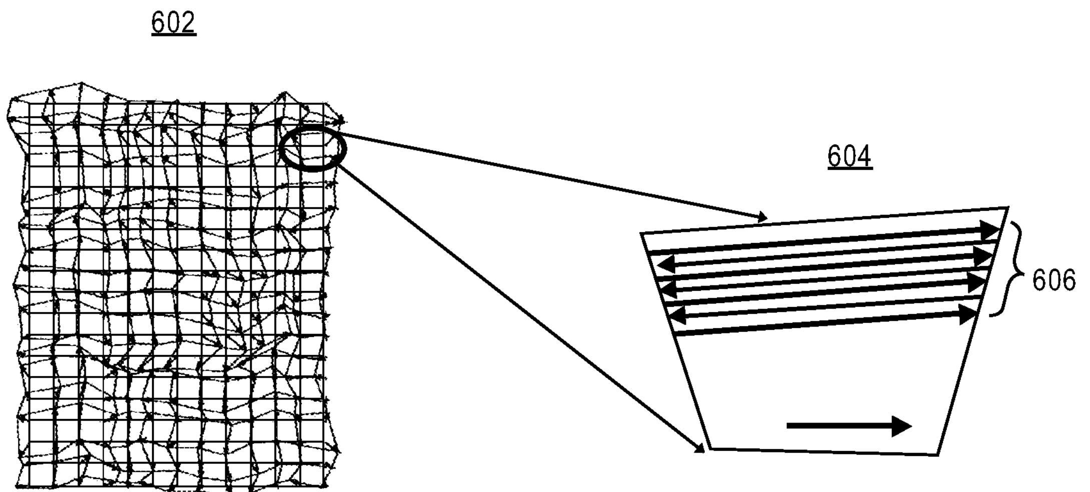


FIG. 6

$$\text{bits/m}^2 = \text{bits/pixel} * 1/(\text{pixelsize})^2 \qquad \text{(A)}$$

$$\frac{\text{bits}}{\text{pixel}} = \log_2\left(1 + \frac{A_p}{\Delta PV}\right) \qquad \text{(B)}$$

$$0.5 * \log2(1+10/5) * 1/(10 * 10^{-9})^2 = 0.5 * 1.585 * 10^{16} \text{ bits/m}^2 = 7.925 * 10^{15} \text{bits/m}^2 \qquad \text{(C)}$$

$$0.0706 * 7.925 * 10^{15} = 5.595 * 10^{14} \text{ bits} = 7 * 10^{13} \text{ bytes} \qquad \text{(D)}$$

FIG. 7

810

804 804 804 804 804

808

806

806

806

806

806

802

800

FIG. 8

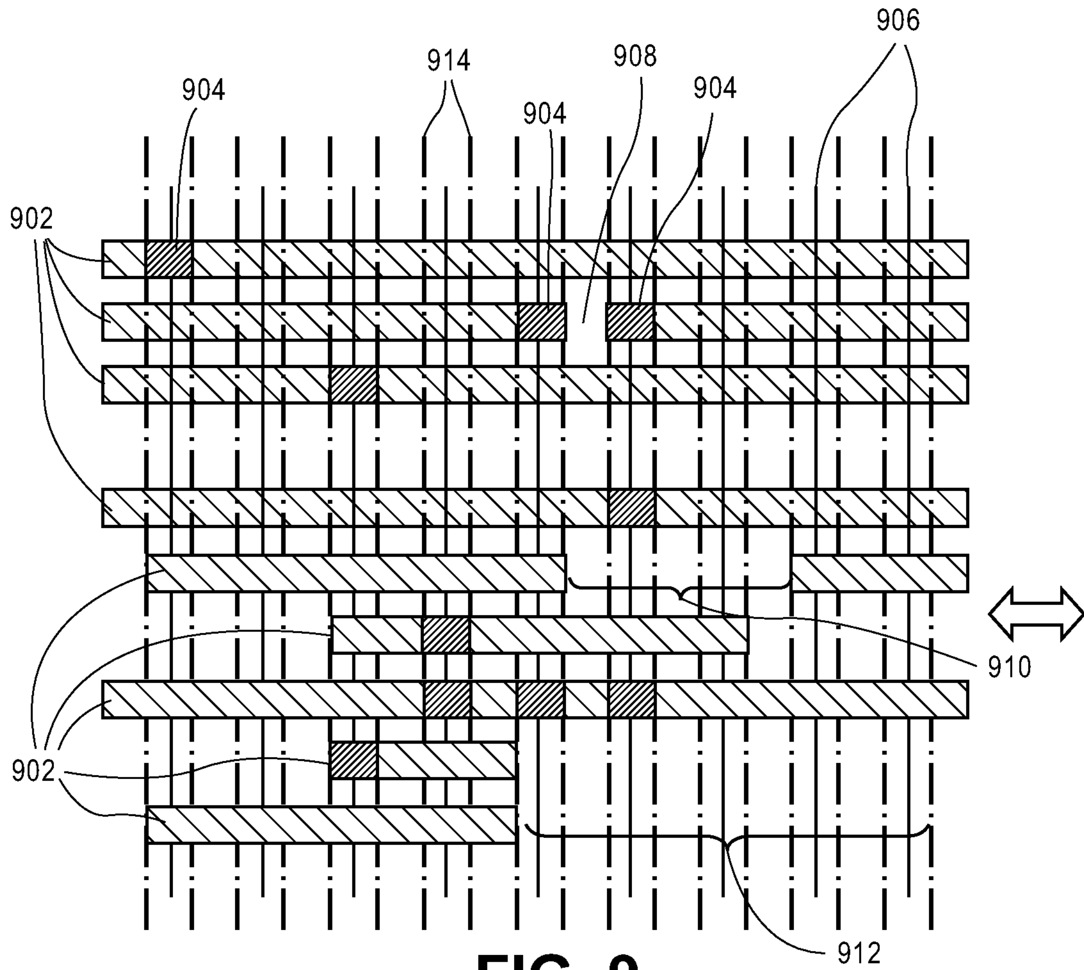


FIG. 9

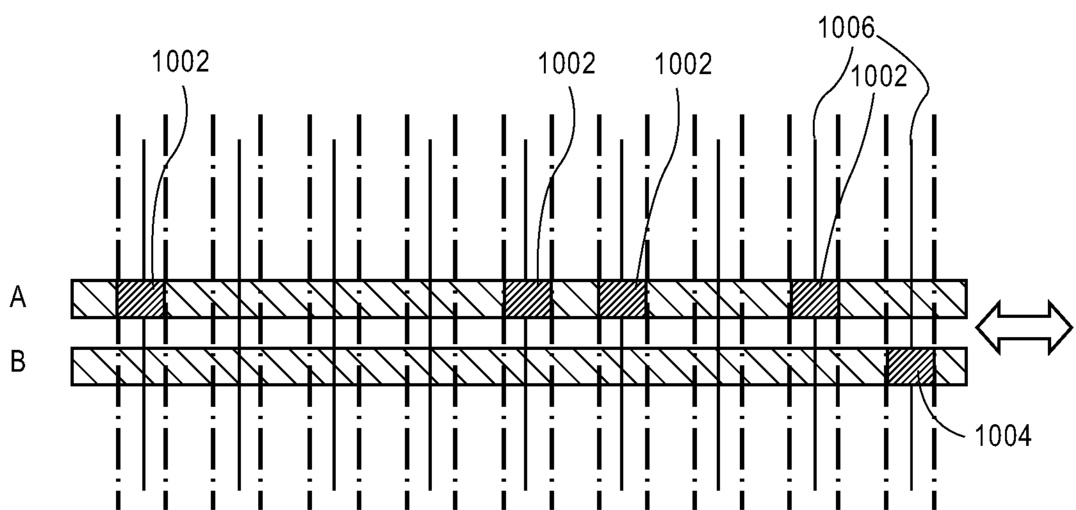


FIG. 10

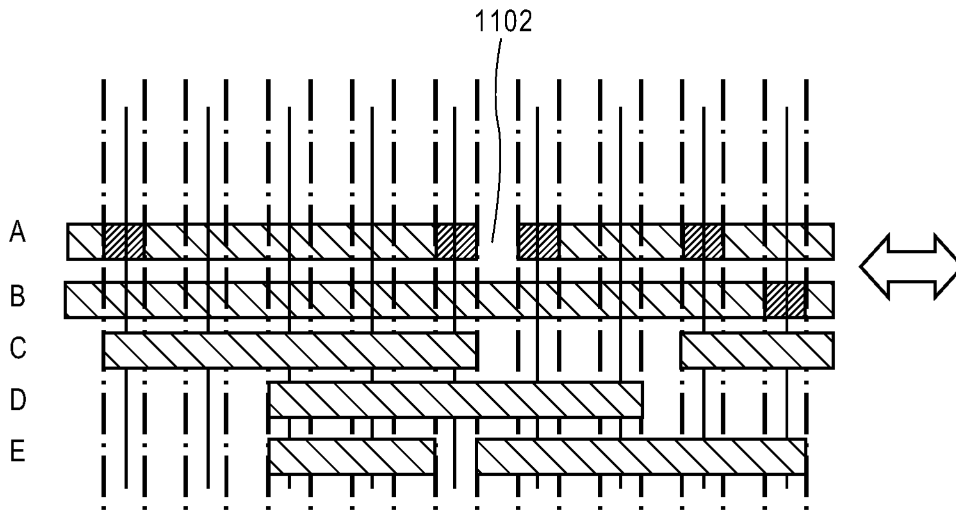


FIG. 11

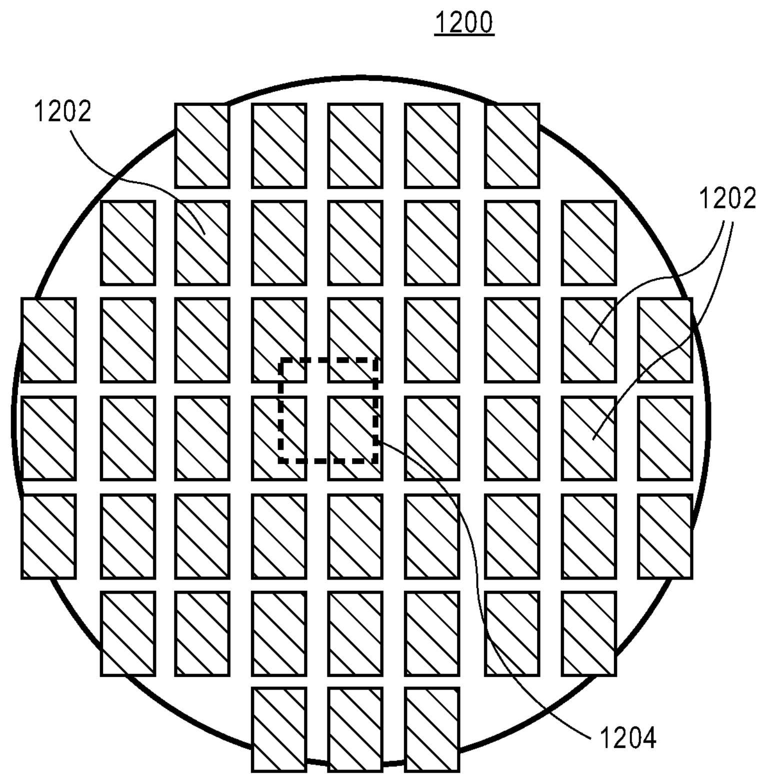


FIG. 12

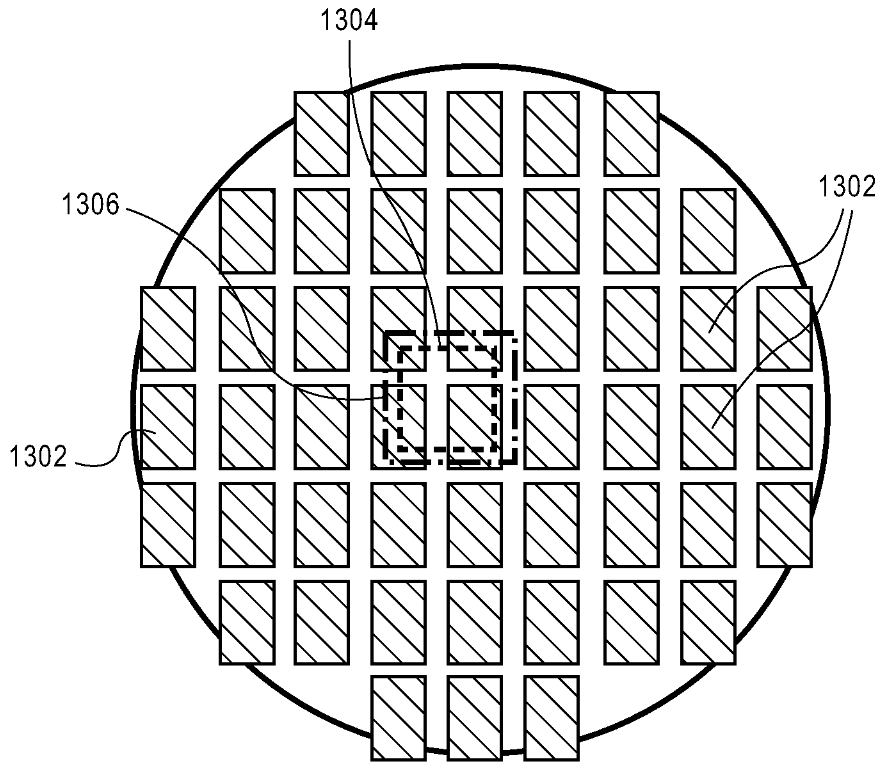


FIG. 13

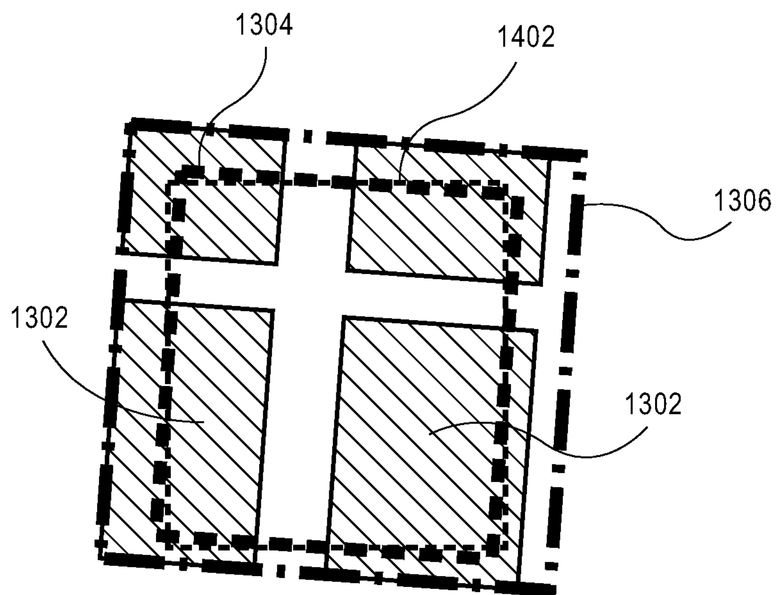


FIG. 14

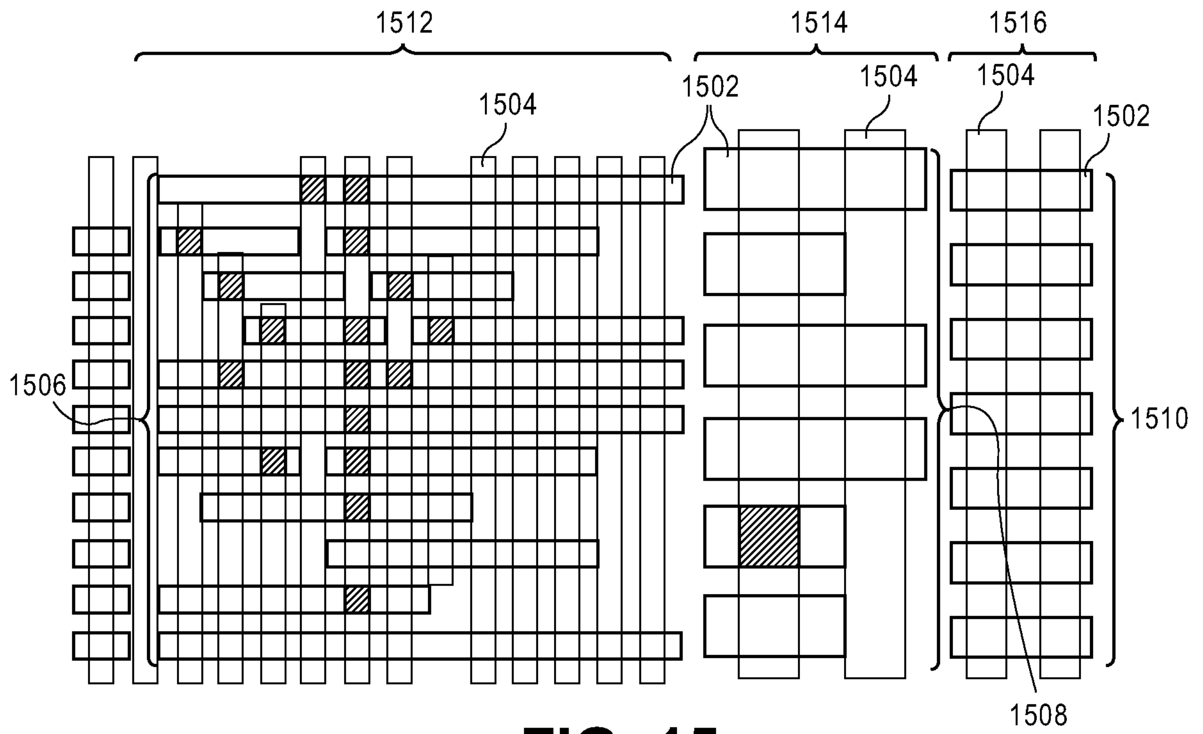


FIG. 15

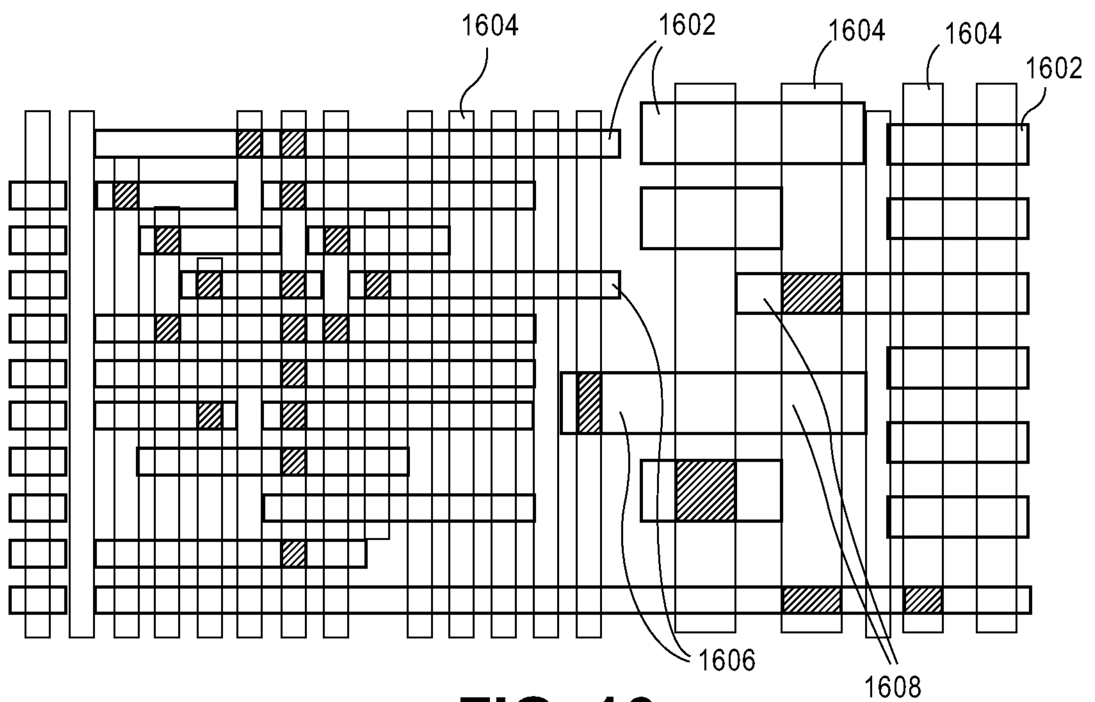


FIG. 16

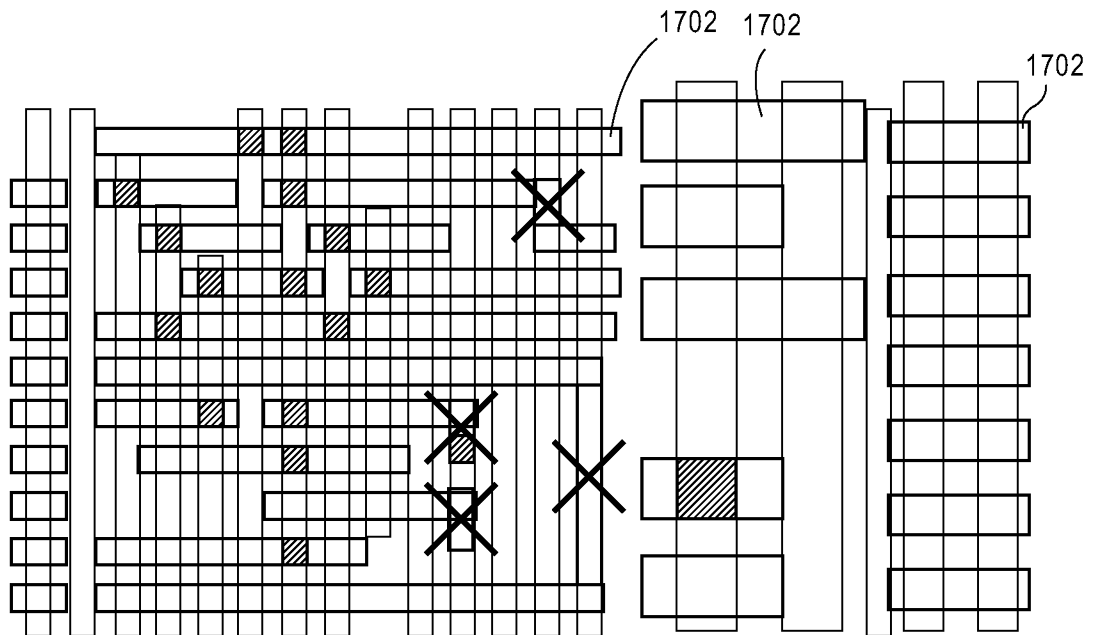


FIG. 17

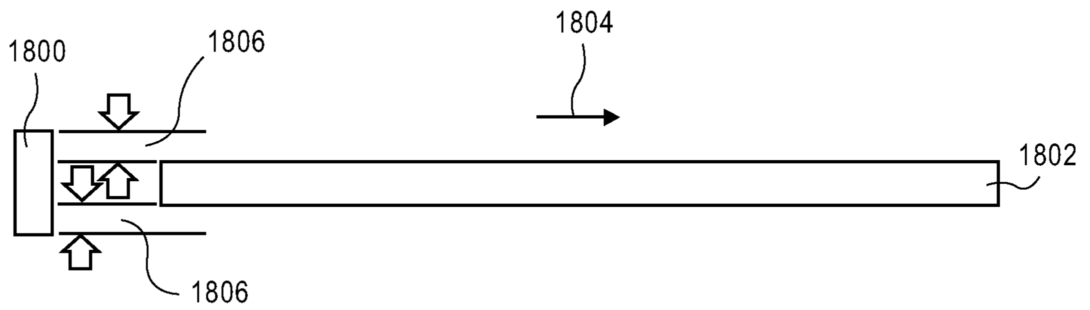


FIG. 18

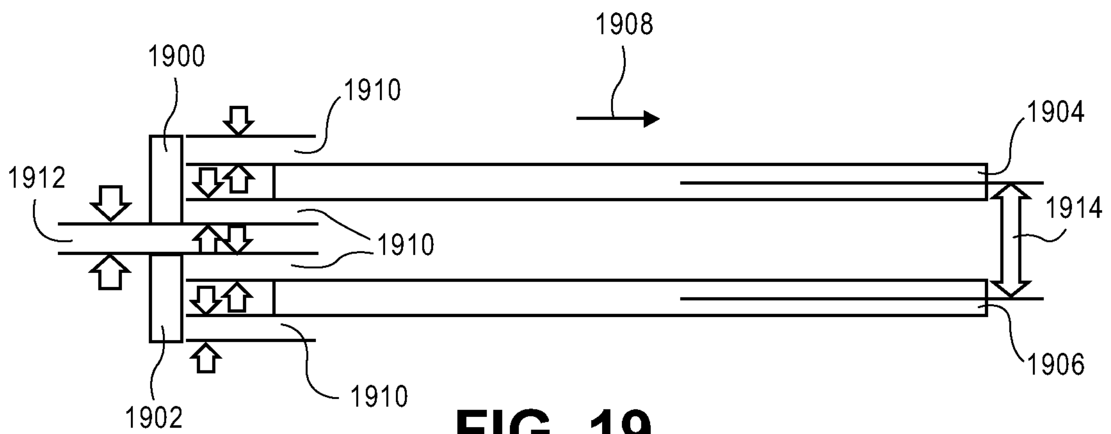


FIG. 19

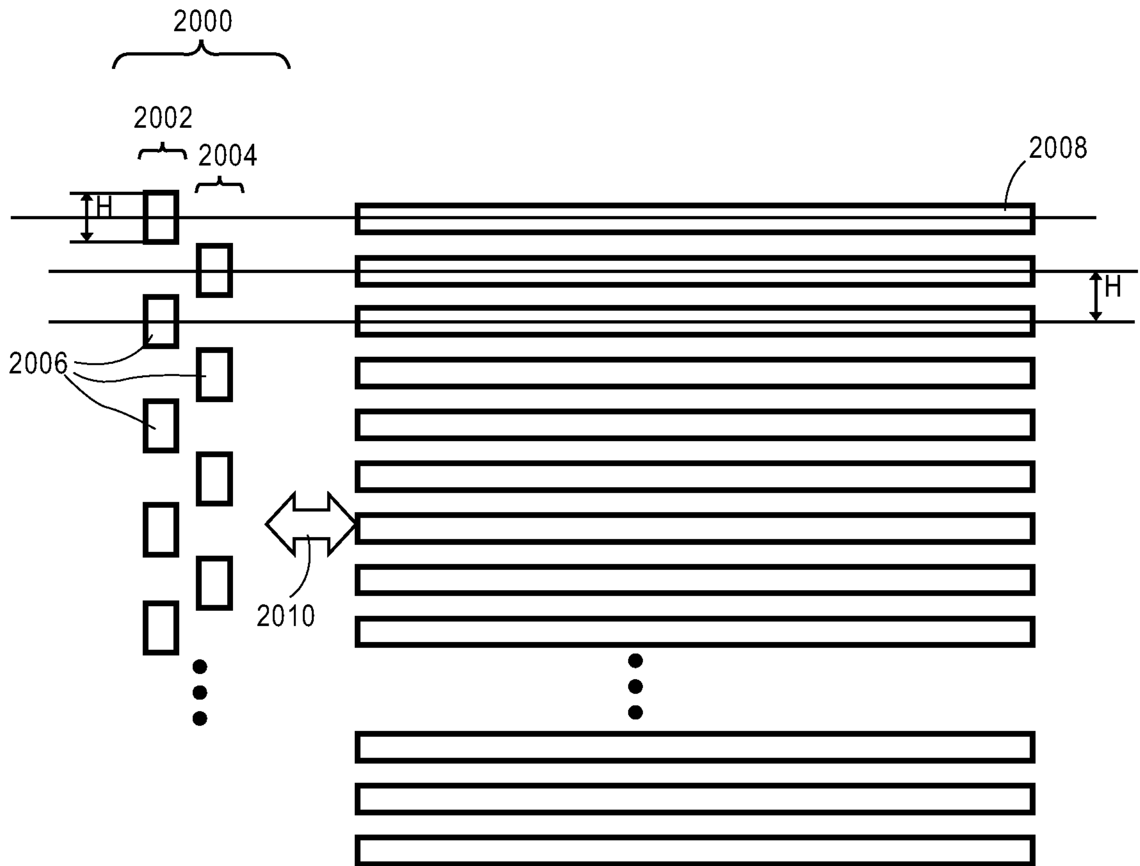


FIG. 20

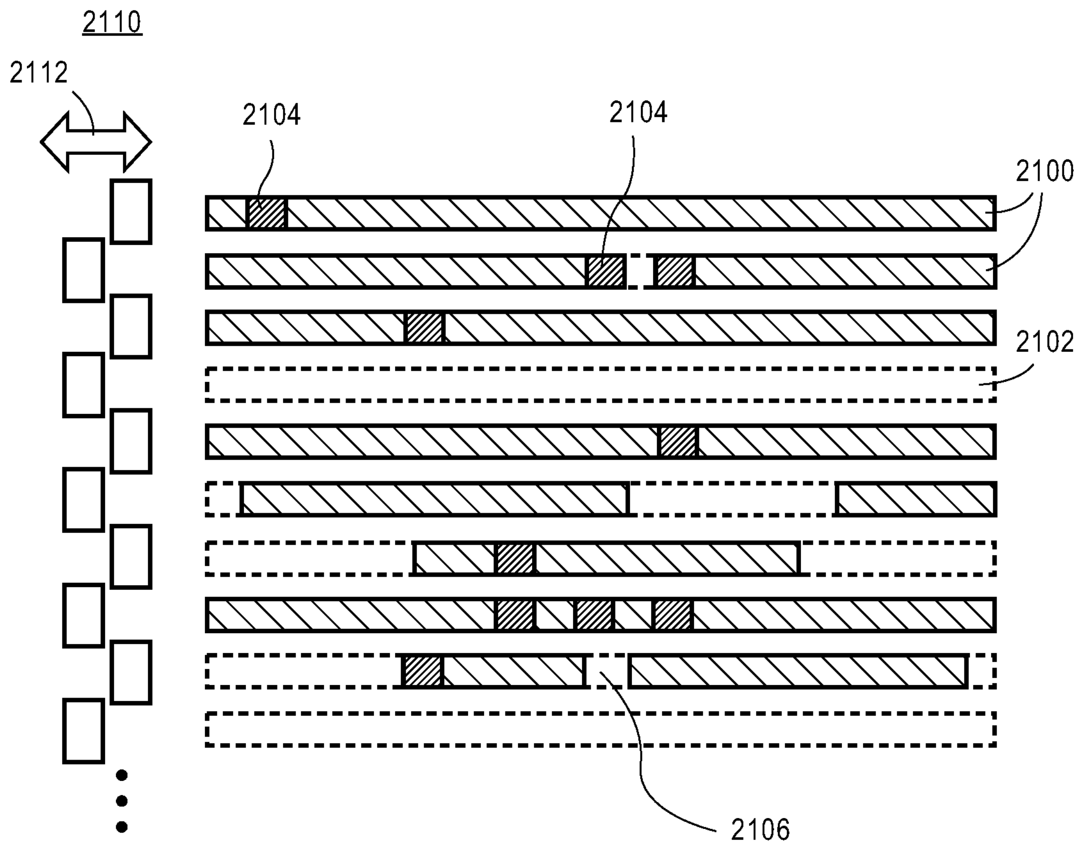


FIG. 21A

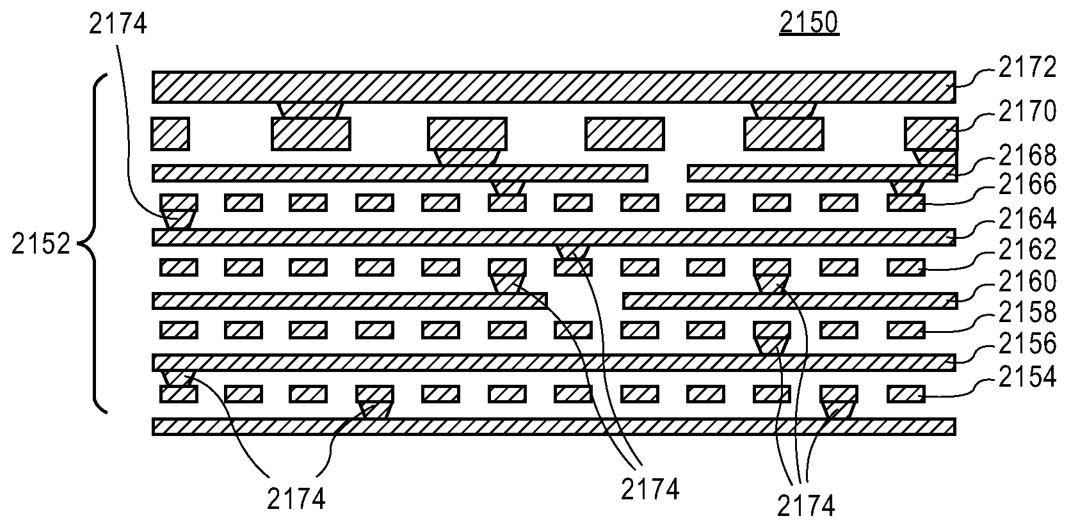


FIG. 21B

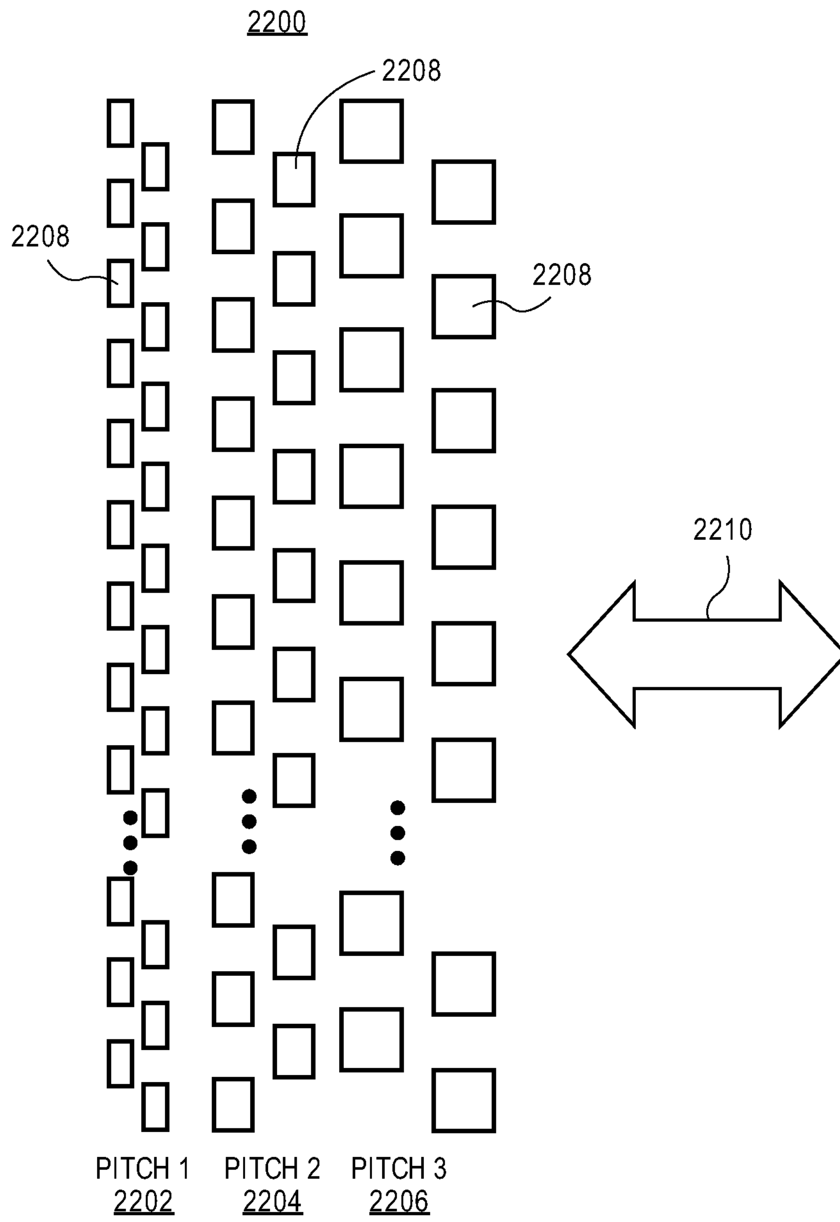


FIG. 22

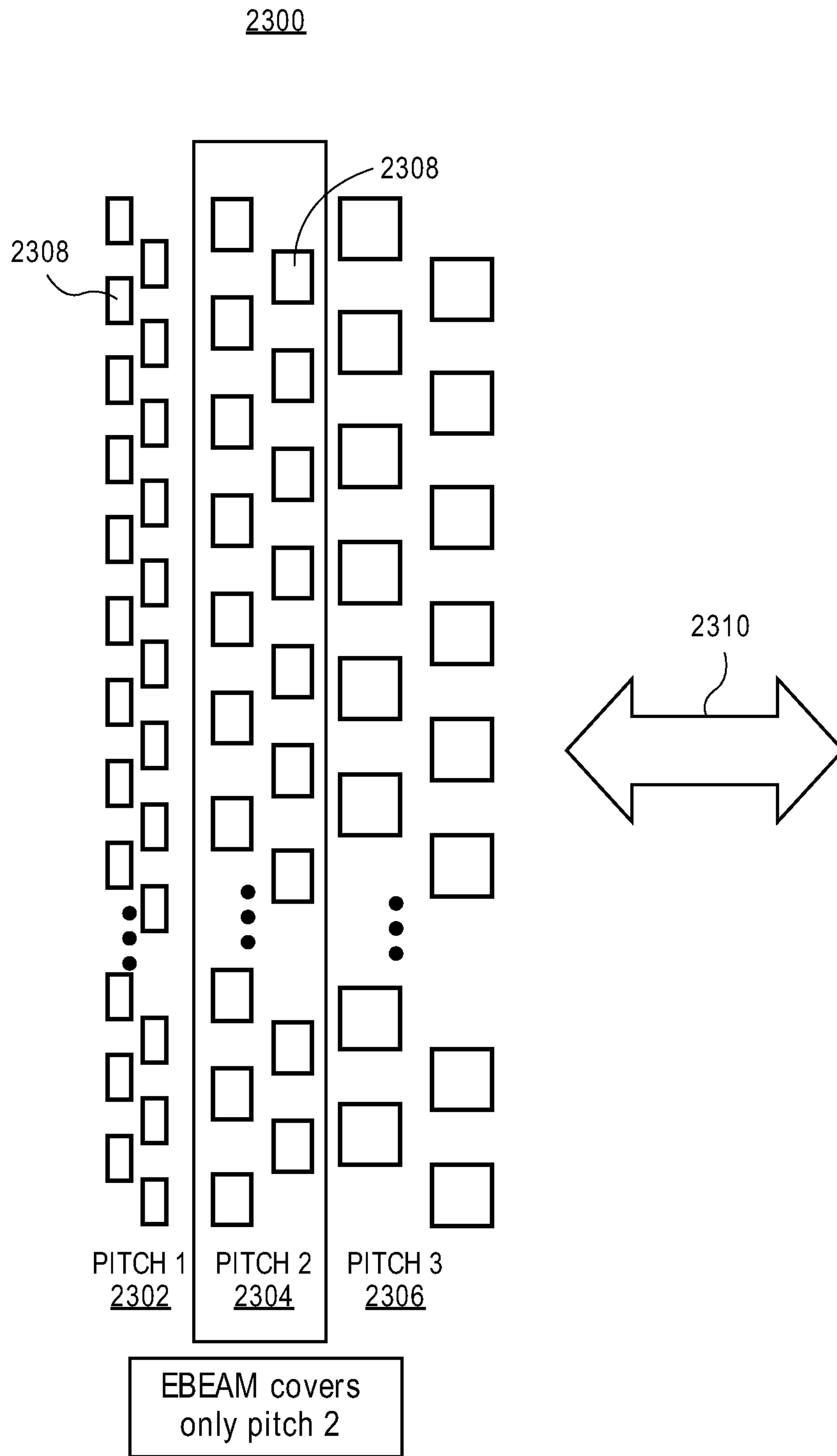


FIG. 23

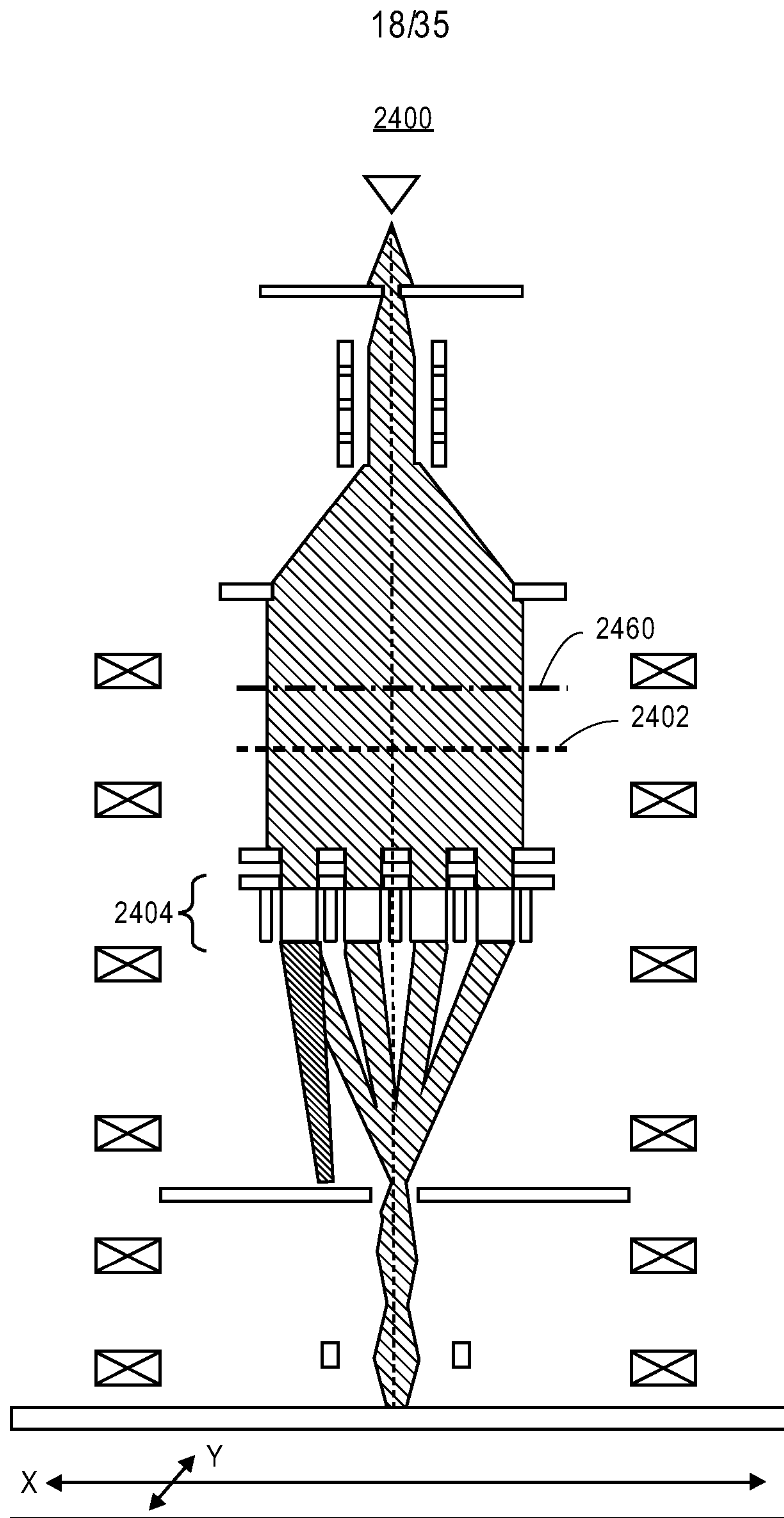


FIG. 24A

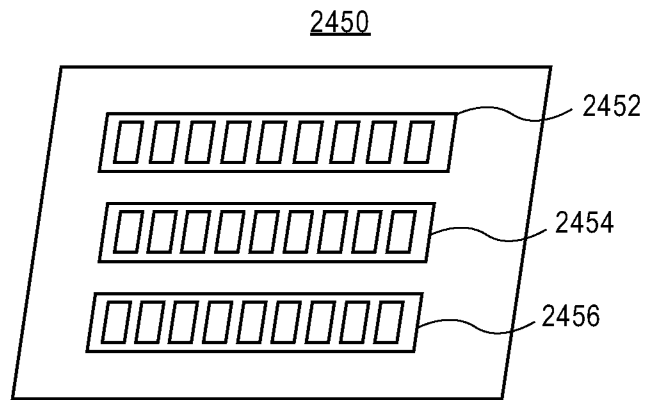


FIG. 24B

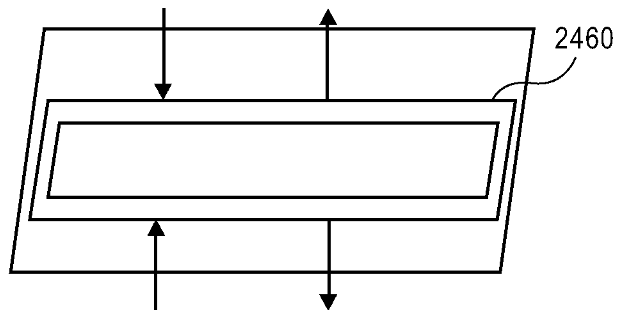


FIG. 24C

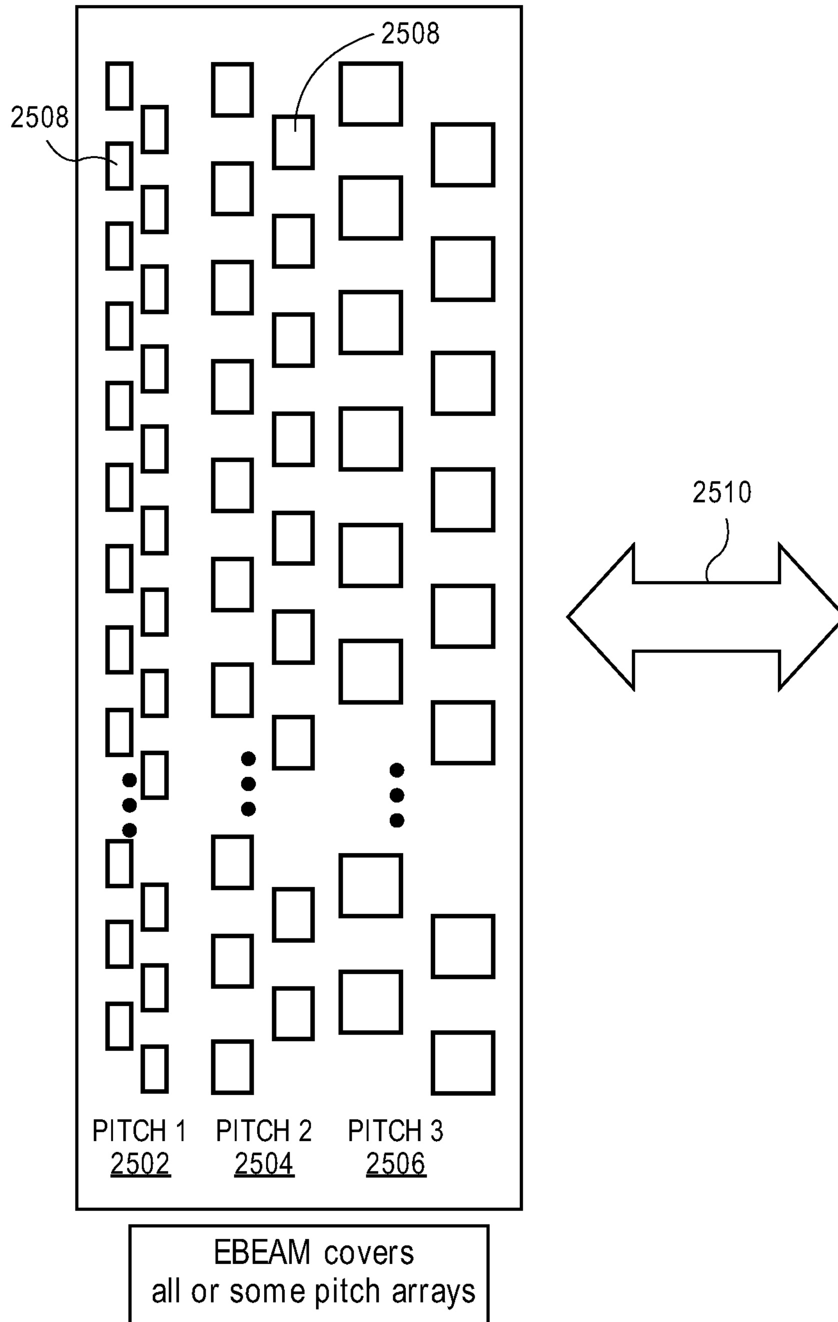


FIG. 25

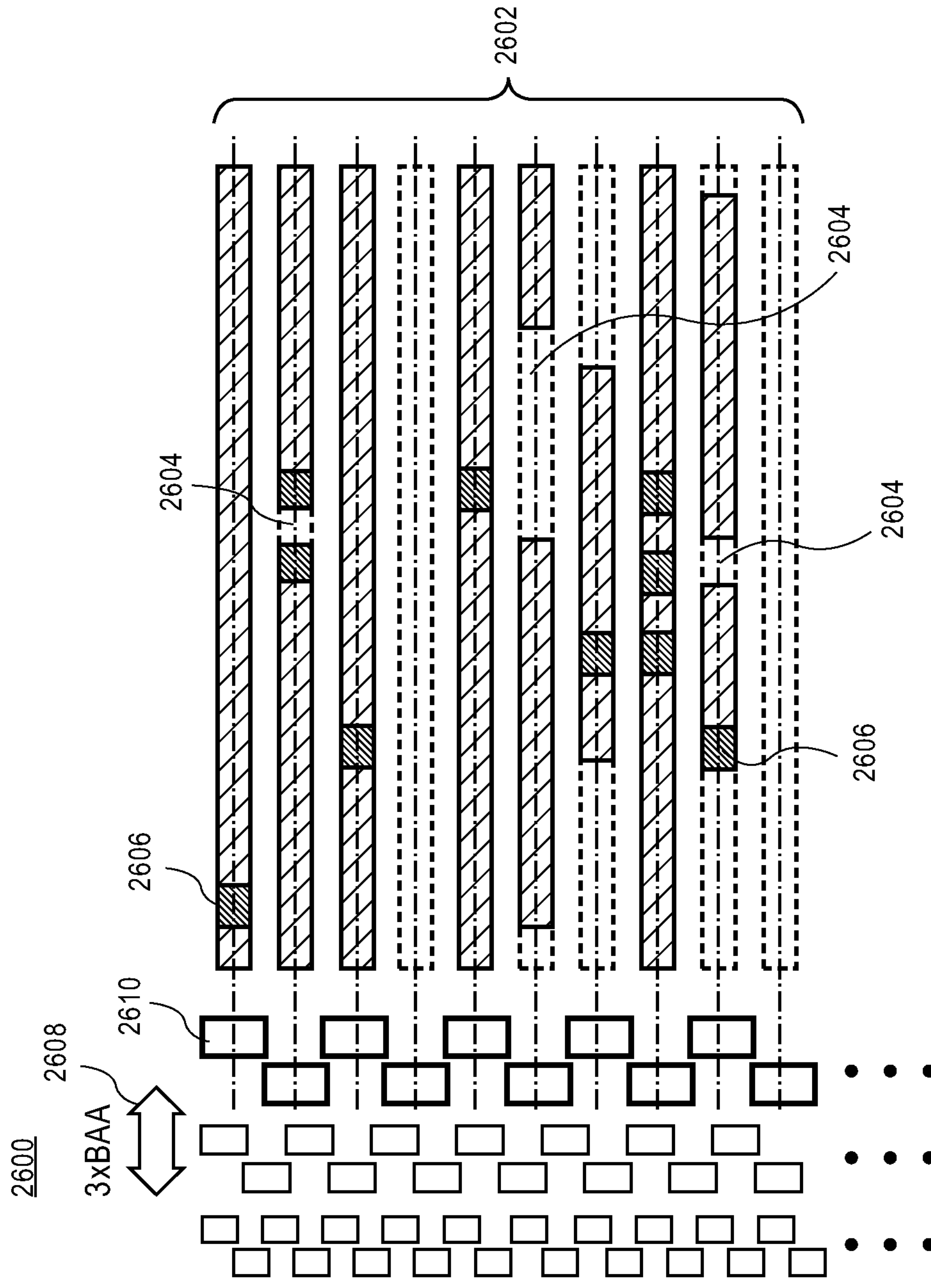


FIG. 26

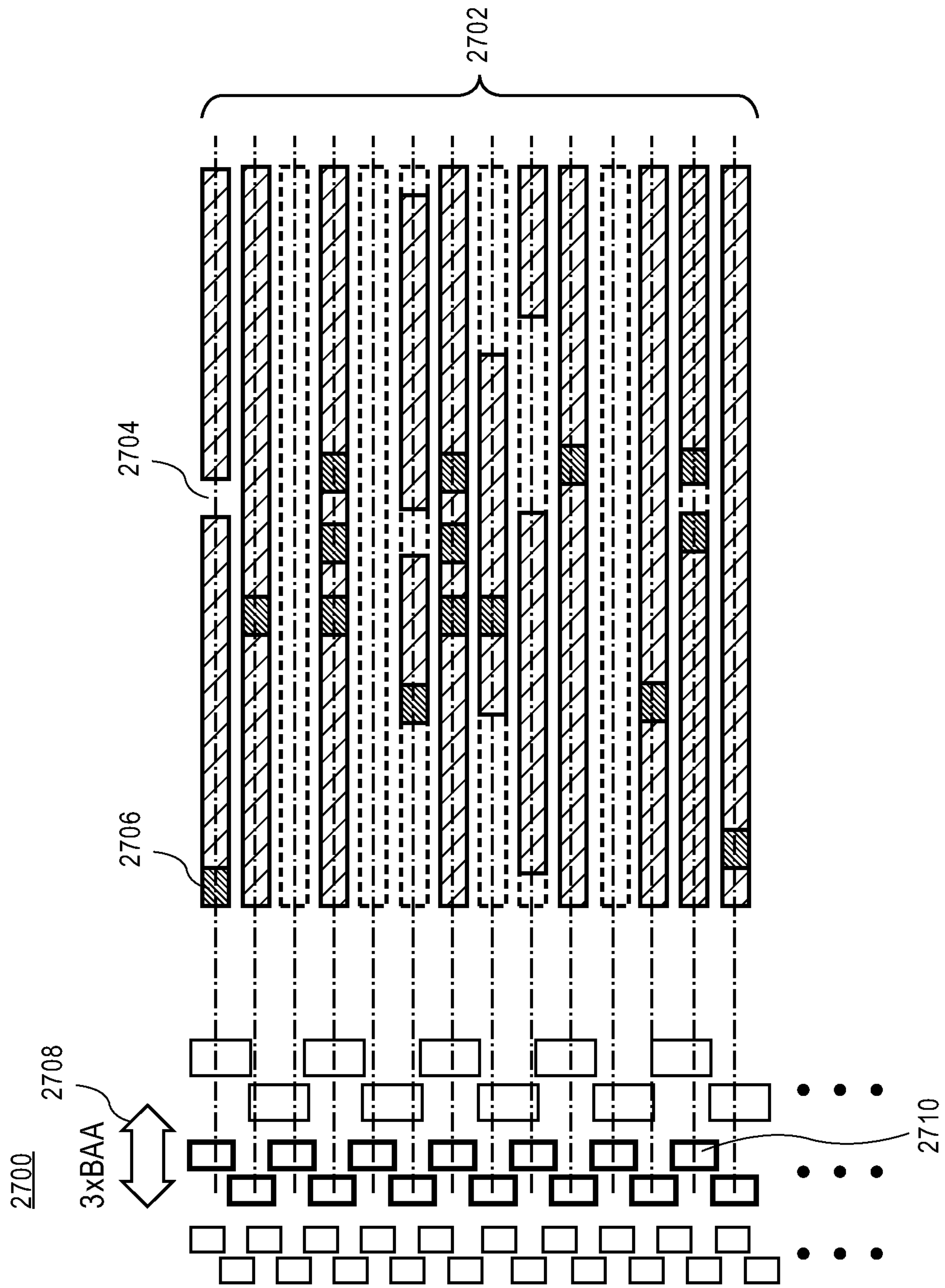


FIG. 27

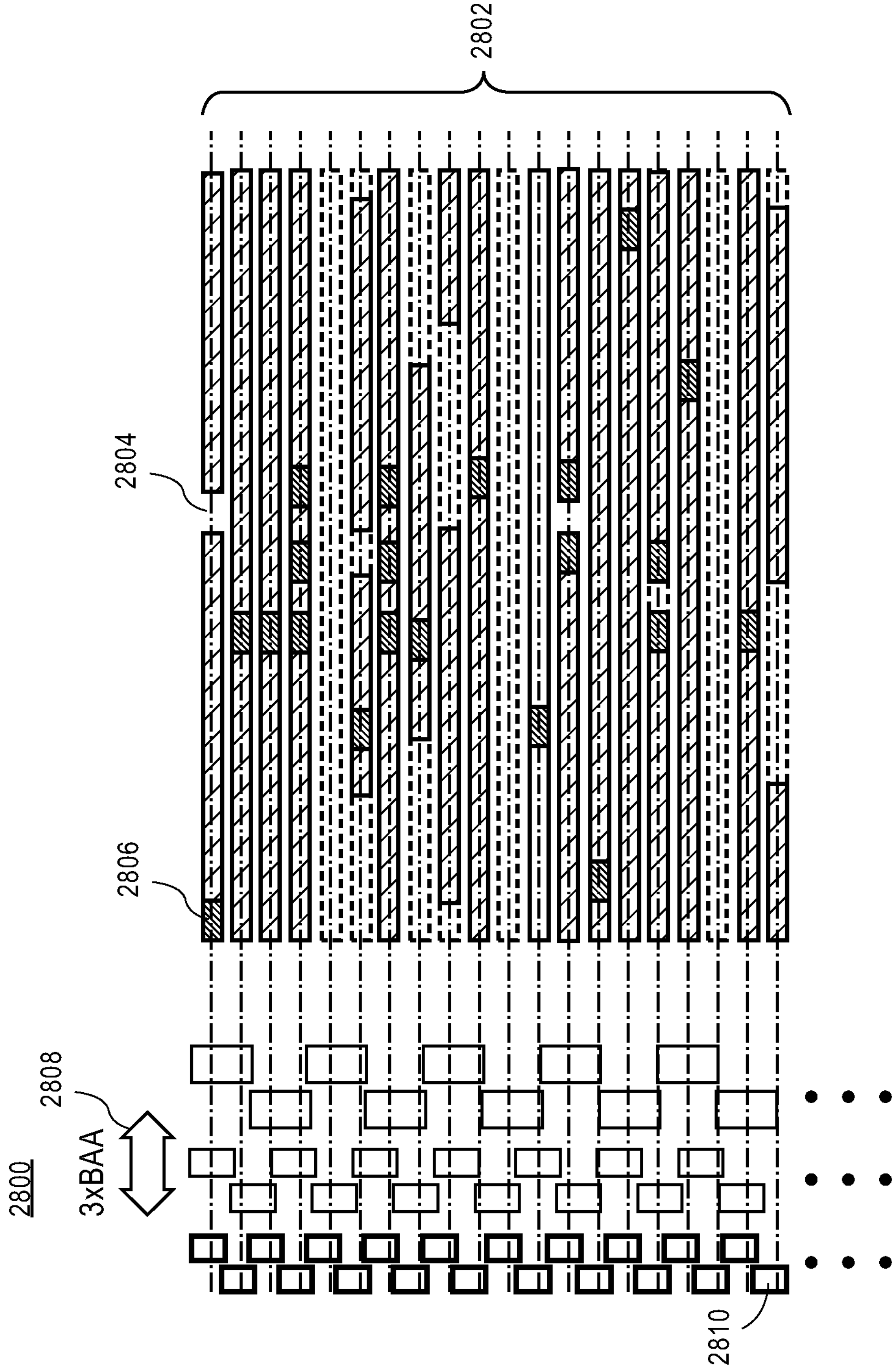


FIG. 28

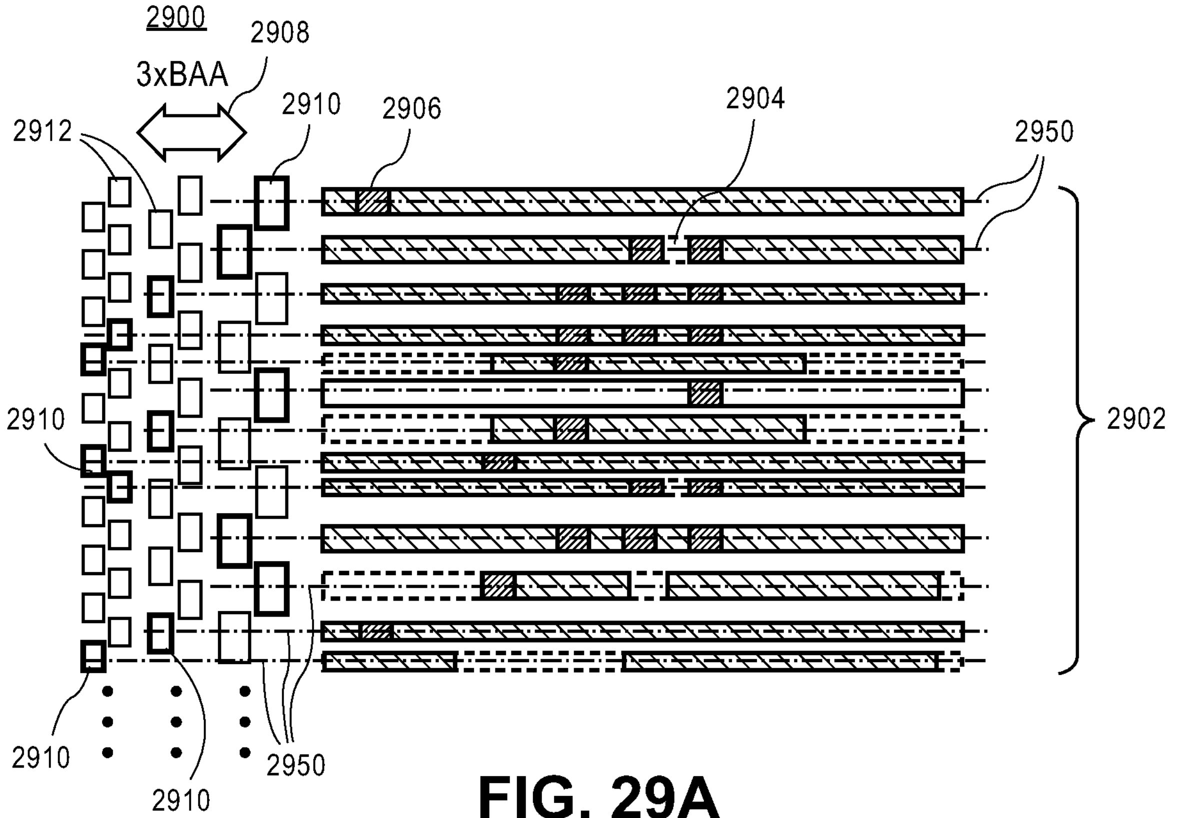


FIG. 29A

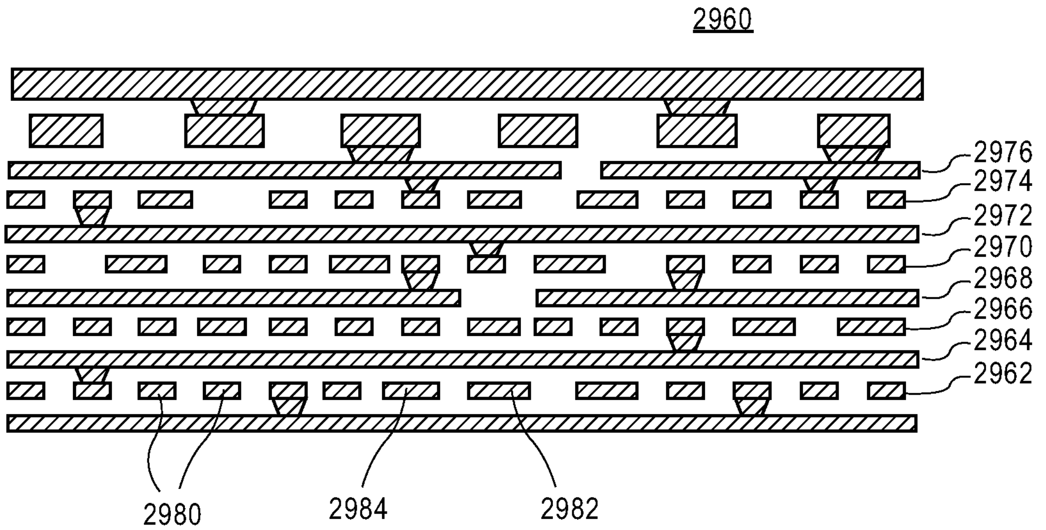


FIG. 29B

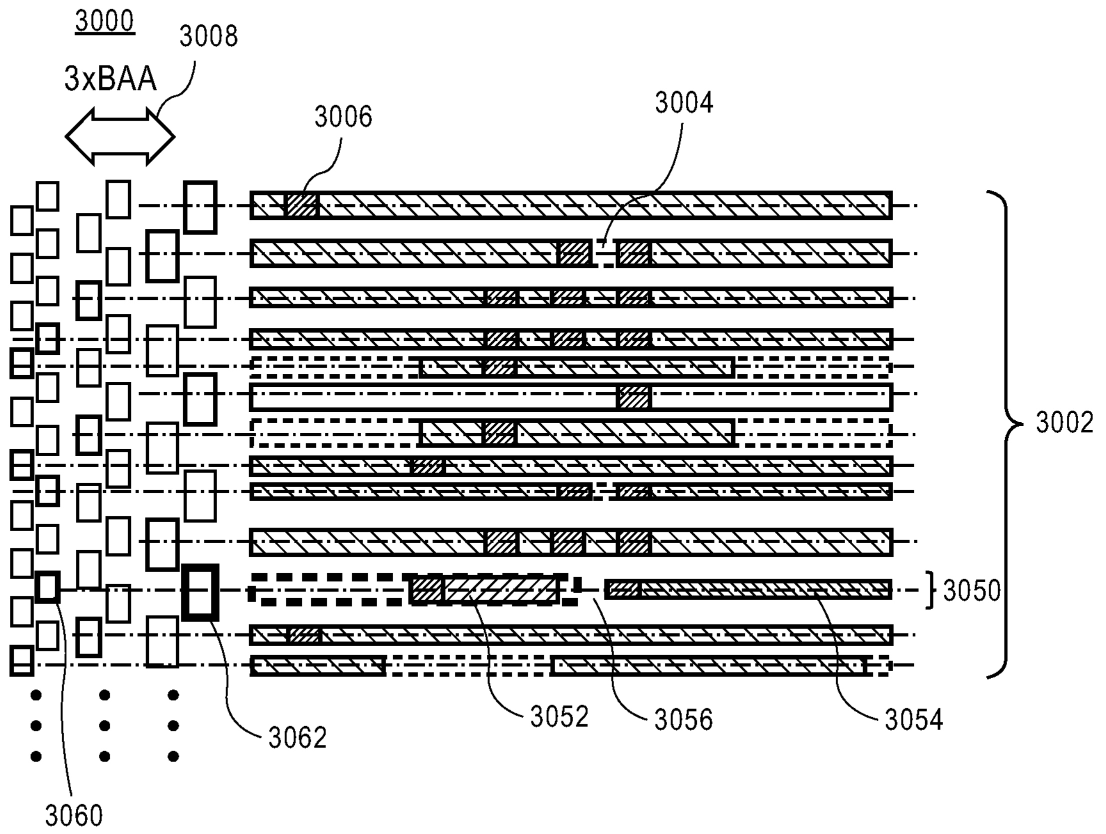


FIG. 30

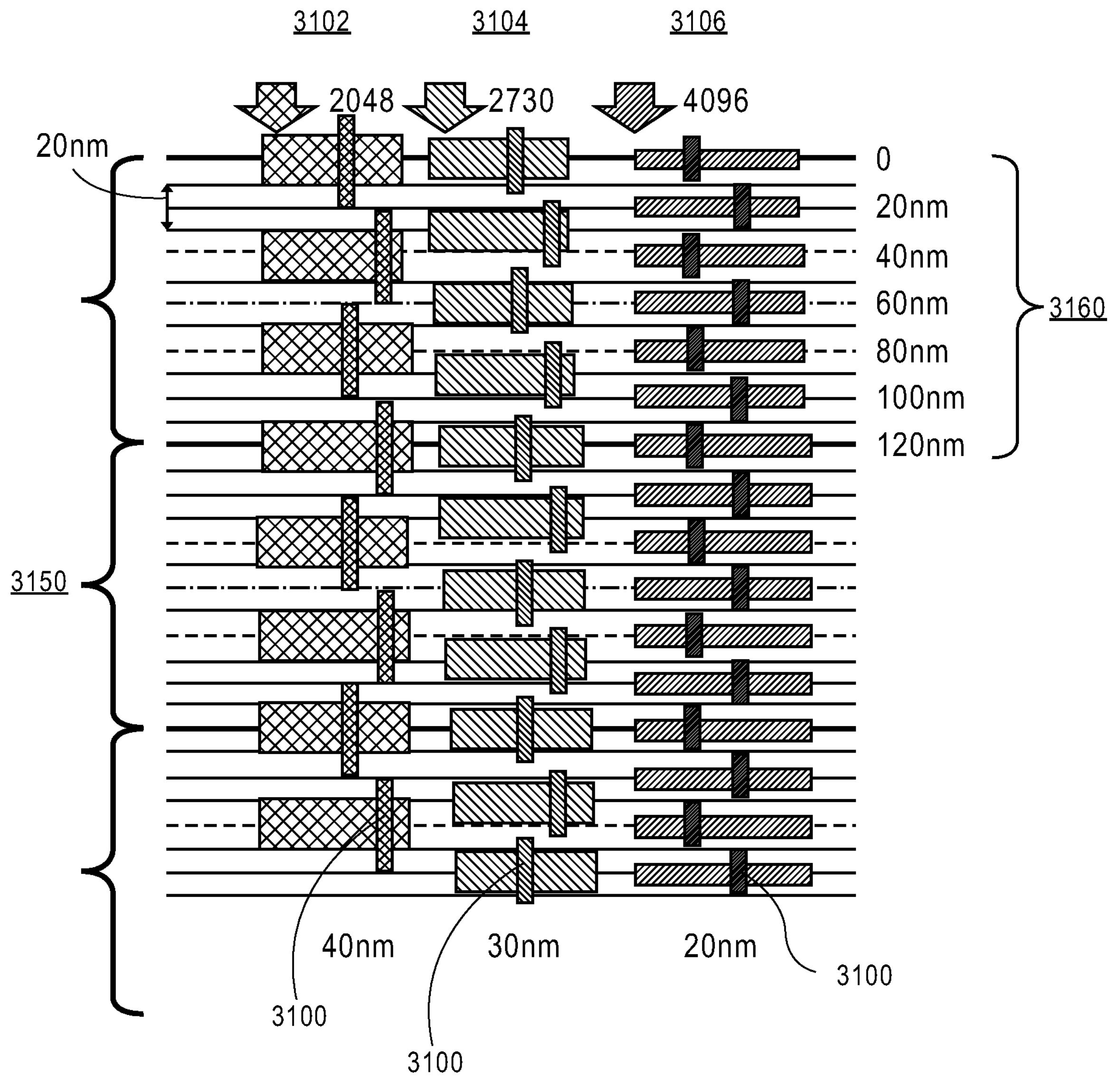


FIG. 31

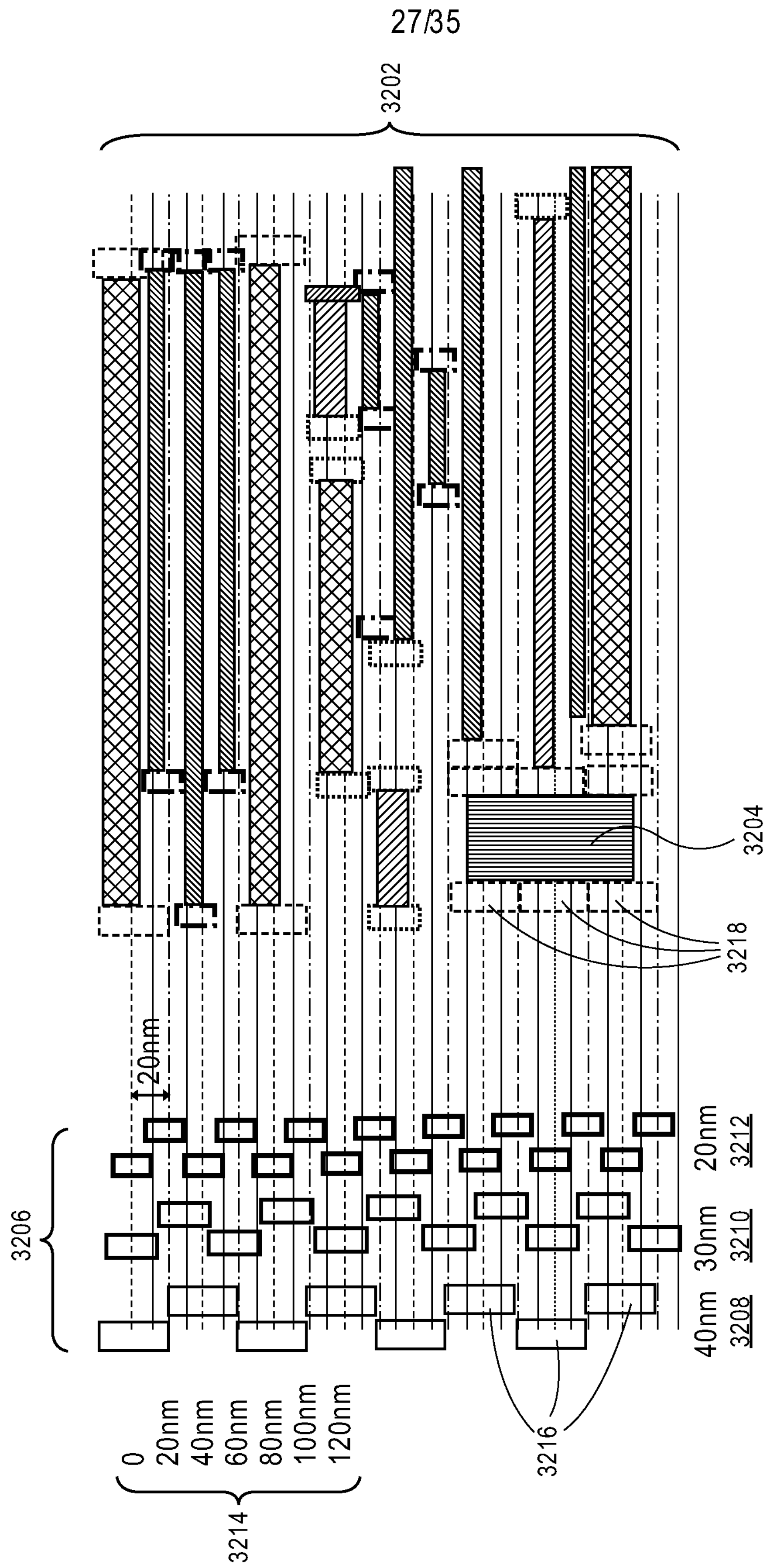


FIG. 32

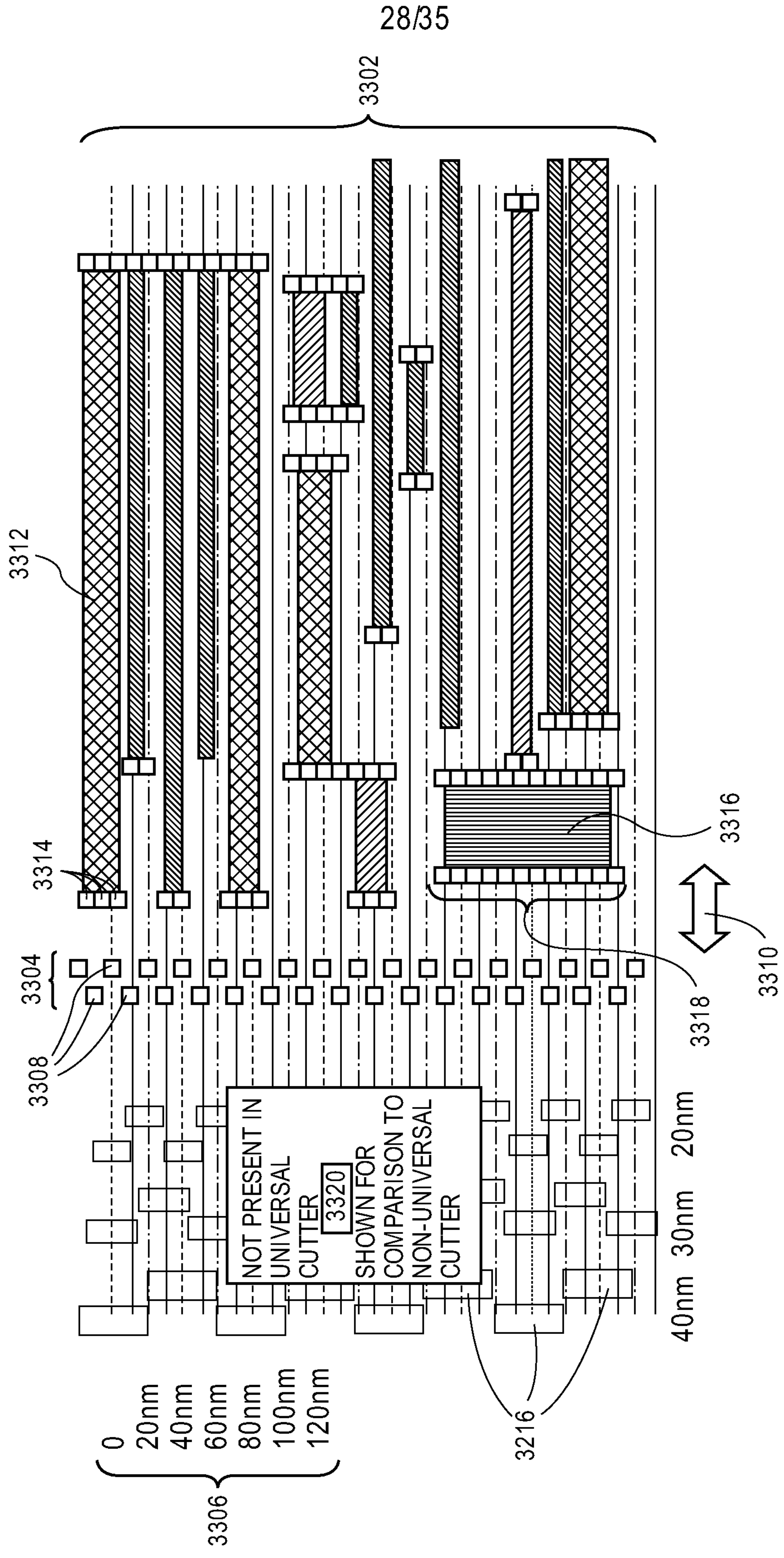


FIG. 33

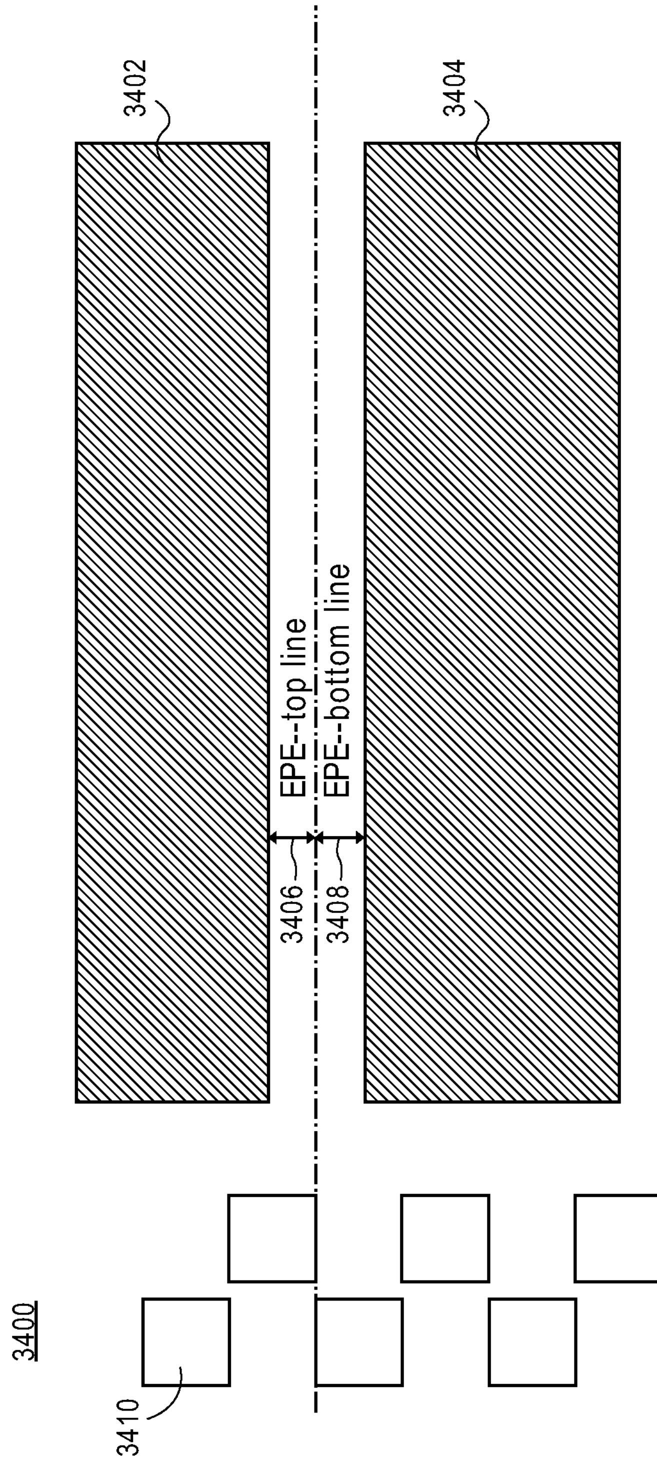
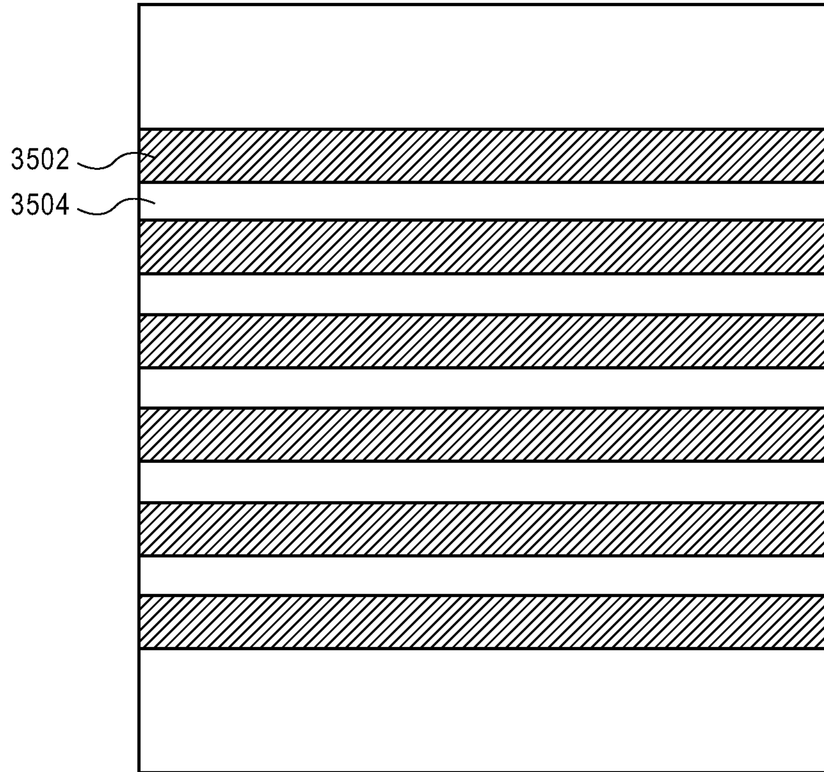


FIG. 34



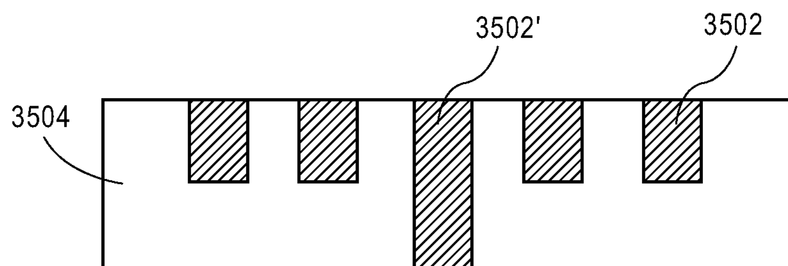


FIG. 35

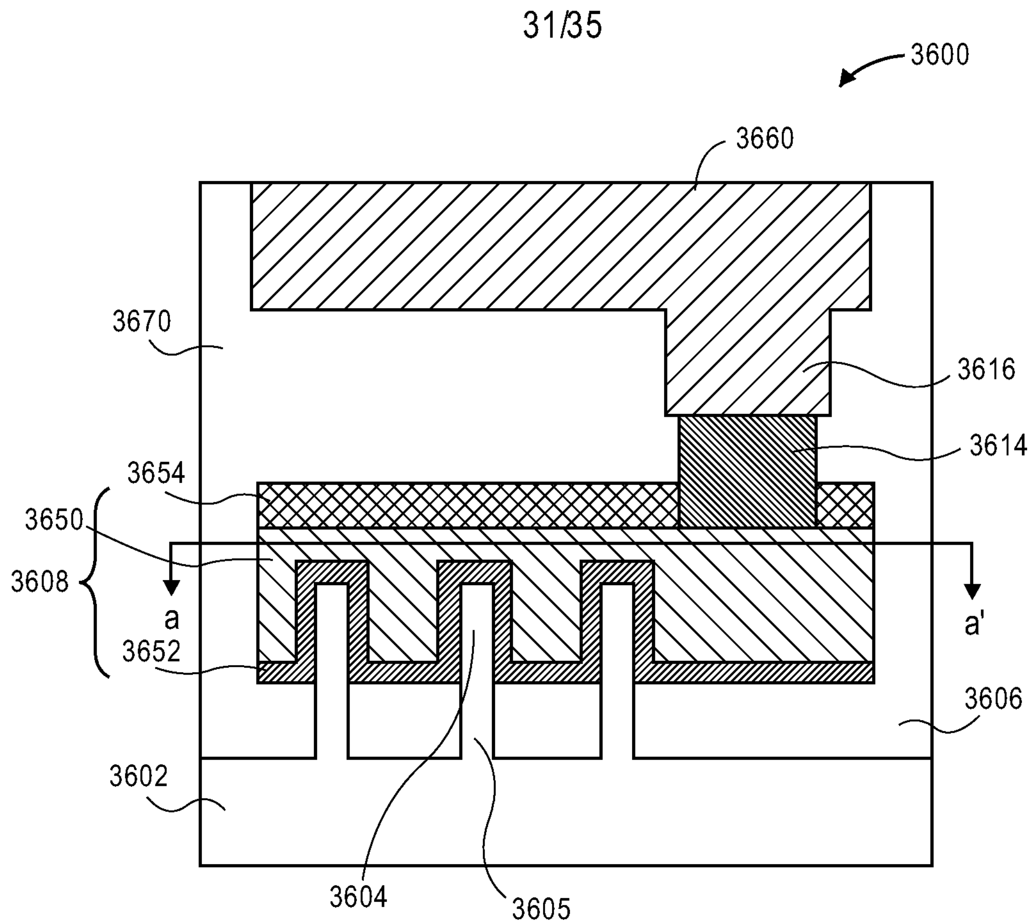


FIG. 36A

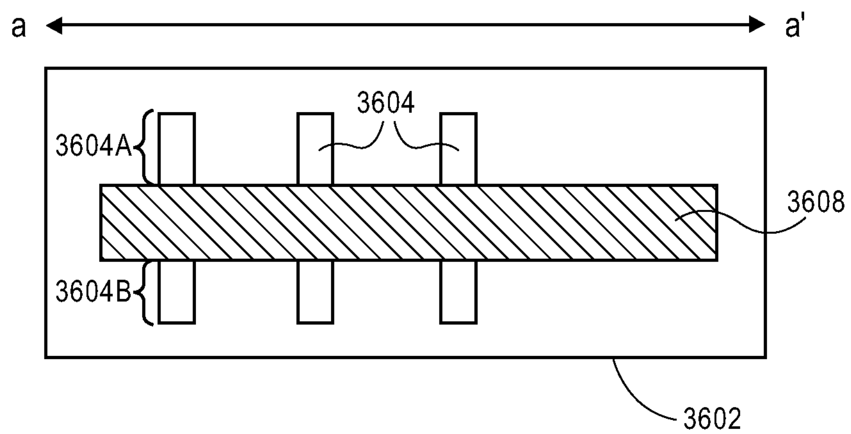


FIG. 36B

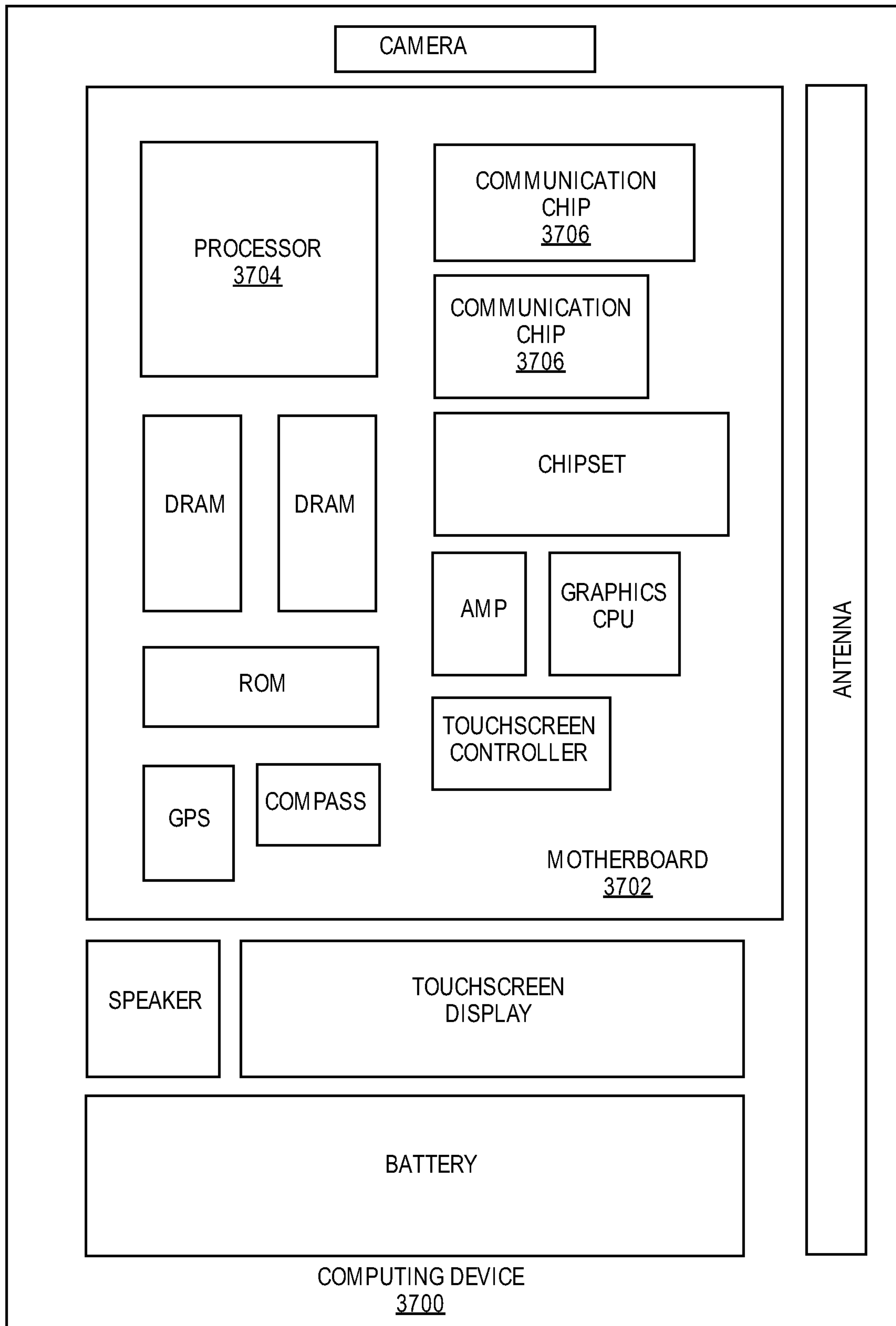


FIG. 37

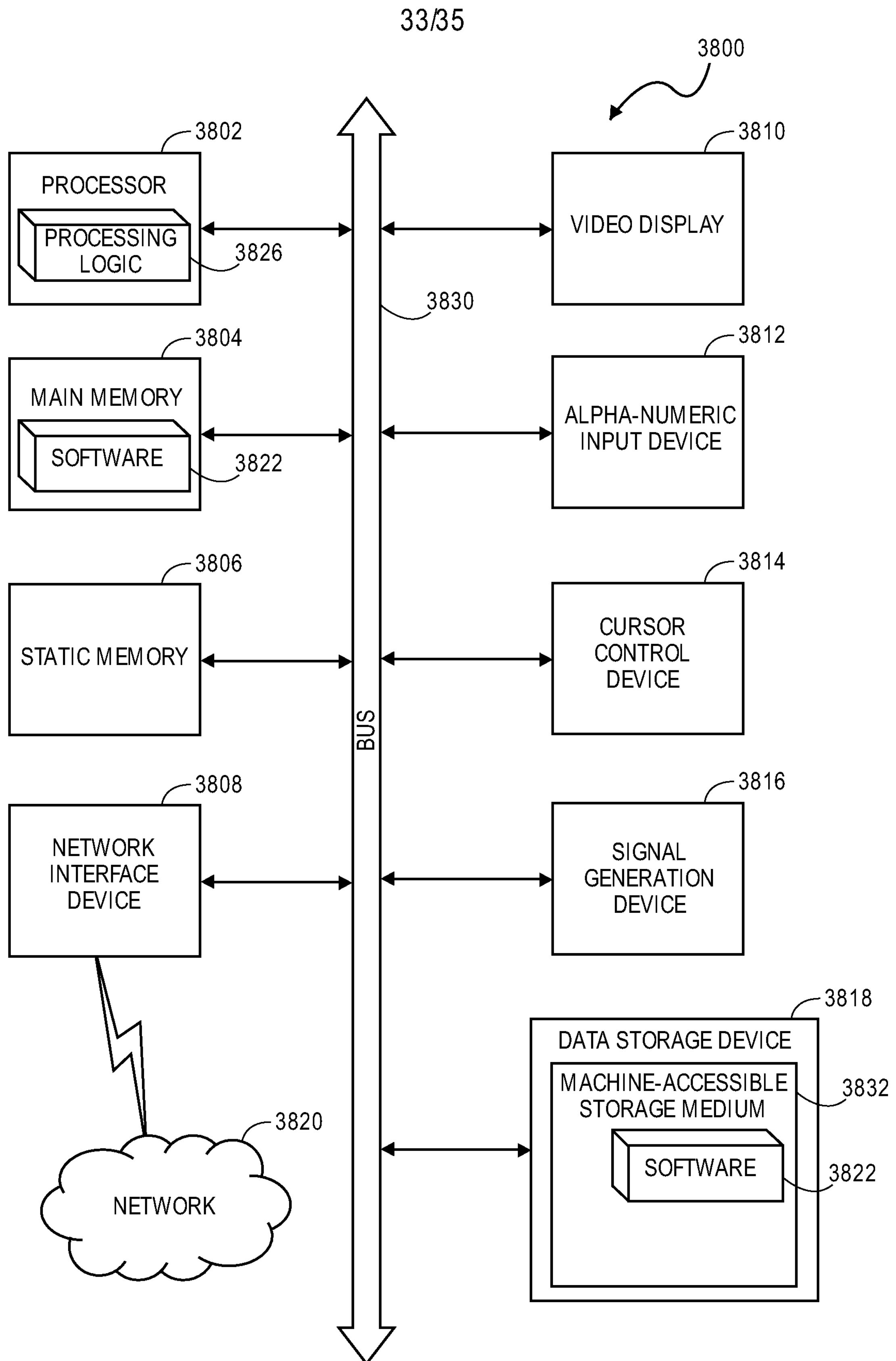


FIG. 38

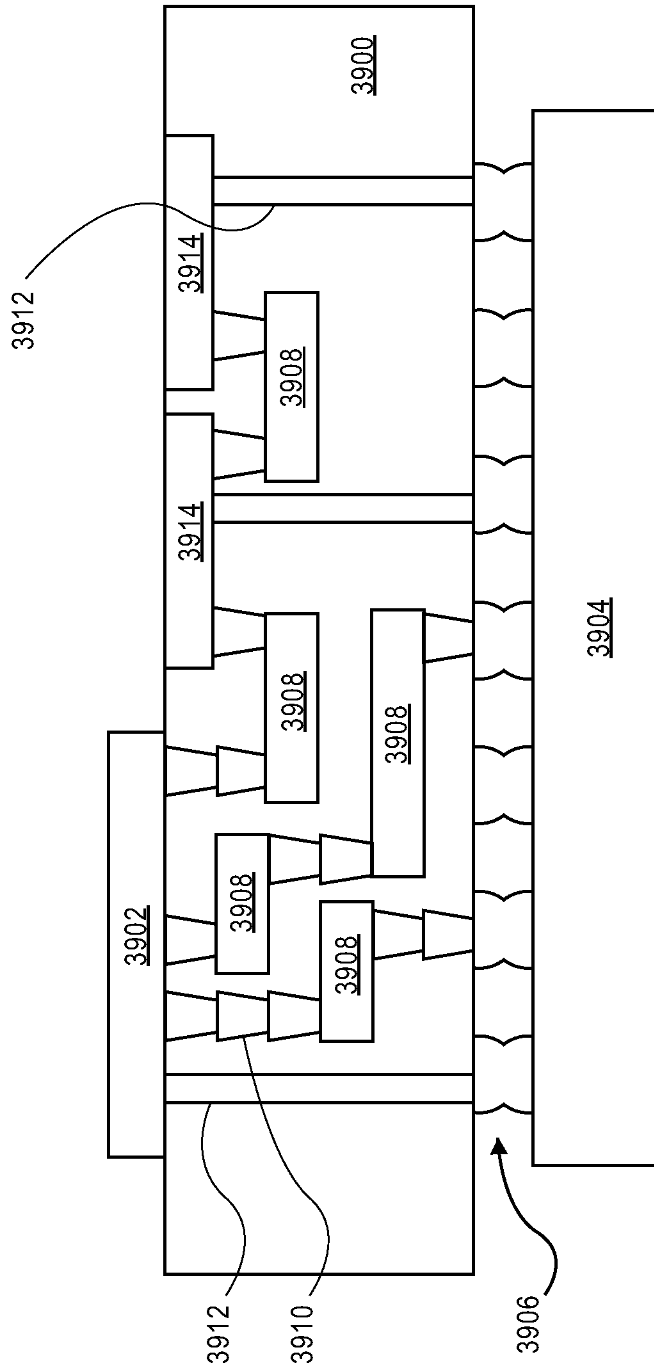


FIG. 39

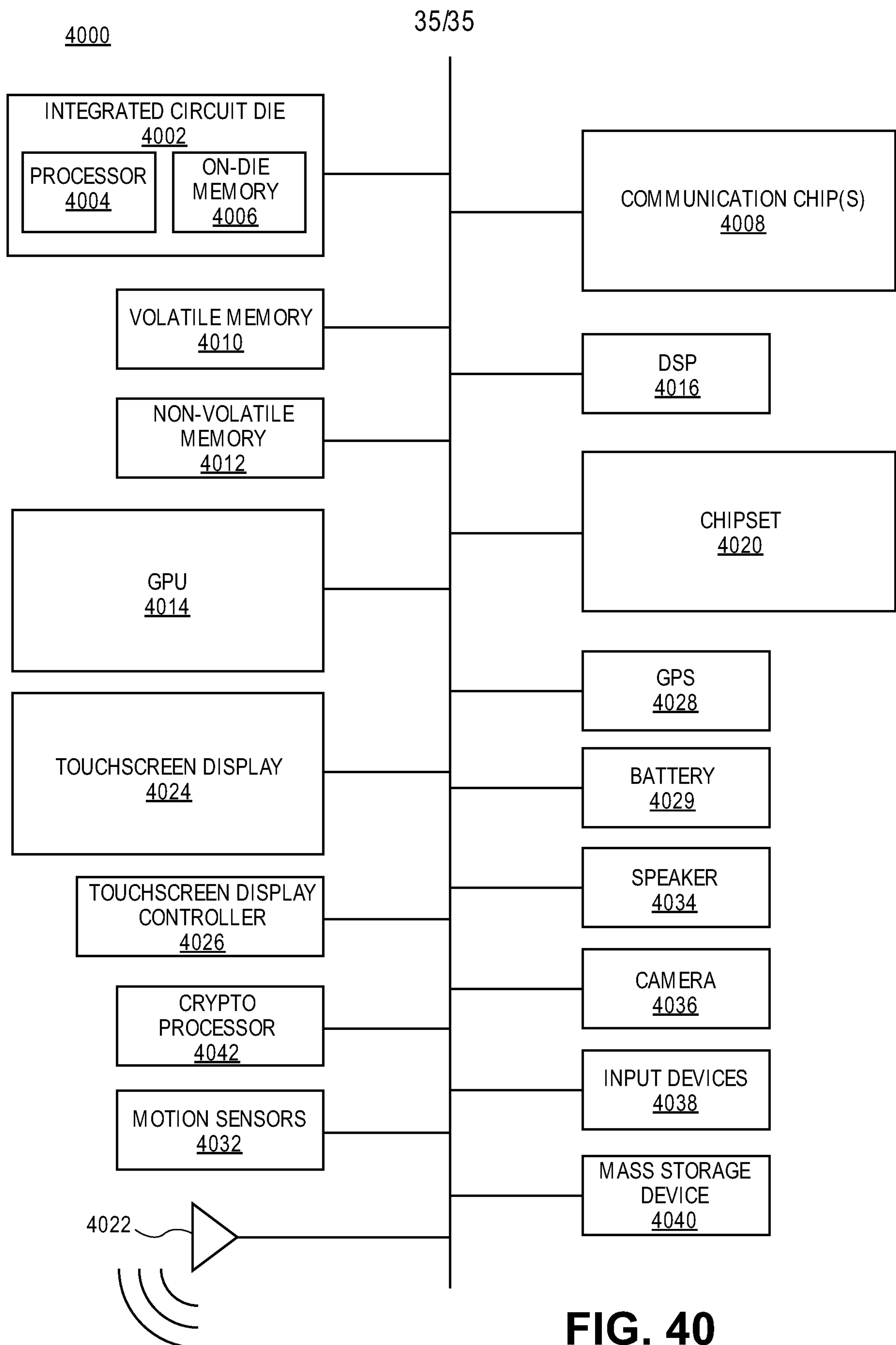


FIG. 40

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/071645

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/027(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/027; H01J 37/305; A61K 27/02; H03K 19/177; G03F 9/00; G03C 5/00; H01J 37/302

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: unidirectional, lines, integrated, pitch, logic region, analog/IO region, SRAM region

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5341049 A (ATSUSHI SHIMIZU et al.) 23 August 1994 See column 21, line 62 - column 23, line 4, claims 1, 13, 17 and figure 19.	1-14
A		15-20
A	US 7704653 B2 (VINCENZO LORDI et al.) 27 April 2010 See column 13, line 17 - column 14, line 36, claims 1, 21 and figures 1-7.	1-20
A	JP 2013-093567 A (PARAM CO., LTD.) 16 May 2013 See paragraphs [0053]-[0058], claim 1 and figures 6-18.	1-20
A	US 5294800 A (VIRGINIA M. CHUNG et al.) 15 March 1994 See column 6, line 55 - column 12, line 49, claim 3 and figures 3-5C.	1-20
A	US 4151421 A (MASAHIKO SUMI) 24 April 1979 See abstract, column 2, line 56 - column 8, line 58 and figures 2-16.	1-20

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:
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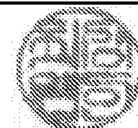
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 March 2015 (31.03.2015)	**31 March 2015 (31.03.2015)**

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. ++82 42 472 7140

Authorized officer
CHOI, Sang Won

Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2014/071645

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