(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 June 2025 (26.06.2025)

WIPO | PCT

(10) International Publication Number
WO 2025/133293 A1

(51) International Patent Classification:
G01R 31/28 (2006.01) *H03L 7/06* (2006.01)
G01R 31/317 (2006.01) *G11C 29/02* (2006.01)
G06F 1/08 (2006.01) *H03M 1/10* (2006.01)
G06F 30/367 (2020.01) *H03M 1/00* (2006.01)
G04F 10/00 (2006.01) *H04B 17/00* (2015.01)
H03L 7/08 (2006.01)

(21) International Application Number:
PCT/EP2024/088162

(22) International Filing Date:
20 December 2024 (20.12.2024)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20237214 22 December 2023 (22.12.2023) FI

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE,

(54) Title: INTEGRATED CIRCUIT TESTING

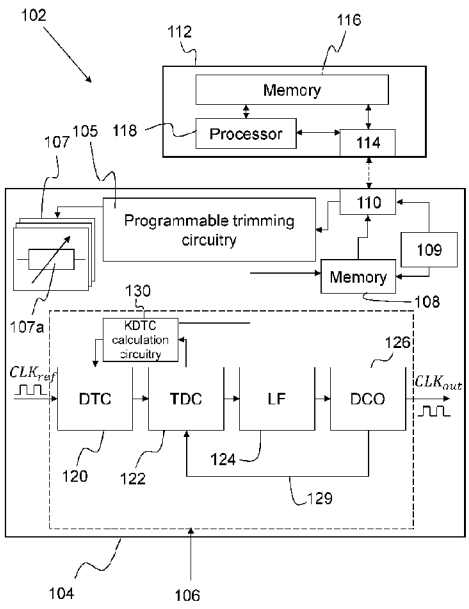


FIG. 1

(57) Abstract: A system (102) for characterising an integrated circuit (104) comprises an integrated circuit (104), a processor (118) and a memory (116) storing instructions that cause the processor (118) to run a characterisation model. The integrated circuit (104) comprises an all-digital phase-locked loop (106) that generates an output clock signal with the same phase as a reference clock signal. The all-digital phase-locked loop (106) comprises a digital-to-time converter (120) that delays the reference clock signal. The integrated circuit (104) also includes circuitry (130) for generating an indication of the step size of the digital-to-time converter (120), and memory (108) for storing this indication. The processor (118) receives the indication from the memory (108), and runs the characterisation model to generate a characterisation of the integrated circuit (104) based on the step-size of the digital- to-time converter (120).

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SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

Integrated Circuit Testing

Technical Field

The present invention relates to the testing and/or characterisation of integrated circuits (ICs).

Background

Modern integrated circuits such as radio frequency integrated circuits (RFICs) are designed to a specification that defines features of the circuit that relate to its performance. Specifications for each sub-circuit within the integrated circuit can be derived from this broad specification.

The design of the circuit is performed with process, voltage and temperature (PVT) variations in mind, to help to ensure that the manufactured circuit will be capable of meeting the specification under a range of conditions. In particular it is necessary to ensure that a minimum performance is maintained even under the 'worst' combination of conditions, known as "corners".

One way to obtain information relating to PVT variations is from Process Control Monitoring (PCM). This information can then be used to characterise the integrated circuit, which may involve indicating to what extent the circuit meets the specification, or indicating one or more parameters of the circuit that should be adjusted in order to meet the specification (known as "trimming" the integrated circuit, e.g. changing the bias voltage and/or the supply from low-dropout regulators (LDOs) within the circuit).

However, PCM is typically a complex process and may incur significant costs, including upfront costs for investing in the required analysis equipment and operational costs, owing at least in part to the time-consuming nature of the process.

Furthermore, PCM is typically performed only once, shortly after manufacturing the integrated circuit, and it is often difficult or even impossible to perform PCM after the integrated circuit has been implemented in an end product. As transistor performance can degrade over time, then the information obtained from PCM may become outdated over the lifetime of the integrated circuit, meaning that the trimming strategy may become less effective. This can lead to unnecessary power consumption and/or a decrease in performance of the integrated circuit.

Some attempts have been made to provide dedicated circuitry on the integrated circuit to generate in-situ PVT variation information. However, this occupies silicon area and requires that the integrated circuit be run in a “test mode” in order to obtain the data.

The present invention seeks to provide an improved approach.

Summary of the Invention

When viewed form a first aspect, the present invention provides a system for characterising an integrated circuit, the system comprising:

a) an integrated circuit comprising:

i) an all-digital phase-locked loop configured to receive a reference clock signal and to generate an output clock signal having the same phase as the reference clock signal, wherein the all-digital phase-locked loop comprises:

a digital-to-time converter configured to delay the reference clock signal by a delay length; and

circuitry configured to generate an indication of a step size of the digital-to-time converter, wherein the step-size of the digital-to-time converter is proportional to the shortest non-zero delay length that the digital-time converter is configured to generate; and

ii) a first memory configured to store the indication of the step size of the digital-to-time converter;

b) a processor; and

c) a second memory storing instructions which, when executed by the processor, cause the processor to run a characterisation model for characterising the integrated circuit,

wherein the processor is configured to receive the indication of the step size of the digital-to-time converter from the first memory and run the characterisation model to generate a characterisation of the integrated circuit based on the step-size of the digital-to-time converter.

When viewed from a further aspect, the invention provides a method of characterising an integrated circuit, the integrated circuit comprising:

i) an all-digital phase-locked loop configured to receive a reference clock signal and to generate an output clock signal having the same phase as the reference clock signal, wherein the all-digital phase-locked loop comprises:

a digital-to-time converter configured to delay the reference clock signal by a delay length; and

circuitry configured to generate an indication of a step size of the digital-to-time converter, wherein the step-size of the digital-to-time converter is proportional to the shortest non-zero delay length that the digital-time converter is configured to generate; and

ii) a first memory configured to store the indication of the step size of the digital-to-time converter;

the method comprising:

the circuitry of the all-digital phase-locked loop generating an indication of the step size of the digital-to-time converter and storing the indication in the first memory; and

executing a computer-implemented characterisation model for characterising the integrated circuit to generate a characterisation of the integrated circuit based on the step size of the digital-to-time converter.

Modern integrated circuits typically comprise a digital-to-time converter (DTC), e.g. as part of an all-digital phase-locked loop (ADPLL). The Applicant has appreciated that the step-size of the digital-to-time converter can be used to provide a good characterisation of the process parameters applicable to a given IC and thus how far it is from known process corners. As the step-size of the DTC is often determined as part of the normal operation of the ADPLL, the requirement for additional, dedicated circuitry to be provided on the integrated circuit in order to characterise the IC can be avoided. This can reduce cost or improve the

performance of the integrated circuit. It will also be appreciated that this can obviate the need for complex PCM.

Furthermore, as the step-size of the DTC can be obtained in-situ on the integrated circuit, the characterisation could, in theory, be performed after deployment of the integrated circuit and throughout the lifetime of the integrated circuit. This may allow the integrated circuit to be trimmed later in its lifetime to compensate for deteriorations in performance resulting from transistors degrading over time, thereby helping to extend the lifetime of the integrated circuit.

The Applicant has further appreciated that the step-size of the DTC may be particularly useful for providing an indication of the performance of NMOS transistors in an integrated circuit in isolation from the performance of PMOS transistors. As NMOS transistors often have higher performance than PMOS transistors, being able to isolate the characterisation of the performance of the NMOS transistors enables a better indication of the integrated circuit's capabilities.

In some embodiments, the characterisation of the integrated circuit comprises a classification indicating whether the integrated circuit meets a specification. The classification may be a binary value, e.g. PASS or FAIL, KEEP or DISCARD, etc. The classification may be one of a plurality of possible categories, e.g. LOW QUALITY, ACCEPTABLE QUALITY, or HIGH QUALITY. The classification may be a score, e.g. a numeric value on a scale, indicating the extent to which the integrate circuit conforms to the specification.

In some embodiments, the characterisation comprises an estimated or calculated parameter, e.g. a noise factor, a linearity, a phase noise, a gain (e.g. a reception or a transmission gain), an efficiency, and/or a maximum power output, of the integrated circuit.

The specification may be a set of criteria that the integrated is expected to meet. The specification may comprise a set of acceptable ranges for one or more parameters of the integrated circuit. The specification may comprise an acceptable range for the step size of the digital-to-time converter.

The integrated circuit may comprise an adjustable component, wherein a parameter of the adjustable component is selectively adjustable. The adjustable component may comprise a variable resistor, a current source, a voltage regulator (e.g. a low dropout (LDO) regulator), or a variable capacitor. The integrated circuit may comprise a plurality of adjustable components. The parameter may comprise a resistance, a current, a voltage, or a capacitance.

In some embodiments, the characterisation of the integrated circuit comprises a trimming instruction for adjusting a parameter of an adjustable component of the integrated circuit. The trimming instruction may be a signal, e.g. a binary signal, generated by the characterisation model and output by the processor. In some embodiments, the parameter of the adjustable component is adjusted according to the trimming instruction. The integrated circuit may comprise programmable trimming circuitry for adjusting the parameter of the adjustable component based on the trimming instruction. It will be appreciated that this may allow the performance and/or the efficiency of the integrated circuit to be optimised.

For example, an IC that is characterised as operating at a low performance level may be optimised by increasing voltage or a current so that the IC can meet an imposed specification. Conversely, an IC that is characterised as operating at a high performance level may be optimised in terms of efficiency by reducing a voltage or current in order to save power.

The trimming instruction may be an instruction to adjust a plurality of parameters of the adjustable component. The trimming instruction may be an instruction to adjust one or more parameters of a plurality of adjustable components.

In some embodiments, the integrated circuit comprises a temperature sensor for measuring a temperature of the integrated circuit. The temperature sensor may store a temperature reading in the first memory. The processor may receive the temperature reading such that it is used by the characterisation model.

In some embodiments the processor receives a voltage reading from the integrated circuit. The integrated circuit may store the voltage reading in the first memory.

The DTC may be configured to delay the reference clock signal by at least one clock period of the output clock signal. The DTC may be configured to generate the delay length based on the value of a digital control word received by the DTC. In some embodiments, the shortest non-zero delay length that the DTC is configured to generate is equal to the change in the delay length when the least significant bit (LSB) of the digital control word is incremented by one.

In some embodiments, the step-size of the DTC is proportional to a change in the delay length when the current flowing through the DTC increases from a first current value to a second current value. The change in current from the first current value to the second current value may correspond to an increment of one in the LSB of the digital control word.

The Applicant has identified that the step size of the DTC provides an effective indication of at least the process variations of the integrated circuit. Thus, by using the step size of the DTC as an input to the characterisation model in combination with a voltage reading and/or a temperature reading, it may be possible to obtain a complete process, voltage, and temperature (PVT) variation characterisation of the integrated circuit which may further inform any decision regarding trimming etc. It may also obviate the need for careful control of voltage and/or temperature during testing, or make in-field adjustment more viable.

In some embodiments, the characterisation model comprises a regression model. The regression model may be based on statistical data relating to variations in the step size of a digital-to-time converter under different PVT conditions. The statistical data may be empirically obtained, e.g. through process control monitoring (PCM).

In some embodiments, the characterisation model comprises a machine learning model. The machine learning model may be trained based on statistical data relating to variations in the step size of a digital-to-time converter under different PVT conditions. The statistical data may be empirically obtained, e.g. through PCM. The machine learning model may be trained to output the characterisation based on the step size indication received as an input.

The integrated circuit may comprise a radio transceiver. The radio transceiver may be configured to read data stored in the first memory and transmit the data as a radio signal. The integrated circuit may comprise a radio frequency integrated circuit, e.g. a WiFi, Bluetooth or cellular telecommunications transceiver.

The all-digital phase-locked loop (ADPLL) will typically comprise an oscillator for generating an output clock signal. The ADPLL typically further comprises a time comparison portion configured to receive the output clock signal or information relating to the output clock signal and compare the output clock signal with the reference clock signal to determine a time difference between the reference clock signal and the output clock signal. The information relating to the output clock signal may be provided to the time comparison portion as part of a feedback loop, such that the oscillator is configured to adjust the frequency and phase of the output clock based on the time difference determined by the time comparison portion.

The ADPLL comprises a component, e.g. the time-to-digital converter (TDC) or a phase-to-digital converter (PDC), for detecting the phase difference between the reference clock signal and the output clock signal, e.g. based on information received via the feedback loop. The time comparison portion may comprise the component for detecting the phase difference between the reference clock signal and the output clock signal (e.g. the TDC or PDC). The ADPLL typically comprises a component, e.g. a loop filter, configured to generate a control signal for controlling the frequency of the oscillator based on the detected phase difference.

In some embodiments, the digital-to-time converter comprises a plurality of inverters connected in series. Each inverter of the plurality of inverters may be configured to introduce a respective delay to the reference clock signal. The respective delay introduced by each of the plurality of inverters may be configurable, so as to adjust the total delay generated by the digital-to-time converter.

In some embodiments, the delay generated by an inverter is configurable by changing the capacitive loading of the inverter.

In some embodiments, at least a first inverter of the plurality of inverters comprises a transistor having a path to ground. The path to ground may be defined between ground and a drain terminal or a source terminal of the first transistor. The first transistor may comprise an N-Channel Metal-Oxide-Semiconductor (NMOS) or a P-Channel Metal-Oxide-Semiconductor (PMOS).

In some embodiments, the digital-to-time converter comprises one or more control transistors arranged in the path to ground of the first transistor. Each of the one or more control transistors may be configured to be independently enabled or disabled depending on the value of a control signal received at the gate terminal of the respective control transistor. This may allow the impedance to ground to be varied, thereby varying the current starving of the inverter and thus the delay implemented by the inverter. It will be appreciated that, in some embodiments, the impedance to ground may be varied by providing a plurality of capacitors and/or resistors.

Where a plurality of control transistors is provided, they may be arranged in parallel. This allows the current starving of the inverter, and thus the delay generated by the inverter, to be finely adjusted. One or more (e.g. all) of the other inverters of the plurality of inverters may have substantially the same structure as the first transistor (e.g. comprising a respective transistor with a path to ground in which one or more control transistors are arranged).

The circuitry configured to generate the indication of the step size of the digital-to-time converter may be configured to receive a fractional phase error (e.g. from the TDC or PDC of the ADPLL) and a reference phase, derived from the reference clock signal. The circuitry may be configured to generate the indication of the step size iteratively.

In some embodiments, the integrated circuit comprises the processor and the second memory. The first memory and the second memory may be the same memory, or may be different. In such embodiments the integrated circuit may comprise an output for outputting an indication of the characterisation of the integrated circuit – e.g. to a remote testing apparatus.

The integrated circuit may comprise a memory portion, wherein the first memory and the second memory comprise respective partitions of the memory portion. The processor may control the operation of the programmable trimming circuitry by sending the trimming instruction to the programmable trimming circuitry.

In some embodiments, the system further comprises a remote computing device that is separate from the integrated circuit. This could be, for example, part of a larger test apparatus. The remote computing device may comprise the processor and the second memory. The integrated circuit may comprise a transmitter for communicating with a receiver of the remote computing device, e.g. via radio signals. The integrated circuit may send the indication of the step size of the digital-to-time converter to the remote computing device via the transmitter and receiver. The integrated circuit and/or the remote computing device may comprise a transceiver. This enables two-way communication between the integrated circuit and the remote computing device, such that a trimming instruction can be sent to the integrated circuit.

In some embodiments, the integrated circuit and/or the remote computing device comprises an output for outputting an indication of the characterisation of the integrated circuit. The output may comprise a user interface, e.g. comprising a display (e.g. an electronic display or a speaker). The output may comprise a radio transmitter. This allows the characterisation to be interpreted by a human operator or a further computing device.

The integrated circuit described herein is considered to be novel and inventive in its own right. In particular, the Applicant has appreciated that the provision of a memory that is configured to receive the indication of the step size of the digital-to-time converter enables the step size to be used to characterise the integrated circuit, even when the processing is performed off-chip. Thus, when viewed from a further aspect the invention provides an integrated circuit comprising:

an all-digital phase-locked loop configured to receive a reference clock signal and to generate an output clock signal having the same phase as the reference clock signal, wherein the all-digital phase-locked loop comprises:

a digital-to-time converter configured to delay the reference clock signal by a delay length; and

circuitry configured to generate an indication of the step size of the digital-to-time converter, wherein the step-size of the digital-to-time converter is proportional to the shortest non-zero delay length that the digital-time converter is configured to generate; and

a first memory configured to store the indication of the step size of the digital-to-time converter.

It will be appreciated that any aspect or embodiment described herein may, wherever appropriate, comprise one or more features of any other aspect or embodiment described herein. For example, the integrated circuit of the second aspect may comprise the processor and the second memory as described above.

Brief Description of Drawings

A preferred embodiment of the present invention will now be described, by way of example only, with reference to the following drawings in which:

Figure 1 shows schematically a system for characterising an integrated circuit in accordance with an embodiment of the present invention;

Figure 2 is a more detailed schematic view of the digital-to-time converter of the integrated circuit shown in Figure 1;

Figure 3 shows a graph of the outputs of the DTC when the control word is changed, resulting in a change in current through an inverter of the DTC; and

Figure 4 shows the steps of a method of characterising the integrated circuit of Figure 1, in accordance with an embodiment of the present invention.

Detailed Description

Figure 1 shows a system 102 for characterising an integrated circuit, in accordance with an embodiment of the present invention. The system 102 comprises a radio frequency integrated circuit (RFIC) 104 that comprises an all-digital phase-locked loop (ADPLL) 106, a memory 108 and a radio transceiver 110. The RFIC 104 also comprises programmable trimming circuitry 105 which can adjust one or more parameters (e.g. output voltage, output current, capacitance, resistance etc.) of one or more adjustable components 107 of the RFIC 104. The RFIC 104 also comprises a temperature sensor 109 that is configured to measure a temperature of the RFIC

104 and to output the measurement to the first transceiver 110 and/or the memory 108 of the RFIC 104.

In this exemplary embodiment the one or more adjustable components 107 comprise a variable resistor 107a, but the RFIC 104 may comprise other adjustable components 107, such as voltage regulators, variable capacitors, and current sources. The programmable trimming circuitry 105 adjusts parameters of the components 107 depending on a trimming instruction received by the programmable trimming circuitry 105, as will be described below, in order to improve the performance and/or efficiency of the RFIC 104. Additional circuitry of the RFIC 104 is omitted for clarity.

The system 102 further comprises a remote computing device 112 with a second radio transceiver 114 that communicates with the transceiver 110 of the RFIC 104, a memory 116 and a processor 118.

The ADPLL 106 of the RFIC 104 comprises a digital-to-time converter (DTC) 120, a time-to-digital converter (TDC) 122, a loop filter 124, a digitally controlled oscillator (DCO) 126, and a feedback loop 129.

Operation of the system 102 will now be described with reference to Figures 1 to 4, wherein Figure 4 illustrates the individual steps of a method in accordance with an embodiment of the invention.

In use, the ADPLL 106 receives a reference clock signal CLK_{ref} (the source of which is omitted for clarity) and generates an output clock signal CLK_{out} that matches the phase of the reference clock signal CLK_{ref}. The reference clock signal CLK_{ref} is received by the DTC 120 of the ADPLL 106. Timing information relating to the output clock signal CLK_{out} (e.g. a subsampled clock edge of the output clock signal CLK_{out}) is provided to the TDC 122 via the feedback loop 129, and is used by the TDC 122 to determine a time difference between the reference clock signal CLK_{ref} and the output clock signal CLK_{out}.

The ADPLL 106 further comprises K_{DTC} calculation circuitry 130 that, in a first step S100 of the method shown in Figure 4, generates an indication of the step size K_{DTC} of the DTC 120 based on a phase error signal and fractional phase information received from the TDC 122. The step size K_{DTC} of the DTC 120 will be described in more detail below, with reference to Figure 3.

The DTC 120 makes small adjustments to the phase of the reference clock signal CLK_{ref} based on a digital control word, which is calculated based on the phase difference between the reference clock signal CLK_{ref} and information relating to the output clock signal (received via the feedback loop 129), as well as the indication of the step size K_{DTC} of the DTC 120.

The output of the DTC 120 is provided to the TDC 122, which detects the phase difference between the reference clock signal CLK_{ref} and the output clock signal (based on the information received via the feedback loop 129). The loop filter 124 uses the detected phase difference to generate a control signal for controlling the frequency of the DCO 126, and the DCO 126 generates the output clock signal CLK_{out} based on the control signal from the loop filter 124.

As well as being output to the DTC 120, the indication of the step size K_{DTC} of the DTC 120 is also stored in the memory 108, before being sent by the radio transceiver 110 to the remote computing device 112.

In a second step S102 of the method shown in Figure 4, the indication of the K_{DTC} is provided to the processor 118 of the remote computing device 112.

The processor 118 also receives a temperature and a voltage reading from the RFIC 104 via the first transceiver 110 and the receiver 114.

In a third step S104 of the method shown in Figure 4, the processor 118 of the remote computing device 116 executes software stored in the memory 116 of the remote computing device 112 in order to run a model for generating a characterisation of the RFIC 104. The processor 118 provides the indication of the K_{DTC}, as well as the received temperature and voltage readings, as inputs to the

characterisation model. The model generates a characterisation of RFIC 104 that is based on the K_{DTC} indication and the voltage and temperature readings.

Together with a supply voltage value, the step size can be used to provide an estimate of, for example, the RF performance of an IC. As this estimate can be generated based on variables obtained through relatively simple DC measurements, the test time (and hence the associated costs) can be reduced.

A higher step size indicates a “slower” transistor speed for the IC. In the event that the performance of the IC does not meet the specification, appropriate currents can be increased or bias levels changed to compensate for the “slower” transistor speed and thereby meet (or move closer to) the specification.

Conversely, a lower step size may indicate that currents can be reduced in order to reduce power consumption of the IC.

It will be appreciated that the characterisation model can be based upon relationships such as these between the step size and characteristics of the IC.

In the exemplary embodiment described herein, the characterisation model is a machine learning algorithm trained on empirical data obtained from one or more DTCs of other chips under approximately one thousand different PVT conditions, together with corresponding step size K_{DTC} values.

Each of the PVT conditions is associated with one or more corresponding trimming instructions for improving the performance of the RFIC. For example, a PVT condition in which the RF performance is slow may be associated with a trimming instruction to increase the current by a certain amount, in order to improve the RF performance of the RFIC.

PVT variations can affect the performance of transistors within the IC, particularly parameters such as threshold voltages and current flow. For example, a high operating temperature may reduce threshold voltages or increase the leakage current in transistors of the IC. Variations in these parameters can result in changes to the characteristics of the IC such as propagation delay and power consumption.

The model is trained to output an indication of a variable of the RFIC 104 to adjust in order to improve the performance and/or the efficiency of the RFIC 104. The indication is in the form of an instruction for interpretation by the programmable trimming circuitry 105 on the RFIC 104 to adjust suitable parameters of the adjustable components 107. For example, the model might output an instruction to adjust:

- a resistance value of a variable resistor (e.g. to adjust the gain of an operational amplifier to control its accuracy and stability);
- a reference voltage provided to a component (e.g. an analog-to-digital converter (ADC), so as to improve its accuracy);
- a capacitance value of a capacitor (e.g. to tune the oscillation frequency of an oscillator); or
- a current provided to a component (e.g. in a bandgap reference circuit, to improve the accuracy and stability of the reference voltage).

For example, the resistance of a feedback resistor in an operational amplifier of the RFIC 104 may be adjusted to control the gain of the amplifier so as to control its accuracy and stability,

In another exemplary embodiment, the characterisation model involves a look-up table comprising the empirical data obtained from the DTCs, as well as the corresponding step size for each PVT condition of the dataset. The look-up table also includes one or more trimming instructions associated with each PVT condition, indicating one or more changes to a parameter of the RFIC that should be adjusted in order to improve the performance and/or the efficiency of the RFIC.

In such embodiments, the characterisation model uses the indication of the K_{DTC} to search the look-up table and identify a set of candidate PVT conditions. The set is further filtered using the temperature and voltage measurements obtained from the RFIC in order to identify a suitable trimming instruction that should be performed. .

Returning to the exemplary embodiment illustrated herein, in the event that the RFIC104 is characterised as too poor to be compensated by trimming, the model

instead provides an indication that the RFIC 104 should simply be discarded. In other, simpler embodiments, a similar model could instead be trained just to output a rating indicating how well the RFIC 104 meets a specification, e.g. POOR or GOOD. This rating can be used to decide whether to keep the RFIC 104, e.g. so as to deploy it in a product, or to discard it. It could also be used to characterise the RFIC 104 as high, average or low performance which might be useful in allowing a greater effective yield by taking account of applications where performance is less critical.

The characterisation is used to generate a trimming instruction indicating an adjustment that should be made by the programmable trimming circuitry 105. As discussed above, the trimming instructions are associated with particular PVT conditions within the empirical DTC data used by the characterisation model. The model uses the indication of the K_{DTC} and the voltage and temperature readings obtained from the RFIC 104 to identify the corresponding trimming instruction.

In the exemplary embodiment described herein, the trimming instruction indicates an adjustment that should be made to the resistance of a variable resistor 107a on the RFIC 104 in order to improve the performance of the RFIC 104.

In a fourth step S106 of the method shown in Figure 4, the trimming instruction is sent by the processor 118 of the remote computing device 112 to the programmable trimming circuitry 105 of the RFIC 104 via the respective transceivers 114, 110 of the remote computing device 112 and the RFIC 104. The programmable trimming circuitry 105 interprets the trimming instruction and accordingly adjusts the resistance of the variable resistor 107a of the RFIC 104.

Figure 2 is a more detailed schematic view of the DTC 120 of the RFIC 104 of Figure 1.

The DTC 120 comprises a chain of sixty-four inverters 132, arranged in series.

The structure of the first inverter 132a of the chain is shown in more detail in Figure 2, although each inverter 132 of the chain has substantially the same structure as the first inverter 132a.

The inverter 132a comprises a first transistor pair 138, comprising a first N-Channel Metal-Oxide-Semiconductor (NMOS) transistor 140 and a first P-Channel Metal-Oxide-Semiconductor (PMOS) transistor 142 arranged in series with their gate terminals connected together and their drain terminals connected together.

The connected drain terminals are connected to the gate terminals of a second transistor pair 144, comprising a second NMOS transistor 146 and a second PMOS transistor 148 connected in parallel, again with their gate terminals connected together and their drain terminals connected together. The source terminals of the first and second PMOS transistors 142, 148 are also connected together.

The inverter 132a further comprises two control transistors 150, 152, arranged in parallel between the source terminal of the first NMOS transistor 140 and ground. The control transistors 150, 152 are switched on or off depending on the value of respective control signals CTRL0, CTRL1 received at the respective gate inputs of the control transistors 150, 152. In other embodiments, a single control transistor or more than two could be used.

When both the first and second control transistors 150, 152 are switched off, the impedance between the source terminal of the first NMOS transistor 140 and ground is relatively high, meaning that a relatively small amount of current flows through the inverter 132a. Conversely, when both the control transistors 150, 152 are switched on, the impedance to ground is relatively low, meaning that a relatively large amount of current flows through the inverter 132a.

When a high current is flowing through the inverter 132a (when the control transistors 150, 152 are both switched on), the delay time is relatively short. Conversely, when a low current is flowing through the inverter 132a (when the control transistors 150, 152 are both switched off), the delay time is relatively long.

Thus, depending on the values of the control signals CTRL0, CTRL1, the delay of the DTC 120 can be adjusted. The values of the control signals CTRL0, CTRL1 are set according by a digital control word from another part of the circuit (not shown).

Figure 3 shows a graph of the delay generated by the DTC 120 over time as the current through the inverter 132a is increased from a first current level 134 to a second current level 136 by incrementing the least significant bit (LSB) of the digital control word by one, and thereby adjusting the control signals CTRL0, CTRL1.

When the current is at the first level 134, the DTC 120 provides a first delay length T_1, and when the current is at the second level 136, the DTC 120 provides a second delay length T_2. The second delay length T_2 is shorter than the first delay length T_1 as the second current level 136 is higher than the first current level 134.

The difference ΔT between the first delay length T_1 and the second delay length T_2 is the same as the smallest delay length that the DTC 120 is configured to generate (as it corresponds to one increment of the LSB in the digital control word), and is thus proportional to the step size K_{DTC} of the DTC 120.

Claims

1. A system for characterising an integrated circuit, the system comprising:

a) an integrated circuit comprising:

i) an all-digital phase-locked loop configured to receive a reference clock signal and to generate an output clock signal having the same phase as the reference clock signal, wherein the all-digital phase-locked loop comprises:

a digital-to-time converter configured to delay the reference clock signal by a delay length; and

circuitry configured to generate an indication of a step size of the digital-to-time converter, wherein the step-size of the digital-to-time converter is proportional to the shortest non-zero delay length that the digital-time converter is configured to generate; and

ii) a first memory configured to store the indication of the step size of the digital-to-time converter;

b) a processor; and

c) a second memory storing instructions which, when executed by the processor, cause the processor to run a characterisation model for characterising the integrated circuit,

wherein the processor is configured to receive the indication of the step size of the digital-to-time converter from the first memory and run the characterisation model to generate a characterisation of the integrated circuit based on the step-size of the digital-to-time converter.

2. The system of claim 1, wherein the characterisation of the integrated circuit comprises:

an indication of whether the integrated circuit meets a specification; and/or

a trimming instruction for adjusting a parameter of an adjustable component of the integrated circuit.

3. The system of claim 2, wherein the integrated circuit further comprises programmable trimming circuitry for adjusting the parameter of the adjustable component of the integrated circuit based on the trimming instruction, and wherein the processor is configured to output the trimming instruction to the programmable trimming circuitry.

4. The system of claim 3, wherein the adjustable component comprises a variable resistor, a current source, a voltage regulator, or a variable capacitor.

5. The system of any of claims 2 to 4, wherein the parameter comprises a resistance, a current, a voltage, or a capacitance.

6. The system of any preceding claim, wherein the integrated circuit further comprises a temperature sensor for measuring a temperature of the integrated circuit, and wherein the processor is configured to receive the measured temperature and input the measured temperature to the characterisation model.

7. The system of any preceding claim, wherein the processor is configured to receive a voltage reading from the integrated circuit and input the voltage reading to the characterisation model.

8. The system of any preceding claim, wherein the characterisation model comprises a regression model.

9. The system of any preceding claim, wherein the characterisation model comprises a machine learning model.

10. The system of any preceding claim, wherein the digital-to-time converter comprises:

a plurality of inverters connected in series, wherein at least a first inverter of the plurality of inverters comprises a transistor having a path to ground; and

a plurality of control transistors arranged in parallel along the path to ground of the transistor, wherein each of the plurality of control transistors is configured to be independently enabled or disabled depending on the value of a control signal received at the gate terminal of the respective control transistor.

11. The system of any preceding claim, further comprising a remote computing device, wherein the remote computing device comprises the processor and the second memory.

12. The system of any of claims 1 to 10, wherein the integrated circuit comprises the processor and the second memory.

13. A method of characterising an integrated circuit, the integrated circuit comprising:

i) an all-digital phase-locked loop configured to receive a reference clock signal and to generate an output clock signal having the same phase as the reference clock signal, wherein the all-digital phase-locked loop comprises:

a digital-to-time converter configured to delay the reference clock signal by a delay length; and

circuitry configured to generate an indication of the step size of the digital-to-time converter, wherein the step-size of the digital-to-time converter is proportional to the shortest non-zero delay length that the digital-time converter is configured to generate; and

ii) a first memory configured to store the indication of the step size of the digital-to-time converter;

the method comprising:

the circuitry of the all-digital phase-locked loop generating an indication of the step size of the digital-to-time converter and storing the indication in the first memory; and

executing a computer-implemented characterisation model for characterising the integrated circuit to generate a characterisation of the integrated circuit based on the step size of the digital-to-time converter.

14. The method of claim 13, wherein the characterisation comprises a trimming instruction for adjusting a parameter of an adjustable component of the integrated circuit, and wherein the method comprises adjusting the parameter of the adjustable component according to the trimming instruction.

15. An integrated circuit comprising:

an all-digital phase-locked loop configured to receive a reference clock signal and to generate an output clock signal having the same phase as the reference clock signal, wherein the all-digital phase-locked loop comprises:

a digital-to-time converter configured to delay the reference clock signal by a delay length; and

circuitry configured to generate an indication of the step size of the digital-to-time converter, wherein the step-size of the digital-to-time converter is proportional to the shortest non-zero delay length that the digital-time converter is configured to generate; and

a first memory configured to store the indication of the step size of the digital-to-time converter.

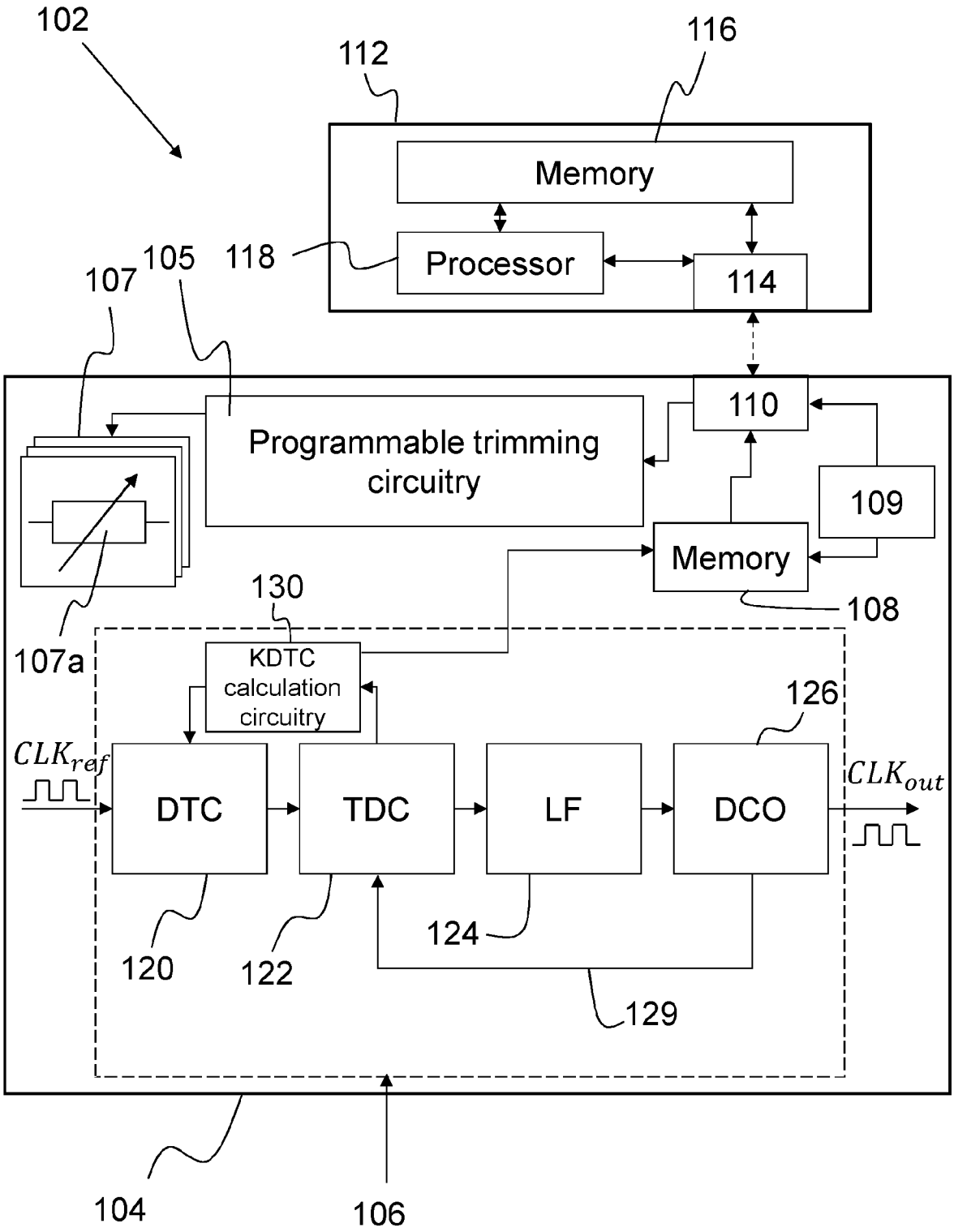

102
112
116
Memory
Processor
114
118
105
107
110
Programmable trimming circuitry
109
Memory
108
130
107a
KDTC calculation circuitry
126
CLK_{ref}
DTC
TDC
LF
DCO
CLK_{out}
120
122
124
129
104
106

FIG. 1

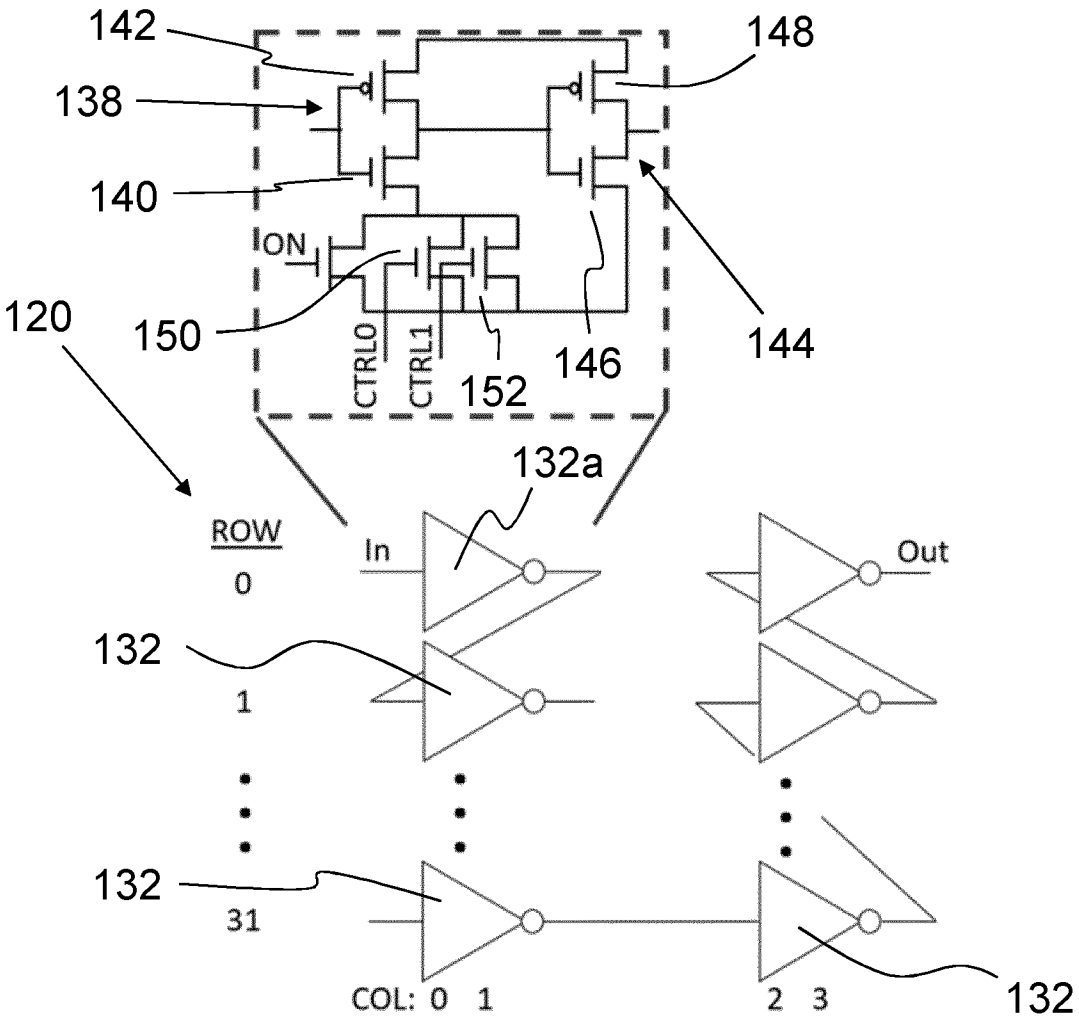

142
148
138
140
ON
120
150
CTRL0
CTRL1
152
146
144
132a
ROW
0
In
Out
132
1
132
31
COL: 0 1
2 3
132

FIG. 2

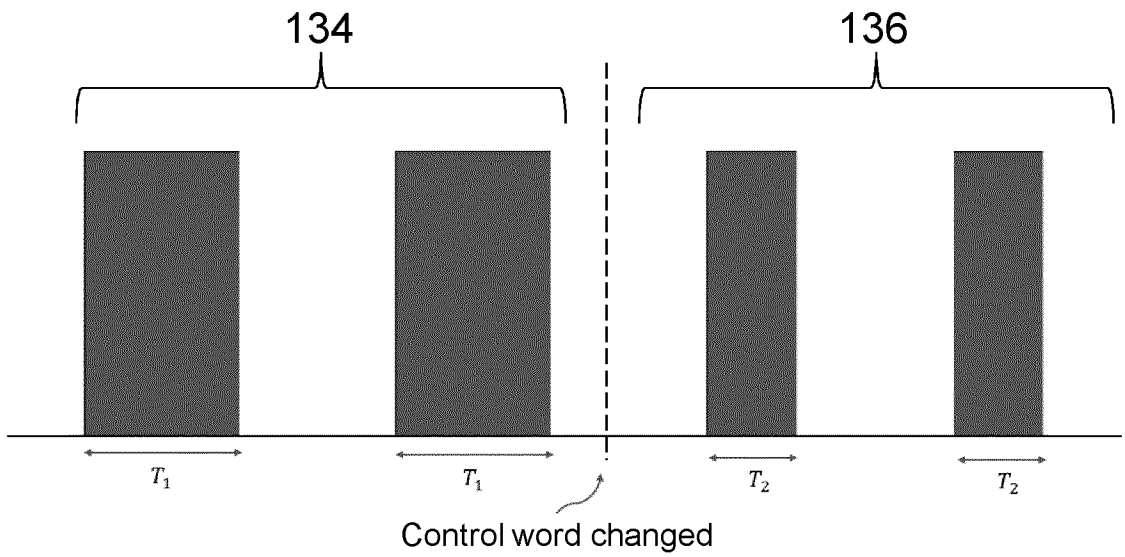

134
136
T_1
T_1
T_2
T_2
Control word changed

FIG. 3

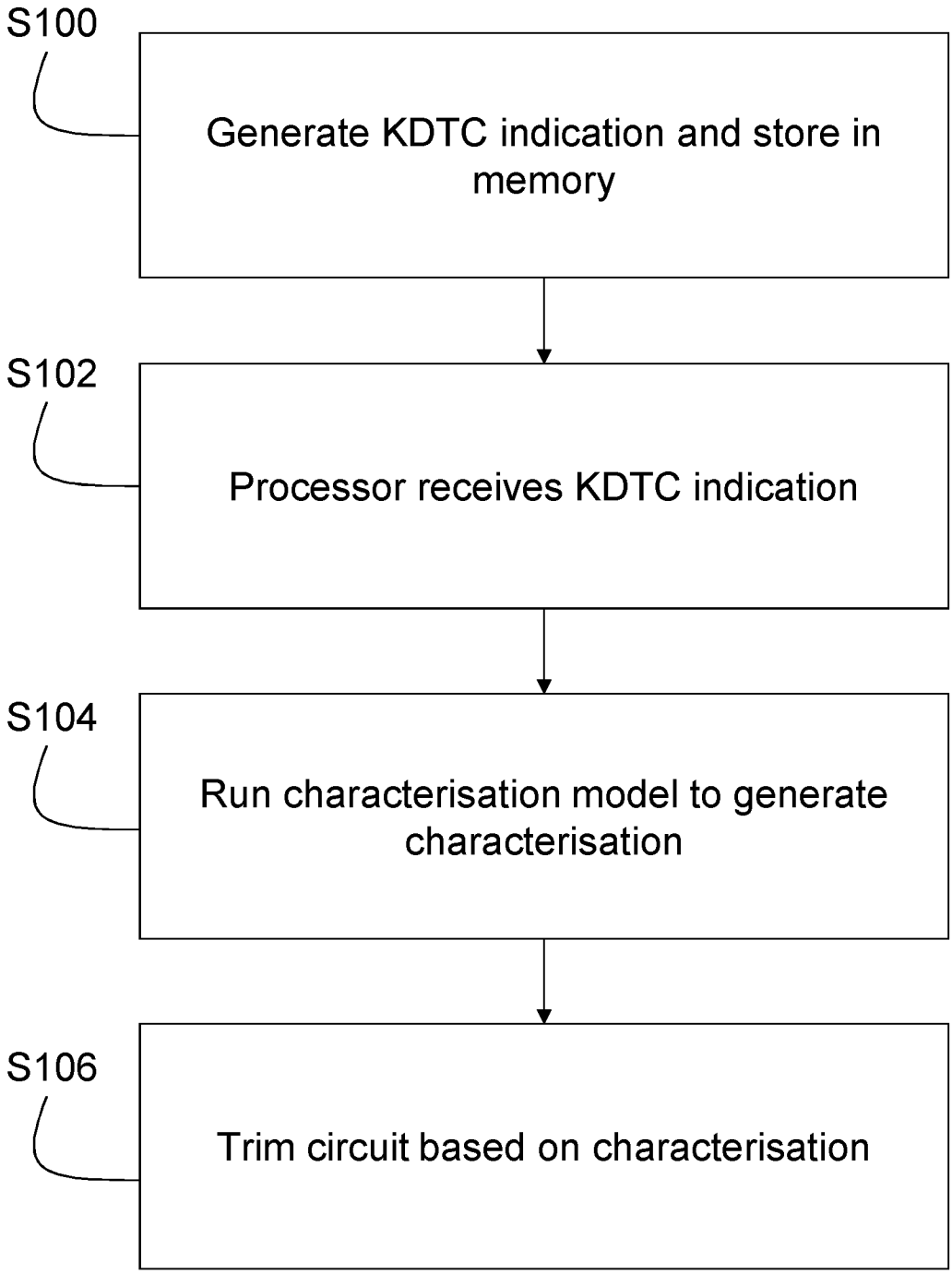

S100
Generate KDTC indication and store in memory
S102
Processor receives KDTC indication
S104
Run characterisation model to generate characterisation
S106
Trim circuit based on characterisation

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/088162

A. CLASSIFICATION OF SUBJECT MATTER

INV. G01R31/28 G01R31/317 G06F1/08 G06F30/367 G04F10/00
H03L7/08 H03L7/06 G11C29/02 H03M1/10 H03M1/00
H04B17/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R G06F G04G H03L G04F H03M G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/056827 A1 (VLACHOGIANNAKIS GERASIMOS S [NL] ET AL) 25 February 2016 (2016-02-25)	15
A	figures 1, 18 paragraph [0007] - paragraph [0013] paragraph [0035] - paragraph [0039] paragraph [0049] - paragraph [0050] paragraph [0064] - paragraph [0067] paragraph [0088] paragraph [0117] - paragraph [0120] claims 1-12	1-14

A	CN 107 046 421 A (MARVELL WORLD TRADE LTD) 15 August 2017 (2017-08-15) figures 1, 9 paragraph [0005] paragraph [0036] - paragraph [0039] paragraphs [0094], [0113]	1-15

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[x] Further documents are listed in the continuation of Box C.

[x] See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 April 2025	02/05/2025

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kleiber, Michael

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/088162

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015/280842 A1 (MAYER THOMAS [AT] ET AL) 1 October 2015 (2015-10-01) figures 1-5 paragraph [0030] - paragraph [0055]	1-15

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2024/088162

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		US 2016056799 A1	25-02-2016
		US 2016056825 A1	25-02-2016
		US 2016056827 A1	25-02-2016
		WO 2016029000 A2	25-02-2016
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		DE 102014104478 A1	01-10-2015
		TW 201603497 A	16-01-2016
		US 2015280842 A1	01-10-2015