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(54) **Title:** LINEARIZATION CIRCUIT FOR HIGH FREQUENCY SIGNAL PHASE ADJUSTMENT

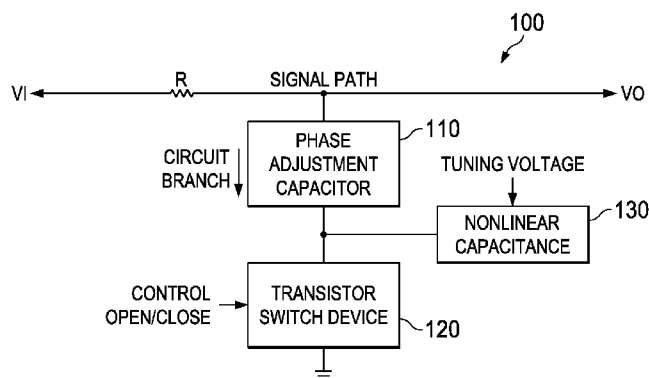


FIG. 1

(57) **Abstract:** A circuit includes a phase adjustment capacitor (PAC) (110) coupled to a signal path and configured to adjust a phase of a signal on the signal path. A transistor switch device (120) is coupled in series with the PAC (110) to provide a circuit branch parallel with the signal path. The transistor switch device (120) is configured to selectively open or close the circuit branch of the signal path to enable or disable, respectively, the adjustment of the phase of the signal on the signal path via the PAC (110). A nonlinear capacitance (130) is coupled to a node interconnecting the PAC (110) and the transistor switch device (120). The nonlinear capacitance (130) is configured to vary inversely proportional with a capacitance of the transistor switch device (120) with respect to the signal on the signal path and to linearize a total capacitance provided by the circuit branch when the circuit branch is open.

LINEARIZATION CIRCUIT FOR HIGH FREQUENCY SIGNAL PHASE ADJUSTMENT

[0001] This relates generally to analog signal processing, and more particularly to a linearization circuit that compensates for nonlinearity of a phase adjustment circuit.

BACKGROUND

[0002] In certain analog signal processing applications, capacitors are added to a signal path to adjust the phase of the signal. For example, this may be performed to match the phase of the signal relative to another signal, or it may be performed to tune the filter characteristics. One of the simplest and the most straightforward techniques to control the capacitance to be adjusted is by connecting a metal oxide semiconductor (MOS) switch in series with the capacitor. Thus, circuitry can turn on the switch to add capacitance to a given signal processing circuit, and turn off the switch to not add the capacitance.

[0003] Generally, the switch size is selected large enough for the switch's on-resistance to be small. For example, for a signal frequency that is 100MHz or less, selecting a very large switch has little side effect to the signal linearity. However, when the signal frequency goes into several hundred MHz, using a large switch can have a negative effect on the signal linearity when the switch is turned off.

SUMMARY

[0004] This disclosure relates to a linearization circuit that compensates for nonlinearity in a switched capacitive branch of a phase adjustment circuit.

[0005] In one example, a circuit includes a phase adjustment capacitor (PAC) coupled to a signal path and configured to adjust a phase of a signal on the signal path. A transistor switch device is coupled in series with the PAC to provide a circuit branch parallel with the signal path. The transistor switch device is configured to selectively open or close the circuit branch of the signal path to enable or disable, respectively, the adjustment of the phase of the signal on the signal path via the PAC. A nonlinear capacitance is coupled to a node interconnecting the PAC and the transistor switch device. The nonlinear capacitance is configured to vary inversely proportional with a capacitance of the transistor switch device with respect to the signal on the signal path and to linearize a total capacitance provided by the circuit branch when the circuit

branch is open.

[0006] In another example, a circuit includes a phase adjustment capacitor (PAC) coupled to a signal path and configured to adjust a phase of a signal on the signal path. A transistor switch device is coupled in series with the PAC to provide a circuit branch parallel with the signal path. The transistor switch device is configured to selectively open or close the circuit branch of the signal path to enable or disable, respectively, the adjustment of the signal phase of the signal path via the PAC. A compensation semiconductor device includes at least one junction having a nonlinear capacitance. The compensation semiconductor device is coupled to a node interconnecting the PAC and the transistor switch device. The nonlinear capacitance of the compensation semiconductor device is configured to vary inversely proportional with a capacitance of the transistor switch device with respect to the signal on the signal path and to linearize a total capacitance provided by the circuit branch when the circuit branch is open.

[0007] In yet another example, a circuit includes a phase adjustment capacitor (PAC) coupled to a signal path and configured to adjust a phase of a signal on the signal path. A transistor switch device is coupled in series with the PAC to provide a circuit branch parallel with the signal path. The transistor switch device is configured to selectively open or close the circuit branch of the signal path to enable or disable, respectively, the adjustment of the signal phase of the signal path via the PAC. A compensation transistor device having a source, a drain and a gate is coupled to a node interconnecting the PAC and the transistor switch device. The compensation transistor device is configured to provide a nonlinear capacitance formed between either the source or the drain with respect to a substrate of the compensation transistor device. The nonlinear capacitance varies inversely proportional with a capacitance of the transistor switch device with respect to the signal on the signal path and linearizes a total capacitance provided by the circuit branch when the circuit branch is open. A tuning voltage is applied to the gate of the compensation transistor device to adjust the nonlinear capacitance of the compensation transistor device based on the tuning voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 illustrates an example circuit configured to compensate for nonlinearity in a phase adjustment circuit.

[0009] FIG. 2 illustrates an example phase adjustment circuit having a circuit branch that is opened via a transistor switch device.

[0010] FIG. 3 illustrates an example phase adjustment circuit having nonlinear capacitance compensation when the circuit branch is opened.

[0011] FIG. 4 illustrates an example phase adjustment circuit that employs a compensation diode providing nonlinear capacitance compensation when the circuit branch is opened.

[0012] FIG. 5 illustrates an example phase adjustment circuit that employs a compensation transistor providing nonlinear capacitance compensation when the circuit branch is opened.

[0013] FIG. 6 illustrates an example phase adjustment circuit that employs a compensation transistor having a common connection for source and drain and providing nonlinear capacitance compensation when the circuit branch is opened.

[0014] FIG. 7 illustrates an alternative example phase adjustment circuit that employs a compensation transistor having a common connection for source and drain and providing nonlinear capacitance compensation when the circuit branch is opened.

[0015] FIG. 8 illustrates a differential signal path where phase adjustment circuits having nonlinear capacitance compensation are applied each path of the differential signal path.

[0016] FIG. 9 illustrates a signal path where multiple phase adjustment circuits having nonlinear capacitance compensation are applied across the signal path.

[0017] FIG. 10 illustrates a side-view of a metal oxide semiconductor transistor depicting a length parameter between source and drain wells in a semiconductor substrate.

[0018] FIG. 11 illustrates a top-view of a metal oxide semiconductor transistor depicting a width parameter for the transistor.

[0019] FIG. 12 illustrates a signal diagram depicting the effects of a width parameter of a nonlinear capacitance compensation transistor with respect to mitigation of signal path nonlinearities.

[0020] FIG. 13 illustrates a signal diagram depicting the effects of a tuning voltage of a nonlinear capacitance compensation transistor with respect to mitigation of signal path nonlinearities.

DETAILED DESCRIPTION

[0021] This disclosure relates to a linearization circuit that compensates for nonlinearity in a switched capacitive branch of a phase adjustment circuit. The phase adjustment circuit includes a phase adjustment capacitor (PAC) that is coupled to a signal path and employed to adjust a signal phase of the signal path. The PAC may be selectively coupled to or decoupled from the

signal path depending on whether or not signal phase adjustment is desired for the signal path. A transistor switch device can be coupled in series with the PAC to provide a parallel circuit branch connection with the signal path. The transistor switch device can selectively open or close the circuit branch of the signal path to enable or disable the adjustment of the signal phase of the signal path by enabling or disabling the circuit connection to the PAC. The transistor switch device can be factory-set and/or set (e.g., on or off) in an application environment depending on the signal phase adjustment needs of the respective application.

[0022] A nonlinear capacitance can be coupled to a node interconnecting the PAC and the transistor switch device. The nonlinear capacitance is employed to compensate for nonlinearities that may appear on the signal path as signal path input frequencies increase and when the transistor switch device is disabled. The respective nonlinearities can be caused by a junction capacitance of the transistor switch device when disabled. Thus, as input voltages are varied, the voltage across the transistor switch device when set to off can vary which in turn can cause the junction capacitance to vary. In order to counteract the effects of the off-state junction capacitance of the transistor switch device, the nonlinear capacitance varies its respective capacitance inversely proportional with the capacitance of the transistor switch device when disabled. This linearizes the total capacitance provided by the circuit branch when the circuit branch is opened via the transistor switch device and thus mitigates nonlinearities on the signal path.

[0023] FIG. 1 illustrates an example of circuit 100 that compensates for nonlinearity in a phase adjustment circuit. As used herein, the term circuit can include a collection of active and/or passive elements that perform a circuit function such as a transistor or capacitor. Also, for example, the term circuit can include an integrated circuit where all the circuit elements are fabricated on a common substrate. As shown in FIG. 1, the circuit 100 includes a signal path where input voltage frequencies are applied as voltage input (VI) and output frequencies are supplied as voltage output (VO). A typical signal path component is shown as resistor (R) but other path components (e.g., inductors, capacitors, semiconductors) including parallel and/or serial combinations are possible.

[0024] The circuit 100 includes a phase adjustment capacitor (PAC) 110 that is coupled to the signal path and employed to adjust a signal phase of the signal path. The PAC 110 can be selectively coupled to or decoupled from the signal path depending on whether or not signal

phase adjustment is desired for the signal path. A transistor switch device 120 can be coupled in series with the PAC 110 to provide a parallel circuit branch connection with the signal path. The transistor switch device 120 (such as NMOS or PMOS field effect transistor) can selectively open or close the circuit branch of the signal path to enable or disable the adjustment of the signal phase of the signal path by enabling or disabling the circuit connection to the PAC 110. As shown, a control input (e.g., gate input) can be employed to open or close the transistor switch device 120. The control input for the transistor switch device 120 can be factory-set and/or set (e.g., high or low) in an application environment depending on the signal phase adjustment needs of the respective application.

[0025] A nonlinear capacitance 130 can be coupled to a node interconnecting the PAC 110 and the transistor switch device 120. The nonlinear capacitance 110 can be employed to compensate for nonlinearities (such as second harmonic distortions) that may appear on the signal path as signal path input voltages V_I increase and when the transistor switch device 120 is disabled (e.g., control input set to ground). The respective nonlinearities can be caused by a junction capacitance of the transistor switch device 120 when disabled. As input voltages V_I applied to the signal path are varied, the voltage across the transistor switch device 120 when set to off can also vary, which in turn can cause the junction capacitance to vary. In order to counteract the effects of the off-state junction capacitance of the transistor switch device 120, the nonlinear capacitance 130 varies its respective capacitance inversely proportional with the capacitance of the transistor switch device when the circuit branch is open. This linearizes the total capacitance provided by the circuit branch when the circuit branch is opened via the transistor switch device 120 and thus mitigates nonlinearities on the signal path.

[0026] As will be illustrated and described below with respect to FIGS. 2-9, various configurations for the circuit 100 are possible. In one example, the nonlinear capacitance 130 can be configured as a compensation diode having a junction capacitance that varies inversely to the junction capacitance of the transistor switch device 120. In another example, the nonlinear capacitance 130 can be configured as a compensation diode having a junction capacitance that is formed from a compensation transistor. For example, the source or the drain (or both) of the compensation transistor can form the compensation diode with respect to a substrate of the compensation transistor. A tuning voltage can be applied to the nonlinear capacitance 130 to adjust its capacitance over a range depending on the voltage setting of the tuning voltage. Other

parameters can also be controlled to adjust the nonlinear capacitance as will be described below.

[0027] FIG. 2 illustrates an example phase adjustment circuit 200 having a circuit branch that is opened via a transistor switch device 210. In this example, a resistor R is connected in series with a signal path. A circuit branch is formed via phase adjustment capacitor (PAC). Signal path voltage is coupled through capacitor PAC and supplied to a connecting node of the transistor switch device 210 as a circuit branch voltage. In this example, a gate of the transistor switch device 210 is at ground potential, which disables the transistor switch device and thus opens the circuit branch. By opening the circuit branch, the capacitor PAC cannot affect the phase of the voltage on the signal path. However, when the transistor switch device 210 is disabled, and as voltages are increased along the signal path, signal path nonlinearities can be introduced due to the disabled transistor switch device 210.

[0028] As shown, when disabled, the transistor switch device 210 when disabled can be modeled as a circuit branch diode (DC) that is reversed biased with respect to the signal path. The diode DC in turn is associated with a junction capacitance (between source or drain with respect to substrate) that is a function of the circuit branch voltage. Thus, as signal path voltages increase, the circuit branch voltage can increase which causes a decrease of the junction capacitance of the diode DC which further increases nonlinearities such as second harmonic distortions to appear on the signal path. The circuits depicted in FIGS. 3-7 illustrate examples of how a nonlinear capacitance can be employed to counteract the junction capacitance of the transistor switch device 210 when switched off.

[0029] FIG. 3 illustrates an example phase adjustment circuit 300 having nonlinear capacitance compensation when the circuit branch is opened. In this example, diode DC is shown in the circuit branch to represent the open transistor switch device depicted in FIG. 2. As noted above, as signal path voltages increase, a corresponding increase in circuit branch voltage nonlinearity can occur due to changes in the junction capacitance of diode DC. In order to counteract such effects, a nonlinear capacitance 310 can be coupled to a node interconnecting the PAC and the transistor switch device which in this example is represented as diode DC.

[0030] The nonlinear capacitance 310 can be configured to vary inversely proportional with the transistor switch device represented by diode DC. As such, this nonlinear capacitance operates to linearize a total capacitance provided by the circuit branch when the circuit branch is open. Thus, when the circuit branch voltage increases, the voltage across the nonlinear

capacitance decreases. The decreasing voltage causes the capacitance of the nonlinear capacitance to in turn increase which mitigates capacitance decreases on diode DC which represents the open transistor switch device. In some examples, a DC tuning voltage can be applied to the nonlinear capacitance 310 to adjust the capacitance of the nonlinear capacitance as disclosed herein. The circuits depicted in FIGS. 4-7 illustrate example configurations for the nonlinear capacitance 310.

[0031] FIG. 4 illustrates an example phase adjustment circuit 400 that employs a compensation diode providing nonlinear capacitance compensation when the circuit branch is opened. In this example, a nonlinear capacitance is configured as a compensation diode 410 and is coupled in parallel with a junction diode DC formed between the interconnecting node to the PAC and a substrate of the transistor switch device when the circuit branch is open. A tuning voltage can be applied to the compensation diode 410 to adjust the nonlinear capacitance of the compensation diode. In this example, if the circuit branch voltage increases with a corresponding decrease in junction capacitance of diode DC, the voltage across the compensation diode 410 increases since it is referenced to the tuning voltage.

[0032] FIGS. 5-7 illustrate alternative nonlinear capacitance configurations where the compensation diode 410 is configured from a compensation transistor.

[0033] FIG. 5 illustrates an example phase adjustment circuit 500 that employs a compensation transistor device 510 providing nonlinear capacitance compensation when the circuit branch is opened via transistor switch device 520. The compensation diode described above with respect to FIG. 4 can be configured from the compensation transistor device 510 having a source, a drain, and a gate. The compensation diode can be formed between either the source or the drain with respect to a substrate of the compensation transistor device 510. In the example depicted in FIG. 5, the compensation diode is formed between the source and the substrate of the compensation transistor device 510 while the drain is tied to the substrate. A tuning voltage can be applied (e.g., by control circuitry – not shown) to adjust the capacitance of the diode formed by the compensation transistor 510. A dotted line represents a substrate connection for the compensation transistor device 510 and, for example, can be coupled to the tuning voltage as shown.

[0034] FIG. 6 illustrates an example phase adjustment circuit 600 that employs a compensation transistor device 610 configured with a common connection for source and drain and providing

nonlinear capacitance compensation when the circuit branch is opened via transistor switch device 620. As shown in the example of FIG. 6, each of the source and the drain of the compensation transistor device 610 are coupled together to form the compensation diode with respect to the substrate of the compensation transistor device. Coupling the source and drain together in this manner increases (such as doubles) the nonlinear capacitance of the compensation diode configured from the compensation transistor device 610. A tuning voltage can be applied (e.g., by control circuitry – not shown) to the gate of compensation transistor device 610 to adjust the nonlinear capacitance of the compensation diode configured from the compensation transistor device. For example, the tuning voltage applied to the gate can be in a range of approximately 1.5 volts to approximately 2.0 volts to adjust the nonlinear capacitance of the compensation diode configured from the compensation transistor device 610. A dotted line represents a substrate connection for the compensation transistor device 610 and, for example, can be coupled to the tuning voltage.

[0035] FIG. 7 illustrates an alternative example phase adjustment circuit 700 that employs a compensation transistor device 710 having a common connection for source and drain and providing nonlinear capacitance compensation when the circuit branch is opened via transistor switch device 720. In this example, the transistor switch device 720 and the compensation transistor device 710 are configured as complimentary devices from the examples shown in FIGS. 5 and 6. With respect to the examples of FIGS. 5 and 6, if the transistor switch device is configured as an NMOS device, then the compensation transistor device is configured as a PMOS device. With respect to the example of FIG. 7, if the transistor switch device 720 is configured as a PMOS device, then the compensation transistor device 710 is configured as an NMOS device. A dotted line represents a substrate connection for the compensation transistor device 710 and, for example, can be coupled to the tuning voltage. As shown, when a PMOS device is employed as the transistor switch device 720, the source of the transistor switch device is coupled to a positive supply voltage, such as VDD.

[0036] FIG. 8 illustrates a differential signal path circuit 800 where phase adjustment circuits having nonlinear capacitance compensation are applied each path of the differential signal path. In this example, a first PAC, transistor switch device, and nonlinear capacitance form a first phase adjuster 810 in a first differential signal path. A second PAC, a second transistor device, and a second nonlinear capacitance form a second phase adjuster 820 in a second differential

signal path to enable differential phase adjustment of a differential signal applied to the first and second differential signal paths.

[0037] FIG. 9 illustrates a signal path 900 where multiple phase adjustment circuits having nonlinear capacitance compensation are applied across the signal path. In this example, a first PAC, transistor switch device, and nonlinear capacitance form a first phase adjuster 910 for the signal path. A second PAC, a second transistor device, and a second nonlinear capacitance form a second phase adjuster 920. An Nth phase adjuster 930 can also be utilized in the signal path to enable multiple phase adjustments along the signal path, wherein N is a positive integer.

[0038] FIG. 10 illustrates a side-view of a metal oxide semiconductor transistor 1000 depicting a length parameter (L) between source and drain wells in a semiconductor substrate 1010. A gate 1020 separated by an oxide layer 1030 controls the channel formed between the source and drain. In one particular example for the parameter L, the length L for both transistor switch device and the compensation transistor switch device can be approximately 0.13 micrometers, however other dimensions are possible.

[0039] FIG. 11 illustrates a top-view of a metal oxide semiconductor transistor 1100 depicting a width parameter (WP) for the transistor. With respect to the circuit examples describe above with respect to FIGS. 5-9, the transistor switch device 1100 can be configured with a first width parameter and the compensation transistor device can be configured with a second width parameter that is less than the first width parameter. For example, the first width parameter (1WP) and the second width parameter (2WP) form a ratio of $1WP/2WP$, wherein the ratio of $1WP/2WP$ is in a range of approximately 5 to approximately 2; however, other ranges are possible. In one example, the first width parameter can be approximately 40 micrometers and the second width parameter can be in a range of approximately 8 micrometers to approximately 16 micrometers however other ranges of width parameters are possible.

[0040] FIG. 12 illustrates a signal diagram 1200 depicting the effects of a width parameter of a nonlinear capacitance compensation transistor with respect to mitigation of signal path nonlinearities. In this example, signal nonlinearity is depicted on the vertical axis of diagram 1200 as $|H2(dBc)|$, wherein H2 is second harmonic distortion and dBc is decibels relative to a carrier. The horizontal axis of diagram 1200 represents a width parameter (WP) for the compensation transistor device described above which ranges from approximately 8 micrometers to approximately 16 micrometers. Three signal plots 1210, 1220, and, 1230 are shown which

were plotted at temperatures -40C, +40, and +127C, respectively. Peak nonlinear compensation performance occurs when the width parameter WP is between approximately 11 micrometers and 14 micrometers and depending on the respective temperature. The corresponding width parameter for the transistor switch device when plotting the signal diagram 1200 was held at approximately 40 micrometers.

[0041] FIG. 13 illustrates a signal diagram 1300 depicting the effects of a tuning voltage of a nonlinear capacitance compensation transistor with respect to mitigation of signal path nonlinearities. In this example, tuning voltages were set from 1.5 volts to 2.0 volts with a given signal plot for each 0.1 v. Thus, signal plot 1310 is for 1.5 volts, signal plot 1320 is for 1.6 volts, signal plot 1330 is for 1.7 volts, signal plot 1340 is for 1.8 volts, signal plot 1350 is for 1.9 volts, and signal plot 1360 is for 2.0 volts, respectively.

[0042] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit comprising:
 - a phase adjustment capacitor (PAC) coupled to a signal path and configured to adjust a phase of a signal on the signal path;
 - a transistor switch device coupled in series with the PAC to provide a circuit branch parallel with the signal path, the transistor switch device configured to selectively open or close the circuit branch of the signal path to enable or disable, respectively, the adjustment of the phase of the signal on the signal path via the PAC; and
 - a nonlinear capacitance coupled to a node interconnecting the PAC and the transistor switch device, the nonlinear capacitance configured to vary inversely proportional with a capacitance of the transistor switch device with respect to the signal on the signal path and to linearize a total capacitance provided by the circuit branch when the circuit branch is open.
2. The circuit of claim 1, wherein the nonlinear capacitance is configured as a compensation diode that is coupled in parallel with a junction diode formed between the interconnecting node and a substrate of the transistor switch device when the circuit branch is open.
3. The circuit of claim 2, wherein a tuning voltage is applied to the compensation diode to adjust the nonlinear capacitance of the compensation diode.
4. The circuit of claim 1, further comprising a compensation transistor device configured to provide the nonlinear capacitance, the compensation transistor device having a source, a drain, and a gate, the nonlinear capacitance formed between either the source or the drain and a substrate of the compensation transistor device.
5. The circuit of claim 4, wherein one of the source or the drain of the compensation transistor device is coupled to the node interconnecting the PAC and the transistor switch device to provide the nonlinear capacitance with respect to the substrate of the compensation transistor device and the other of the source or the drain is coupled to the substrate of the compensation transistor device.
6. The circuit of claim 4, wherein each of the source and the drain of the compensation transistor device are coupled together to provide the nonlinear capacitance with respect to the substrate of the compensation transistor device and to increase the nonlinear capacitance of the compensation transistor device.

7. The circuit of claim 4, wherein a tuning voltage is applied to the gate and substrate of the compensation transistor device to adjust the nonlinear capacitance based on the tuning voltage that is applied.
8. The circuit of claim 7, wherein the tuning voltage applied to the gate is in a range of approximately 1.5 volts to approximately 2.0 volts to adjust the nonlinear capacitance.
9. The circuit of claim 4, wherein the transistor switch device is configured with a first width parameter and the compensation transistor device is configured with a second width parameter that is less than the first width parameter.
10. The circuit of claim 9, wherein the first width parameter (1WP) and the second width parameter (2WP) form a ratio of 1WP/2WP, wherein the ratio of 1WP/2WP is in a range of approximately 5 to approximately 2.
11. The circuit of claim 4, wherein the transistor switch device and the compensation transistor device are configured as complimentary devices such that if the transistor switch device is configured as an NMOS device, then the compensation transistor device is configured as a PMOS device or if the transistor switch device is configured as a PMOS device, then the compensation transistor device is configured as an NMOS device.
12. The circuit of claim 1, wherein the PAC, the transistor switch device, and the nonlinear capacitance form a first phase adjuster in a first differential signal path, the circuit further comprising a second PAC, a second transistor device, and a second nonlinear capacitance configured to form a second phase adjuster in a second differential signal path, the first and second differential signal paths being configured to enable differential phase adjustment of a differential signal applied to the first and second differential signal paths.
13. The circuit of claim 1, wherein the PAC, the transistor switch device, and the nonlinear capacitance form a first phase adjuster for the signal path, the circuit further comprising a second PAC, a second transistor device, and a second nonlinear capacitance configured to form a second phase adjuster in the signal path, such that the first and second phase adjusters are configured to enable multiple phase adjustments along the signal path.
14. A circuit comprising:
- a phase adjustment capacitor (PAC) coupled to a signal path and configured to adjust a phase of a signal on the signal path;
 - a transistor switch device coupled in series with the PAC to provide a circuit branch

parallel with the signal path, the transistor switch device configured to selectively open or close the circuit branch of the signal path to enable or disable, respectively, the adjustment of the signal phase of the signal path via the PAC; and

a compensation semiconductor device that includes at least one junction having a nonlinear capacitance, the compensation semiconductor device being coupled to a node interconnecting the PAC and the transistor switch device, the nonlinear capacitance of the compensation semiconductor device configured to vary inversely proportional with a capacitance of the transistor switch device with respect to the signal on the signal path and to linearize a total capacitance provided by the circuit branch when the circuit branch is open.

15. The circuit of claim 14, wherein the compensation semiconductor device is configured from a compensation transistor device having a source, a drain, and a gate, the compensation semiconductor device formed between either the source or the drain with respect to a substrate of the compensation transistor device.

16. The circuit of claim 15, wherein a tuning voltage is applied to the gate and substrate of the compensation transistor device to adjust the nonlinear capacitance provided by the compensation transistor device based on the tuning voltage.

17. The circuit of claim 15, wherein the transistor switch device is configured with a first width parameter (1WP) and the compensation transistor device is configured with a second width parameter (2WP) and form a ratio of $1WP/2WP$, wherein the ratio of $1WP/2WP$ is in a range of approximately 5 to approximately 2.

18. A circuit comprising:

a phase adjustment capacitor (PAC) coupled to a signal path and configured to adjust a phase of a signal on the signal path;

a transistor switch device coupled in series with the PAC to provide a circuit branch parallel with the signal path, the transistor switch device configured to selectively open or close the circuit branch of the signal path to enable or disable, respectively, the adjustment of the signal phase of the signal path via the PAC; and

a compensation transistor device having a source, a drain, and a gate, the compensation transistor device coupled to a node interconnecting the PAC and the transistor switch device, the compensation transistor device configured to provide a nonlinear capacitance formed between either the source or the drain with respect to a substrate of the compensation transistor device,

the nonlinear capacitance varying inversely proportional with a capacitance of the transistor switch device with respect to the signal on the signal path and to linearize a total capacitance provided by the circuit branch when the circuit branch is open,

a tuning voltage being applied to the gate and substrate of the compensation transistor device to adjust the nonlinear capacitance of the compensation transistor device based on the tuning voltage.

19. The circuit of claim 18, wherein the transistor switch device is configured with a first width parameter (1WP) and the compensation transistor device is configured with a second width parameter (2WP) and form a ratio of 1WP/2WP, wherein the ratio of 1WP/2WP is in a range of approximately 5 to approximately 2.

20. The circuit of claim 18, wherein the transistor switch device and the compensation transistor device are configured as complimentary devices such that if the transistor switch device is configured as an NMOS device, then the compensation transistor device is configured as a PMOS device or if the transistor switch device is configured as a PMOS device, then the compensation transistor device is configured as an NMOS device.

1/5

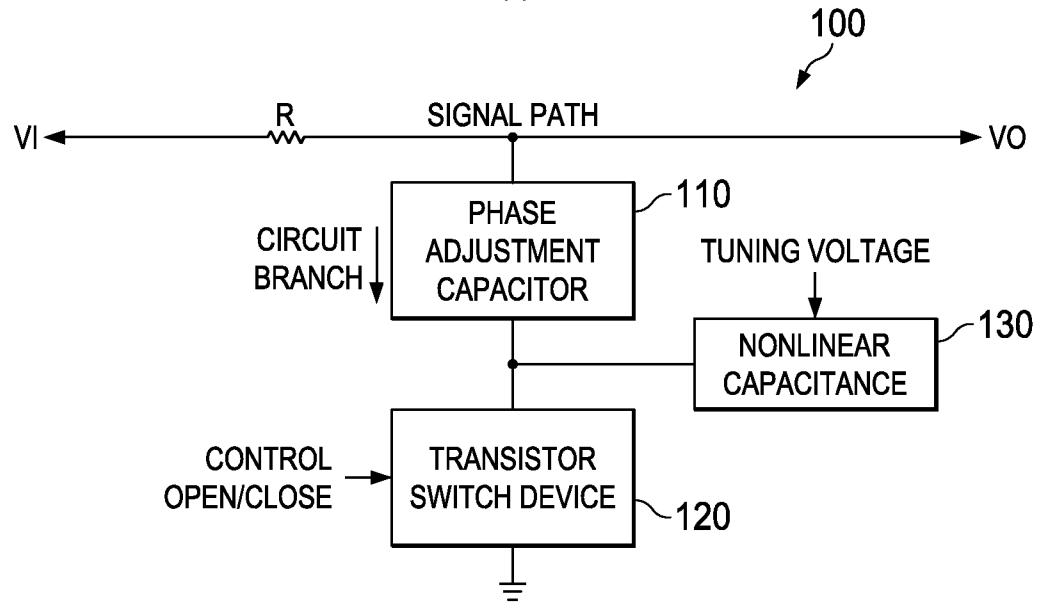


FIG. 1

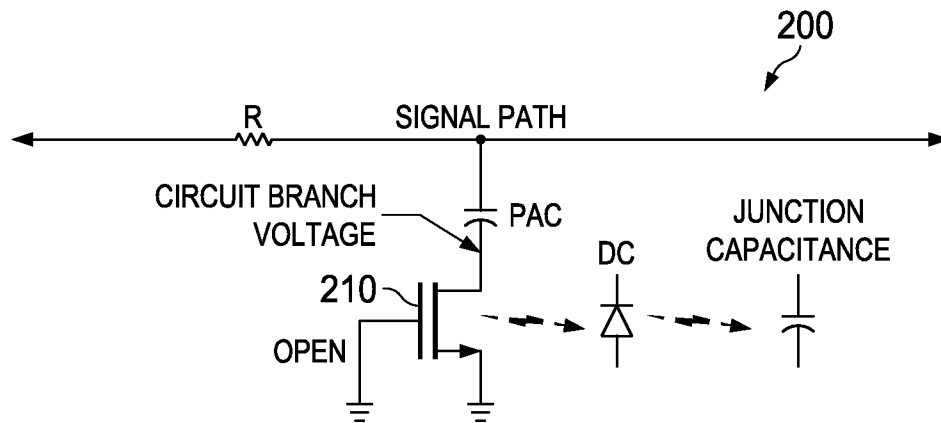


FIG. 2

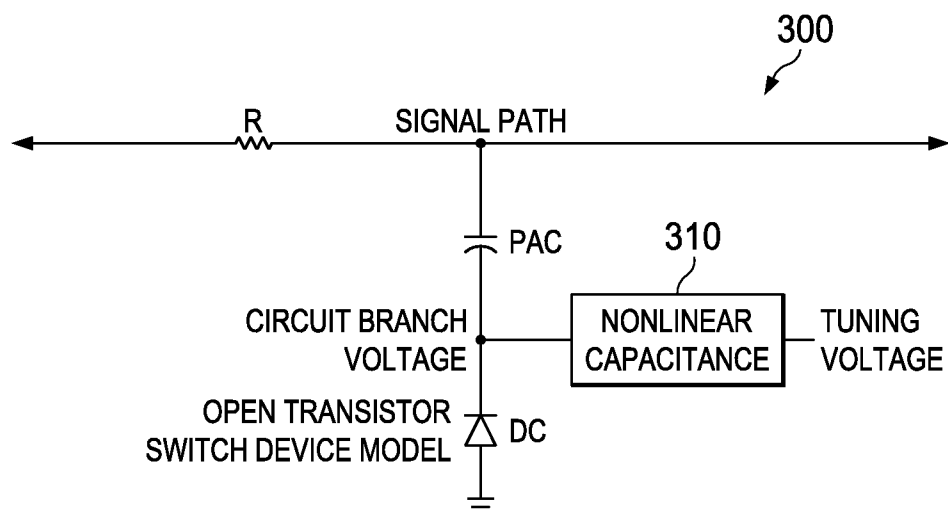


FIG. 3

2/5

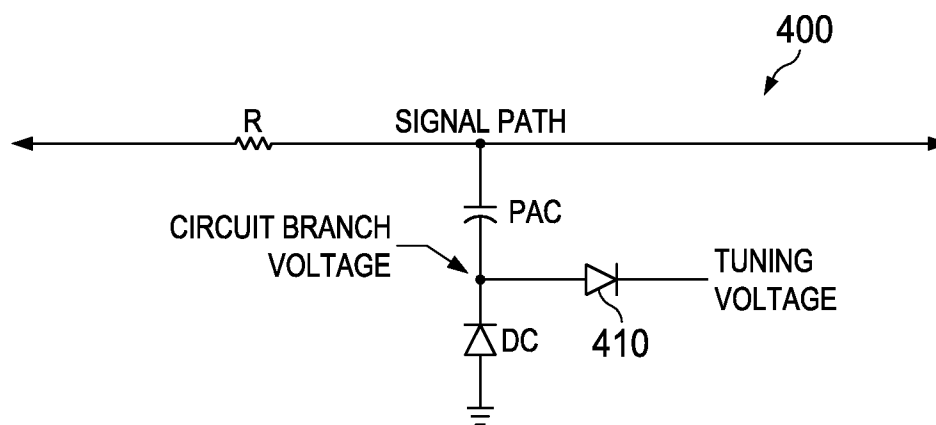


FIG. 4

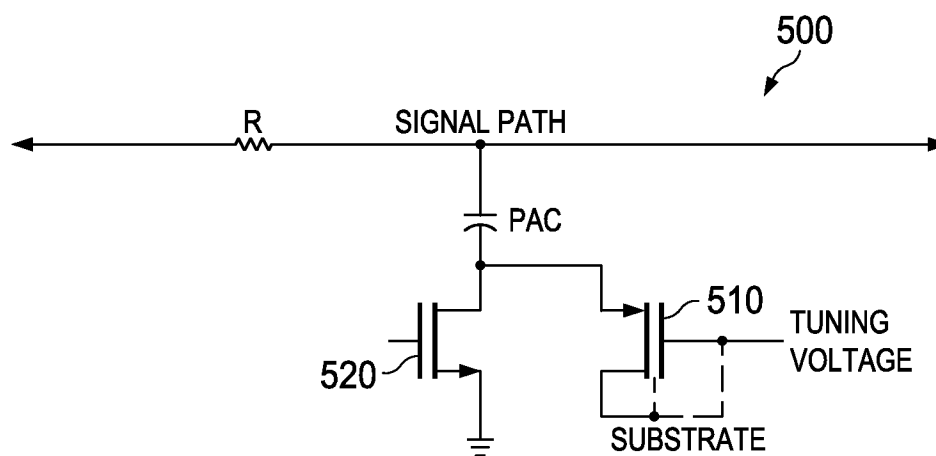


FIG. 5

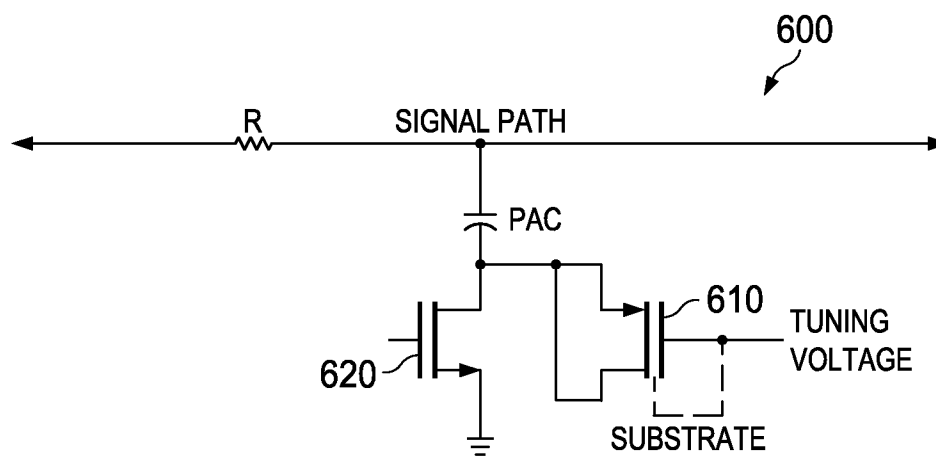


FIG. 6

3/5

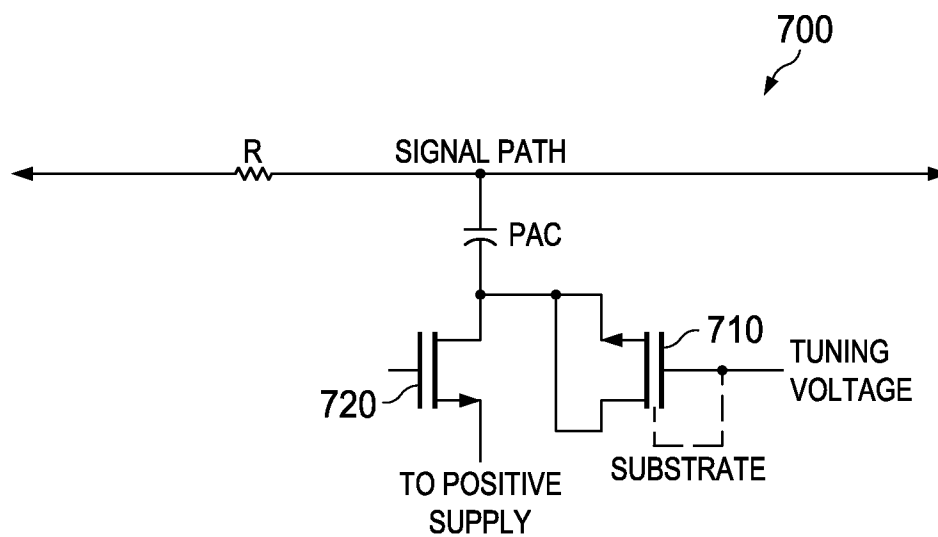


FIG. 7

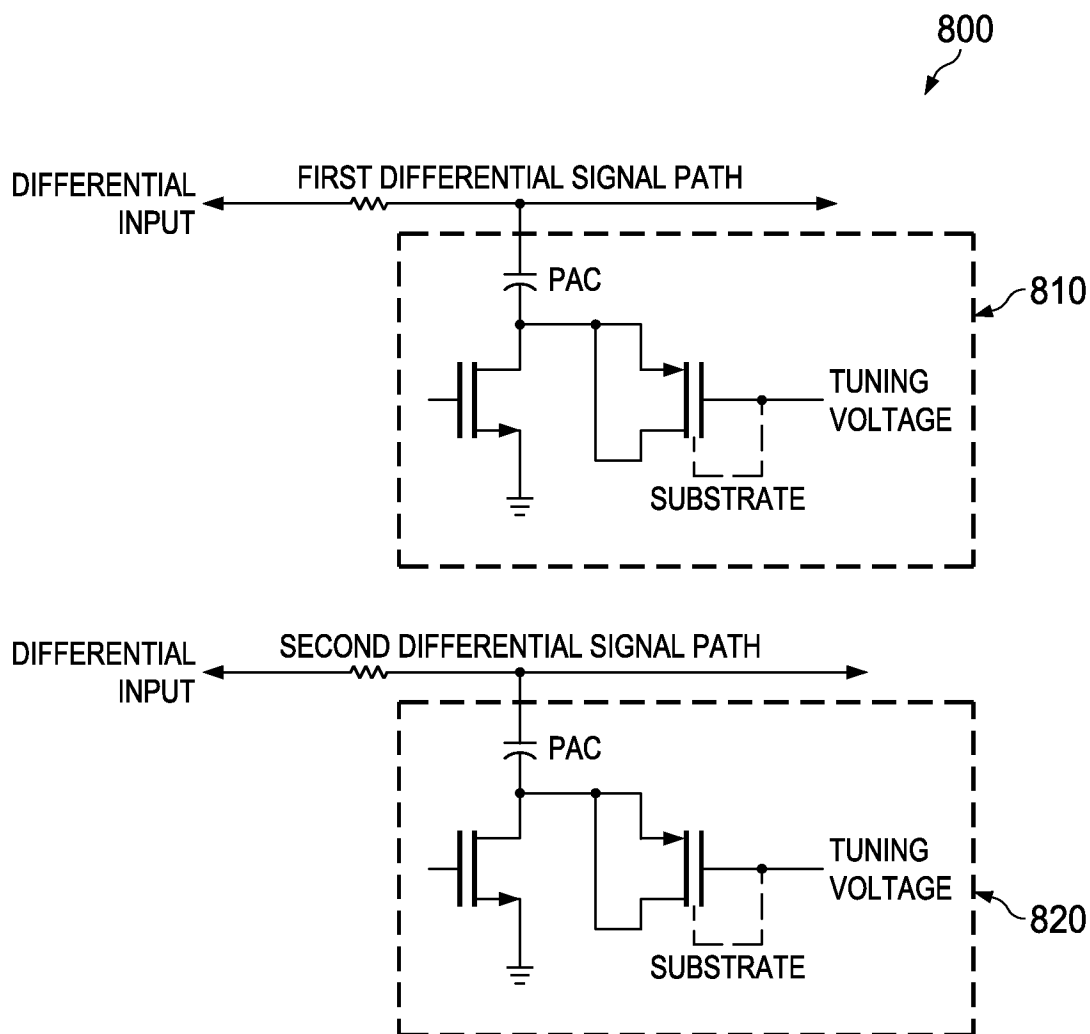


FIG. 8

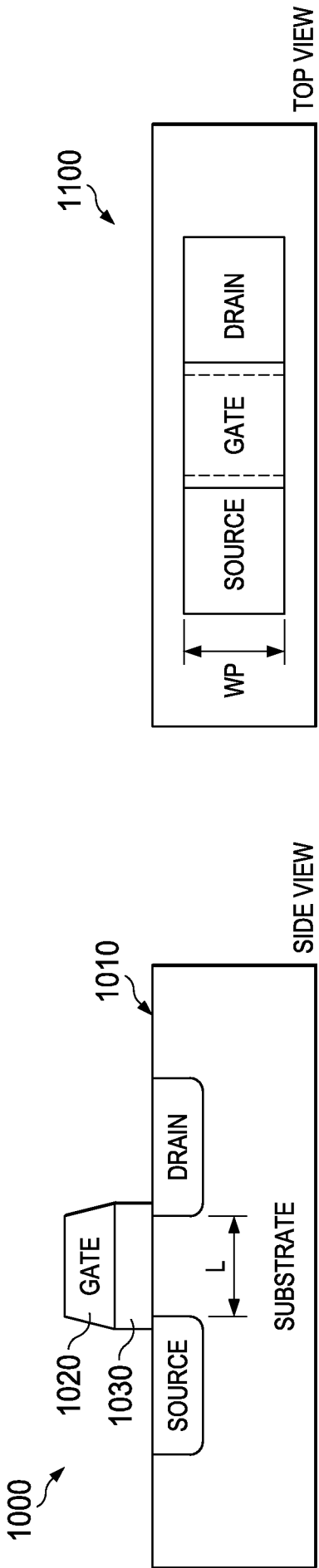
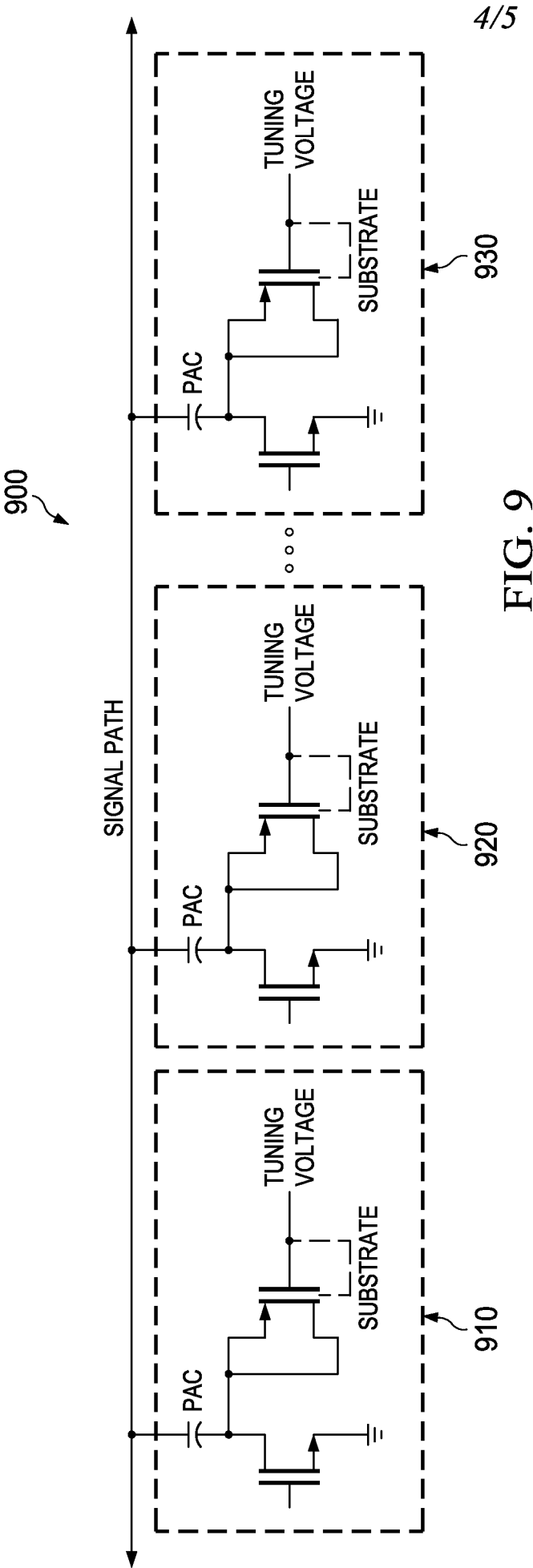


FIG. 11

5/5

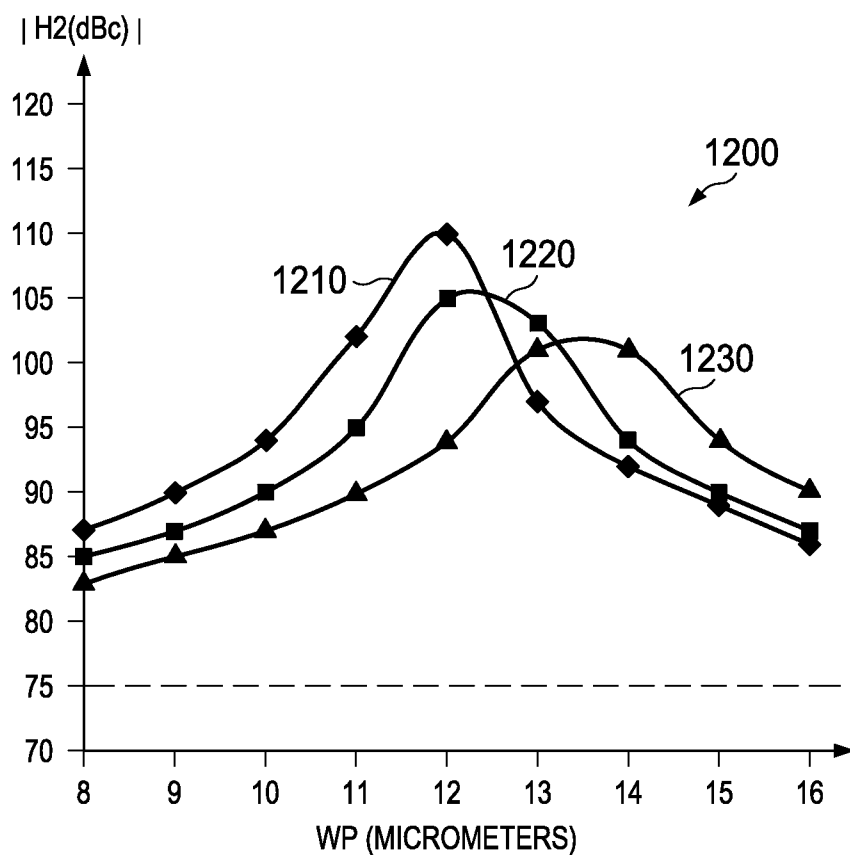


FIG. 12

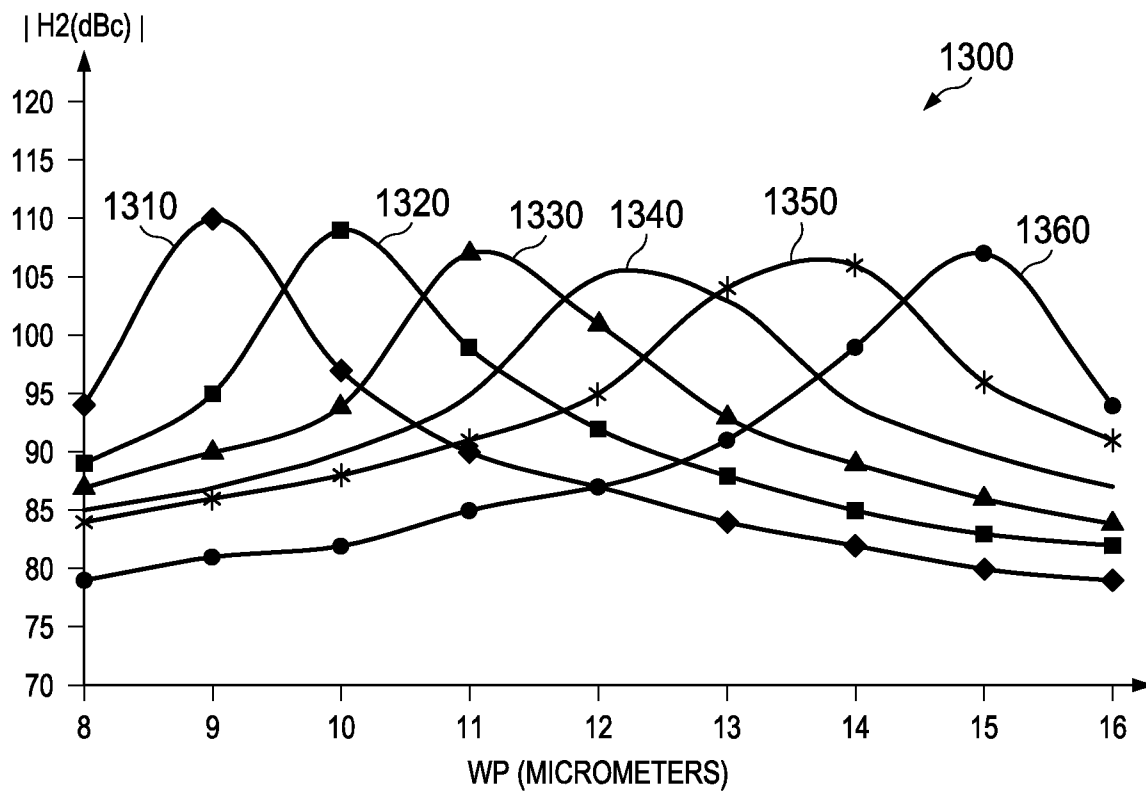


FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2015/023382

A. CLASSIFICATION OF SUBJECT MATTER

H03F 1/32 (2006.01)**H04B 1/04 (2006.01)**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03B 1/00, 1/08, 1/14, 1/32, H03G 3/00, 3/20, 3/30, H04B 1/00, 1/02, 1/04, 1/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2007/006868 A1 (NOKIA CORPORATION et al.) 18.01.2007, p. 2, line 34-p. 3, lines 7, 34-p. 4, lines 2, p. 8, line 31-p. 9, lines 6, 21-28, p. 10, lines 24-30, p. 13, lines 11-31, p. 22, lines 33-34, claims 1, 4-5, fig. 3A-3C, 6A-6B, 13	1-20
A	US 2003/0193371 A1 (LARRY LARSON et al.) 16.10.2003, paragraphs [0028]-[0029, [0035]-[0037], [0053], fig. 3a	1-20
A	WO 2009/066211 A2 (NXP B.V. et al.) 28.05.2009	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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“&” document member of the same patent family

Date of the actual completion of the international search

09 July 2015 (09.07.2015)

Date of mailing of the international search report

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