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Description

The invention relates to an electronic musical instrument equipped with an envelope generating means, wherein said envelope generating means is composed of an envelope memory for storing envelope data, and an address calculator for calculating the address data for the envelope memory in a time division multiplex fashion.

An instrument of this kind is known from US-A-3,844,379, in which a musical tone wave shape memory stores in analog a wave shape to be reproduced. The musical tone wave shape is read from this wave shape memory at a reading rate corresponding to the tone clock thus selected. Attack and decay of the musical tone wave shape envelope are also stored in analog in an envelope memory.

Conventionally, many kinds of proposals concerning digital tone source circuits for electronic musical instruments have been often tried. The complex waves including many harmonics have been read in wave data with a given clock from a read only memory (hereinafter referred to as ROM) or from a random access read/write memory (hereinafter referred to as RAM) to provide tone waves. Thereafter, the given envelope has been attached to the tone wave by digital or an analog techniques to provide the tone signals.

Some problems as follows exist. As a first problem, a calculation for generating the waves exist. Since to change the tone color, the complex waves are changed in shape within the instrument, when the tone color data are given at the proportion of each of the harmonics, like the draw-bar most used for the electronic musical instrument, in the order of the level of the 8 feet (fundamental), the level of the 4 feet (second harmonics) and the level of the $2\frac{2}{3}$ feet (third harmonics), the complex wave corresponding in shape to it has to be made from the tone color data. Namely, an inverted fourier transformation is required. Although recently, microcomputers are available at lower cost, the inverted fourier transformation requires time from several hundreds of milliseconds to approximately one second. In addition, the inverted fourier transformation is required everytime a player changes draw-bars or tone tables. Thus, when more time is required for calculation, the tone color cannot change immediately or for some time no tones can be generated. Accordingly, these solutions are not suitable for the performance of the musical setting which often requires frequent color-tone switching.

As a second problem, the tone color remains unchanged from the time of generation of a tone to the time at which the tone disappeares. If the inverted fourier transformation is performed from the tone color data and the wave data as provided, the wave data is written in the memory and the wave data of the memory is repeatedly read at a given clock rate, with the result that the wave normally becomes constant. Even if a given envelope is attached to the wave, the tone color remains unchanged. To change the tone color at any time, the memory wave has to be rewritten every time. Since the memory itself is normally read, it is required to be written between the read timings in synchronous relation with the read cycle for rewriting of the memory contents. The read clock rate is not always constant, since it changes with the produced step, and it is very difficult to rewrite the waves in terms of hardware. As described hereinabove, a tone-color change means a high-speed inverted fourier transformation each time, since the inverted fourier transformation is required to be performed each time from the tone color data to provide the wave data. Even from this point, it is apparent that an instantaneous change of the tone color is extremely difficult.

As a third problem, there is a problem of the system clock of the whole hardware. The digital circuit is adapted to operate under a fixed clock for easier synchronous relation of the whole system, whereby the timing between the logic circuits is definite and the construction of the hardware is rendered simpler. On the other hand, in the tone source circuit of the electronic musical instrument, twelve different clocks are necessary to obtain the tone signal of each note of C, C#, D ... B thereby to change the read speed. For instance, to change the octave in the order of C_1, C_2, C_3 ..., the clock for C note is required to be 1/2, 1/4, 1/8 ..., or the memory address is required to be read by 2 jumps, 4 jumps, 8 jumps, ... However, the clock of the C# note is required to be $2\frac{1}{12}$ times as fast as the clock of the C note. Similarly, the clock of the D note is required to be $2\frac{1}{12}$ times as fast as the clock of, the C note. The clock of the D# note is required to be $2\frac{1}{12}$ times as fast as the clock of the C note. Since these $2\frac{1}{12}$, $2\frac{2}{12}$, $2\frac{3}{12}$, ... are irrational numbers, 12 independent clock generators are required to generate these 12 clocks by the hardware. The problem is that synchronous relation cannot be provided, and the hardware cannot be used in common since the twelve clock speeds are completely independent. Accordingly, since a plurality of envelope multipliers and a plurality of digital-to-analog converters (hereinafter referred to as D/A converter) are required, the hardware becomes extremely larger in scale, thus resulting in complicated system construction.

Since in the electronic musical instrument as described in US-A-3,844,379, the musical tone wave as well as the attack and decay data are stored as analog signals in a wave shape memory and an envelope memory, the output data of these memories have to be performed by analog multiplication between the wave data and the envelope data. This causes problems of signal drifts and noises peculiar to analog processing.

Accordingly, it is an object of the present invention to provide an electronic musical instrument which avoides the above problems and which should be suitable for LSI integration.

According to the invention, an electronic musical instrument as defined in the preamble of claim 1 is characterized in that the envelope memory is a digital memory, that the address calculator for the envelope memory comprises a read/write memory having a multiple address for storing parameters supplied from control means via an initial loading interface, and an arithmetic logic circuit consisting of at least an adder for calculating the address data for the digital envelope memory in order to obtain a plurality of digital envelope data from the digital envelope memory in time division multiplex fashion.

Preferable embodiments are defined in the dependent claims.

These objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings in which:

Fig. 1 is a block diagram showing all components of an electronic musical instrument in which the present invention is being used;

Fig. 2 is a graph showing a single sine wave of a wave ROM 6 accessed by the address calculator of Fig. 1;

Fig. 3 is a graph showing a set of sine waves outputted from the ROM 6 of Fig. 1;

Fig. 4 is a block diagram showing parts of the ROM address calculator of Fig. 1;

Fig. 5 is a graph showing a set of waves outputted from the registers of Fig. 4;

Fig. 6 is a graph showing a sine curve outputted from the wave ROM 6 of Fig. 1;

Fig. 7 is a graph for illustrating the wave reading operation of the wave ROM address calculator of Fig. 1;

Fig. 8 is a graph showing sine curves of 3 phase clocks outputted from the wave ROM 6 of Fig. 1;

Fig. 9 is an explanatory diagram showing the construction of the envelope ROM 7 of Fig. 1;

Fig. 10 is an explanatory diagram showing a set of addresses outputted from the envelope ROM 7 of Fig. 1;

Fig. 11 is a block diagram showing parts of the envelope ROM address calculator of Fig. 1 according to the invention;

Fig. 12 is a graph showing waves outputted from the envelope ROM 7 of Fig. 1;

Fig. 13 is a block diagram of an electronic musical instrument in the second embodiment of the present invention;

Fig. 14 is a block diagram of the amplitude data storing means of Fig. 13;

Fig. 15 is a block diagram showing a modification of the wave ROM6 of Fig. 13;

Fig. 16 is a graph showing a set of sine curves outputted from the ROM 6 of Fig. 13; and

Fig. 17 is a block diagram of an electronic musical instrument in the third embodiment of the present invention.

Referring to Fig. 1, a tone selecting means 1 includes draw-bars, tone tablet switches, etc., and a player can operate the draw-bars, tone tablet switches, etc. to select the tones. Keyboards 2 mean a solo keyboard, an upper keyboard, a lower keyboard, a pedal keyboard, etc., and the player performs a tune on these keyboards. A microcomputer 3 inputs the tone color data and key data from the tone selecting means and the keyboards 2, gives necessary instructions to an address calculator 4 for a wave ROM 6 and an address calculator 5 for an envelope ROM 7 in accordance with the tone color data and key data. The address calculator 4 for the wave ROM 6 and the address calculator 5 for the envelope ROM 7 access the wave ROM 6 and the envelope ROM 7, respectively. The digital wave data and the digital envelope data obtained through the accessing operation of the wave ROM 6 and the envelope ROM 7 are digitally multiplied by a multiplier 8 to provide envelope-added tone signal data. The tone signal data are converted into analog values from the digital values by a D/A converter 9 and pass through a clock rejection filter 10 and a power amplifier 11 to pronounce from a loud speaker 12.

The wave ROM 6 will be described hereinafter. Referring to Fig. 2, if a period (x=0 through 2 π radian) of the x axis of sinusoidal wave represented by the following equation:

$$f(x) = A\sin x \quad (1)$$

is equally divided by n and $x_0, x_1, x_2, \ldots x_i \ldots x_{n-1}$ ($x_n = x_0$) are provided, then

$$x_i = \frac{2\pi i}{n} (i = 0, 1, 2, \ldots, n-1) \quad (2)$$

is established. The sampled value $f(x_i)$ of sinusoidal wave with respect to the x_i is as follows from the equation (1),

$$f(x_i) = A\sin x_i = A\sin\frac{2\pi i}{n} \quad (3)$$

The $f(x_i)$ is quantized, is written, in a digital value, in the wave ROM 6 and is arranged to be sequentially read by the clock f_{CK}[Hz]. Since i increases one by one for each $1/f_{CK}$[sec] (assume that $x_n=x_0$ is read after the x_{n-1} and x_1, x_2, x_3 ... are repeated in sequence) to establish

$$i = \frac{t}{1/f_{CK}} = f_{CK} \cdot t \quad (4)$$

Similarly, when the jumping read is performed m by m, i increases m by m for each $1/f_{CK}$[sec] to establish the following equation.

$$i = \frac{t}{1/f_{CK}} \cdot m = m \cdot f_{CK} \cdot t \quad (5)$$

When the equation (5) is substituted in the equation (3),

$$f(x_i) = A\sin 2\pi \cdot \frac{mf_{CK}}{n} \cdot t = A\sin 2\pi ft \quad (6)$$

is established. Namely, the frequency f of the sinusoidal wave to be read from the wave ROM 6 is as follows.

$$f = \frac{m}{n} f_{CK} \quad (7)$$

Assume that the wave from ROM having such a value of n as shown in Table 1 is provided for each of the notes, and the reading operation is performed at a constant f_{CK} so that the tone signal (sinusoidal wave) of each note of the notes C, C#, D, ... B with error of ±1.19 percents or less in practical use.

Table 1 Divisor n of Each Note

Note	Divisor n	Percent Error
C	451	+0.078
C#	426	-1.193
D	402	-0.804
D#	379	+1.193
E	358	-0.121
F	338	-0.597
F#	319	-0.437
G	301	+0.114
G#	284	+0.762
A	268	+1.151
A#	253	+0.866
B	239	-0.582

When the f_{CK} is rendered constant like f_{CK}= 14749.802 [Hz], the sinusoidal wave of approximately 8 feet of C_1 (about 65.4 Hz) is provided as apparent from the equation (7) wherein n=451, m=2, and the sinusoidal wave of approximately 69.3 Hz (8 feet of $C\#_1$) is provided as apparent from the equation (7) wherein n=426, m=2. Similarly, the wave ROM 6 which is different in n is read with a constant f_{CK} to provide the tone signals of all the notes.

Also, since 8 feet (about 65.4 Hz) of C_1 is provided during n=451 and m=2, 8 feet of C_2 (about 130.8 Hz) is provided during n=451 and m=4, and 8 feet of C_3 (about 261.6 Hz) is provided during N=451 and m=8. It has been found out that the octave treatment of the same note can be performed by the proper change of the value m.

Since the 8 feet of C_1 (about 65.4 Hz) is provided by n=451 and m=2, the 4 feet of the C_1, i.e., second harmonics (about 130.8 Hz) is provided by n=451 and m=4, the $2\frac{2}{3}$ feet of the C_1, i.e., third harmonics (about 196.2 Hz) is provided by n=451 and m=6, and the 2 feet of the C_1, i.e., fourth harmonics (about 261.6 Hz) is provided by n=451 and m=8. Accordingly, it has been found out that the tone signals of the generating harmonics can be controlled through the selection of the value of the m. One example of the values of the m will be described in Table 2.

Table 2 One Example of Values of m

Note / frequency	$C_1 \sim B_1$	$C_2 \sim B_2$	$C_3 \sim B_3$	$C_4 \sim B_4$	$C_5 \sim B_5$	C_6
16'	1	2	4	8	16	32
8'	2	4	8	16	32	64
$5\frac{1}{3}$'	3	6	12	24	48	96
4'	4	8	16	32	64	128
$2\frac{2}{3}$'	6	12	24	48	96	192
2'	8	16	32	64	128	256
$1\frac{3}{5}$'	10	20	40	80	160	320
$1\frac{1}{3}$'	12	24	48	96	192	384
1'	16	32	64	128	256	512

As apparent from the equation (7), the value of n or m is changed, even if f_{CK} is constant, to allow the tone frequency to be controlled freely.

If about 65.4 Hz (sound of C_1), which is obtained during n=451 (wave ROM of C) and m=2, is rendered fundamental in wave about 686.7 Hz which is frequency of 10.5 times of the fundamental frequency, i.e., non-integer harmonics is obtained during n=451 and m=21. Also, during n=301 (wave ROM of G) and m=4, about 196.0 Hz, i.e., slightly lower third harmonics, $2\frac{2}{3}$ feet which is lower by about two percents.

The wave ROM of each tone of C, C#, D, ... B is constructed as shown in Fig. 3. Assume that the value of n is as shown in Table 1, and the address of the wave ROM 6 of the C note is 0 through 450, C# note is 451 through 876, D note is 877 through 1278, ... B note is 3779 through 4017. The entire address is 4018, which is the total of 0 through 4017. The wave data of the sinusoidal wave is written, in the form of a digital value, in the wave ROM. When the optional address value up to 4017 from 0 is given to the wave ROM, the wave data of the sinusoidal wave stored in the wave ROM is read as a digital value.

A method of reading the wave data from the wave ROM 6 will be concretely described hereinafter in conjunction with Fig. 4 showing a circuit construction for describing the operation of the wave ROM address calculator 4.

As shown in Fig. 4, there are disposed a k register 21 for storing the address value of the wave ROM 6, a m register 22 for storing the number m of jumps, an E register 23 for storing the end address value, a ⊖ N register for storing the negative value of the divisor n, an adder 25, a comparator 26, an adder 27 and an AND gate 28.

For example, a case where the wave form of 8 feet of C_2# (about 69.2Hz) as an example will be read, will be described. As in the previous case, assume that f_{CK}= 14749.802 Hz. At this time, the wave ROM (n=426) of C# is required to be read with two jumps (m=2). Since the wave data are from the address 451 to 876 as shown in Fig. 3, 451 as the start address is stored in the k register 21, and 876 as the end address is stored in the E register 23. Since the divisor n=426 and jump m=2, ⊖ 426 as a negative value of the divisor is stored in the ⊖ N register 24 and 2 as the jump is stored in the m register 22. Since f_{CK}=14749.802 Hz, $1/f_{CK}$=67.8 μs is established. As shown in Fig. 5, a read clock ϕ_1 and a write clock ϕ_2 for four registers 21 through 24 are both assumed to have 67.8 μs and two phases. Upon application of the read clock ϕ_1, a value of 451 is obtained from the output terminal of the k register 21 and is applied to the address terminal of the wave ROM 6 to provide the wave data of C#. The 451 from the output terminal of the k register 21 and the 2 from the m register 22 are added by the full adder 25, and the value of 453 is given to the A terminal of the comparator 26 and to the full adder 27. The end address 876 from the E register 23 is applied to the B terminal of the comparator 26 to compare the value of the A terminal with the value of the B terminal. However, in this case, no output is provided at the A > B terminal and the value is 0, since 876 is larger than 453. As a result, the output of the AND gate 28 becomes 0 independently of the value ⊖ 426 of the ⊖ N register 24. The full adder 27 adds a value 453 coming from the full adder 25 and 0 coming from the AND gate 28 (thus resulting in no addition) to give a value of 453 to the input terminal of the k register 21. When the write clock ϕ_2 has come, the value of 453 from the full adder 27 is written in the k register. As a result, the value of the k register is rewritten to 453 from 451 and the value of the m register is rewritten from 451 to 453, which is obtained through addition of the value 2 of the m register 22.

Upon application of the read clock ϕ_1 to four registers 21, 22, 23, 24 again, the value of 453 is obtained from the output terminal of the k register 21 and is added to the address terminal of the wave ROM6 to provide the wave data of the C#. Simultaneously, through the full adder 25, the comparator 26, the AND gate 28 and the full adder 27, 455, which is provided through addition of 453 coming from the output terminal of the k register 21 to 2 coming from the m register 22, is added to the input terminal of the k register 21 and is written when the write clock ϕ_2 has come.

In this manner, the value of the k register 21 sequentially increases by two jumps in the order of 451, 453, 455, 457, 459 .... In keeping with the sequential increase, the wave data of two address jumps are sequentially obtained from the wave ROM 6. However, the address of the wave ROM 6 ranges from 451 to 876. Beyond the range, the wave data of the C# results in that of its adjacent D note. To prevent it, the comparator 26 compares the value from the full adder 25 with the end address 876 from the E register 23. If the value from the full adder 25 is 876 or or more, the output terminal A > B of the comparator 26 becomes 1 to provide the output of the AND gate 28 with the value ⊖ 426 from the ⊖ N register. The full adder 27 adds the value of the full adder 25 to the value of ⊖ 426 from the AND gate 28, i.e., subtracts 426 so that the end address 876 may not be exceeded by any means. The value of the k register 21 increases from 451 in the order of 453, 455, 457, 459, ... When 875 has been reached, the output of the full adder 25 becomes 877. Through comparison thereof with 876 by the comparator 26, the full adder 27 performs the operation of 877-426 to write 451 in the k register 21. Accordingly, since the value of the k register 21 is normally repeated in the order of 451, 453, 455, 457, ... 875, 451, 453, ..., only the values from 451 to 876 are available. The wave data of only the C# note of the wave ROM 6 is repeatedly read. If m=4, the order of 451, 455, 459, 463, 467, ... 875, 453, 457, 461 ... is repeated.

Since the value of the k register 21 is updated for each period 67.8 μs of the two phase clocks ϕ_1, ϕ_2, the wave data obtained from the wave ROM 6 is obtained for each 67.8 μs as shown in Fig. 6 so that sampled sinusoidal wave is obtained by the clock of f_{CK}=14749.802 Hz.

When 8 feet of the other note such as D_2 note is read, n=402 and m=4 are established. Since the wave data of the D note ranges from the address 877 of the wave ROM 6 to 1278 as shown in Fig. 3, 877 is written in the k register 21 and 1278 is written in the E register 23. Write ⊖ 402 in the ⊖ N register 24 and 4 in the m register 22, and the waveform data is automatically read, through the similar operation, from the wave ROM 6 for each 67.8 μs.

In the above-described manner, the wave data can be read from the wave ROM 6 by such a wave ROM address calculator as shown in Fig. 4. Only one wave can be read simultaneously. In the case of such a draw-bar tone source, assume that the number of the pitches of the draw-bars is rendered 9, i.e., 16 feet, 8 feet, $5\frac{1}{3}$ feet, 4 feet, $2\frac{2}{3}$ feet, 2 feet, $1\frac{3}{5}$ feet, $1\frac{1}{3}$ feet and 1 feet, and the number of the channels for maximum, simultaneous pronunciation is rendered 8, and that seventy two (nine pitches x 8 channels) wave ROM address calculators are required.

However, since the clock frequency is normally fixed in accordance with the method of the present invention, the circuit is suitable for common use if the timing of the hardware is rendered definite. Namely, a time division multiplexing operation can be effected. Fig. 7 shows a wave ROM address calculator 4, which can read seventy-two (in maximum) independent waveforms by the time division multiplexing operation. The timing for reading one wave is performed for each 67.8 μs as shown in Fig. 6, and the 67.8 μs is divided in time to 72 slots. Namely, one slot is approximately 0.942 μs. The completely independent waveform reading operation is performed for each of the slots. The minimum data necessary for reading one wave requires address value k for accessing the wave ROM6, number m of jumps, end address E and the negative figure ⊖ n of the divisor n. In Fig. 7, four random access read/write memories (hereinafter referred to as RAM) 31, 32, 33 and 34) having 72 addresses are provided, which independently stores the k, m, E and ⊖ n for 72 slots. Since RAMs of high storage capacity at low cost are available, they do not add much to the overall hardware cost.

The initial value to these RAMs is written through an initial loading interface 35 from the microcomputer 3. A full adder 25, a comparator 26, a full adder 27, an AND gate 28 and a wave ROM 6 may be the same as those of Fig. 4. These circuits may be common in 72 slots to perform the time division multiplexing calculation, which helps to simplify the hardware. Four RAMs are accessed in common by a slot counter 36 which counts a clock ϕ'_0. Also, the clocks ϕ'_1 and ϕ'_2 for reading to and storing in these RAMs commonly works for four RAMs. The timing of three clocks of these ϕ'_0, ϕ'_1 and ϕ'_2 is, respectively, 0.942 μs as shown in Fig. 8 and is a 3-phase clock which is different in phase.

How to assign the seventy-two addresses of RAMs 31, 32, 33, 34 is completely optional. For example, the assignment can be performed as in Table 3. These address values conform to the slot values of the time division multiplexing.

Table 3 RAM Assignment

RAM Address	Address Values			
	k	m	E	Θn
0	k value of 16' of CH1	m value of 16' of CH1	E value of 16' of CH1	Θn value of 16' of CH1
1	" 8' "	" 8' "	" 8' "	" 8' "
2	" $5\frac{1}{3}$' "	" $5\frac{1}{3}$' "	" $5\frac{1}{3}$' "	" $5\frac{1}{3}$' "
3	" 4' "	" 4' "	" 4' "	" 4' "
⋮	⋮	⋮	⋮	⋮
9	k value of 16' of CH2	m value of 16' of CH2	E value of 16' of CH2	Θn value of 16' of CH2
10	" 8' "	" 8' "	" 8' "	" 8' "
11	" $5\frac{1}{3}$' "	" $5\frac{1}{3}$' "	" $5\frac{1}{3}$' "	" $5\frac{1}{3}$' "
12	" 4' "	" 4' "	" 4' "	" 4' "
⋮	⋮	⋮	⋮	⋮
18	k value of 16' of CH3	m value of 16' of CH3	E value of 16' of CH3	Θn value of 16' of CH3
19	" 8' "	" 8' "	" 8' "	" 8' "
20	" $5\frac{1}{3}$' "	" $5\frac{1}{3}$' "	" $5\frac{1}{3}$' "	" $5\frac{1}{3}$' "
21	" 4' "	" 4' "	" 4' "	" 4' "
⋮	⋮	⋮	⋮	⋮
71	k value of 1' of CH8	m value of 1' of CH8	E value of 1' of CH8	Θn value of 1' of CH8

Assume that the draw-bars of 8 feet and 4 feet are in their pulled positions and three keys of C_3, E_3 and G_3 are in their depressed positions. Assume that the microcomputer 3 inputs these data, assigns C_3 to CH1,

E_3 to CH_2 and G_3 to CH3. The writing operation is effected, through an initializing interface 35, with respect to four RAMs 31, 32, 33 and 34. As apparent from Table 3, the 8 feet of the C_3 becomes a RAM address 1, the 4 feet of the C_3 becomes a RAM address 3, the 8 feet of the E_3 becomes a RAM address 10, the 4 feet of the E_3 becomes a RAM address 12, the 8 feet of the G_3 becomes a RAM address 19 and the 4 feet of the G_3 becomes a RAM address 21. Thus, as apparent from Table 2 and Fig. 3, 0 is written in the kRAM of the RAM address 1, 8 is written in the mRAM, 450 is written in the ERAM, $\ominus$ 451 is written in the $\ominus$ NRAM, 0 is written in the kRAM of the RAM address 3, 16 is written in the mRAM, 450 is written in the ERAM, and $\ominus$ 451 is written in the $\ominus$ NRAM. The initial values from Table 2 and Fig. 3 are written even in the kRAM, mRAM, ERAM and $\ominus$ NRAM of the RAM addresses 10, 12, 19 and 21.

When a clock enters the ϕ'_0 of Fig. 7, the address counter 36 is renewed to simultaneously update the addresses of four RAMs 31, 32, 33 and 34. Assume that the RAM address has changed from 0 to 1, and the k, m, E, $\ominus$ n of the RAM address 1 are read from the respective RAMs when the read clock ϕ'_1 has been given. The value 0 of the kRAM is given to the wave ROM 6 to provide the wave data of 8 feet of the C_3. The value 8 is written to the kRAM when the write clock ϕ'_2 has been given by the same operation as the operation already described in Fig. 4. When the clock of the ϕ'_0 has been given, the address counter 36 counts up to change the RAM address from 1 to 2. The similar operation is effected even in the RAM address 2. Set that the RAM address is adapted to make a round again to return to its original value upon application of 72 clocks to the ϕ_0' and the address becomes the address 1 again. The value of 8 is applied upon the ROM address from the kRAM when the ϕ'_1 clock has been given and simultaneously the value of 16 is written in the kRAM at the ϕ'_2 clock. Namely, as apparent from the RAM address 1 only, the ϕ_0' repeats the same operation as that of Fig. 4 everytime 72 clocks enter. Even in the other RAM address such as RAM address 10 to which the 8 feet of E_3 is assigned, the ϕ_0' performs the same operation as that of Fig. 4 everytime 72 clocks enter. Since the clock of the ϕ_0' is 0.942 µs, the 72 clocks is 67.8 µs and remains the same as in Fig. 4.

Namely, the use is performed under the time division multiplexing operation, with the adder 25, the comparator 26, the full adder 27, the AND gate 28 and the wave ROM 6 remaining unchanged, through the replacement of the RAM having 72 addresses therein instead of four registers 21, 22, 23 and 24 in Fig. 4. For the time division multiplexing operation of 72 data, a multiplexer (multiplex selection means) for switching the seventy-two signals is normally required to be provided, but in Fig. 7, the multiplexer is not required to be provided. The time division multiplexing operation is automatically performed. An arithmetic logic circuit of the adder 25, the comparator 26, the full adder 27 and the AND gate 28 performs the time division multiplexing operation of each 0.942 µs one time in accordance with the order of the RAM addresses. In terms of a specific RAM address, it follows that one operation is performed for each 67.8 µs. Even in reading of the wave data from the ROM 6, the time division multiplexing reading for each 0.942 µs is performed in accordance with the order of the RAM address. In terms of a specific RAM address, it follows that a given wave data is sequentially read for each 67.8 µs. Time division multiplexing operation of the 72 slots is performed during 67.8 µs and the 72 sinusoidal waves are read at maximum. One tone wave is read with one slot. In addition, the reading of each slot is completely independent. Namely, it is considered that the system construction of Fig. 7 is equivalent to seventy-two independent sinusoidal wave oscillators.

The envelope generation will be described hereinafter. The envelope is generated in synchronous relation with the wave generation. The seventy-two (at maximum) envelope signals are provided in the form of time division multiplexing operation. There are some generating methods for envelope signals, and one of them will be described hereinafter although the generating method is not specified.

First, the envelope ROM 7 will be described hereinafter.

Fig. 9 is one example, wherein the envelope ROM 7 is composed of a 256 address ROM from 00000000(2) to 11111111(2). The whole is equally divided into eight divisions. The rise-up and fall-down exponential envelopes quantized which are different in amplitude are sequentially written digitally in each of eight divisions. The condition of the respective rise-up envelope and fall-down envelope is apparent in the address of the ROM seen from binary. Namely, as shown in Fig. 10, 3 bits from the most significant bit, i.e., D_7 through D_5 can have eight values from 000 to 111. The 000 is least in amplitude and the 111 is biggest in amplitude. When the bit D_4 is 0, the rise-up envelope is indicated. When the bit D_4 is 1, the fall-down envelope is indicated. When the D_3 through D_0 shows 0000, it means the beginning of the rise-up envelope or the fall-down envelope. When the D_3 through D_0 shows 1111, it means the end of the rise-up envelope or the fall-down envelope.

The concrete construction of the envelope ROM address calculator 5 is shown in Fig. 11. The calculator 5 generates seventy-two (at maximum) independent envelope data through the time division multiplexing operation. The calculator is adapted to operate in synchronous relation with the wave ROM address calculator 4. The minimum data necessary for reading 1 envelope requires an address value J for accessing the envelope ROM, an attack speed value A for determining the attack speed of the envelope, a decay speed value D for determining the decay speed, a sustain address value S for determining the sustain level, a release speed value

R for determining the release speed, and a state code showing which of the attack, decay, sustain, release and completion the envelope is located in. They are independently stored for the 72 slots with respect to six RAMs 41, 42, 43, 44 45 and 46 having one address. The writing of these initial values to the RAM is performed through the initial loading interface 35 (which is the same as that of Fig. 7) from the microcomputer 3. The slot counter 36 is used in common with that of Fig. 7. The four RAMs 21, 22, 23 and 24 of Fig. 7 become completely the same in address as the six RAMs 41, 42, 43, 44, 45 and 46 of Fig. 11, so that the wave ROM address calculator 4 and the envelope ROM address calculator 5 will operate, retaining the synchronous relation at the same timing. In the Figures full adders are generally designated at 47, 49, respectively, a comparator is generally designated at 48, and an AND gate is generally designated at 50.

Dividers 62, 63, 64, 65, 66, 67, 68 and 69, respectively, divide the pulse of 67.4 μs from 1/8 to l/2048 to generate the pulse from 539.2 μs to 138.04 ms. One of the dividing pulses from these dividers is selectively switched by a multiplexer 51. Registers 71, 72, 73, 74 and 75 store comparative data to selectively switch these data by a multiplexer 52. Registers 81, 82, 83, 84 and 85 are adapted to temporarily retain the data to be selectively switched by a multiplexer 53. The full adders 47, 49, the comparator 48, the AND gate 50, the multiplexers 51, 52, 53 may be common in 72 slots and use the time division multiplexing. The read clock ϕ'_1 and the write clock ϕ'_2 are the same as those of Fig. 7. The timing thereof is shown in Fig. 8.

The assignment of each slot of the six RAMs 42 through 46 is required to be the same as that of the wave ROM address calculator of Fig. 7. Namely, the RAM address 0 is required to become the 16 feet of the CH1, the RAM address 1 is required to become the 8 feet of the CH1, ... The RAM address 72 is required to become 1 feet of the CH8.

Assume that the keys of C_3, E_3, G_3 are depressed as in the case described hereinabove, the draw-bar of the 8 feet is in its fully pulled position and the draw-bar of the 4′ is in its slightly pulled position. As a result, assume that the microcomputer 3 assigns C_3 to the CH1, E_3 to the CH2, and G_3 to the CH3, and the microcomputer 3 writes the data necessary for the six RAMs through the initial loading interface 35. The 8 feet envelope data for C_3 is written in the RAM address 1 and the 4 feet envelope data for C_3 is written in the RAM address 3. Similarly, the 8 feet envelope data for E_3 is written in the RAM address 10. The 4 feet envelope data for E_3 is written in the RAM address 12. The 8 feet envelope data for G_3 is written in the RAM address 19. The 4 feet envelope data for G_3 is written in the RAM address 21.

Since the 8 feet draw-bar is fully pulled, 11100000(2) (envelope of maximum volume) is written in the J-RAMs of the RAM addresses 1, 10 and 19. Also, since the 4-feet draw-bar is slightly pulled, 00000000(2) (envelope of minimum volume) is written in the J-RAMs of the RAM addresses 3, 12 and 21. Also, 0 is written, respectively, in all the state code RAMs of the RAM addresses 1, 3, 10, 12, 19 and 21. The state codes are shown as in Table 4. At the same time, the attack data, the decay data and the sustain data are written, respectively, in the A-RAM, D-RAM, S-RAM and R-RAM.

Table 4

State Code	Condition
0	attack
1	decay
2	sustain
3	release
4	completion

A method of generating the ADSR envelope will be described hereinafter. In the case of the RAM address 1, the attack condition exists, since the initial value 0 is written in the state code RAM. The multiplexer 53 selects the value of the A-RAM of the RAM address 1 through the attack register 81. If the value of 2 is written therein, it is given to the multiplexer 51 through the multiplexer 53. As apparent from Fig. 5, the pulse of 2.156 ms is supplied to the AND gate 54 from the l/32 divider 68. Since the output of the AND gate 54 becomes 1 for each 2.156 ms and the output otherwise 0, the full adder 47 adds the value of the J-RAM of the RAM address 1 one by one for each 2.156 ms to increase to 11100001(2), 11100010(2), 11100011(2) ..., 11101111(2) from 11100000(2) thereby to access from the envelope ROM 7 the rise-up portion of the envelope of the maximum amplitude of Fig. 9. In this case, since the number of the addresses of the rise-up portion is 16, the rise-up time comes to 2.156 ms x 16 = 34.5 ms.

Table 5

ARD Data	Frequency Division Ratio	Frequency Division Pulse
0	1/8	0.539 ms
1	1/16	1.078 ms
2	1/32	2.156 ms
3	1/64	4.313 ms
4	1/128	8.627 ms
5	1/256	17.25 ms
6	1/512	34.5 ms
7	1/1024	69.0 ms
8	1/2048	138.0 ms
9	"0"	∞ ms

On the other hand, the value of 0 from the state code RAM is supplied even to the multiplexer 52 to select the register 71. The 5 bits from the least significant bit of the address of the envelope ROM 7, i.e., the address data 01111(2) of the D_4 through D_0 as shown in Fig. 10 is retained in the register. As apparent from Fig. 9, the value shows 5 bits, from the least significant bit, of the last address of the rise-up envelope. The value of of the 01111(2) from the register 71 is given to the B terminal of the comparator 48 through the multiplexer 52. The 5 bits from the least significant bit of the full adder 47 is supplied to the A terminal. The comparator 48 checks whether or not the rise-up envelope has been completed. When the value of the A terminal has exceeded the value of the B terminal, the comparator A>B becomes 1 so that the output of the AND gate 50 becomes 1. Thus, the full adder 49 adds 1 to the value of the state code RAM of the RAM address 1, and, namely, the value changes from 0 to 1. As apparent from Table 4, the 1 means the decay condition. The multiplexer 53 selects the value of the D-RAM of the RAM address 1 through the register 82. When the value is 5, the value of 5 is added to the multiplexer 51. As apparent from Table 5, the multiplexer 51 selects the frequency divider 65 of 1/256 to give a pulse to the AND gate 54 for each 17.25 ms. Thus, the value of the J-RAM keeps increasing one by one for each 17.25 ms and changes in the order from 11110000(2) to 11110001(2), 11110010(2), 11110011(2), ... The fall-down envelope of the envelope RAM of Fig. 9 is accessed. On the other hand, the value of 1 from the state code RAM is supplied to the multiplexer 52 and the value of S-RAM of the RAM address 1 is supplied to the B terminal of the comparator 48 through the register 72. The value of the S-RAM can have the values from 10000(2) to 11111(2) at the 5 bits, from the least significant bit, of the ROM address of the envelope ROM 7. As apparent from Fig. 9, the value is the address value of the fall-down envelope. For example, if the value of the S-RAM is 10111(2), the value is added to the B terminal of the comparator 48. The value of 5 bits, from the least significant bit, from the full adder 47 is given to the A terminal. The value of the A terminal is compared with the 10111(2) of the B terminal. When the A exceeds B, 1 is provided at the A>B terminal and is supplied to the AND gate 50. The full adder 49 increases the value of the state code RAM by one, and, namely, the value changes from 1 to 2. As apparent from Table 4, it means that the condition has been switched from the decay to the sustain. Under the decay condition, the value of the J-Ram has 8 addresses from 11110000(2) to 11110111(2) and thus time becomes 17.25 ms x 8 = 138 ms.

Under the sustain condition, the value of 2 from the state code RAM gives to the multiplexer 51 a value of 9, which is retained in the register 83 by the multiplexer 53. As apparent from Table 5, the frequency divider 61 is selected with a value of 9. However, no pulses are provided for ever from the frequency divider 61, and thus the value is normally 0. Accordingly, the output of the AND gate 54 is 0 for ever, and the value of the J-

RAM remains 11110111(2). Since the ROM address 11110111(2) of the envelope ROM 7 remains accessed for ever, the envelope retains a constant level, which does not change together with time, to realize a so-called sustain condition. Under this sustain condition, the multiplexer 52 selects the register 73 with a value of 2 from the state code RAM 42. But the 11111(2) which is a value of 5 bits from the least significant bit of the envelope ROM 7 is retained in the register. As apparent from Fig. 9, the value shows the last address of the fall-down envelope. Although the value is added to the B terminal of the comparator 48, the value of the J-RAM 41 remains 11110111(2) and does not increase. 1 does not appear at the A>B terminal of the comparator 48. The output of the AND gate 50 remains 0. As a result, the value of the state code RAM 42 does not increase and retains 2.

Since the RAM address 1 has the 8 feet of the C_3 assigned thereto, the sustain condition remains for ever so long as the key of the C_3 is in its depressed condition.

When the key of the C_3 is released, the microcomputer 3 inputs the keyboard data to instruct the value of 3 to the state code RAM 42 of the RAM address 1 and the RAM address 3 (since the 4 feet of C_3 is assigned even to the RAM address 3) through the initial loading interface 35. As apparent from Table 4, this means release. The value of the 3 is applied to the multiplexer 53. The multiplexer 53 selects the value of the R-RAM 46 through the register 84 to supply it to the multiplexer 51. If the value of 8 is written in the R-RAM 46, the 1/2048 frequency divider 63 is selected as apparent from Table 5 and the pulse is fed to the AND gate 54 once for each 138.0 ms. Accordingly, the value of the J-RAM 41 starts to increase again for each 138.0 ms by the full adder 47 and changes from 11110111(2) to 11111000(2), 11111001(2), 11111010(2), ... to sequentially access the fall-down envelope of the envelope ROM 7. On the other hand, the value of 3 from the state code RAM 42 is given even to the multiplexer 52 to select the register 74. The 11111(2) of the 5 bits of the least significant bit of the ROM address of the envelope ROM 7 is stored even in the register. This is the last address of the fall-down envelope. This value is applied to the B terminal of the comparator 48 through the multiplexer 52 and is always compared with the value of the A terminal from the full adder 47. If the value of A exceeds the value of B, and the value of J-RAM 41 becomes 1111111(2) and comes to the fall-down last address of the envelope ROM 7, the A>B terminal of the comparator 48 becomes 1. The full adder 49 adds 1 to the value of the state code RAM 42, and, namely, the value changes from 3 to 4. As apparent from Table 4, the value of 4 means that the envelope has been completed. Since the value of the J-RAM 41 has 8 addresses from the 11110111(2) to the 11111111(2) in the release period, 138.0 ms x 8 = 1.104 seconds is established.

The value of 4 from the state code RAM 42 is applied to the multiplexer 53 and the value of 9 is selected from the register 85. Thus, the value is supplied to the multiplexer 51 through the multiplexer 53 to select the frequency divider 61 as apparent from Table 5. As described hereinabove, since no pulses are supplied and 0 normally remains, only the 0 is normally supplied through the multiplexer 51 to the AND gate 54. As a result, the value of the J-RAM 41 remains 11111111(2). On the other hand, the value of 4 from the state code RAM 42 is fed even to the multiplexer 52. As a result, the value 11111(2) of the 5 bits from the least significant bit of the envelope ROM 7 is given to the B terminal of the comparator 48 through the multiplexer 52 from the register 75. Since the value of the J-RAM 41 remains unchanged to 11111111(2), the five bits value, from the least significant bit, from the full adder 47 becomes 11111(2) so that the A terminal of the comparator 49 does not exceed the value of the B terminal. Accordingly, since the A>B terminal of the comparator 49 becomes 0 for ever and the output of the AND gate 50 remains 0, the state code RAM 42 remains 4. As a result, unless a new key is assigned, from the microcomputer 3, to the RAM address 1, the 11111111(2) is retained for ever in the J-RAM and 4 remains in the state code RAM 42. The final envelope data of the fall-down envelope of the envelope ROM 7, i.e., a condition where the envelope has been fallen down (condition of no sounds) remains.

The ADSR envelope obtained by the above description is shown in Fig. 12. It can be easily understood from the above description that the attack time, the decay time, the sustain level and the release time can be freely changed when the initial value to be written from the microcomputer 3 in each of the A-RAM 43, D-RAM 44, S-RAM 45, R-RAM 46 is changed. As apparent from Table 5, the attack time, the decay time and the release time becomes shorter when the initial values, to be written in the A-RAM 43, D-RAM 44 and R-RAM 46, are rendered smaller, and become longer when the initial values are rendered larger. Also, as apparent from Fig. 9, when the initial value to be written in the S-RAM becomes closer to 10000(2), the sustain level becomes larger. When it becomes closer to 11111(2), the sustain level becomes smaller. Since the ADSR envelope can be freely set as described hereinabove, most of the simulations for existing musical instruments can be realized.

Although the case of only the RAM address 1 in the construction of Fig. 11 has been described hereinabove, the same things can be said even to all the 72 addresses from the address 0 to 71. Since it can be easily understood from the description of Fig. 7 that the time of 67.8 μs is divided into 72 slots and the time division multiplexing operation can be effected with the time of one slot 0.942 μs, the description is omitted.

Returning to Fig. 1, the ROM address for the wave ROM 6 is calculated by the time division multiplexing operation of the 72 slots and is calculated from the wave ROM address calculator 4 so that the wave data is also obtained in the form of the time division multiplexing of the 72 slots from the wave ROM 6. Since the ROM address for the envelope ROM 7 is obtained in the form of the time division multiplexing of the 72 slots even from the envelope ROM address calculator 5 at a timing synchronized with it, the envelope data from the envelope ROM 7 is obtained in the form of the time division multiplexing of the 72 slots. Since these wave data are multiplied by the envelope data with a multiplier 8, the wave data with the envelope attached thereto is obtained in the form of the time division multiplexing of the 72 slots, and the output is also provided as tone signals from the speaker 12 through a D/A converter 9, a clock rejection filter 10 and a power amplifier 11.

In the above description, the rise-up and fall-down envelope data of the various amplitudes are stored as the envelope ROM 7 as shown in Fig. 9. An embodiment wherein the envelope data of the amplitude of one type is accommodated and the ROM size is rendered smaller will be described hereinafter.

Fig. 13 shows the entire system thereof. The difference from the construction of Fig. 1 lies in the addition of the amplitude data storing means 13 and the multiplier 14. Since the amplitude data is obtained with time division multiplexing from the amplitude data storing means 13, only the envelope data of a constant amplitude is required to be stored in the envelope ROM 7. As shown in Fig. 14, the RAM 47 of 72 addresses where the amplitude data W are stored is required to be provided as the actual construction of the amplitude data storing means. The slot counter 36, the microcomputer 3 and the initial loading interface 35 may be the same as those shown already in Fig. 7 and Fig. 11.

When the amplitude data is written in each address, through the initial loading interface 35, from the microcomputer with respect to the wave data RAM 47, the address counter sequentially accesses the RAM 47 for each counting of the ϕ'_0 to provide the amplitude data in the form of the time division multiplexing to the output.

The wave ROM 6 can also be rendered smaller in size by the addition of some hardwares.

One example of the construction of the wave ROM 6 will be shown in Fig. 15. As shown in Fig. 16, the wave ROM 6 has the one-half-period wave data of the sinusoidal wave stored therein. One bit of sign RAM 48 is provided adjacent to the K-RAM 31 and the value of $\ominus$ n/2 is stored in the RAM 34. Since the wave ROM 6 is stored by half the wave in such a manner as described hereinabove, the ROM size can be reduced to one half. The size of the wave ROM can be made necessarily smaller in size due to addition of some hardwares even in the one-fourth wave.

Details of the multichannel construction of Fig. 1 can be seen in Fig. 17. Referring to Fig. 17, the converters 91, 92, 93, the clock rejection filters 101, 102, 103, the power amplifiers 111, 112, 113 and the speakers 121, 122, 123 are disposed by three channels. The channel data from the channel data means 14 determines which channel makes sounds. The demultiplexer 15 distributes the tone signal data, which is obtained from the multiplier 8 and has already had the envelope to a given channel by a channel data. Accordingly, the microcomputer 3 writes in the channel data means 14 a channel to be assigned in each of the 72 slots.

The channel data means 14 is the same in construction as the amplitude data means of Fig. 14.

Some advantages of the embodiment will be enumerated hereinafter.

In the time division multiplex of 72 slots, anything can be assigned to the 72 slots. In the embodiment, the assignment has been performed as shown in Table 3, considering the use as the tone source for the draw-bar application, but the assignment is not restricted. Extremely speaking, the 72 slots may be assigned up to the seventy-second harmonics from the fundamental in the use as the tone source of the monotony. Also, since the number of the maximum, simultaneous pronunciations is considered for in the use as the accompaniment chord, 18 slots can be assigned per one tone and can be assigned from the fundamental to the eighteenth harmonics. In this manner, flexibility is allowed with respect to any tone source.

Secondly, since the sinusoidal wave is read as the wave data, purer and soft tones can be provided than flute type waves are, which have been provided through the filter from the rectangular wave or the saw-tooth waves as before.

Thirdly, the present system does not require a tone color filter at all as in conventional systems, since the tone color is adapted to be changed by the composition of the sinusoidal wave. The use of tone color filters not only complicates the system, but also causes undesirable results such as S/N reduction, distortion inducement, etc. In the case of the present system, the D/A conversion allows the direct connection up to the power amplifier without extra work.

Fourthly, the system wherein no wave calculation is performed is one of the characteristics in accordance with the present invention. Assume that the harmonics from the fundamental to the seventy-second are assigned to the 72 slots. According to conventional methods, upon application of the spectrum from the fundamental to the seventy-second harmonics as the tone color data, the sinusoidal wave amplitude of each of the 72 harmonics is multiplied by the respective spectrum amount in accordance with the spectrum. They are added to provide complex waves, which are written into a wave memory. Thereafter, the wave reading is performed for multiplication with the envelope data, and a so-called inverted fourier transform is provided. On the other hand, according to the present system, all the 72 sinusoidal waves will be read with the same amplitude straight without the wave calculation. And a given tone color is provided as the multiplication results with the 72 envelope data. The problems involved in the wave calculation are provided as described in the beginning. In the system of the present invention, all these problems can be settled.

Fifthly, the characteristic is that the instantaneous tone color can be changed. The 72 slots can control the frequency of the wave independently and can set the envelope of the ADSR independently. Since the instantaneous color tone variation means an instantaneous spectrum variation, assume that the seventy-two harmonics are assigned from the fundamental to the 72 slots, and the attack time is made faster with lower order in harmonics and the attack time is made sufficiently slower with higher order in harmonics so that soft tones which are less in harmonics starts at the beginning of the key depression, and tone which are more in harmonics are provided as time passes. Also, assume that the longer decay time with lower order in harmonics and the shorter decay time with higher order in harmonics, and sharp sounds which are produced when an object has been beaten are caused at the beginning upon depression of the key, and the harmonics decrease immediately after the sharp sounds thereby to leave the soft sounds behind. At this time, sounds like piano can be simulated. The ADSR of each harmonic envelope is improved to become free from the electric characteristics such as continuous fixed tone-color, which can be often found in the conventional electronic musical instruments.

Sixthly, since the clocks ϕ'_0, ϕ'_1 ϕ'_2 are rendered constant as 0.942 μs, which is not changed for every circuit and is fixed without changes for each note, the system construction is extremely simple. In the case of the embodiment, only the RAM address requires 72 waves or envelopes independently, although the 72 waves or envelopes are read independently. Not only the full adder, comparator necessary for calculation, but also the wave ROM, envelope ROM, multiplier, D/A converter, etc. are not disposed by 72. If they are disposed one by one, the employment can be performed by the time division multiplex of 72 slot portions. In the time division multiplex of 72 slots, 72 data are normally provided and are sequentially switched by the multiplexer. However, according to the present invention, the RAM of the 72 addresses is used. Thus, the time division multiplexing can be realized freely, by the rotation of the addresses, without the use of the multiplexer. This point is an advantageous point in the system construction of the present invention.

Seventhly, the major system portion of the present invention is all digital. Digital circuits are better in view of noise margin as compared with analog circuits. Namely, since all the circuit repeats 1 and 0 fully in the power source voltage, all the signals can be handled in volt units. On the other hand, analog circuits require to handle the signals in millivolt or microvolt units. Thus, special care is required in design even in view of S/N, distortion or earth wiring. In addition, in analog circuits, the problems such as drift, offset or the like are normally required to be taken into consideration during design. However, in digital circuits, 1 remains 1 strictly and 0 remains 0 strictly unless an unavoidable thing occurs. Since 1+1=2 and 0x0=0, 1+1=2.001 is not correct and 0x0=0.001 is not correct. In digital circuits, the problems such as drift and offset are irrelevant in normal design.

Eightly, fluctuations caused by element variations, or adjustment requirements are removed. For example, the construction of the same instrument as that of the above-described embodiment, using analog circuits requires 72 sinusoidal wave oscillators, 72 envelope generating means and 72 analog multipliers. Speaking about the oscillator, the oscillation amplitude causes variations due to the value of the transistor or CR to be used. When necessary, the adjustment may be required. The same things can be said even about the variations in the 72 envelope generating means and the analog multiplier. On the other hand, in the digital system of the present invention, no variations are caused among the 72 slots so long as the operation is normal even in the wave data and the envelope data. Accordingly, conventional adjusting operations can be avoided.

Ninthly, advantages are provided in assembling the electronic musical instrument. Namely, major portions of the present invention are of digital construction easier for large scale integration and can be realized with the use of approximately 10,000 transistors in the number of the elements except for the microcomputers. Current digital LSI can sufficiently include in 1 chip 64K bit mask ROMs and 16K bit static RAMs. The major portions of the electronic musical instrument, even if the microcomputer is contained, can be constructed on one printed circuit board, thus resulting in a remarkable progress as compared with the conventional construction of using ten-odd or several tens of printed circuit boards.

For easier understanding in the above description, concrete numeral values are used. However, the present invention is not restricted to these numeral values. The wave ROM may be a RAM without any restriction to the ROM.

As described hereinabove, the present invention can realize a tone source system for a superior electronic musical instrument which is suitable for LSI application, since the wave data can be provided in the form of the time division multiplexing, or the envelope data can be provided in the form of time division multiplexing in synchronous relation with it, and the wave data to which the envelopes are attached can be provided in the form of time division multiplexing through multiplication of these data.

Claims

1. An electronic musical instrument equipped with an envelope generating means, wherein said envelope generating means is composed of an envelope memory (7) for storing envelope data, and an address calculator (5) for calculating the address data for the envelope memory (7) in a time division multiplex fashion, characterized in that the envelope memory (7) is a digital memory, that the address calculator (5) for the envelope memory (7) comprises a read/write memory (41-46) having a multiple address for storing parameters (J, state code, A, D, S, R) supplied from control means (3) via an initial loading interface (35), and an arithmetic logic circuit (47-50) consisting of at least an adder for calculating the address data for the digital envelope memory (7) in order to obtain a plurality of digital envelope data from the digital envelope memory (7) in time division multiplex fashion.

2. An instrument in accordance with claim 1,
wherein a state code register (42) for storing and retaining a state code of attack, decay, sustain, release and completion from depression of a key of keyboards to the vanishing of sound is provided within an address calculator (5) for the digital envelope memory (7) to control the read state of the envelope memory (7) by the state code from said state code register (42).

3. An instrument in accordance with claim 2,
wherein selection from the attack state to the decay state, selection from the decay state to the sustain state and selection from the release state to the completion state are performed through the comparison of the value of the multiplexer with the given address value of the digital envelope memory (7).

4. An instrument in accordance with claim 2,
wherein when the state code from the state code register (42) is the attack state, the decay state or the release state, the respective state code uses clock-selecting data for selecting a clock for reading the envelope data from the envelope memory (7), whereby the attack time, the decay time and the release time can be optionally varied.

5. An instrument in accordance with claim 2,
wherein when the state code from the state code register (42) is the sustain state, a clock for reading from the envelope memory (7) is in its stop position.

6. An instrument in accordance with claim 1,
wherein a plurality of groups of digital envelope data which are different in amplitude value are stored within the digital envelope memory (7) and a group of envelope data of a desired amplitude value is selectively read from the plurality of groups of digital envelope data obtained through time division multiplex to control the amplitude of the tone signals.

7. An instrument in accordance with claim 1,
wherein the digital envelope memory (7) is composed of a read only memory.

8. An instrument in accordance with anyone of the preceding claims, having digital wave generating means for generating in time division multiplex digital data of a plurality of tone waves, characterized by digital multiplier means for multiplying in time division multiplex the digital data of a plurality of tone waves by the digital data of a plurality of digital envelope data from said envelope generating means.

9. An instrument in accordance with claim 8,
characterized by a digital-to-analog converter for converting the digital data from said multiplier means into analog signals.

Patentansprüche

1. Elektronisches Musikinstrument mit einer Hüllkurven-Erzeugungseinrichtung, bei welchem die Hüllkurven-Erzeugungseinrichtung aus einem Hüllkurvenspeicher (7) zum Speichern von Hüllkurvendaten und

einem Adreßrechner (5) zum Berechnen der Adreßdaten für den Hüllkurven-Speicher (7) im Zeitmultiplexverfahren gebildet ist,
dadurch gekennzeichnet, daß der Hüllkurven-Speicher (7) ein digitaler Speicher ist, daß der Adreßrechner (5) für den Hüllkurven-Speicher (7) einen Lese-/Schreib-Speicher (41-46) mit einer Mehrfachadresse zum Speichern von Parametern (J, Zustandscode, A, D, S, R), welche von einer Steuerungseinrichtung (3) über eine Anfangslade-Schnittstelle (35) abgegeben werden und eine arithmetische Logikschaltung (47-50) umfaßt, die aus wenigstens einem Addierer zum Errechnen der Adreßdaten für den digitalen Hüllkurven-Speicher (7) besteht, um mehrere digitale Hüllkurvendaten von dem digitalen Hüllkurven-Speicher (7) im Zeitmultiplexverfahren zu erhalten.

2. Instrument nach Anspruch 1,
bei welchem ein Statuscoderegister (42) zum Speichern und Behalten eines Statuscodes des Anschlagens, des Nachklingens, des Anhaltens, des Auslösens und des Ausklingens vom Betätigen einer Taste einer Tastatur bis zum Verschwinden eines Tones in einem Adreßrechner (5) für den digitalen Hüllkurven-Speicher (7) zum Steuern des Lesezustandes des Hüllkurvenspeichers (7) durch den Zustandscode aus dem Zustandscoderegister (42) vorgesehen ist.

3. Instrument nach Anspruch 2,
bei welchem die Selektion vom Anstiegszustand zum Nachklingzustand, die Selektion vom Nachklingzustand zum Anhaltezustand und die Selektion vom Auslösezustand zum Ausklingzustand durch den Vergleich des Multiplexer-Wertes mit dem vorgegebenen Adreßwert des digitalen Hüllkurvenspeichers (7) ausgeführt wird.

4. Instrument nach Anspruch 2,
bei welchem, wenn der Zustandscode des Zustandscoderegisters (42) der Anstiegszustand, der Nachklingzustand oder der Auslösezustand ist, der jeweilige Zustandscode Taktselektionsdaten zum Selektieren eines Taktes zum Lesen der Hüllkurvendaten aus dem Hüllkurvenspeicher (7) verwendet, wodurch die Anstiegszeit, die Nachklingzeit und die Auslösezeit optional veränderbar sind.

5. Instrument nach Anspruch 2,
bei welchem, wenn der Statuscode aus dem Statuscoderegister (42) der Anhaltestatus ist, ein Takt zum Lesen des Hüllkurvenspeichers (7) in seiner Stopposition ist.

6. Instrument nach Anspruch 1,
bei welchem mehrere Gruppen digitaler Hüllkurvendaten, welche unterschiedliche Amplitudenwerte aufweisen, in dem digitalen Hüllkurvenspeicher (7) gespeichert sind und eine Gruppe von Hüllkurvendaten mit einem gewünschten Amplitudenwert selektiv aus den Gruppen der digitalen Hüllkurvendaten ausgelesen wird, welche durch Zeitmultiplex erhalten werden, um die Amplitude der Tonsignale zu steuern.

7. Instrument nach Anspruch 1,
bei welchem der digitale Hüllkurvenspeicher (7) aus einem Nur-Lese-Speicher gebildet ist.

8. Instrument nach einem der vorstehenden Ansprüche, mit einer digitalen Wellenerzeugungseinrichtung zum Erzeugen digitaler Zeitmultiplexdaten mehrerer Tonwellen,
gekennzeichnet durch eine digitale Multipliziereinrichtung zum Zeitmultiplex-Multiplizieren der Digitaldaten der Tonwellen mit den Digitaldaten mehrerer digitaler Hüllkurvendaten von der Hüllkurvenerzeugungseinrichtung.

9. Instrument nach Anspruch 8,
gekennzeichnet durch einen Digital-/Analog-Wandler zum Wandeln der Digitaldaten von der Multiplexeinrichtung in analoge Signale.

Revendications

1. Instrument de musique électronique équipé d'un moyen de génération d'enveloppe, dans lequel ledit moyen de génération d'enveloppe est composé d'une mémoire d'enveloppe (7) pour stocker des données d'enveloppe, et un calculateur d'adresse (5) pour calculer des données d'adresse pour la mémoire d'enveloppe (7) dans une forme de multiplexage par partage dans le temps, caractérisé en ce que la mémoire d'enveloppe (7) est une mémoire digitale, en ce que le calculateur d'adresse (5) pour la mémoire d'enveloppe (7) comporte une mémoire lecture/écriture (41-46) ayant une adresse multiple pour stocker des paramètres (J, code d'état, A, D, S, R) fournis par un moyen de commande (3) via une interface de chargement initial (35), et un circuit logique arithmétique (47-50) constitué d'au moins un calculateur par addition pour calculer les données d'adresse pour la mémoire d'enveloppe digitale (7) afin d'obtenir une multitude de données d'enveloppe digitales de la mémoire d'enveloppe digitale (7) dans une forme de multiplexage par partage dans le temps.

2. Instrument selon la revendication 1, dans lequel un registre de code d'état (42) pour stocker et retenir un code d'état d'attaque, de déclin, de maintien, de libération et d'achèvement depuis l'enfoncement d'une touche des claviers jusqu'à la disparition du son est prévu à l'intérieur d'un calculateur d'adresse (5) pour que la mémoire d'enveloppe digitale (7) commande l'état de lecture de la mémoire d'enveloppe (7) par le code d'état dudit registre de code d'état (42).

3. Instrument selon la revendication 2, dans lequel la sélection depuis l'état d'attaque jusqu'à l'état de déclin, la sélection depuis l'état de déclin jusqu'à l'état de maintien et la sélection depuis l'état libération jusqu'à l'état d'achèvement sont effectuées par comparaison de la valeur du multiplexeur avec la valeur d'adresse donnée de la mémoire d'enveloppe digitale (7).

4. Instrument selon la revendication 2, dans lequel, lorsque le code d'état du registre de code d'état (42) est l'état d'attaque, l'état de déclin ou l'état de libération, le code d'état respectif utilise des données de sélection d'horloge pour sélectionner une horloge pour lire les données d'enveloppe de la mémoire d'enveloppe (7), d'où il résulte que le temps d'attaque, le temps de déclin et le temps de libération peuvent être éventuellement variés.

5. Instrument selon la revendication 2, dans lequel, lorsque le code d'état du registre de code d'état (42) est l'état de maintien, une horloge pour lire la mémoire d'enveloppe (7) est dans sa position d'arrêt.

6. Instrument selon la revendication 1, dans lequel une multitude de groupes de données d'enveloppe digitales qui sont différentes en valeur d'amplitude sont stockées à l'intérieur de la mémoire d'enveloppe digitale (7) et un groupe de données d'enveloppe d'une valeur d'amplitude désirée est lue sélectivement à partir d'une multitude de qroupes de données d'enveloppe digitales obtenues par multiplexage par partage dans le temps pour commander l'amplitude des signaux sonores.

7. Instrument selon la revendication 1, dans lequel la mémoire d'enveloppe digitale (7) est composée d'une mémoire morte.

8. Instrument selon l'une quelconque des revendications précédentes, ayant un moyen de génération d'ondes digital pour générer des données digitales en multiplexage par partage dans le temps d'une multitude d'ondes sonores, caractérisé par un moyen de multiplicateur digital pour multiplier les données digitales en multiplexage par partage dans le temps d'une multitude d'ondes sonores par les données digitales d'une multitude de données d'enveloppe digitales dudit moyen de génération d'enveloppe.

9. Instrument selon la revendication 8, caractérisé par un convertisseur digital-vers-analogique pour convertir les données digitales dudit moyen de multiplicateur en signaux analogiques.

Fig. 1

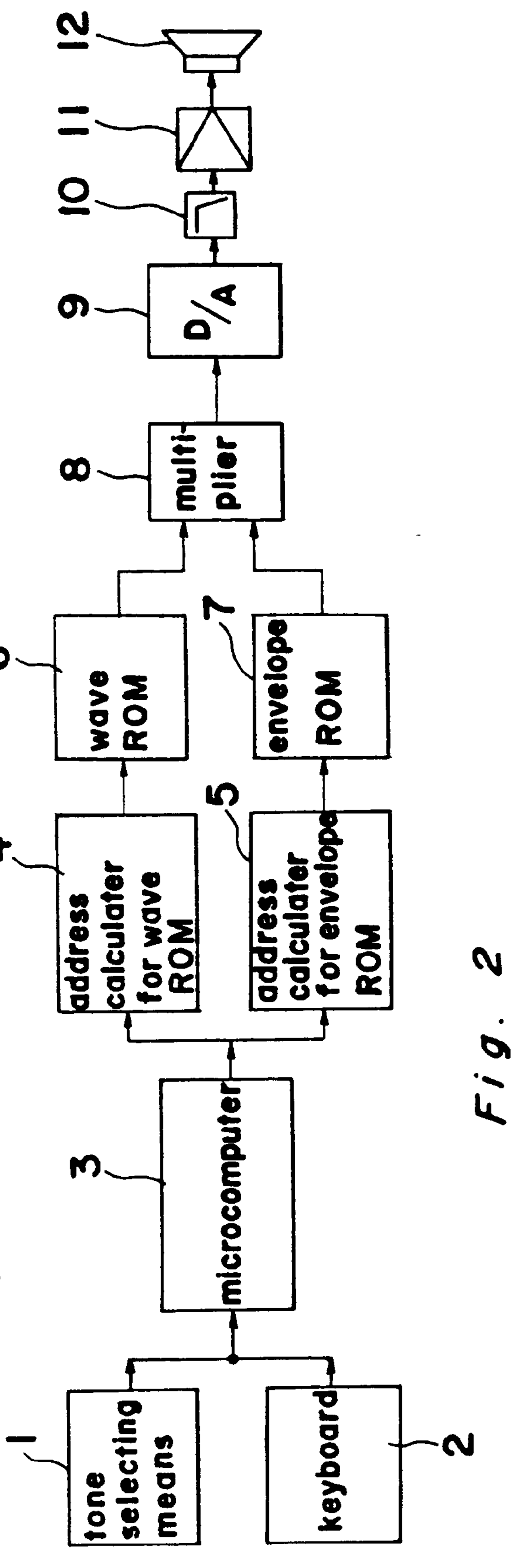

1
tone selecting means
2
keyboard
3
microcomputer
4
address calculater for wave ROM
5
address calculater for envelope ROM
6
wave ROM
7
envelope ROM
8
multi-plier
9
D/A
10
11
12

Fig. 2

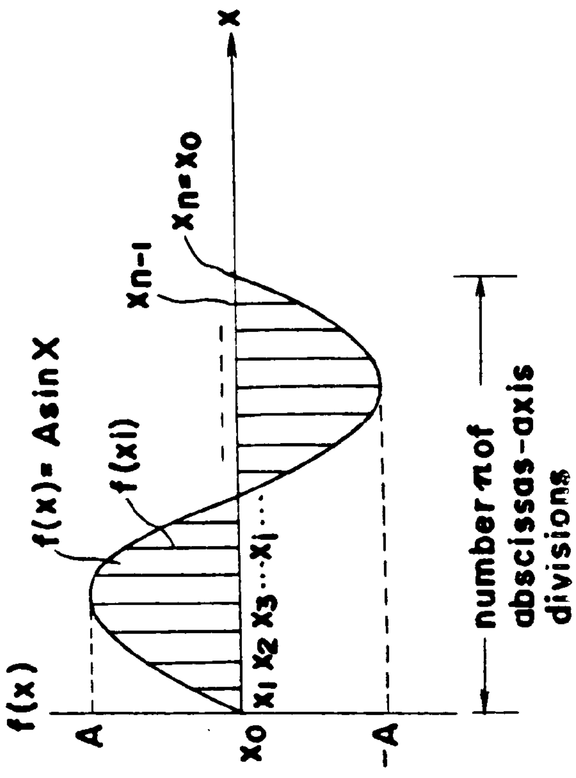

f(x)
A
x0
-A
f(x)= AsinX
f(xi)
x1 x2 x3 ··· xi ···
xn-1
xn=x0
x
number n of abscissas-axis divisions

Fig. 3

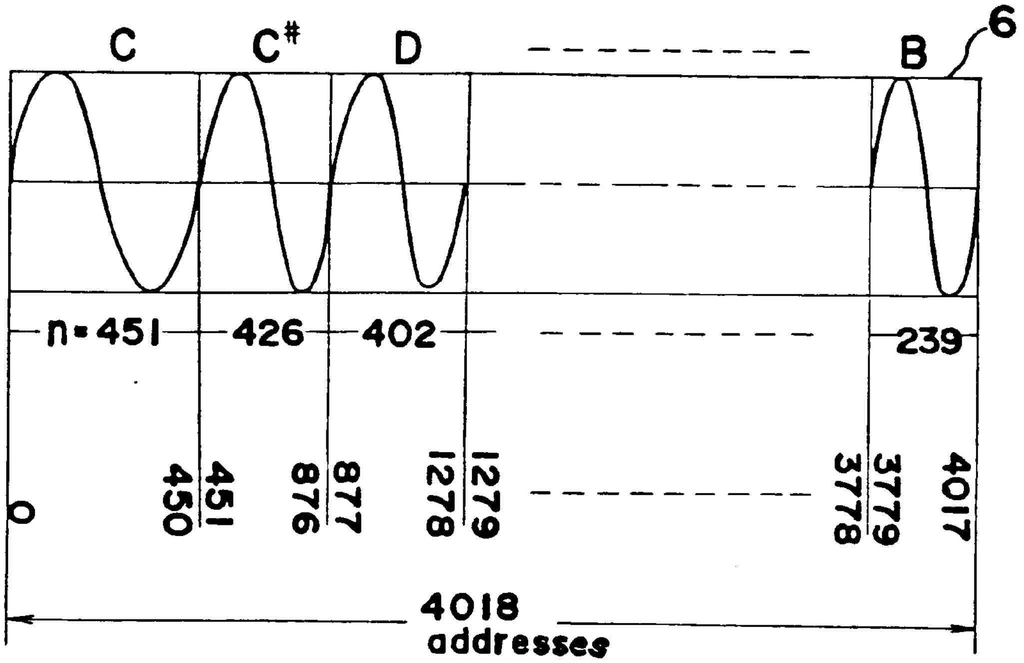


Fig. 4

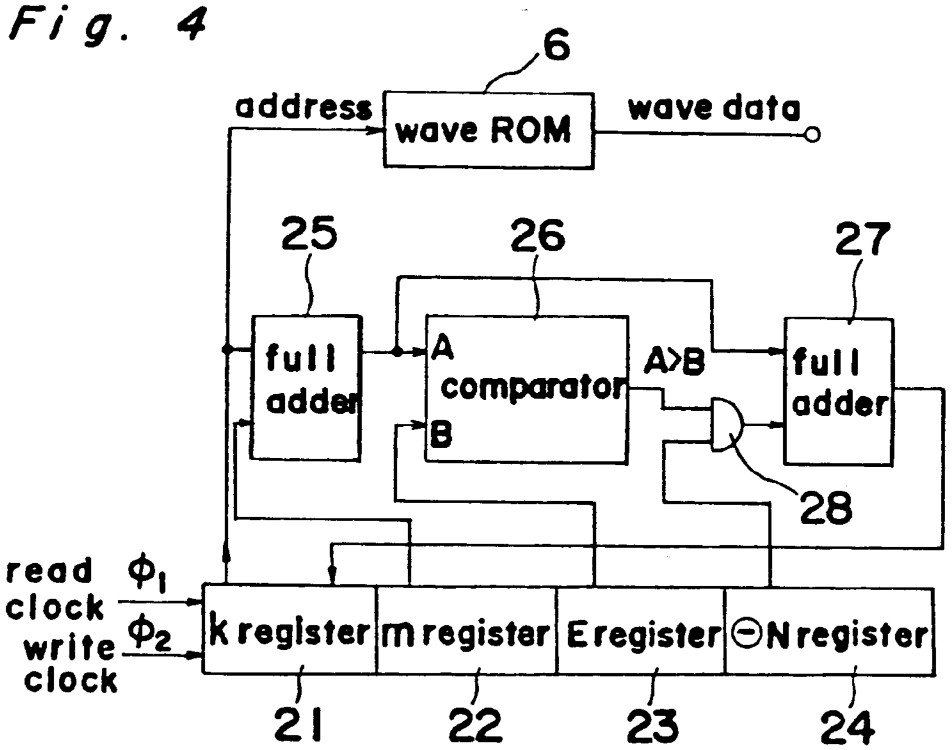


Fig. 5

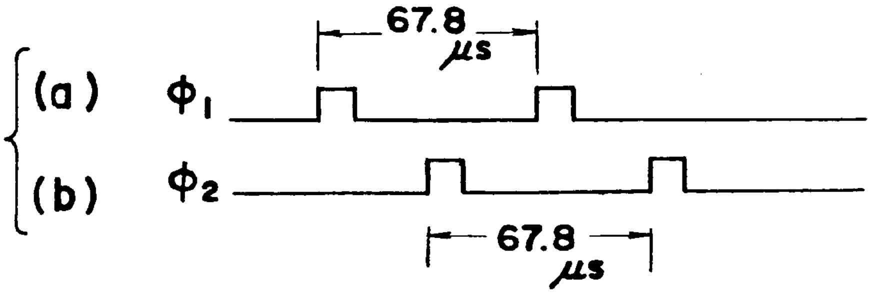


Fig. 6

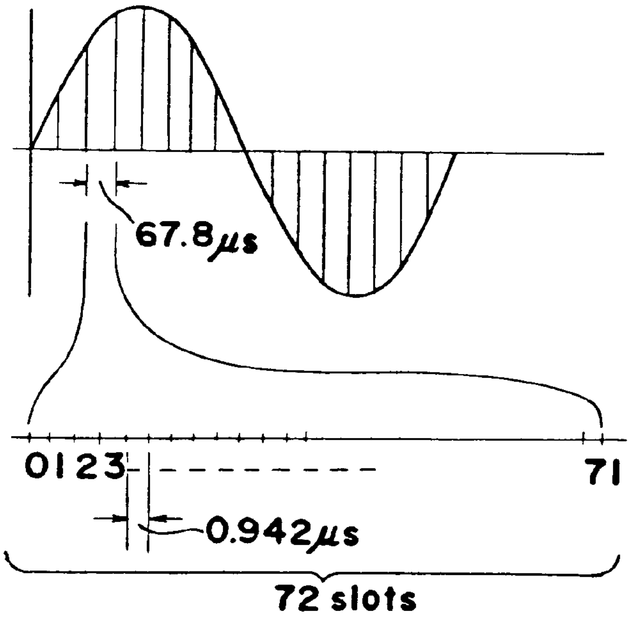

67.8μs
0 1 2 3
71
0.942μs
72 slots

Fig. 7

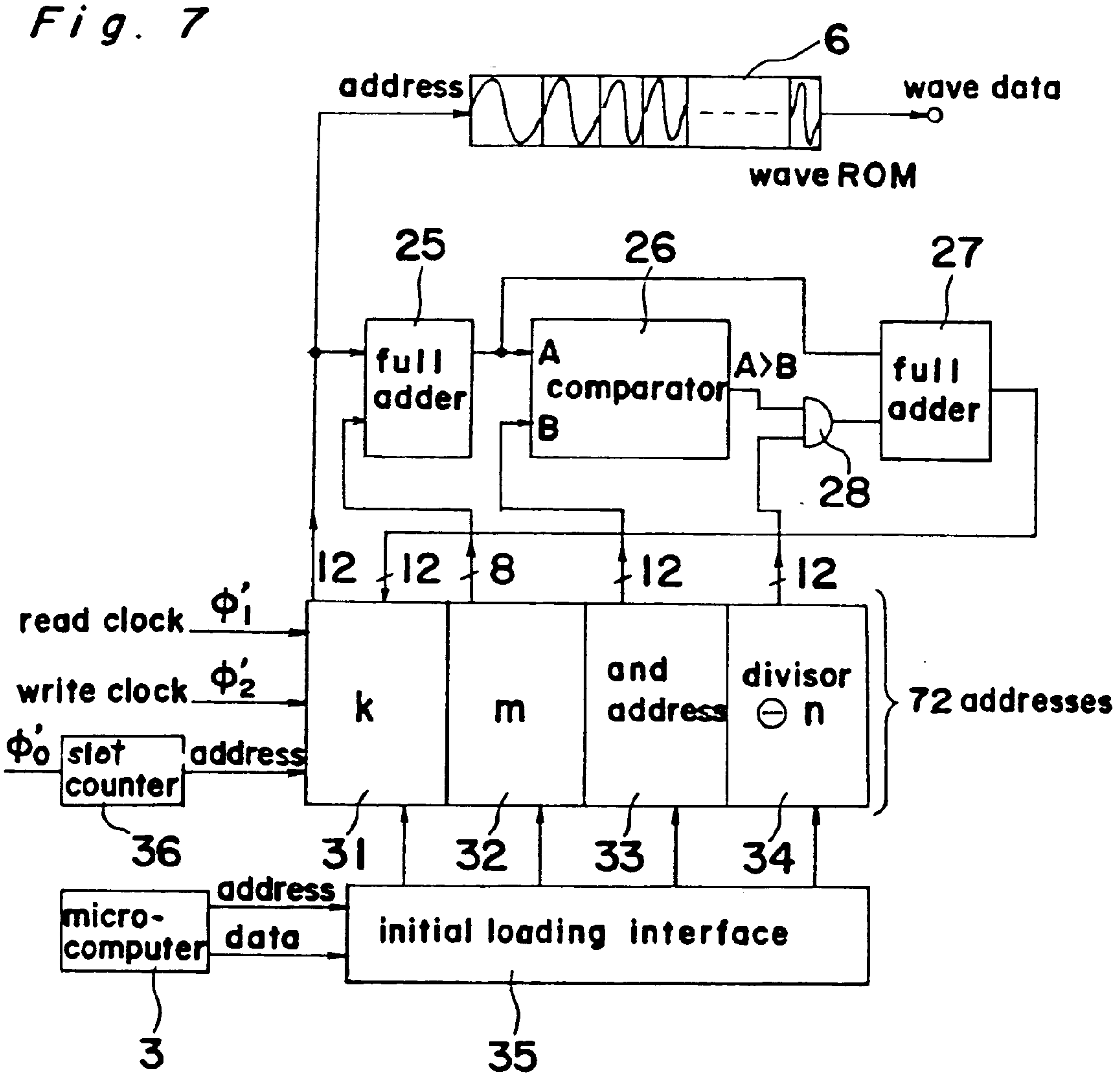

6
address
wave data
wave ROM
25
26
27
full adder
A
comparator
B
A>B
full adder
28
12
12
8
12
12
read clock ϕ'_1
write clock ϕ'_2
ϕ'_0
slot counter
address
k
m
and address
divisor ⊖ n
72 addresses
36
31
32
33
34
address
micro-computer
data
initial loading interface
3
35

Fig. 8

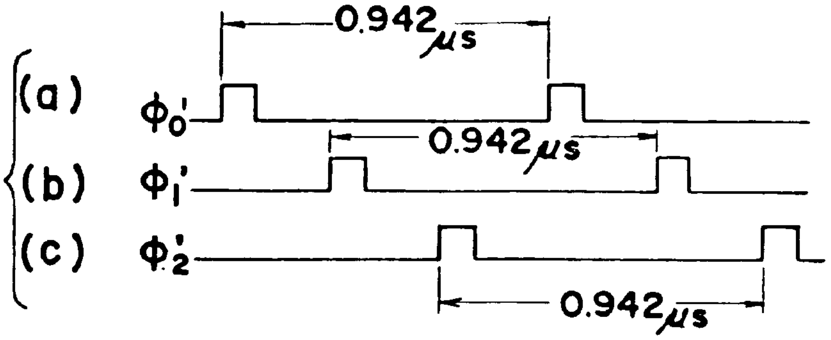


Fig. 9

construction of envelope ROM 7

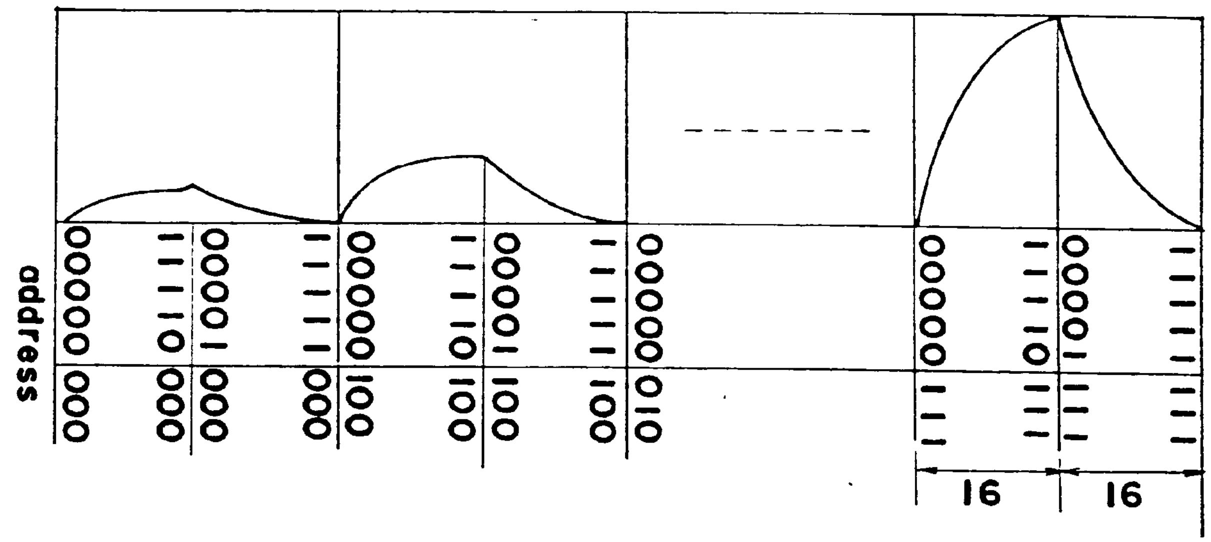


Fig. 10

address of envelope ROM

D7	D6	D5	D4	D3	D2	D1	D0

Fig. 11

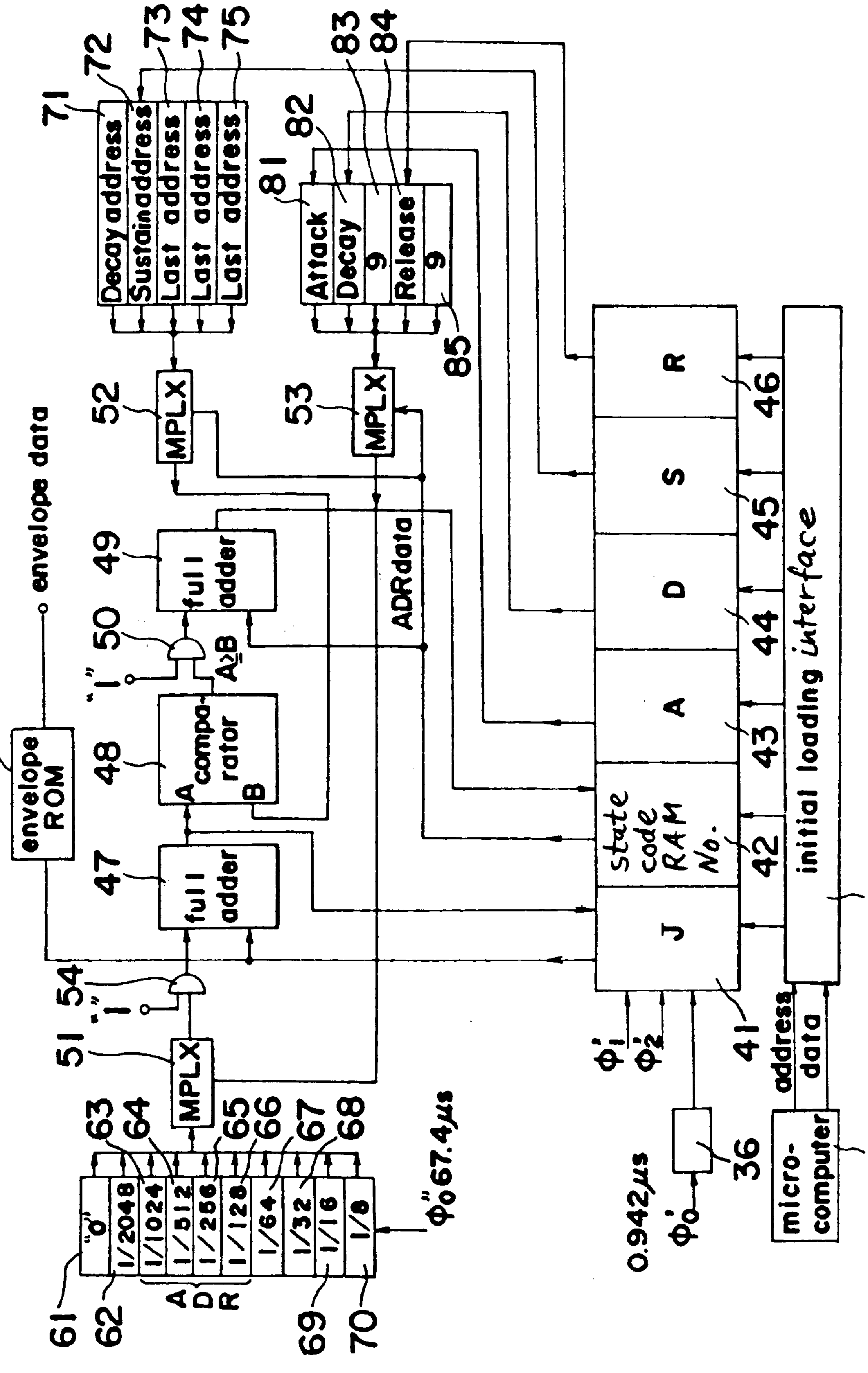

7
envelope ROM
envelope data
47
full adder
48
comparator
A
B
A≥B
49
full adder
50
"1"
54
"1"
51
MPLX
52
MPLX
53
MPLX
ADRdata
71
72
73
74
75
Decay address
Sustain address
Last address
Last address
Last address
81
82
83
84
85
Attack
Decay
9
Release
9
61
62
63
64
65
66
67
68
69
70
"0"
1/2048
1/1024
1/512
1/256
1/128
1/64
1/32
1/16
1/8
A
D
R
Φ"0 67.4μs
41
J
state code RAM No.
42
43
A
44
D
45
S
46
R
35
initial loading interface
Φ'1
Φ'2
36
0.942μs
Φ'0
address
data
3
micro-computer

Fig. 12

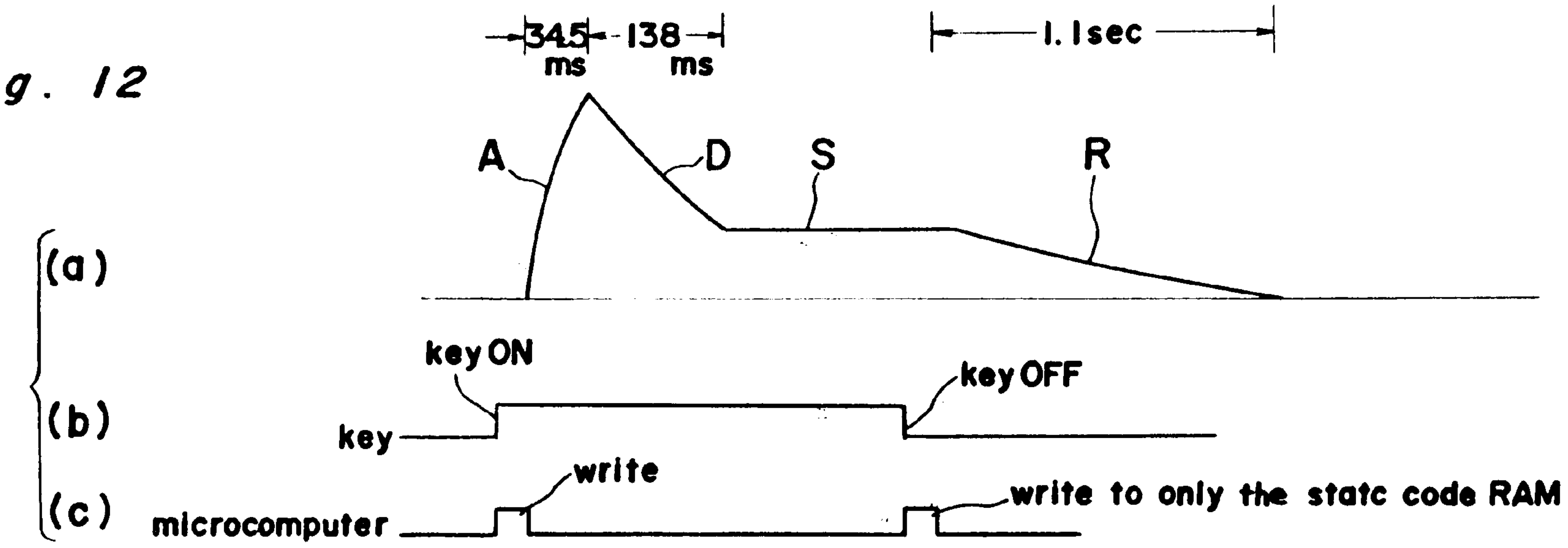

345 ms
138 ms
1.1sec
A
D
S
R
(a)
(b)
(c)
key ON
key OFF
key
write
microcomputer
write to only the statc code RAM

Fig. 13

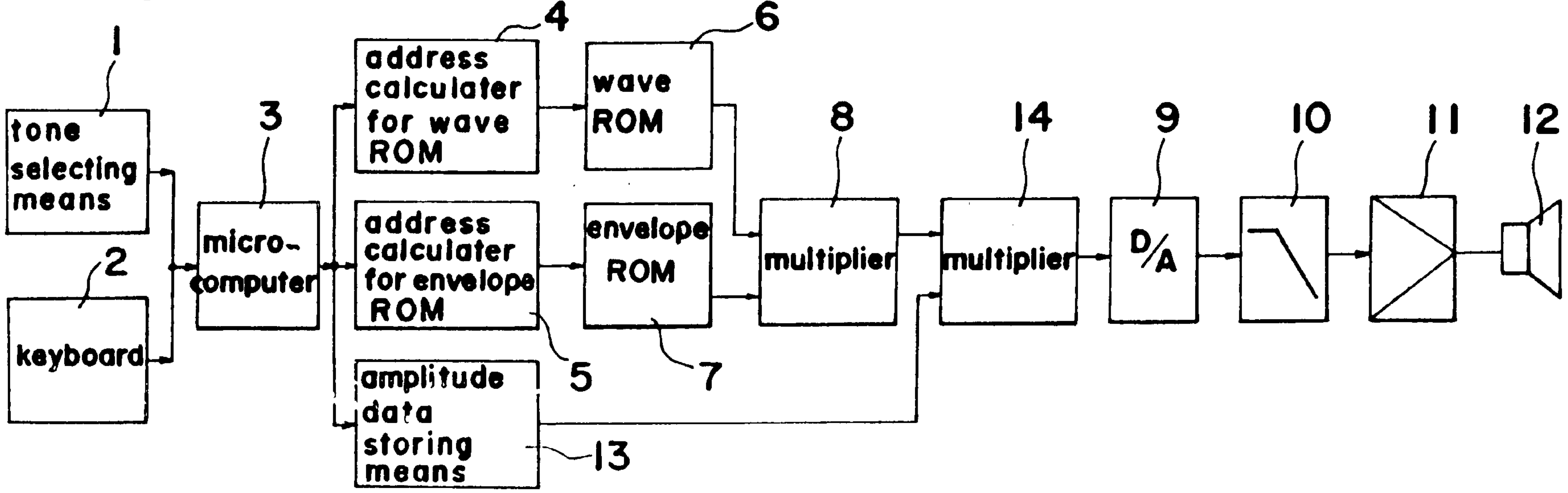

1
tone selecting means
2
keyboard
3
micro-computer
4
address calculater for wave ROM
5
address calculater for envelope ROM
13
amplitude data storing means
6
wave ROM
7
envelope ROM
8
multiplier
14
multiplier
9
D/A
10
11
12

Fig. 14

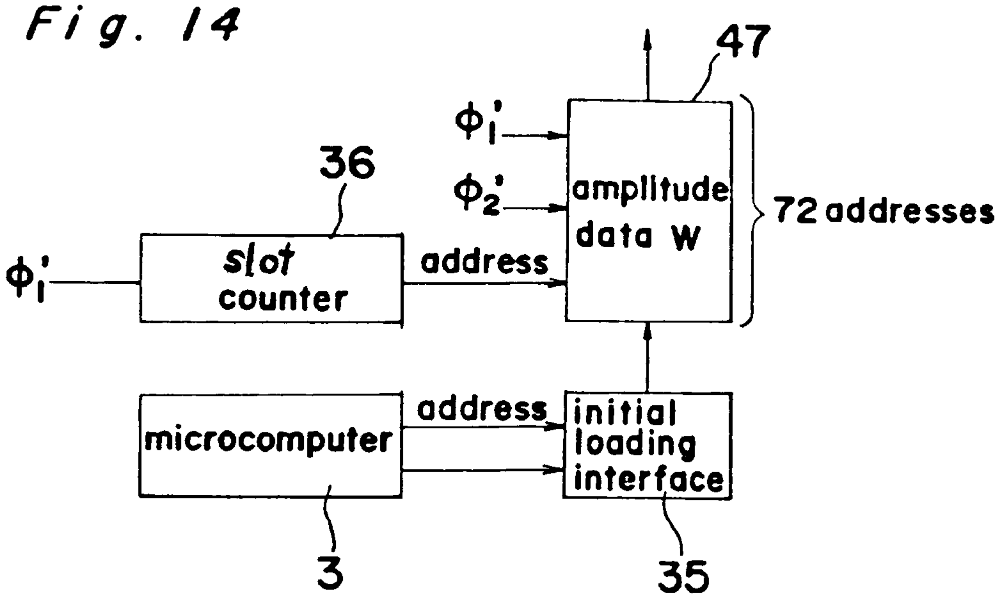

47
Φ1'
Φ2'
amplitude data W
72 addresses
36
slot counter
Φ1'
address
address
microcomputer
initial loading interface
3
35

Fig. 15

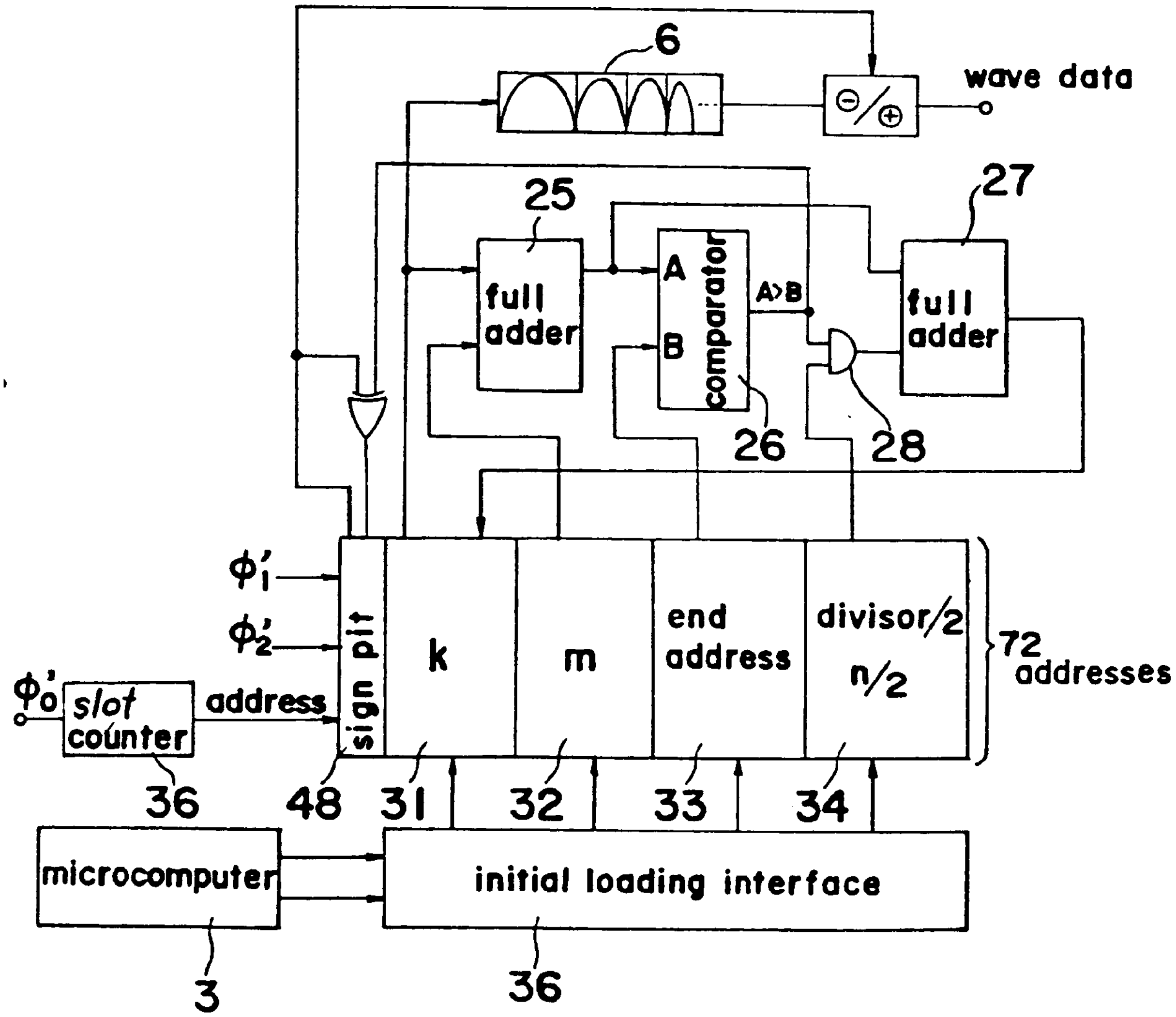

6
wave data
25
27
full adder
A
B
comparator
A>B
full adder
26
28
Φ1'
Φ2'
Φ0'
slot counter
address
sign bit
k
m
end address
divisor/2 n/2
72 addresses
36
48
31
32
33
34
microcomputer
initial loading interface
3
36

Fig. 16

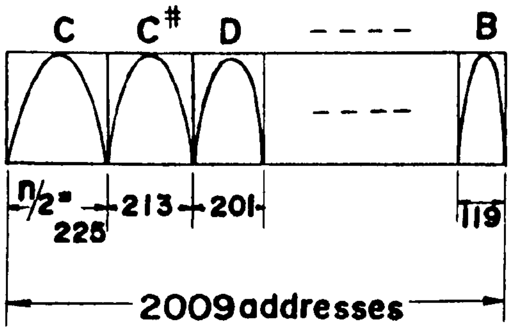
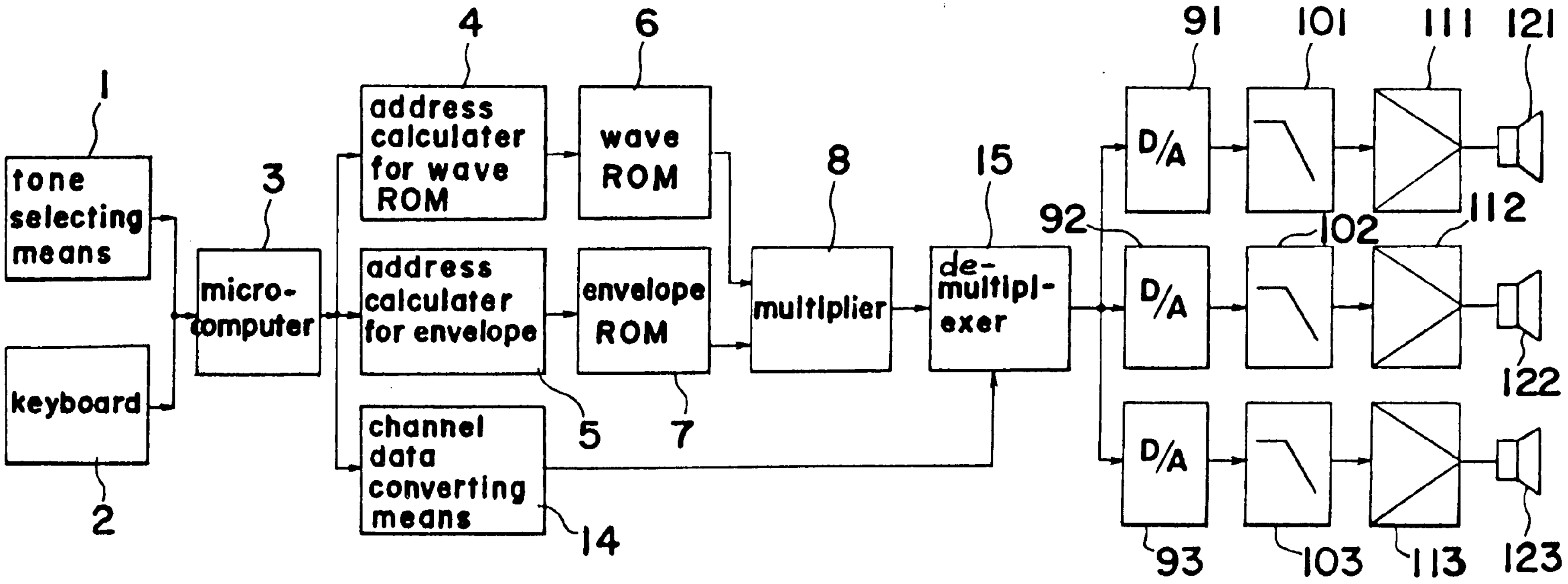

C
C#
D
- - - -
B
n/2= 225
213
201
119
2009addresses

Fig. 17


1
tone selecting means
2
keyboard
3
micro-computer
4
address calculater for wave ROM
5
address calculater for envelope
14
channel data converting means
6
wave ROM
7
envelope ROM
8
multiplier
15
de-multipl-exer
91
92
93
D/A
D/A
D/A
101
102
103
111
112
113
121
122
123