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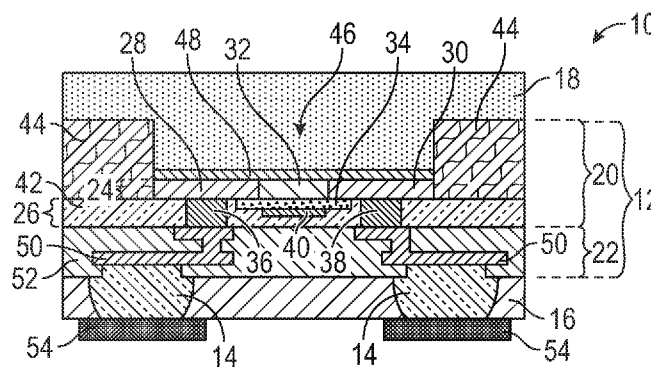


FIG. 1

(57) Abstract: The disclosure relates to a radio frequency device that includes a device region with a back-end-of-line portion and a front-end-of-line portion, first bump structures, a first mold compound, and a second mold compound. The FEOL portion includes an active layer, a contact layer, and isolation sections. The active layer and the isolation sections reside over the contact layer, and the active layer is surrounded by the isolation sections. The BEOL portion is formed underneath the FEOL portion, and the first bump structures and the first mold compound are formed underneath the BEOL portion. Each first bump structure is partially encapsulated by the first mold compound, and electrically coupled to the FEOL portion via connecting layers within the BEOL portion. The second mold compound resides over the active layer without a silicon material, which has a resistivity between 5 Ohm-cm and 30000 Ohm-cm, in between.



***RF SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF***Related Applications

5 **[0001]** This application claims the benefit of provisional patent application serial number 62/692,945, filed July 2, 2018, the disclosure of which is hereby incorporated herein by reference in its entirety.

**[0002]** This application is related to concurrently filed U.S. patent application number \_\_\_\_\_, entitled "RF DEVICES WITH ENHANCED PERFORMANCE  
10 AND METHODS OF FORMING THE SAME," the disclosure of which is hereby incorporated herein by reference in its entirety.

Field of the Disclosure

**[0003]** The present disclosure relates to a radio frequency (RF) device and a  
15 process for making the same, and more particularly to an RF device with enhanced thermal and electrical performance, and a wafer-level packaging process to provide the RF device with enhanced performance.

Background

20 **[0004]** The wide utilization of cellular and wireless devices drives the rapid development of radio frequency (RF) technologies. The substrates on which RF devices are fabricated play an important role in achieving high level performance in the RF technologies. Fabrications of the RF devices on conventional silicon handle substrates may benefit from low cost of silicon materials, a large scale  
25 capacity of wafer production, well-established semiconductor design tools, and well-established semiconductor manufacturing techniques.

**[0005]** Despite the benefits of using conventional silicon handle substrates for the RF device fabrications, it is well known in the industry that the conventional silicon handle substrates may have two undesirable properties for the RF  
30 devices: harmonic distortion and low resistivity values. The harmonic distortion is a critical impediment to achieve high level linearity in the RF devices built over silicon handle substrates. In addition, high speed and high performance

transistors are more densely integrated in RF devices. Consequently, the amount of heat generated by the RF devices will increase significantly due to the large number of transistors integrated in the RF devices, the large amount of power passing through the transistors, and/or the high operation speed of the transistors. Accordingly, it is desirable to package the RF devices in a configuration for better heat dissipation.

**[0006]** To accommodate the increased heat generation of the RF devices and to reduce deleterious harmonic distortion of the RF devices, it is therefore an object of the present disclosure to provide an improved packaging process for enhanced thermal and electrical performance. Further, there is also a need to enhance the performance of the RF devices without increasing the package size.

### Summary

**[0007]** The present disclosure relates to a radio frequency (RF) device with enhanced thermal and electrical performance, and a process for making the same. The disclosed RF device includes a device region, a number of first bump structures, a first mold compound, and a second mold compound. The device region includes a back-end-of-line (BEOL) portion with a number of connecting layers, and a front-end-of-line (FEOL) portion residing over the BEOL portion. The FEOL portion includes an active layer, a contact layer, and isolation sections. Herein, both the active layer and the isolation sections reside over the contact layer. The active layer is surrounded by the isolation sections and does not extend vertically beyond the isolation sections. The first bump structures are formed at a bottom surface of the BEOL portion, and electrically coupled to the FEOL portion via the connecting layers within the BEOL portion. The first mold compound is formed over the bottom surface of the BEOL portion and partially encapsulates each first bump structure, such that a bottom portion of each first bump structure is not covered by the first mold compound. The second mold compound resides over the active layer of the FEOL portion without a silicon material, which has a resistivity between 5 Ohm-cm and 30000 Ohm-cm, in between.

**[0008]** In one embodiment of the RF device, a portion of the second mold compound resides over the isolation sections.

**[0009]** In one embodiment of the RF device, the isolation sections extend vertically beyond a top surface of the active layer to define an opening within the isolation sections and over the active layer, wherein the second mold compound  
5 fills the opening.

**[0010]** According to another embodiment, the RF device further includes a passivation layer directly over the top surface of the active layer and within the opening. Herein, the passivation layer is formed of silicon dioxide, silicon nitride,  
10 or combination of both, and in contact with the second mold compound.

**[0011]** According to another embodiment, the RF device further includes an interfacial layer directly over the top surface of the active layer and within the opening. Herein, the interfacial layer is formed of silicon germanium (SiGe) and directly connected to the second mold.

**[0012]** In one embodiment of the RF device, the second mold compound is in contact with the top surface of the active layer.  
15

**[0013]** In one embodiment of the RF device, a top surface of each isolation section and a top surface of the active layer are coplanar. Herein, the second mold compound resides over both the active layer and the isolation sections.  
20

**[0014]** According to another embodiment, the RF device further includes a number of second bump structures. Each second bump structure is in contact with a corresponding first bump structure, and protrudes from the first mold compound.  
25

**[0015]** In one embodiment of the RF device, the second bump structures are formed from solder paste, conductive epoxy, or reflowable metals.

**[0016]** In one embodiment of the RF device, the first bump structures are solder balls or copper pillars.

**[0017]** In one embodiment of the RF device, the first mold compound is formed from a same material as the second mold compound. Herein, the first  
30 mold compound and the second mold compound have a thermal conductivity

greater than 1 W/m·K, and a dielectric constant less than 8 or a dielectric constant between 3 and 5.

**[0018]** In one embodiment of the RF device, the first mold compound and the second mold compound are formed from different materials.

5 **[0019]** In one embodiment of the RF device, the first mold compound is transparent.

**[0020]** In one embodiment of the RF device, the FEOL portion is configured to provide at least one of a switch field effect transistor (FET), a diode, a capacitor, a resistor, and an inductor.

10 **[0021]** According to an exemplary process, a device wafer having a number of device dies is firstly provided. Herein, each device die includes first bump structures and a device region with a BEOL portion and a FEOL portion over the BEOL portion. The FEOL portion includes an active layer, a contact layer, and isolation sections. Herein, the active layer and the isolation sections reside over  
15 the contact layer, the isolation sections surround the active layer, and the active layer does not extend vertically beyond the isolation sections. A combination of a bottom surface of each BEOL portion forms a bottom surface of the device wafer. The first bump structures are formed at the bottom surface of each BEOL portion. In addition, an interfacial layer formed of SiGe, is directly over the active layer of  
20 each device die. A silicon handle substrate is directly over each interfacial layer. Next, a first mold compound is applied over the bottom surface of the device wafer to encapsulate the first bump structures of each device die. The silicon handle substrate is then removed completely. A second mold compound is formed over the active layer of each device die from where the silicon handle  
25 substrate is removed. There is no silicon material residing between the second mold compound and each active layer. After the second mold compound is formed, the first mold compound is thinned until exposing a bottom portion of each first bump structure.

**[0022]** According to another embodiment, the exemplary process further  
30 includes removing the interfacial layer before applying the second mold

compound. Herein the active layer of each device die is in contact with the second mold compound after the second mold compound is applied.

**[0023]** According to another embodiment, the exemplary process further includes removing the interfacial layer and applying a passivation layer directly

5 over the active layer of each device die before applying the second mold compound. Herein, the passivation layer is formed of silicon dioxide, silicon nitride, or combination of both. The passivation layer is in contact with the second mold compound after the second mold compound is applied.

**[0024]** According to another embodiment, the exemplary process further

10 includes forming a number of second bump structures after thinning the first mold compound. Herein, each second bump structure is in contact with an exposed bottom portion of a corresponding first bump structure, and protrudes from the first mold compound.

**[0025]** According to another embodiment, the exemplary process further

15 includes forming at least one window component at the periphery of the bottom surface of the device wafer before applying the first mold compound. Herein, the at least one window component is encapsulated by the first mold compound after the first mold compound is applied.

**[0026]** In one embodiment of the exemplary process, the at least one window

20 component is taller than each first bump structure, such that the least one window component is exposed before the first bump structures during the thinning process.

**[0027]** In one embodiment of the exemplary process, providing the device

25 epitaxial layer, a common interfacial layer over the common silicon epitaxial layer, and the silicon handle substrate over the common interfacial layer. The common interfacial layer is formed of SiGe. A complementary metal-oxide-

semiconductor (CMOS) process is then performed to provide a precursor wafer that includes a number of device regions. Herein, the isolation sections extend

30 through the common silicon epitaxial layer and the common interfacial layer, and extend into the silicon handle substrate, such that the common interfacial layer

separates into a number of individual interfacial layers, and the common silicon epitaxial layer separates into a number of individual silicon epitaxial layers. Each active layer of the device regions is formed from a corresponding individual silicon epitaxial layer. Each individual interfacial layer directly resides over a top surface of a corresponding active layer, and the silicon handle substrate resides directly over the individual interfacial layers. Next, the first bump structures are formed at the bottom surface of each BEOL portion to complete the device dies from the device regions.

**[0028]** In one embodiment of the exemplary process, providing the device wafer starts with providing a Si-SiGe-Si wafer that includes a common silicon epitaxial layer, a common interfacial layer over the common silicon epitaxial layer, and the silicon handle substrate over the common interfacial layer. The common interfacial layer includes SiGe, and has a number of interfacial layers that are connected. A CMOS process is then performed to provide a precursor wafer that includes a number of device regions. Herein, the isolation sections extend through the common silicon epitaxial layer and extend into the common interfacial layer, such that the common silicon epitaxial layer separates into a number of individual silicon epitaxial layers and the interfacial layers remain connected. Each active layer of the device regions is formed from a corresponding individual silicon epitaxial layer. Each interfacial layer directly resides over a top surface of a corresponding active layer, and the silicon handle substrate remains directly over the common interfacial layer. Next, the first bump structures are formed at the bottom surface of each BEOL portion to complete the device dies from the device regions.

**[0029]** Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

### Brief Description of the Drawing Figures

**[0030]** The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

5 **[0031]** Figure 1 shows an exemplary radio frequency (RF) device with enhanced thermal and electrical performance according to one embodiment of the present disclosure.

**[0032]** Figures 2-13 provide an exemplary wafer-level packaging process that illustrates steps to fabricate the exemplary RF device shown in Figure 1.

10 **[0033]** It will be understood that for clear illustrations, Figures 1-13 may not be drawn to scale.

### Detailed Description

**[0034]** The embodiments set forth below represent the necessary information  
15 to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that  
20 these concepts and applications fall within the scope of the disclosure and the accompanying claims.

**[0035]** It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from  
25 another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

**[0036]** It will be understood that when an element such as a layer, region, or  
30 substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements

may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

**[0037]** Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

**[0038]** The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

**[0039]** Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further

understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

5 **[0040]** With the looming shortage of conventional radio frequency silicon on insulator (RFSOI) wafers expected in the coming years, alternative technologies are being devised to get around the need for high resistivity using silicon wafers, the trap rich layer formation, and Smart-Cut SOI wafer process. One of these alternative technologies is based on the use of a silicon germanium (SiGe)  
10 interfacial layer instead of a buried oxide layer (BOX) between a silicon substrate and a silicon epitaxial layer, however, which will also suffer from the deleterious distortion effects due to the silicon substrate, similar to what is observed in an RFSOI technology. The present disclosure, which relates to a radio frequency (RF) device with enhanced thermal and electrical performance, and a wafer-level  
15 packaging process for making the same, is based on this Si-SiGe-Si structure without deleterious distortion effects from the silicon substrate.

**[0041]** Figure 1 shows an exemplary RF device 10 formed from a Si-SiGe-Si wafer (processing details are described in following paragraphs) according to one embodiment of the present disclosure. For the purpose of this illustration, the  
20 exemplary RF device 10 includes a device region 12, first bump structures 14, a first mold compound 16, and a second mold compound 18.

**[0042]** In detail, the device region 12 includes a front-end-of-line (FEOL) portion 20 and a back-end-of-line (BEOL) portion 22 underneath the FEOL portion 20. In one embodiment, the FEOL portion 20 is configured to provide a  
25 switch field-effect transistor (FET), and includes an active layer 24 and a contact layer 26. Herein, the active layer 24 has a source 28, a drain 30, and a channel 32 between the source 28 and the drain 30. The source 28, the drain 30, and the channel 32 are formed from a same silicon epitaxial layer. The contact layer 26 is formed underneath the active layer 24 and includes a gate structure 34, a source  
30 contact 36, a drain contact 38, and a gate contact 40. The gate structure 34 may be formed of silicon oxide, and extends horizontally underneath the channel 32

(from underneath the source 28 to underneath the drain 30). The source contact 36 is connected to and under the source 28, the drain contact 38 is connected to and under the drain 30, and the gate contact 40 is connected to and under the gate structure 34. An insulating material 42 may be formed around the source contact 36, the drain contact 38, the gate structure 34, and the gate contact 40 to electrically separate the source 28, the drain 30, and the gate structure 34. In different applications, the FEOL portion 20 may have different FET configurations or provide different device components, such as a diode, a capacitor, a resistor, and/or an inductor.

10 **[0043]** In addition, the FEOL portion 20 also includes isolation sections 44, which reside over the insulating material 42 of the contact layer 26 and surround the active layer 24. The isolation sections 44 are configured to electrically separate the RF device 10, especially the active layer 24, from other devices formed in a common wafer (not shown). Herein, the isolation sections 44 may extend from a top surface of the contact layer 26 and vertically beyond a top surface of the active layer 24 to define an opening 46 that is within the isolation sections 44 and over the active layer 24. The second mold compound 18 fills the opening 46 and may extend over the isolation sections 44. The isolation sections 44 may be formed of silicon dioxide, which may resist etching chemistries such as potassium hydroxide (KOH), sodium hydroxide (NaOH), and acetylcholine (ACH).

20 **[0044]** In some applications, the RF device 10 may further include a passivation layer 48, which is formed of silicon dioxide, silicon nitride, or combination of both, directly over the top surface of the active layer 24 and within the opening 46. As such, the second mold compound 18 is directly over the passivation layer 48. The passivation layer 48 is configured to terminate surface bonds of the active layer 24, which may be responsible for unwanted leakage. The passivation layer may also serve as a barrier and is configured to protect the active layer 24 from moisture or ionic contamination. If the passivation layer 48 is omitted, the second mold compound 18 may be in contact with the top surface of the active layer 24. In some applications, the RF device 10 may further include

an interfacial layer (described in the following paragraphs and not shown herein), which is formed of SiGe, directly over the top surface of the active layer 24 and within the opening 46. As such, the second mold compound 18 may be directly over the interfacial layer. The interfacial layer is from the Si-SiGe-Si wafer (processing details are described in following paragraphs), which is used to fabricate the RF device 10. If the interfacial layer is omitted, the second mold compound 18 may be in contact with the top surface of the active layer 24. Notice that, regardless of the passivation layer 48 or the interfacial layer, silicon crystal, which has no germanium content, does not exist between the second mold compound 18 and the top surface of the active layer 24. Both the passivation layer 48 and the interfacial layer are silicon alloy.

**[0045]** Further, in some applications, a top surface of each isolation section 44 and the top surface of the active layer 24 are coplanar (not shown), and the opening 46 is omitted. The second mold compound 18 resides over both the active layer 24 and the isolation sections 44 of the FEOL portion 20. Note that the active layer 24 is never vertically beyond the isolation sections 44.

**[0046]** The BEOL portion 22 is underneath the FEOL portion 20 and includes multiple connecting layers 50 formed within dielectric layers 52. The first bump structures 14 are formed at a bottom surface of the BEOL portion 22, and electrically coupled to the FEOL portion 20 (the source contact 36 and the drain contact 38 in this illustration) via the connecting layers 50 of the BEOL portion 22. The first mold compound 16 is formed underneath the BEOL portion 22 and encapsulates sides of each first bump structure 14, such that a bottom portion of each first bump structure 14 is not covered by the first mold compound 16.

**[0047]** Herein, the first bump structures 14 do not protrude from a bottom surface of the first mold compound 16. In some applications, it would be desirable to have protruding structures at the bottom surface of the RF device 10 to facilitate and improve the reliability of die attaching (to the printed circuit board) operations. Therefore, the RF device 10 may further include a number of second bump structures 54. Each second bump structure 54 is in contact with a corresponding first bump structure 14, and protrudes from the bottom surface of

the first mold compound 16. The first bump structures 14 may be solder balls or copper pillars. The second bump structures 54 may be formed from solder paste, conductive epoxy, or reflowable metals.

**[0048]** The heat generated in the device region 12 may travel upward to a bottom portion of the second mold compound 18, which is over the active layer 24, and then will pass downward through the device region 12 and the first bump structures 14, which will dissipate the heat. Further, the heat generated in the device region 12 may also travel directly through the first mold compound 16 to be conducted. It is therefore highly desirable to have high thermal conductivities of both the first and second mold compounds 16 and 18. The first mold compound 16 and the second mold compound 18 may have a thermal conductivity greater than 1 W/m·K, or greater than 10 W/m·K. In addition, the first mold compound 16 and the second mold compound 18 may have a low dielectric constant less than 8, or between 3 and 5 to yield low RF coupling. The first mold compound 16 may be formed of a same or different material as the second mold compound 18. In one embodiment, both the first mold compound 16 and the second mold compound 18 may be formed of thermoplastics or thermoset polymer materials, such as PPS (poly phenyl sulfide), overmold epoxies doped with boron nitride, alumina, carbon nanotubes, or diamond-like thermal additives, or the like. Further, the first mold compound 16 may be transparent, and may have a thickness between 25  $\mu\text{m}$  and 500  $\mu\text{m}$  (based on the size of the first bump structure 14). A thickness of the second mold compound 18 is based on the required thermal performance of the RF device 10, the device layout, the distance from the first bump structures 14, and as well as the specifics of the package and assembly. The second mold compound 18 may have a thickness between 200  $\mu\text{m}$  and 500  $\mu\text{m}$ .

**[0049]** Figures 2-13 provide an exemplary wafer-level packaging process that illustrates steps to fabricate the exemplary RF device 10 shown in Figure 1. Although the exemplary steps are illustrated in a series, the exemplary steps are not necessarily order dependent. Some steps may be done in a different order

than that presented. Further, processes within the scope of this disclosure may include fewer or more steps than those illustrated in Figures 2-13.

**[0050]** Initially, a Si-SiGe-Si wafer 56 is provided as illustrated in Figure 2. The Si-SiGe-Si wafer 56 includes a common silicon epitaxial layer 58, a common  
5 interfacial layer 60 over the common silicon epitaxial layer 58, and a silicon handle substrate 62 over the common interfacial layer 60. Herein, the common interfacial layer 60, which is formed of SiGe, separates the common silicon epitaxial layer 58 from the silicon handle substrate 62.

**[0051]** Herein, the common silicon epitaxial layer 58 is formed from a device  
10 grade silicon material, which has desired silicon epitaxy characteristics to form electronic devices. The common interfacial layer 60 is formed from an alloy with any molar ratio of Si and Ge. The higher the Ge concentration, the better the etch selectivity between the silicon handle substrate 62 and the common interfacial layer 60, but also the more difficult the epitaxial growth of the common silicon  
15 epitaxial layer 58 becomes. In one embodiment, the common interfacial layer 60 may have a Ge concentration greater than 15% or greater than 25%. The Ge concentration may be uniform throughout the common interfacial layer 60. In some applications, the Ge concentration may be vertically graded (between 1% and 50%) so as to yield the necessary strain relief for the growth of the common  
20 silicon epitaxial layer 58. The silicon handle substrate 62 may consist of conventional low cost, low resistivity, and high dielectric constant silicon. The common silicon epitaxial layer 58 has higher resistivity than the silicon handle substrate 62, and the common silicon epitaxial layer 58 has lower harmonic generation than the silicon handle substrate 62. A thickness of the common  
25 silicon epitaxial layer 58 may be between 700 nm and 2000 nm, a thickness of the common interfacial layer 60 may be between 100 nm and 1000 nm, and a thickness of the silicon handle substrate 62 may be between 200  $\mu\text{m}$  and 500  $\mu\text{m}$ .

**[0052]** Next, a complementary metal-oxide-semiconductor (CMOS) process is performed to the Si-SiGe-Si wafer 56 to provide a precursor wafer 64 with a  
30 number of device regions 12, as illustrated in Figure 3A. For the purpose of this illustration, the FEOL portion 20 of each device region 12 is configured to provide

a switch FET. In different applications, the FEOL portion 20 may have different FET configurations or provide different device components, such as a diode, a capacitor, a resistor, and/ or an inductor.

**[0053]** In this embodiment, the isolation sections 44 of each device region 12 extend through the common silicon epitaxial layer 58 and the common interfacial layer 60, and extend into the silicon handle substrate 62. As such, the common interfacial layer 60 separates into a number of individual interfacial layers 60I, and the common silicon epitaxial layer 58 separates into a number of individual silicon epitaxial layers 58I, each of which is used to form a corresponding active layer 24 in one device region 12.

**[0054]** The top surface of the active layer 24 is in contact with a corresponding interfacial layer 60I. The silicon handle substrate 62 resides over each individual interfacial layer 60I, and portions of the silicon handle substrate 62 may reside over the isolation sections 44. The BEOL portion 22 of the device region 12, which includes at least the multiple connecting layers 50 and the dielectric layers 52, is formed under the FEOL portion 20. Bottom portions of certain connecting layers 50 are exposed through the dielectric layers 52 at the bottom surface of the BEOL portion 22.

**[0055]** In another embodiment, the isolation sections 44 do not extend into the silicon handle substrate 62. Instead, the isolation sections 44 only extend through the common silicon epitaxial layer 58 and extend into the common interfacial layer 60, as illustrated in Figure 3B. Herein, the common interfacial layer 60 remains continuous, and the individual interfacial layers 60I are connected with each other. The common interfacial layer 60 directly resides over the top surface of each active layer 24, and directly resides over a top surface of each isolation section 44. The silicon handle substrate 62 remains over the common interfacial layer 60. Further, the isolation sections 44 may extend through the common silicon epitaxial layer 58 but do not extend into the common interfacial layer 60. The top surface of each isolation section 44 and the top surface of each active layer 24 may be coplanar (not shown). The common interfacial layer 60 is over

each isolation section 44 and each active layer 24, and the silicon handle substrate 62 remains over the common interfacial layer 60.

**[0056]** The first bump structures 14 are then formed at the bottom surface of each BEOL portion 22 to provide a device wafer 66, as depicted in Figure 4. A combination of the bottom surface of each BEOL portion 22 forms a bottom surface of the device wafer 66. The device wafer 66 includes a number of device dies 68, each of which further includes the first bump structures 14 compared to the device region 12. Each first bump structure 14 is in contact with the exposed portion of a corresponding connecting layer 50. Herein, the first bump structures 14 are electrically coupled to the FEOL portion 20 (the source contact 36 and the drain contact 38 in this illustration) via the connecting layers 50 of the BEOL portion 22. The first bump structures 14 may be formed by a solder ball bumping technology or a copper pillar packaging technology. Each first bump structure 14 protrudes from the bottom surface of the BEOL portion 22 between 20  $\mu\text{m}$  and 350  $\mu\text{m}$ .

**[0057]** Next, at least one window component 70 may be formed at the bottom surface of one BEOL portion 22 where the wafer mark(s) (not shown) is/are located, as illustrated in Figure 5. Herein, the wafer mark indicates the key location(s) of a wafer, which will be utilized for alignment in a following singulation and/or an assembly process. In one embodiment, the at least one window component 70 is located at the periphery of the bottom surface of the device wafer 66. The at least one window component 70 may be formed of a transparent material (for instance: transparent silicone material), such that the wafer mark will be seen through the at least one window component 70. In addition, at least one window component 70 may be formed of an easily removable material (for instance: acrylic polymer), such that the wafer mark will be seen after an easy removal of the at least one window component 70 (more details in following discussion). The at least one window component 70 has a height greater than each first bump structure 14 and is not connected to any first bump structure 14. Notice that the at least one window component 70 is optional.

In some applications, forming the at least one window component 70 at the bottom surface of one BEOL portion 22 may be omitted.

**[0058]** The first mold compound 16 is applied over the bottom surface of the device wafer 66 and encapsulates each first bump structure 14 and the at least one window component 70, as illustrated in Figure 6. The first mold compound 16 may be applied by various procedures, such as compression molding, sheet molding, overmolding, transfer molding, dam fill encapsulation, or screen print encapsulation. The first mold compound 16 may have a superior thermal conductivity greater than 1 W/m·K, or greater than 10 W/m·K, and may have a dielectric constant less than 8, or between 3 and 5. The first mold compound 16 may have a thickness between 25 μm and 500 μm. The first mold compound 16 may resist etching chemistries such as KOH, NaOH, and ACH. In some applications, the first mold compound 16 may be formed of a transparent material. As such, there is no need to form the at least one window component 70 at the bottom surface of the BEOL portion 22, because all locations of a wafer may be seen through the first mold compound 16. A curing process (not shown) is then used to harden the first mold compound 16. The curing temperature is between 100 °C and 320 °C depending on which material is used as the first mold compound 16.

**[0059]** After the first mold compound 16 is formed, the silicon handle substrate 62 is selectively removed to provide an etched wafer 72, where the selective removal is stopped on each interfacial layer 60I, as illustrated in Figure 7. If the isolation sections 44 extend vertically beyond the interfacial layers 60I, the removal of the silicon handle substrate 62 will provide the opening 46 over each active layer 24 and within the isolation sections 44. Removing the silicon handle substrate 62 may be provided by chemical mechanical grinding and an etching process with a wet/dry etchant chemistry, which may be TMAH, KOH, NaOH, ACH, or XeF<sub>2</sub>, or provided by the etching process itself. As an example, the silicon handle substrate 62 may be ground to a thinner thickness to reduce the following etching time. An etching process is then performed to completely remove the remaining silicon handle substrate 62. Since the silicon handle

substrate 62 and the interfacial layers 60I have different characteristics, they may have different reactions to a same etching technique (for instance: different etching speeds with a same etchant). Consequently, the etching system is capable of identifying the presence of the interfacial layers 60I, and capable of  
5 indicating when to stop the etching process.

**[0060]** During the removal process, the isolation sections 44 are not removed and thus protect each FEOL portion 20. The first mold compound 16 protects the bottom surface of each BEOL portion 22. Herein, the top surface of each  
10 isolation section 44 and the top surface of each interfacial layer 60I are exposed after the removing process. If the isolation sections 44 extend into the common interfacial layer 60 (as shown in Figure 3B), or the top surface of each isolation section 44 and the top surface of each active layer 24 are coplanar (not shown), only the top surface of the common interfacial layer 60 will be exposed (not shown).

**[0061]** Due to the narrow gap nature of the SiGe material, it is possible that the interfacial layers 60I (or the common interfacial layer 60) may be conducting. The interfacial layer 60I may cause appreciable leakage between the source 28 and the drain 30 of the active layer 24. Therefore, in some applications, such as FET applications, it is desired to also remove the interfacial layers 60I (or the  
20 common interfacial layer 60), as illustrated in Figure 8. The interfacial layers 60I may be removed by the same etching process used to remove the silicon handle substrate 62, or may be removed by another etching process, such as HCl dry etch systems. If the interfacial layer 60I is thin enough, it may be completely depleted and may not cause any appreciable leakage between the source 28  
25 and the drain 30 of the FEOL portion 20. In that case, the interfacial layers 60I may be left intact.

**[0062]** In some applications, the passivation layer 48, which may be formed of silicon dioxide, silicon nitride, or combination of both, may be formed directly over the active layer 24 of each FEOL portion 20, as illustrated in Figure 9. If there is  
30 one opening 46 over each active layer 24 and within the isolation sections 44, the passivation layer 48 is within the opening 46. The passivation layer 48 is

configured to terminate the surface bonds at the top surface of the active layer 24, which may be responsible for unwanted leakage. The passivation layer 48 may be formed by CVD dielectric filming or passivating plasma.

**[0063]** The second mold compound 18 is then applied over the etched wafer 72 as illustrated in Figure 10. Herein, the second mold compound 18 fills each opening 46 and is in contact with the passivation layer 48 within the opening 46. In addition, portions of the second mold compound 18 may extend over the isolation sections 44. If there is no passivation layer 48 formed in each opening 46, the second mold compound 18 is in contact with the top surface of each active layer 24 (not shown). If the interfacial layer 60I remains over the top surface of each active layer 24, the second mold compound 18 is in contact with the interfacial layer 60I (not shown). The second mold compound 18 always resides over each active layer 24.

**[0064]** The second mold compound 18 may be applied by various procedures, such as compression molding, sheet molding, overmolding, transfer molding, dam fill encapsulation, and screen print encapsulation. During the molding process of the second mold compound 18, the first mold compound 16 provides mechanical strength and rigidity to the etched wafer 72. A curing process (not shown) is followed to harden the second mold compound 18. The curing temperature is between 100 °C and 320 °C depending on which material is used as the second mold compound 18. After the curing process, the second mold compound 18 may be thinned and /or planarized (not shown).

**[0065]** Next, the first mold compound 16 is thinned to provide a mold device wafer 74 as illustrated in Figure 11. Herein, the first mold compound encapsulates sides of the each first bump structure 14 and the bottom portion of each first bump structure 14 is exposed. In addition, since the at least one window component 70 has a height greater than each first bump structure 14, a bottom portion of the at least one window component 70 is also exposed through the first mold compound 16. The thinning procedure may be done with a mechanical grinding process. In one embodiment, the at least one window component 70 may be formed of a transparent material, such that the wafer mark

indicating the key location(s) of a wafer will be seen through the at least one window component 70. In another embodiment, the at least one window component 70 may be formed of an opaque material, such that the wafer mark indicating the key location(s) of a wafer will not be seen through the at least one window component 70. An extra step of removing the at least one window component 70 is needed to expose the wafer mark indicating the key location(s) of a wafer (not shown).

**[0066]** Further, in some applications, the second bump structures 54 may be formed after the first mold compound 16 is thinned, as illustrated in Figure 12. Each second bump structure 54 is directly connected to a corresponding first bump structure 14, electrically coupled to the corresponding FEOL portion 20, and protrudes from the bottom surface of the first mold compound 16. Finally, the mold device wafer 74 is singulated into individual RF devices 10, as illustrated in Figure 13. The singulating step may be provided by a probing and dicing process at certain isolation sections 44. The individual RF device 10 may be assembled on the PCB using a number of die attaching methods.

**[0067]** Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

## Claims

What is claimed is:

1. An apparatus comprising:
  - 5           • a device region including a back-end-of-line (BEOL) portion and a front-end-of-line (FEOL) portion residing over the BEOL portion, wherein:
    - the BEOL portion comprises a plurality of connecting layers;
    - the FEOL portion comprises an active layer, a contact layer, and isolation sections;
    - 10           • the active layer and the isolation sections reside over the contact layer, and the isolation sections surround the active layer;
    - the active layer does not extend vertically beyond the isolation sections;
    - a plurality of first bump structures formed at a bottom surface of the
    - 15 BEOL portion, wherein the plurality of first bump structures is electrically coupled to the FEOL portion via the plurality of connecting layers;
    - a first mold compound formed over the bottom surface of the BEOL portion and partially encapsulating each of the plurality of first bump structures, wherein a bottom portion of each of the plurality of first bump structures is not
    - 20 covered by the first mold compound; and
    - a second mold compound residing over the active layer of the FEOL portion without a silicon material, which has a resistivity between 5 Ohm-cm and 30000 Ohm-cm, in between.
- 25 2. The apparatus of claim 1 wherein a portion of the second mold compound resides over the isolation sections.
3. The apparatus of claim 1 wherein the isolation sections extend vertically beyond a top surface of the active layer to define an opening within the isolation
- 30 sections and over the active layer, wherein the second mold compound fills the opening.

4. The apparatus of claim 3 further comprising a passivation layer directly over the top surface of the active layer and within the opening, wherein:

- the passivation layer is formed of silicon dioxide, silicon nitride, or combination of both; and
- the second mold compound is in contact with the passivation layer.

5. The apparatus of claim 3 further comprising an interfacial layer directly over the top surface of the active layer and within the opening, wherein:

- the interfacial layer is formed of silicon germanium (SiGe); and
- the second mold compound is in contact with the interfacial layer.

6. The apparatus of claim 3 wherein the second mold compound is in contact with the top surface of the active layer.

7. The apparatus of claim 1 wherein a top surface of each isolation section and a top surface of the active layer are coplanar, wherein the second mold compound resides over both the active layer and the isolation sections.

8. The apparatus of claim 1 further comprising a plurality of second bump structures, wherein each of the plurality of second bump structures is in contact with a corresponding one of the plurality of first bump structures, and protrudes from the first mold compound.

9. The apparatus of claim 8 wherein the plurality of second bump structures are formed from solder paste, conductive epoxy, or reflowable metals.

10. The apparatus of claim 1 wherein the plurality of first bump structures are solder balls or copper pillars.

11. The apparatus of claim 1 wherein the first mold compound is formed from a same material as the second mold compound.

5 12. The apparatus of claim 11 wherein the first mold compound and the second mold compound have a thermal conductivity greater than 1 W/m·K.

13. The apparatus of claim 11 wherein the first mold compound and the second mold compound have a dielectric constant less than 8.

10 14. The apparatus of claim 11 wherein the first mold compound and the second mold compound have a dielectric constant between 3 and 5.

15. The apparatus of claim 1 wherein the first mold compound and the second mold compound are formed from different materials.

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16. The apparatus of claim 1 wherein the first mold compound is transparent.

17. The apparatus of claim 1 wherein the FEOL portion is configured to provide at least one of a switch field-effect transistor (FET), a diode, a capacitor, a resistor, and an inductor.

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18. A method comprising:

- providing a device wafer having a plurality of device dies, wherein:
  - each of the plurality of device dies includes a plurality of first bump structures and a device region with a back-end-of-line (BEOL) portion and a front-end-of-line (FEOL) portion over the BEOL portion;
  - the FEOL portion comprises an active layer, a contact layer, and isolation sections, wherein the active layer and the isolation sections reside over the contact layer, the isolation sections

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surround the active layer, and the active layer does not extend vertically beyond the isolation sections;

- 5 • the plurality of first bump structures are formed at a bottom surface of the BEOL portion, wherein a combination of the bottom surface of each BEOL portion forms a bottom surface of the device wafer;
- an interfacial layer formed of silicon germanium (SiGe) is directly over the active layer of each of the plurality of device dies; and
- 10 • a silicon handle substrate is directly over each interfacial layer;
- applying a first mold compound over the bottom surface of the device wafer to encapsulate the plurality of first bump structures of each of the plurality of device dies;
- 15 • removing the silicon handle substrate completely;
- applying a second mold compound over the active layer of each of the plurality of device dies from where the silicon handle substrate is removed, wherein no silicon material resides between the second mold compound and each active layer; and
- 20 • thinning the first mold compound until exposing a bottom portion of each of the plurality of first bump structures.

19. The method of claim 18 further comprising removing the interfacial layer before applying the second mold compound, wherein the active layer of each of the plurality of device dies is in contact with the second mold compound after the second mold compound is applied.

20. The method of claim 18 further comprising removing the interfacial layer and applying a passivation layer directly over the active layer of each of the plurality of device dies before applying the second mold compound, wherein:

- the passivation layer is formed of silicon dioxide, silicon nitride, or combination of both; and
- the passivation layer is in contact with the second mold compound after the second mold compound is applied.

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21. The method of claim 18 further comprising forming a plurality of second bump structures after thinning the first mold compound, wherein each of the plurality of second bump structures is in contact with the exposed bottom portion of a corresponding first bump structure, and protrudes from the first mold  
10 compound.

22. The method of claim 18 further comprising forming at least one window component at the periphery of the bottom surface of the device wafer before applying the first mold compound, wherein the at least one window component is  
15 encapsulated by the first mold compound after the first mold compound is applied.

23. The method of claim 22 wherein the at least one window component is taller than each of the plurality of first bump structures, such that the least one  
20 window component is exposed before the plurality of first bump structures during the thinning process.

24. The method of claim 18 wherein providing the device wafer comprises:  
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- providing a Si-SiGe-Si wafer that includes a common silicon epitaxial layer, a common interfacial layer over the common silicon epitaxial layer, and the silicon handle substrate over the common interfacial layer, wherein the common interfacial layer is formed of SiGe;
- performing a complementary metal-oxide-semiconductor (CMOS) process to provide a precursor wafer that includes a plurality of device  
30 regions, wherein:

- the isolation sections extend through the common silicon epitaxial layer and the common interfacial layer, and extend into the silicon handle substrate, such that the common interfacial layer separates into a plurality of individual interfacial layers, and the common silicon epitaxial layer separates into a plurality of individual silicon epitaxial layers;
  - each active layer of the plurality of device regions is formed from a corresponding individual silicon epitaxial layer; and
  - each of the plurality of individual interfacial layers directly resides over a top surface of a corresponding active layer, and the silicon handle substrate resides directly over the plurality of individual interfacial layers; and
  - forming the plurality of first bump structures at the bottom surface of each BEOL portion to complete the plurality of device dies from the plurality of device regions.
25. The method of claim 18 wherein providing the device wafer comprises:
- providing a Si-SiGe-Si wafer that includes a common silicon epitaxial layer, a common interfacial layer over the common silicon epitaxial layer, and the silicon handle substrate over the common interfacial layer, wherein:
    - the common interfacial layer comprises SiGe; and
    - the common interfacial layer has a plurality of interfacial layers that are connected;
  - performing a CMOS process to provide a precursor wafer that includes a plurality of device regions, wherein:
    - the isolation sections extend through the common silicon epitaxial layer and extend into the common interfacial layer, such that the common silicon epitaxial layer separates into a plurality of individual silicon epitaxial layers and the plurality of interfacial layers remain connected;

- each active layer of the plurality of device regions is formed from a corresponding individual silicon epitaxial layer; and
- each of the plurality of interfacial layers directly resides over a top surface of a corresponding active layer, and the silicon handle substrate remains directly over the common interfacial layer; and
- forming the plurality of first bump structures at the bottom surface of each BEOL portion to complete the plurality of device dies from the plurality of device regions.

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## AMENDED CLAIMS

received by the International Bureau on 04 November 2019 (04.11.2019)

Claims

What is claimed is:

1. An apparatus comprising:
  - a device region including a back-end-of-line (BEOL) portion and a front-end-of-line (FEOL) portion residing over the BEOL portion, wherein:
    - the BEOL portion comprises a plurality of connecting layers;
    - the FEOL portion comprises an active layer, a contact layer, and isolation sections; and
    - the active layer and the isolation sections reside over the contact layer, wherein the isolation sections surround the active layer and extend vertically beyond a top surface of the active layer to define an opening within the isolation sections and over the active layer;
  - a plurality of first bump structures formed at a bottom surface of the BEOL portion, wherein the plurality of first bump structures is electrically coupled to the FEOL portion via the plurality of connecting layers;
  - a first mold compound formed over the bottom surface of the BEOL portion and partially encapsulating each of the plurality of first bump structures, wherein a bottom portion of each of the plurality of first bump structures is not covered by the first mold compound; and
  - a second mold compound residing over the active layer of the FEOL portion to fill the opening, wherein silicon crystal, which has no germanium, nitrogen, or oxygen content, does not exist between the second mold compound and the active layer.
2. The apparatus of claim 1 wherein a portion of the second mold compound resides over the isolation sections.
3. The apparatus of claim 1 further comprising a passivation layer directly over the top surface of the active layer and within the opening, wherein:

- the passivation layer is formed of silicon dioxide, silicon nitride, or combination of both; and
  - the second mold compound is in contact with the passivation layer.
4. The apparatus of claim 1 further comprising an interfacial layer directly over the top surface of the active layer and within the opening, wherein:
- the interfacial layer is formed of silicon germanium (SiGe); and
  - the second mold compound is in contact with the interfacial layer.
5. The apparatus of claim 1 wherein the second mold compound is in contact with the top surface of the active layer.
6. The apparatus of claim 1 further comprising a plurality of second bump structures, wherein each of the plurality of second bump structures is in contact with a corresponding one of the plurality of first bump structures, and protrudes from the first mold compound.
7. The apparatus of claim 6 wherein the plurality of second bump structures are formed from solder paste, conductive epoxy, or reflowable metals.
8. The apparatus of claim 1 wherein the plurality of first bump structures are solder balls or copper pillars.
9. The apparatus of claim 1 wherein the first mold compound is formed from a same material as the second mold compound.
10. The apparatus of claim 9 wherein the first mold compound and the second mold compound have a thermal conductivity greater than 1 W/m·K.
11. The apparatus of claim 9 wherein the first mold compound and the second mold compound have a dielectric constant less than 8.

12. The apparatus of claim 9 wherein the first mold compound and the second mold compound have a dielectric constant between 3 and 5.
13. The apparatus of claim 1 wherein the first mold compound and the second mold compound are formed from different materials.
14. The apparatus of claim 1 wherein the first mold compound is transparent.
15. The apparatus of claim 1 wherein the FEOL portion is configured to provide at least one of a switch field-effect transistor (FET), a diode, a capacitor, a resistor, and an inductor.
16. A method comprising:
  - providing a device wafer having a plurality of device dies, wherein:
    - each of the plurality of device dies includes a plurality of first bump structures and a device region with a back-end-of-line (BEOL) portion and a front-end-of-line (FEOL) portion over the BEOL portion;
    - the FEOL portion comprises an active layer, a contact layer, and isolation sections, wherein the active layer and the isolation sections reside over the contact layer, the isolation sections surround the active layer, and the active layer does not extend vertically beyond the isolation sections;
    - the plurality of first bump structures are formed at a bottom surface of the BEOL portion, wherein a combination of the bottom surface of each BEOL portion forms a bottom surface of the device wafer;
    - an interfacial layer formed of silicon germanium (SiGe) is directly over the active layer of each of the plurality of device dies; and
    - a silicon handle substrate is directly over each interfacial layer;

- applying a first mold compound over the bottom surface of the device wafer to encapsulate the plurality of first bump structures of each of the plurality of device dies;
- removing the silicon handle substrate completely;
- removing the interfacial layer to expose the active layer of each of the plurality of device dies;
- applying a second mold compound over the active layer of each of the plurality of device dies after the interfacial layer is removed, wherein silicon crystal, which has no germanium, nitrogen, or oxygen content, does not exist between the second mold compound and each active layer; and
- thinning the first mold compound until exposing a bottom portion of each of the plurality of first bump structures.

17. The method of claim 16 wherein the active layer of each of the plurality of device dies is in contact with the second mold compound after the second mold compound is applied.

18. The method of claim 16 further comprising applying a passivation layer directly over the active layer of each of the plurality of device dies before applying the second mold compound, wherein:

- the passivation layer is formed of silicon dioxide, silicon nitride, or combination of both; and
- the passivation layer is in contact with the second mold compound after the second mold compound is applied.

19. The method of claim 16 further comprising forming a plurality of second bump structures after thinning the first mold compound, wherein each of the plurality of second bump structures is in contact with the exposed bottom portion of a corresponding first bump structure, and protrudes from the first mold compound.

20. The method of claim 16 further comprising forming at least one window component at the periphery of the bottom surface of the device wafer before applying the first mold compound, wherein the at least one window component is encapsulated by the first mold compound after the first mold compound is applied.
21. The method of claim 20 wherein the at least one window component is taller than each of the plurality of first bump structures, such that the least one window component is exposed before the plurality of first bump structures during the thinning process.
22. The method of claim 16 wherein providing the device wafer comprises:
- providing a Si-SiGe-Si wafer that includes a common silicon epitaxial layer, a common interfacial layer over the common silicon epitaxial layer, and the silicon handle substrate over the common interfacial layer, wherein the common interfacial layer is formed of SiGe;
  - performing a complementary metal-oxide-semiconductor (CMOS) process to provide a precursor wafer that includes a plurality of device regions, wherein:
    - the isolation sections extend through the common silicon epitaxial layer and the common interfacial layer, and extend into the silicon handle substrate, such that the common interfacial layer separates into a plurality of individual interfacial layers, and the common silicon epitaxial layer separates into a plurality of individual silicon epitaxial layers;
    - each active layer of the plurality of device regions is formed from a corresponding individual silicon epitaxial layer; and
    - each of the plurality of individual interfacial layers directly resides over a top surface of a corresponding active layer, and the silicon handle substrate resides directly over the plurality of individual interfacial layers; and
  - forming the plurality of first bump structures at the bottom surface of each BEOL portion to complete the plurality of device dies from the plurality of device regions.

23. The method of claim 16 wherein providing the device wafer comprises:
- providing a Si-SiGe-Si wafer that includes a common silicon epitaxial layer, a common interfacial layer over the common silicon epitaxial layer, and the silicon handle substrate over the common interfacial layer, wherein:
    - the common interfacial layer comprises SiGe; and
    - the common interfacial layer has a plurality of interfacial layers that are connected;
  - performing a CMOS process to provide a precursor wafer that includes a plurality of device regions, wherein:
    - the isolation sections extend through the common silicon epitaxial layer and extend into the common interfacial layer, such that the common silicon epitaxial layer separates into a plurality of individual silicon epitaxial layers and the plurality of interfacial layers remain connected;
    - each active layer of the plurality of device regions is formed from a corresponding individual silicon epitaxial layer; and
    - each of the plurality of interfacial layers directly resides over a top surface of a corresponding active layer, and the silicon handle substrate remains directly over the common interfacial layer; and
  - forming the plurality of first bump structures at the bottom surface of each BEOL portion to complete the plurality of device dies from the plurality of device regions.

**STATEMENT UNDER ARTICLE 19(1)**

Applicant has submitted amendments under Article 19 PCT for the above-referenced application.

Applicant has amended claim 1, and renumbered claims 16-18 (original claims 18-20, respectively). In addition, Applicant has cancelled claims 3 and 7.

Claim 1 has been amended to replace “*the active layer does not extend vertically beyond the isolation sections*” with “*the isolation sections surround the active layer and extend vertically beyond a top surface of the active layer to define an opening within the isolation sections and over the active layer,*” and has been amended to incorporate the feature “*a second mold compound residing over the active layer of the FEOL portion to fill the opening.*” Amended claim 1 clarifies that a top surface of each isolation section and a top surface of the active layer cannot be coplanar, and clarifies that the second mold compound fills the opening formed within the isolation sections. In addition, claim 1 has been amended to replace the feature “*a silicon material, which has a resistivity between 5 Ohm-cm and 30000 Ohm-cm, in between*” with the feature “*silicon crystal, which has no germanium, nitrogen, or oxygen content, does not exist between the second mold compound and the active layer,*” so as to keep consistent to the Specification.

Renumbered claim 16 has been amended to incorporate the feature “*removing the interfacial layer to expose the active layer of each of the plurality of device dies,*” and has been amended to replace “*applying a second mold compound over the active layer of each of the plurality of device dies after the interfacial layer is removed*” with “*applying a second mold compound over the active layer of each of the plurality of device dies from where the silicon handle substrate is removed.*” Renumbered claim 16 clarifies that the interfacial layer is removed to expose each active layer before applying the second mold compound. In addition, renumbered claim 16 has been amended to replace the feature “*no silicon material resides between the second mold compound and each active layer*” with the feature “*silicon crystal, which has no germanium, nitrogen, or oxygen content, does not exist between the second mold compound and the active layer,*” so as to keep consistent to the Specification.

Renumbered claim 17 has been amended to remove the feature “*further comprising removing the interfacial layer before applying the second mold compound,*” which has been included in renumbered claim 16.

Renumbered claim 18 has been amended to remove the feature “*removing the interfacial layer,*” which has been included in renumbered claim 16.

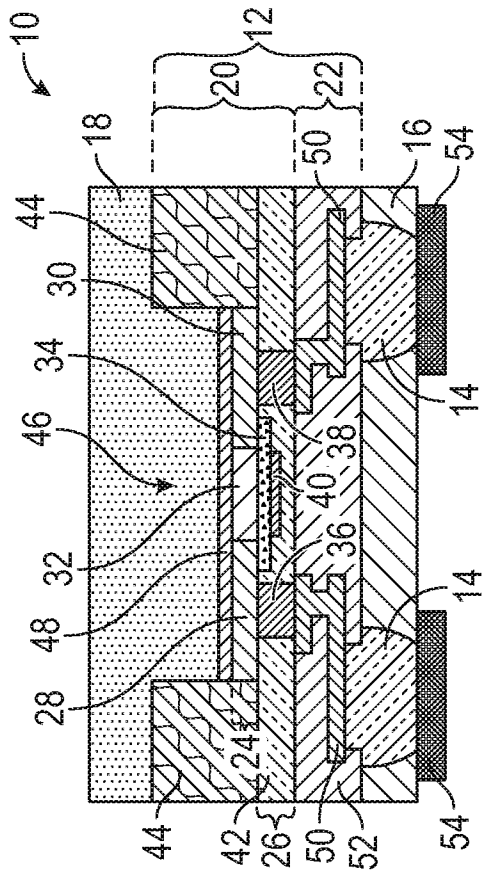


FIG. 1

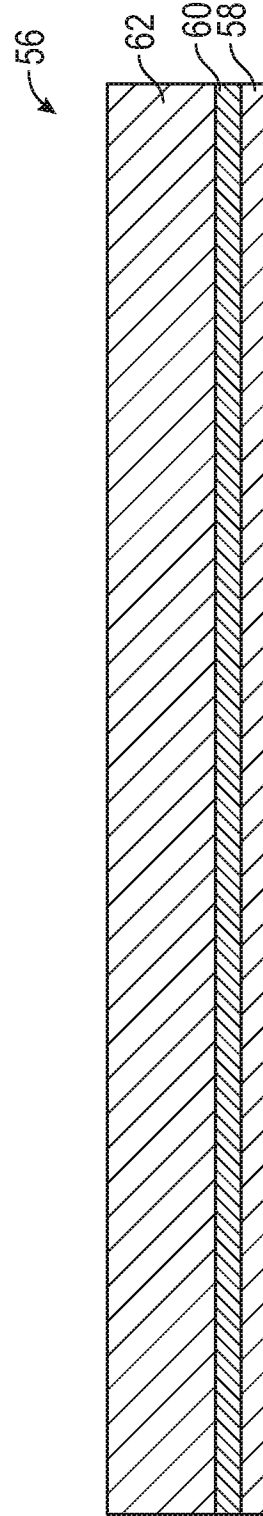


FIG. 2



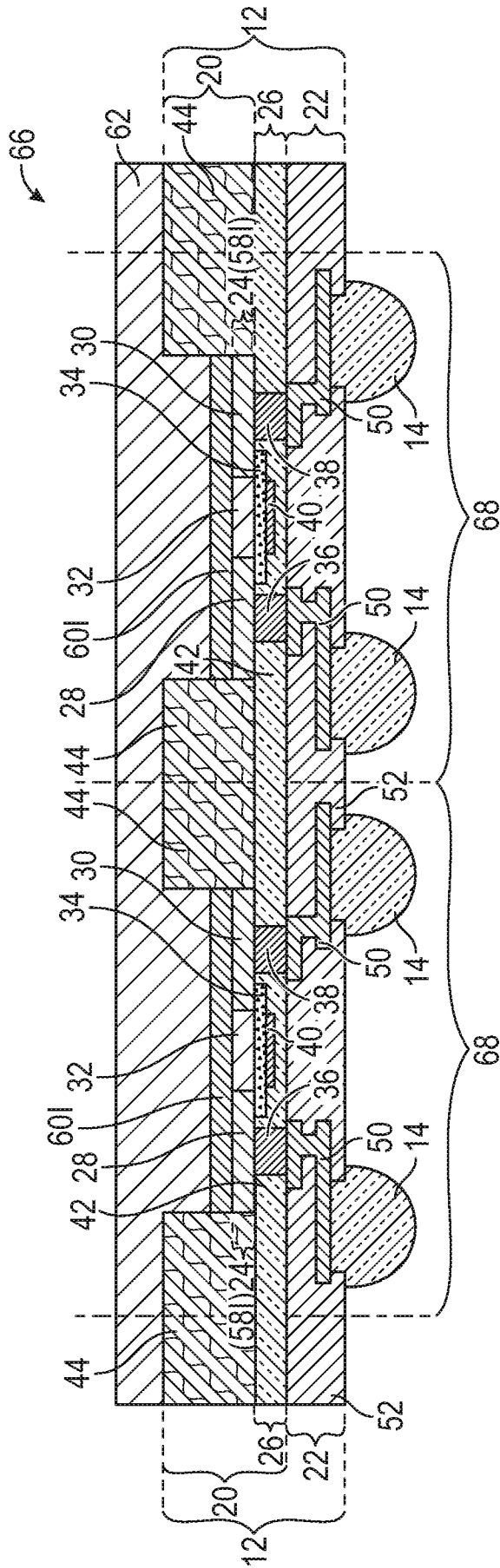


FIG. 4

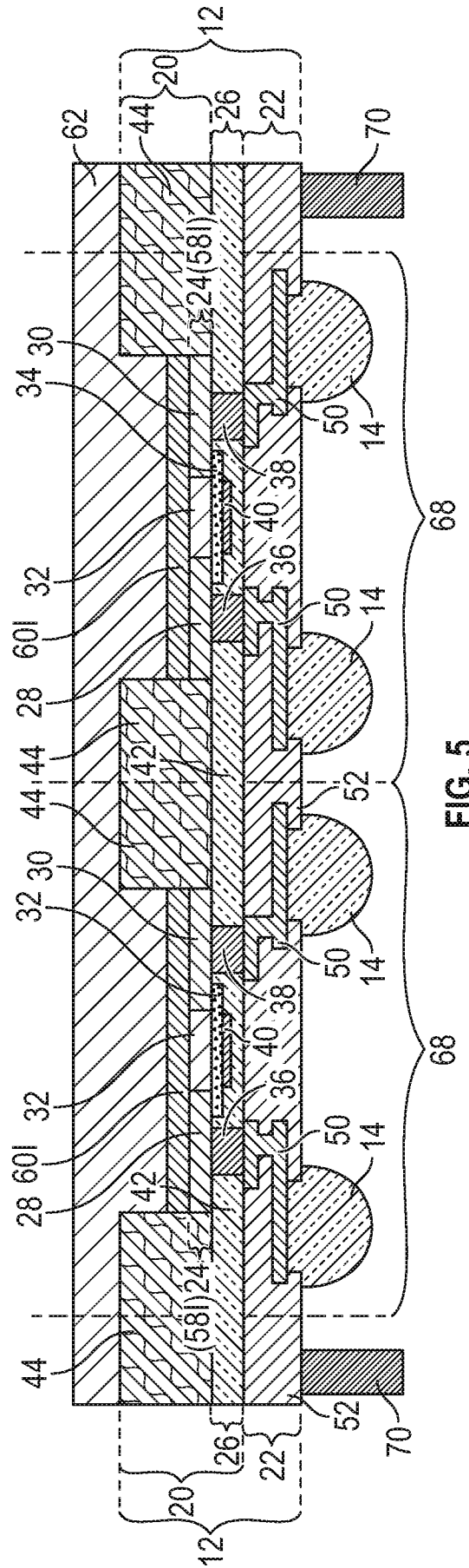


FIG. 5

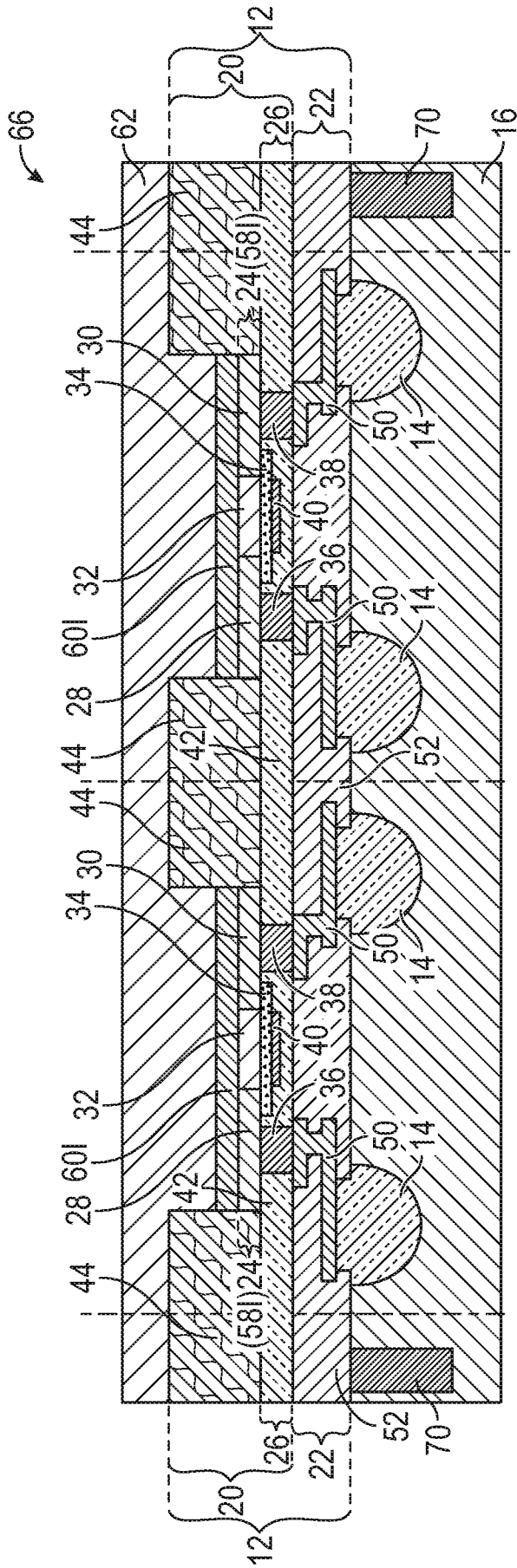


FIG. 6

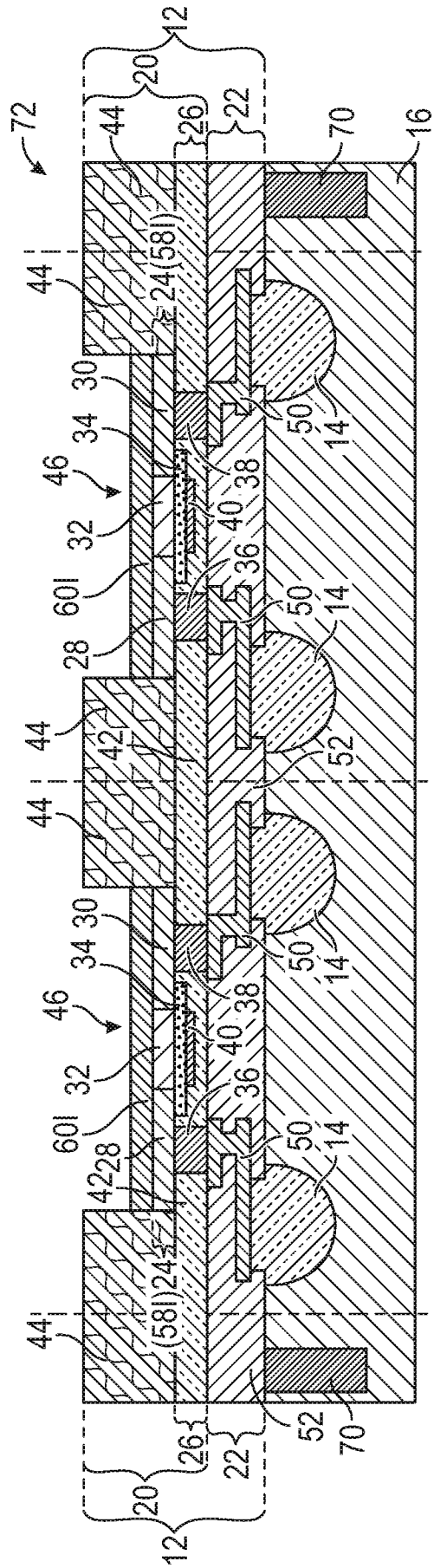
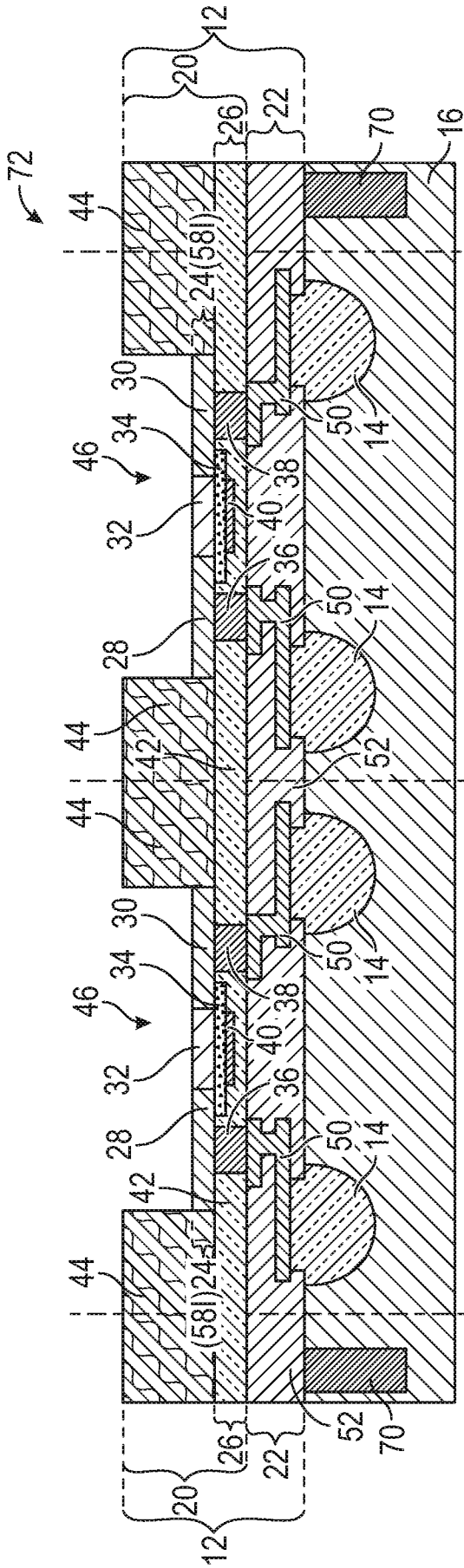


FIG. 7



5/7

FIG. 8

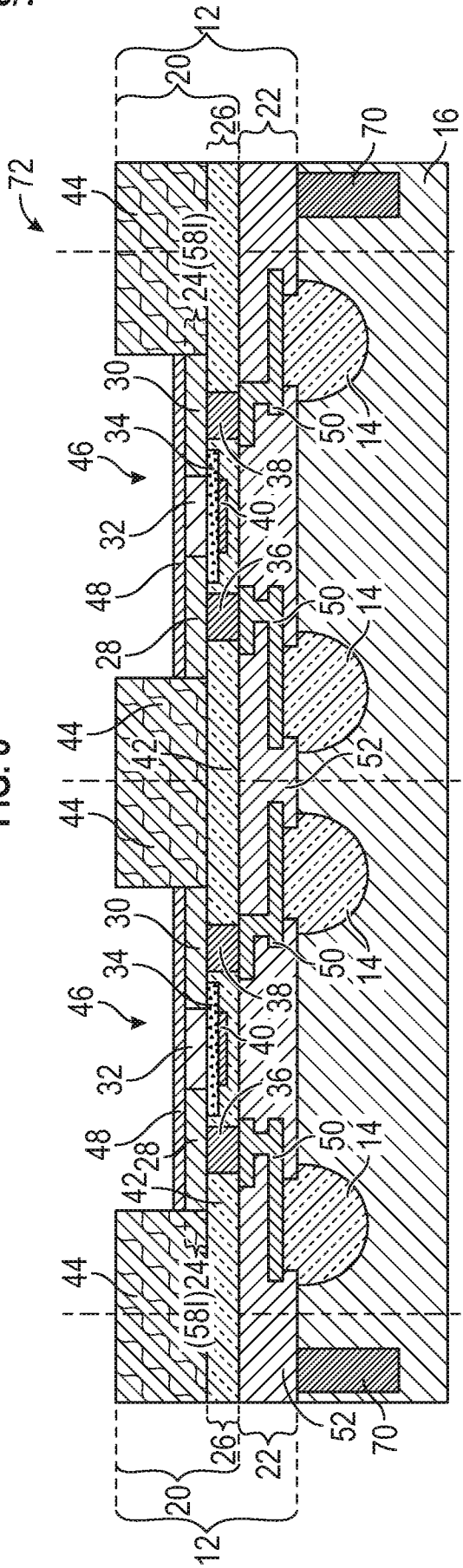


FIG. 9

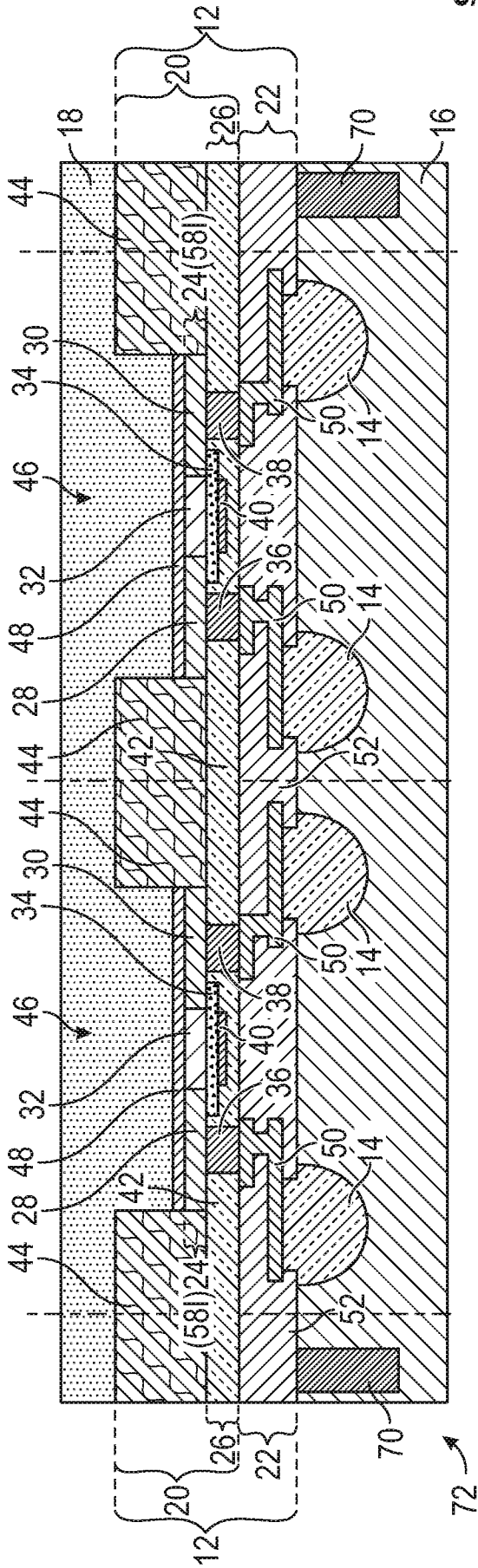


FIG. 10

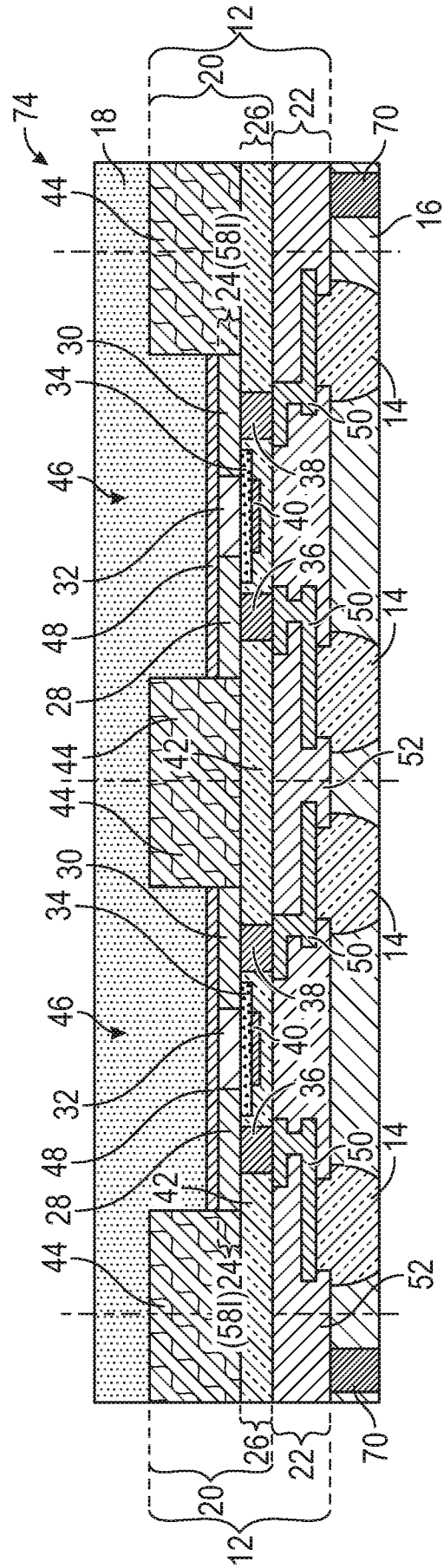


FIG. 11

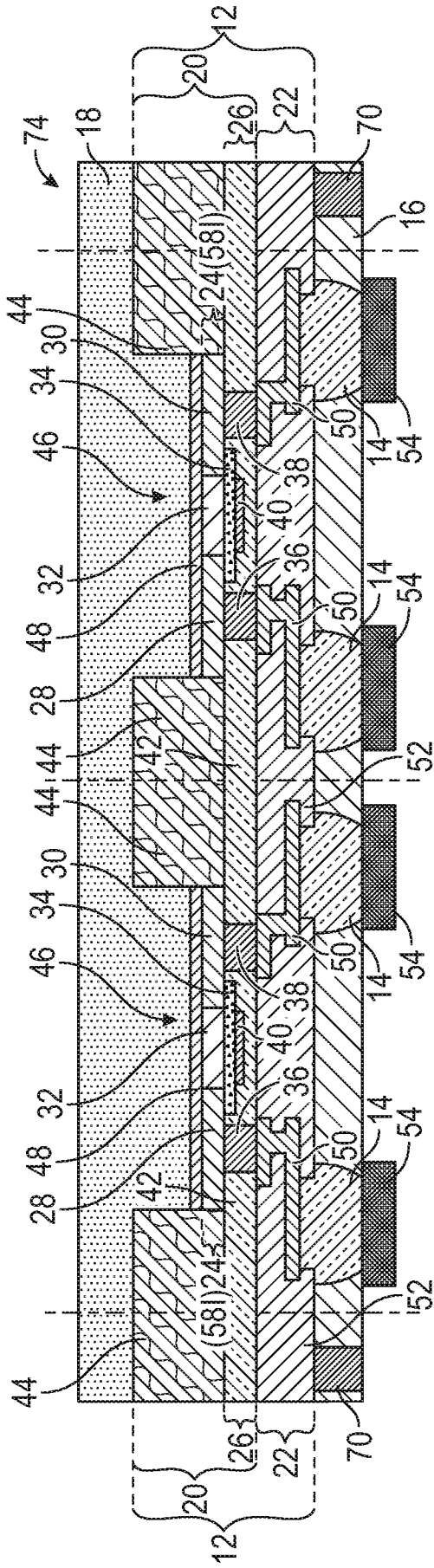


FIG. 12

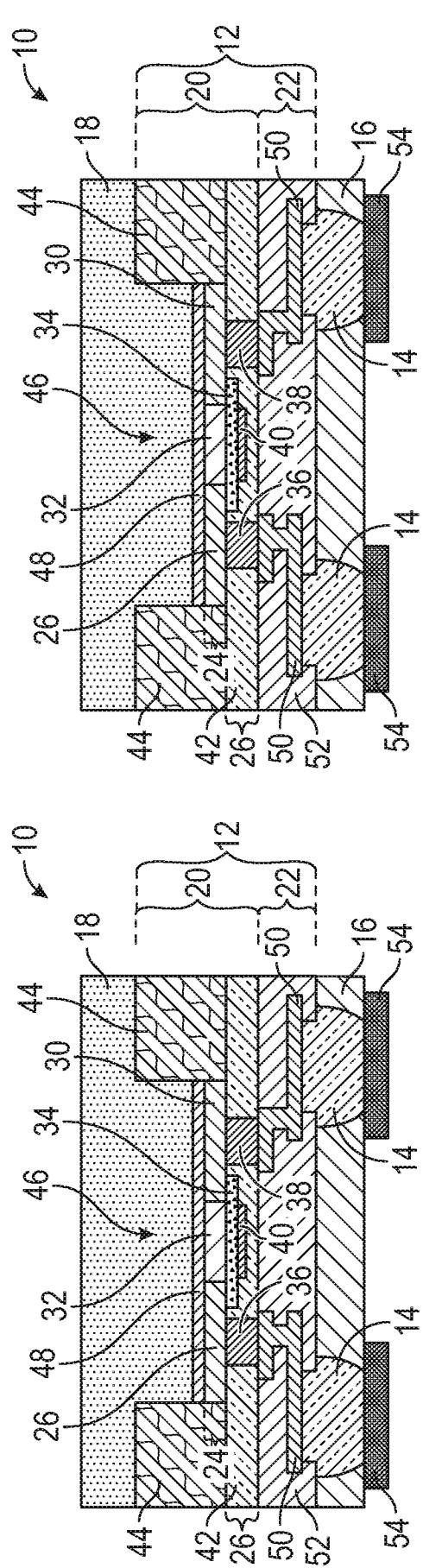


FIG. 13

# INTERNATIONAL SEARCH REPORT

International application No PCT/US2019/034645
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**A. CLASSIFICATION OF SUBJECT MATTER**  
 INV. H01L21/56      H01L23/31      H01L27/12      H01L29/786  
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
 EPO-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 2015/255368 A1 (COSTA JULIO C [US]) 10 September 2015 (2015-09-10) paragraphs [0040] - [0057]; figure 14  ----- US 5 013 681 A (GODBEY DAVID J [US] ET AL) 7 May 1991 (1991-05-07) column 3, line 24 - column 5, line 14; figures 1-5  ----- US 2018/166358 A1 (COSTA JULIO C [US] ET AL) 14 June 2018 (2018-06-14) paragraph [0028]; figure 1  ----- US 2016/133591 A1 (HONG SUNG WOONG [KR] ET AL) 12 May 2016 (2016-05-12) the whole document -----	1,2,4, 7-17 3,5,18, 21 6,19,20, 22-25  5,18,21  3  22,23

Further documents are listed in the continuation of Box C.       See patent family annex.

\* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
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Date of the actual completion of the international search  <b>10 September 2019</b>	Date of mailing of the international search report  <b>19/09/2019</b>
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer  <b>Edmeades, Michael</b>
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# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2019/034645

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015255368 A1	10-09-2015	US 2015255368 A1 US 2017271200 A1	10-09-2015 21-09-2017
-----			
US 5013681 A	07-05-1991	CA 2066193 A1 EP 0493503 A1 JP 2684455 B2 JP H04506587 A KR 950006967 B1 US 5013681 A WO 9105366 A1	30-03-1991 08-07-1992 03-12-1997 12-11-1992 26-06-1995 07-05-1991 18-04-1991
-----			
US 2018166358 A1	14-06-2018	US 2018166358 A1 US 2018342439 A1	14-06-2018 29-11-2018
-----			
US 2016133591 A1	12-05-2016	KR 20160054795 A TW 201618197 A US 2016133591 A1	17-05-2016 16-05-2016 12-05-2016
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