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MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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Declarations under Rule 4.17:

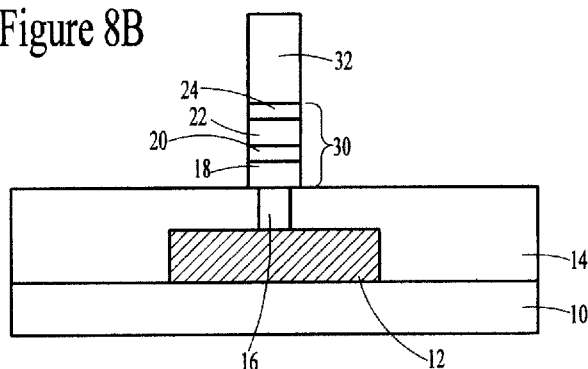
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
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(54) Title: MTJ DEVICE PROCESS/INTEGRATION METHOD WITH PRE-PATTERNED SEED LAYER

Figure 8B



(57) Abstract: A method for etching a magnetic tunneling junction (MTJ) structure is described. A bottom electrode layer (12) is provided on a substrate (10). A seed layer (16) is deposited on the bottom electrode layer. The seed layer and bottom electrode layer are patterned. A dielectric layer is deposited over the patterned seed layer and bottom electrode layer and planarized wherein the seed layer is exposed. Thereafter, a stack (30) of MTJ layers is deposited on the patterned seed layer comprising a pinned layer (18), a tunnel barrier layer (20), and a free layer (22). The MTJ stack is then patterned to form a MTJ device. Because the seed layer was patterned before the MTJ patterning step, the exposure of the device to etching plasma gases is shortened and thus, etch damage is minimized.



MTJ DEVICE PROCESS / INTEGRATION METHOD WITH PRE-PATTERNED SEED LAYER

TECHNICAL FIELD

This application relates to the general field of magnetic tunneling junctions (MTJ) and, more particularly, to etching methods for forming MTJ structures.

BACKGROUND

Fabrication of magneto-resistive devices normally involves a sequence of processing steps during which many layers of metals and dielectrics are deposited and then patterned to form a magneto-resistive stack as well as electrodes for electrical connections. The magneto-resistive stack usually includes the free and pinned layers of the device, sandwiched around one or more dielectric layers functioning as the tunnel junction for the magnetic tunnel junction (MTJ) device.

A critical challenge in magnetic random access memory (MRAM) technology is the patterning of the magnetic tunnel junction (MTJ) stack without damaging the device. The thin magnetic layers used in the MTJ stack, are easily damaged during plasma etch processes. Therefore a processing scheme for manufacturing the MTJ device that can minimize the exposure of the tunnel junction to plasma processes is desired.

U.S. Patents 6,849,465 (Park et al) and 9,373,782 (Li et al) teach patterning the bottom electrode first, then depositing and patterning the MTJ stack, but these methods are different from the present disclosure.

SUMMARY

It is an object of the present disclosure to provide an improved method of forming MTJ structures.

Yet another object of the present disclosure is to provide a method of MTJ device patterning that can minimize etch damage of the device caused by long exposure to etching plasma gases.

In accordance with the objectives of the present disclosure, a method for etching a magnetic tunneling junction (MTJ) structure is achieved. A bottom electrode layer is provided on a substrate. A seed layer is deposited on the bottom electrode layer. The seed layer and bottom electrode layer are patterned. A dielectric layer is deposited over the patterned seed layer and bottom electrode layer and planarized. Thereafter, a stack of MTJ layers is deposited on the patterned seed layer comprising a pinned layer, a tunnel barrier layer, and a free layer. The MTJ stack is then patterned to form a MTJ device. Because the seed layer was patterned before the MTJ patterning step, the exposure of the device to etching plasma gases is shortened and thus, etch damage is minimized.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Fig. 1 is a flowchart of a MTJ process sequence of the prior art.

Figs 2 and 3 are cross-sectional representations of steps in a process of the prior art.

Fig. 4 is a flowchart of a first preferred embodiment of the present disclosure.

Figs. 5 through 8A and 8B illustrate in cross-sectional representation steps in a first preferred embodiment of the present disclosure.

Figs. 8A and 8B illustrate in cross-sectional representation two options for a seed layer width in a preferred embodiment of the present disclosure.

Fig. 9 is a flowchart of a second preferred embodiment of the present disclosure.

Figs. 10 through 13 illustrate in cross-sectional representation steps in a second preferred embodiment of the present disclosure.

.DETAILED DESCRIPTION

A novel integration scheme for avoiding damage to MTJ layers due to long exposure to plasma processes is described. Fig. 1 is a flowchart showing a standard method of forming a magnetic tunnel junction (MTJ) device, as shown in cross-section in Figs. 2 and 3.

As shown in Fig. 1, in a first step 101, a CMOS substrate with vias is built to connect with the MTJ device to be formed subsequently. The substrate 10 is shown in Fig. 2. Next in step 102, a bottom electrode is patterned. Fig. 2 illustrates bottom electrode 12 and subsequently deposited and planarized dielectric layer 14. Next in step 103, the MTJ film layers are deposited, including a seed layer 16, pinned layer 18, barrier layer 20, free layer 22, and cap layer 24, as shown in Fig. 2. These layers form the MTJ film stack 30.

In step 104, a photoresist pattern is made to pattern the MTJ device. Fig. 2 illustrates patterned hard mask 32. In step 105, the MTJ stack is etched. Fig. 3 illustrates the etching of the MTJ stack which includes the seed layer 16. The magnetic film stack is etched using the hard mask. The MTJ layers are very thin and can be damaged easily during plasma etch. In the standard MRAM etching process, the etching plasmas may physically or chemically damage the layers or may cause re-deposition of metal-containing residues. This may be due to the low etch selectivity and non-volatile nature of by-products that are formed during the etch process. Such residues may build up along the sidewall of the patterned film stack

and form a conductive path as shown by 35 in Fig. 3. This conductive path or damaged layers may cause electrical short-circuits within a MRAM device, e.g., between the magnetic layers separated by the tunnel layer, or may degrade the MRAM device performance or the MRAM device may not be functional at all.

The basic idea of the present disclosure is to create a novel process integration scheme to minimize the physical or chemical damage of the magnetic layers and reduce re-deposition of metal-containing residues. The bottom layer of a magnetic memory device is the seed layer. The purpose of the seed layer is to promote the growth of large crystal grains and also sometimes to provide the correct crystallographic orientation. The seed layer needs to be thick enough to serve these purposes. It could be about 1/3 the thickness of the entire MTJ stack. Because of this thickness, sometimes it takes a long time to etch the seed layer and a long over etch time to confirm there is no residue left on the surface. This long exposure to etching plasma gases can cause physical or chemical damage to other critical layers, e.g. pinned layer, barrier layer and free layer, and can also cause re-deposition of metal-containing residues 35 along the sidewall as shown in Fig. 3. If the etching time can be reduced, the physical or chemical damage and the re-deposition along the sidewall also can be reduced.

A key feature of the present disclosure is the combination of the seed layer etching process with the bottom electrode etching. The seed layer will be deposited along with the bottom electrode deposition.

Fig. 4 is a flowchart of a first preferred embodiment process of the present disclosure. Refer also to Figs. 5-8a and 8b. In step 401, a CMOS substrate with vias is built to connect with the MTJ device to be formed subsequently. The substrate 10 is shown in Fig. 5. Next in step 402, a bottom electrode and seed layer are patterned. Fig. 5 illustrates bottom electrode layer 12, seed layer 16, and a protective layer 17 such as Ta or TiN to be used as a hard mask for etching the seed layer. The bottom electrode and the seed layer can be patterned together using the seed layer as a hard mask for etching the bottom electrode or separately using two

photolithographic steps and subsequently planarized. Photoresist pattern 42 is shown in Fig. 5.

Fig. 6 shows the patterned bottom electrode 12 and seed layer 16. Dielectric layer 14 is deposited and planarized, as shown in Fig. 7. Protective layer 17 is removed by chemical mechanical polishing (CMP) or another planarization process either before or after the dielectric layer 14 is formed. The protective layer 17 also can be removed during the sputter etch before MTJ film deposition. Prior to MTJ film deposition, the seed layer is exposed, such as during the planarization step.

Now in step 403, the MTJ film layers are deposited, including pinned layer 18, barrier layer 20, free layer 22, and cap layer 24, as shown in Fig. 7. The first layer of the stack will directly contact the seed layer 16. These layers form the MTJ film stack 30. Hard mask layer 32 is deposited on top of the MTJ layer stack.

In step 404, a photoresist pattern is made to pattern the MTJ device and the pattern is transferred to the hard mask 32. In step 405, the MTJ stack is etched. Fig. 8 illustrates the etching of the MTJ stack. Since the seed layer 16 has already been patterned, the tunnel junction etching time is significantly reduced. Hence, there will be less etch damage and less re-deposition on the sidewall. The pre-patterned seed layer can be larger, equal to, or slightly smaller than the MTJ device. Fig. 8a shows a seed layer larger than the MTJ device and Fig. 8b shows a seed layer smaller than the MTJ device. In the case of the equal or smaller seed layer, the metal re-deposition on the sidewall will be reduced even more since during over etching only dielectric material 14 will be exposed.

Fig. 9 is a flowchart of a second preferred embodiment process of the present disclosure. Refer also to Figs. 10 - 13. In step 901, a CMOS substrate with vias is built to connect with the MTJ device to be formed subsequently. The substrate 10 is shown in Fig. 10. Next in step 902, a bottom electrode and partial seed layer are patterned. Fig. 10 illustrates bottom electrode layer 12, seed layer 16a, and a protective layer 17 such as Ta or TiN to be used as a hard mask for etching the seed

layer. The bottom electrode and the seed layer can be patterned together using the seed layer as a hard mask for etching the bottom electrode or separately using two photolithography steps and subsequently planarized. Between about 60% and 80%, and preferably about 80% of the desired seed layer thickness could be deposited as layer 16a. 20% of the thickness will be deposited layer as layer 16b.

If a thin seed layer is deposited along with the MTJ film it may better act as a buffer layer for crystal growth continuity between the seed layer and the MTJ film. Depositing and patterning most of the seed layer now will provide the advantage of reducing plasma exposure time while also providing a thin buffer layer for crystal growth continuity when the MTJ layers are deposited.

Fig.11 shows the patterned bottom electrode 12 and seed layer 16a. Dielectric layer 14 is deposited and planarized, as shown in Fig. 12. Protective layer 17 is removed by chemical mechanical polishing (CMP) or another planarization process either before or after the dielectric layer 14 is formed. Protective layer 17 can also be removed during a sputter etch before MTJ film deposition. The seed layer 16a will be exposed, such as by the planarization step.

Now in step 903, the remainder of the seed layer 16b, about 20% of the desired seed layer thickness, is deposited directly contacting the first seed layer 16a, followed by the remaining MTJ film layers including pinned layer 18, barrier layer 20, free layer 22, and cap layer 24, as shown in Fig. 12. These layers form the MTJ film stack 30. Hard mask layer 32 is deposited on top of the MTJ layer stack.

In step 904, a photoresist pattern is made to pattern the MTJ device and the pattern is transferred to the hard mask 32. In step 905, the MTJ stack is etched. Fig. 13 illustrates the etching of the MTJ stack. Since only a thin seed layer 16b is to be etched along with the rest of the MTJ film layers, the tunnel junction etching time is significantly reduced. Hence, there will be less etch damage and less re-deposition on the sidewall. As in the first embodiment, the pre-patterned seed layer 16a can be larger, equal to, or slightly smaller than the MTJ device.

In this second embodiment, the tunnel junction layers will grow on top of a continuous seed layer; however, etching time will be significantly reduced since the majority of the seed layer materials will be etched along with the bottom electrode prior to the MTJ etching. Therefore, there will be less etching damage and less re-deposition on the sidewall.

Depositing the seed layer along with the bottom electrode layer and patterning them together will reduce the MTJ device etching time and hence reduce etching damage and metal re-deposition along the MTJ sidewall. This should significantly improve the electrical short circuit issue and also improve device performance. The option to pattern the seed layer equal in width or narrower than the MTJ device further reduces metal re-deposition along sidewall. Optionally, instead of depositing all the seed layer along with the bottom electrode, the majority of the seed layer, about 80%, is deposited along with the bottom electrode layer and the seed layer and bottom electrode layer are patterned together. This way, only a thin layer of seed will be deposited along with the other MTJ film stack layers to reduce the MTJ device etching time and hence result in reduced etching damage and reduced metal re-deposition along the MTJ sidewall. The seed layer may be about 1/3 the thickness of the entire MTJ stack. Removing the etching of the seed layer to prior to depositing the MTJ layers can reduce MTJ stack etching time by as much as one-half.

Although the preferred embodiment of the present disclosure has been illustrated, and that form has been described in detail, it will be readily understood by those skilled in the art that various modifications may be made therein without departing from the spirit of the disclosure or from the scope of the appended claims.

What is claimed is:

1. A method for etching a magnetic tunneling junction (MTJ) structure comprising:
 - providing a bottom electrode layer on a substrate;
 - depositing a seed layer on said bottom electrode layer;
 - patterning said seed layer and said bottom electrode layer;
 - depositing a dielectric layer over patterned said seed layer and bottom electrode layer and planarizing said dielectric layer wherein said seed layer is exposed;
 - thereafter depositing a stack of MTJ layers on said patterned seed layer comprising a pinned layer, a tunnel barrier layer, and a free layer; and
 - patterning said MTJ stack to form a MTJ device.
2. The method according to claim 1 wherein said seed layer is patterned to have a width equal to a width of said MTJ device.
3. The method according to claim 1 wherein said seed layer is patterned to have a width wider than a width of said MTJ device.
4. The method according to claim 1 wherein said seed layer is patterned to have a width narrower than a width of said MTJ device.
5. The method according to claim 1 wherein said seed layer is a first seed layer and further comprising:
 - depositing a second seed layer over patterned said first seed layer wherein a first thickness of said first seed layer is between about 60% and 80% of a second thickness of said first and second seed layers together; and
 - patterning said second seed layer as part of said MTJ stack.
6. The method according to claim 1 wherein said seed layer and said bottom electrode layer are patterned separately.
7. The method according to claim 1 wherein said seed layer and said bottom electrode layer are patterned together.

8. A method for etching a magnetic tunneling junction (MTJ) structure comprising:
- providing a bottom electrode layer on a substrate;
 - depositing a seed layer on said bottom electrode layer;
 - patterning said seed layer and said bottom electrode layer;
 - depositing a dielectric layer over patterned said seed layer and bottom electrode layer and planarizing said dielectric layer wherein said seed layer is exposed;
 - thereafter depositing a stack of MTJ layers on said patterned seed layer comprising a pinned layer, a tunnel barrier layer, and a free layer; and
 - patterning said MTJ stack to form a MTJ device wherein said seed layer is patterned to have a width equal to or smaller than a width of said MTJ device.
9. The method according to claim 8 wherein said seed layer is a first seed layer and further comprising:
- depositing a second seed layer over patterned said first seed layer wherein a first thickness of said first seed layer is between about 60% and 80% of a second thickness of said first and second seed layers together; and
 - patterning said second seed layer as part of said MTJ stack.
10. The method according to claim 8 wherein said seed layer and said bottom electrode layer are patterned separately.
11. The method according to claim 8 wherein said seed layer and said bottom electrode layer are patterned together.
12. A method for etching a magnetic tunneling junction (MTJ) structure comprising:
- providing a bottom electrode layer on a substrate;
 - depositing a first seed layer on said bottom electrode layer;
 - patterning said first seed layer and said bottom electrode layer;
 - depositing a dielectric layer over patterned said first seed layer and bottom electrode layer and planarizing said dielectric layer wherein said first seed layer is exposed;

thereafter depositing a stack of MTJ layers on said patterned first seed layer comprising a second seed layer, a pinned layer, a tunnel barrier layer, and a free layer; and

patterning said MTJ stack to form a MTJ device.

13. The method according to claim 12 wherein said first seed layer is patterned to have a width equal to a width of said MTJ device.

14. The method according to claim 12 wherein said first seed layer is patterned to have a width wider than a width of said MTJ device.

15. The method according to claim 12 wherein said first seed layer is patterned to have a width narrower than a width of said MTJ device.

16. The method according to claim 12 wherein a first thickness of said first seed layer is between about 60% and 80% of a second thickness of said first and second seed layers together.

17. The method according to claim 12 wherein said first seed layer and said bottom electrode layer are patterned separately.

18. The method according to claim 12 wherein said first seed layer and said bottom electrode layer are patterned together.

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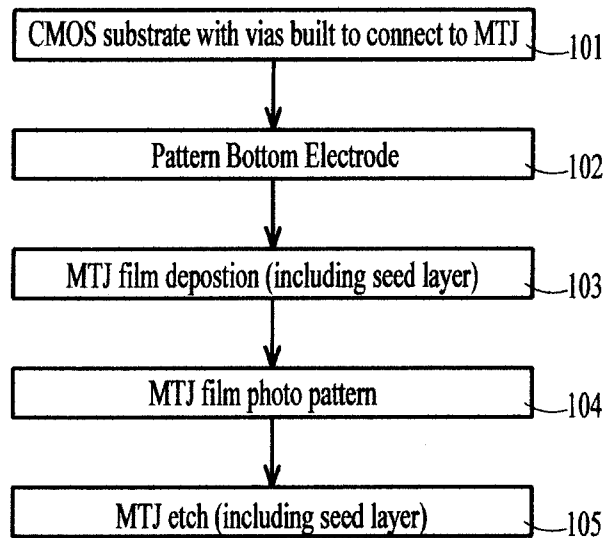


Figure 1 Prior Art

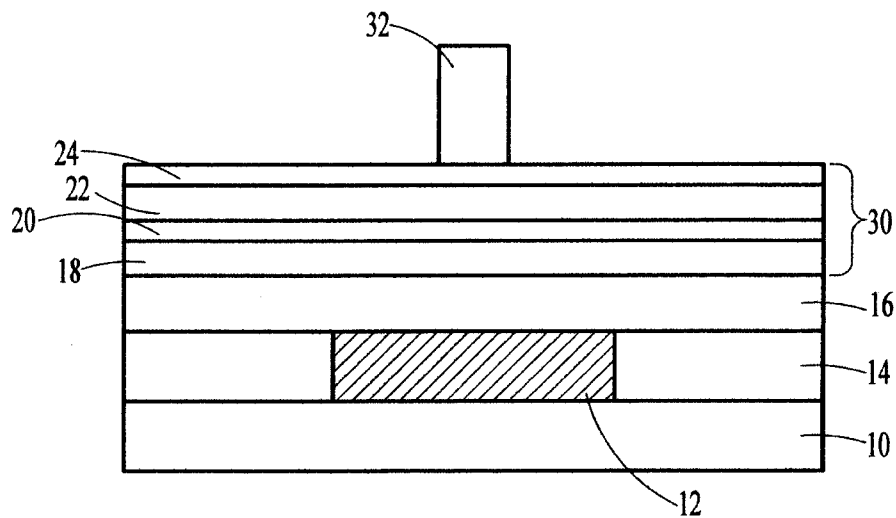


Figure 2 Prior Art

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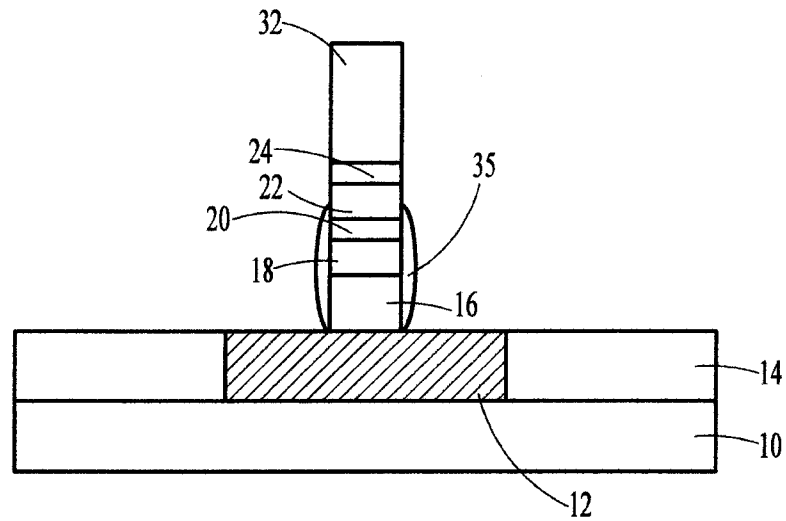


Figure 3 Prior Art

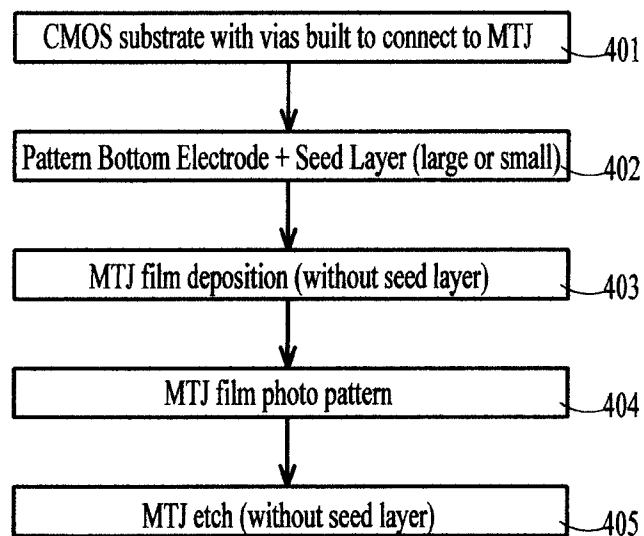


Figure 4

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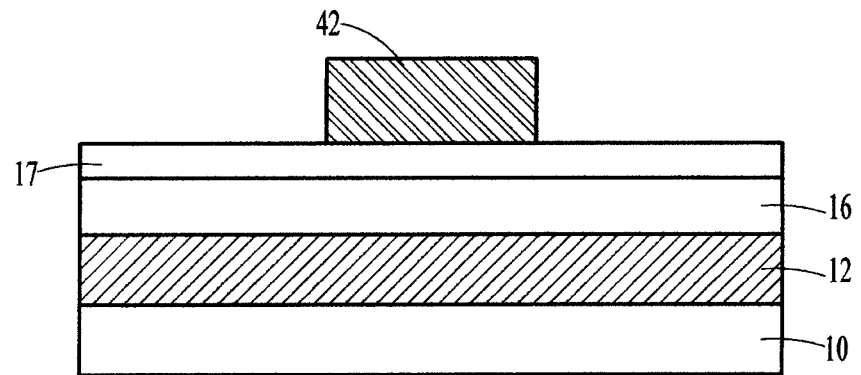


Figure 5

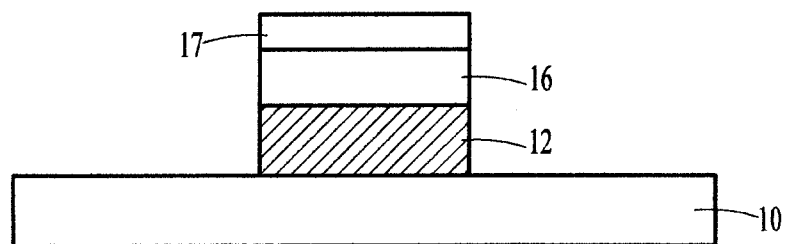


Figure 6

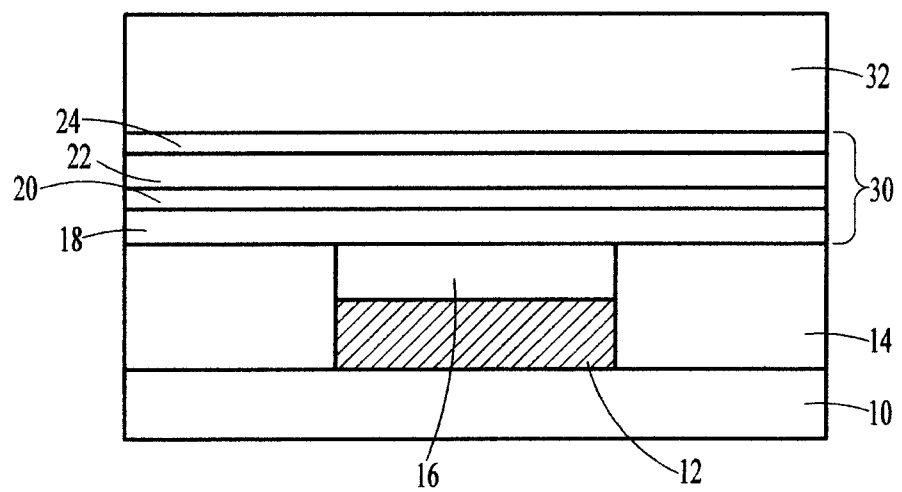


Figure 7

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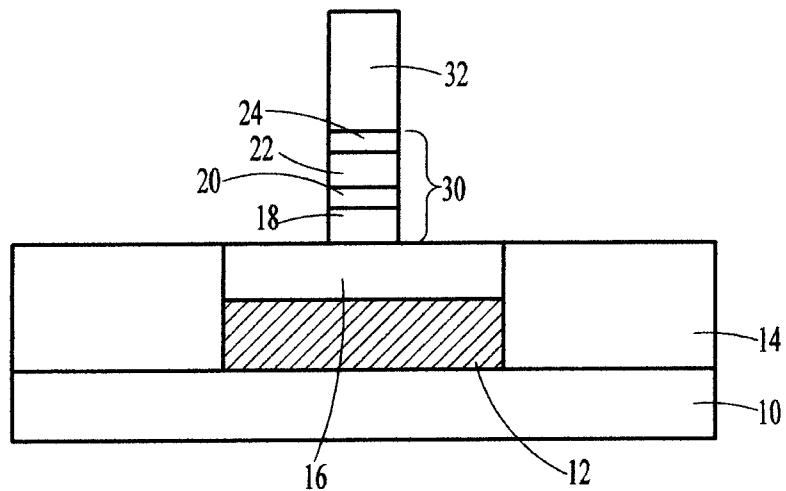


Figure 8A

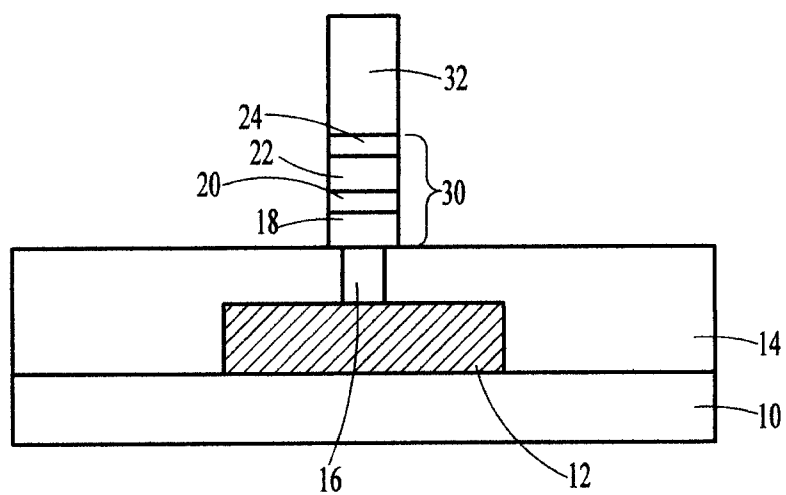


Figure 8B

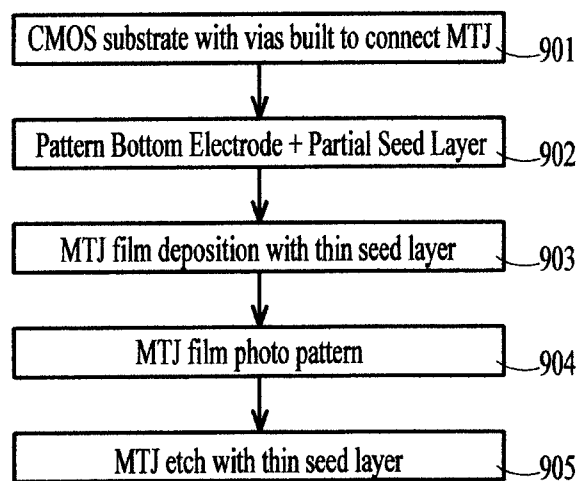


Figure 9

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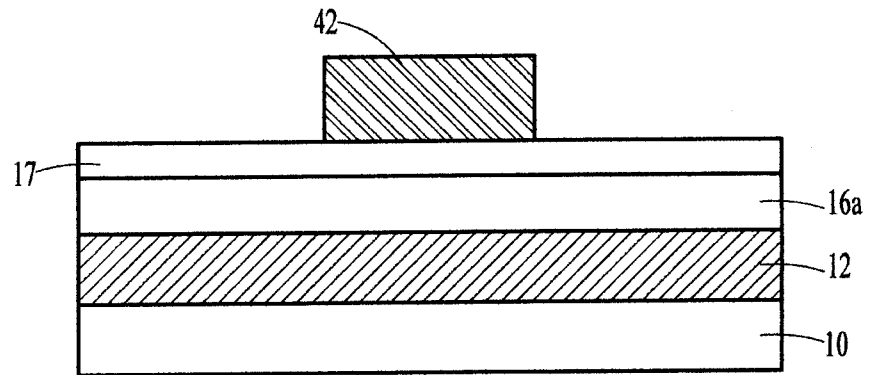


Figure 10

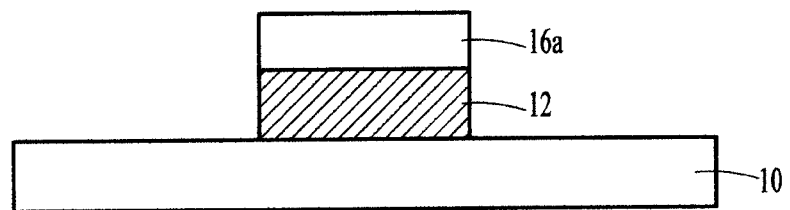


Figure 11

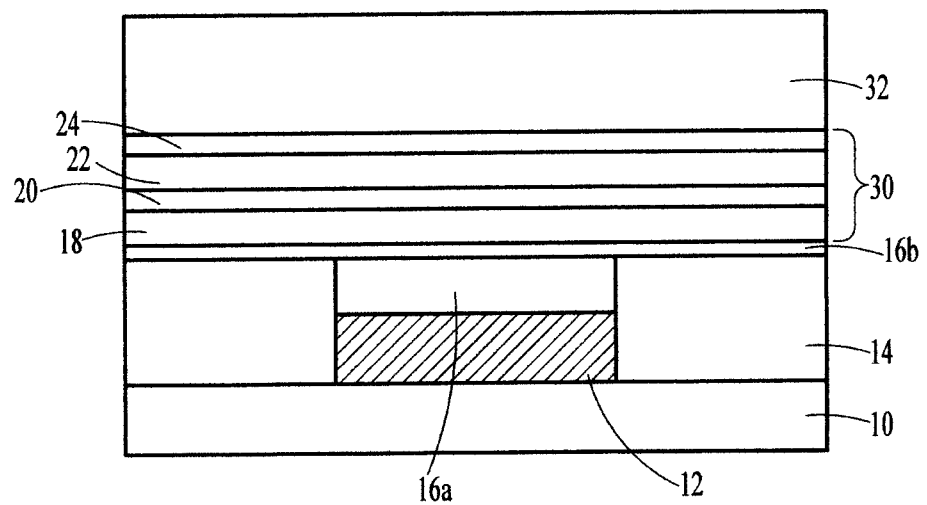


Figure 12

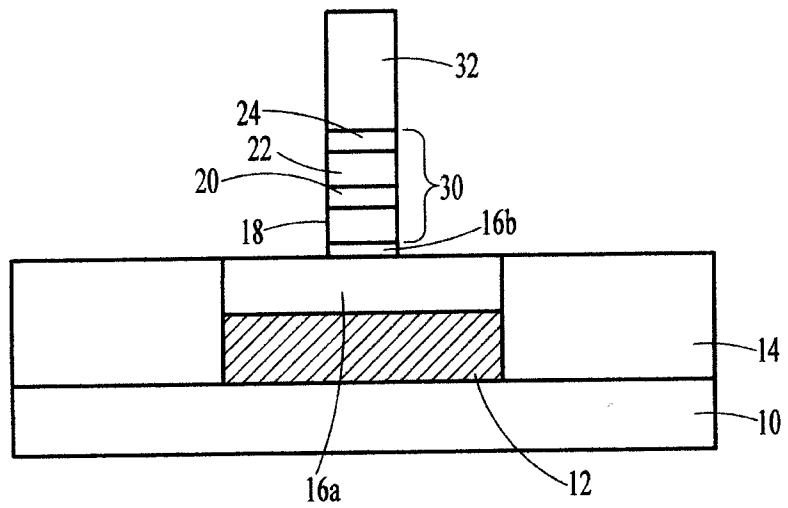


Figure 13

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2018/021286

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L43/12 ADD. H01L43/08		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, COMPENDEX		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 5 June 2018		Date of mailing of the international search report 06/07/2018
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Gröger, Andreas

INTERNATIONAL SEARCH REPORT

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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