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(54) Title: METHOD OF OPTIMIZING TEMPERATURE COEFFICIENT AND FREQUENCY SYNTHESIZER

(57) Abstract:

Description

METHOD OF OPTIMIZING TEMPERATURE COEFFICIENT AND FREQUENCY SYNTHESIZER

Technical Field

[1] The present invention relates to a frequency synthesizer, and more particularly, to a frequency synthesizer which is not sensitive to temperature changes.

Background Art

[2] In order to generate a frequency signal, a voltage controlled oscillator is used. The voltage controlled oscillator changes a frequency of an output signal in response to a voltage applied to an input. A direct current (DC) voltage input to the voltage controlled oscillator includes noises that exist in a path between a device for generating the DC voltage and the voltage controlled device. The noises may cause a situation in which a waveform of the signal generated by the voltage controlled oscillator trembles.

[3] In order to solve the aforementioned problem, that is, in order to decrease noise components in the DC voltage applied to the voltage controlled oscillator by using a signal output from the voltage controlled oscillator and generate a DC voltage accurately corresponding to a frequency to be generated, a frequency synthesizer employing a phase locked loop that will be described later is used.

[4] FIG. 1 is a block diagram showing a frequency synthesizer.

[5] Referring to FIG. 1, the frequency synthesizer includes a voltage controlled oscillator 10, a 1/N divider 20, a temperature compensated crystal oscillator 30, a 1/R divider 40, a phase frequency detector 50, a charge pump 60, and a loop filter 70.

[6] The voltage controlled oscillator 10 generates an oscillating signal responding to a DC voltage output from the loop filter 70.

[7] The 1/N divider 20 divides a frequency of the oscillating signal by N (N is an integer).

[8] The temperature compensated crystal oscillator 30 outputs a signal having a stable frequency without tremble against temperature changes. Since the frequency of the signal output from the crystal oscillator 30 is very high, the frequency of the signal output from the oscillator 30 is divided by R (R in an integer) by using the 1/R divider 40.

[9] The phase frequency detector 50 compares frequencies and phases of signals output from the 1/R divider 40 and the 1/N divider 20 with each other to generate an up/down signal corresponding to a compared value.

[10] When the up/down signal indicates up, the charge pump 60 supplies a steady current pulse to a high supply voltage VDD, and when the up/down signal indicates down, the

charge pump 60 supplies the steady current pulse to a ground terminal.

[11] The loop filter 70 performs low-pass filtering on the current pulse to generate a stable DC voltage from which high-frequency noises included in the current pulse are removed.

[12] In general, in mobile communications such as code division multiple access (CDMA) and global system for mobile communications (GSM), a user is identified by using the frequency synthesizer shown in FIG. 1.

[13] As important parameters required by the frequency synthesizer described with reference to FIG. 1, there are a locking time and a phase noise.

[14] Here, the locking time means a time consumed until a frequency of an oscillating signal output from the voltage controlled oscillator 10 of the frequency synthesizer has a desired frequency. The phase noise is a measure showing how accurate and how clean the frequency of the oscillating signal is without noises. One of the most important factors to determine the two measures is a loop bandwidth of the frequency synthesizer.

[15] When the loop bandwidth is designed to be small, more accurate oscillating signal can be generated. However, there are problems in that a response speed of the entire system (frequency synthesizer) becomes slow, the locking time lengthens, and a large amount of noises of the voltage controlled oscillator 10 is included in the oscillating signal. On the contrary, when the loop bandwidth is designed to be large, there is an advantage in that the response speed of the entire system becomes fast. However, there is a problem in that removing noises in an input path of the voltage controlled oscillator 10, that is, in the crystal oscillator 30, the phase frequency detector 50, and the divider 20 is not easy, so that phase noise characteristic of the entire system can be worsen.

[16] In order for the frequency synthesizer to be used for a mobile communication device, optimal loop bandwidth characteristic satisfying both the two measures is needed.

[17] Here, the loop bandwidth (BW) of the Phase Locked Loop circuit may be represented by Equation 1.

[18] [Equation 1]

[19]

$$BW \approx \frac{I_{cp} \cdot R_1 \cdot K_{vco}}{N}$$

[20] As shown in Equation 1, the loop bandwidth BW is obtained by using a current I_{cp} of the current pump 60, a resistance value

R_1

of a resistance in the loop filter 70, a dividing value N of the divider 20, and a slope

K_{vco}

of a frequency for a voltage of the voltage controlled oscillator 10. Here, a unit of the current

I_{cp}

is Ampere, a unit of the resistance

R_1

is Ohm, a unit of the slope

K_{vco}

of the frequency for the voltage is Hz/V, and the dividing value N of the divider is an integer.

[21] A change in the loop bandwidth BW of the frequency synthesizer due to temperature changes may be represented by Equation 2. Here, since the frequency synthesizer employs the PLL structure, hereinafter, the loop bandwidth of the frequency synthesizer is used as a bandwidth of the Phase Locked Loop.

[22] [Equation 2]

[23] $$BW = BW_{nom} \cdot [1 + \alpha_{BW} \cdot (T - T_{nom})]$$

[24] Referring to Equation 2, in order not to change electrical characteristics of the loop bandwidth of the frequency synthesizer though temperature changes, the temperature coefficient

α_{BW}

of the Phase Locked Loop (PLL) loop bandwidth has to be minimized.

Disclosure of Invention

Technical Problem

[25] The present invention provides a frequency synthesizer capable of minimizing a change in a phase locked loop (PLL) loop bandwidth (BW) due to temperature change.

[26] The present invention also provides a method of optimizing a temperature coefficient capable of minimizing a temperature coefficient

α_{BW}

of the PLL loop bandwidth.

Technical Solution

[27] The present invention provides a frequency synthesizer including a temperature compensated crystal oscillator, a 1/R divider, a voltage controlled oscillator, a 1/N divider, a phase frequency detector, a charge pump, and a loop filter, wherein a loop bandwidth of the frequency synthesizer is represented by

[28] $$BW \approx \frac{I_{cp} \cdot R_1 \cdot K_{vco}}{N}$$

,

[29] wherein values of a slope K_{vco}, a resistance R_1, and a current I_{cp} according to temperature changes are represented by

[30] $$K_{vco} = kvco_{nom} \cdot [1 + \alpha_{kvco} \cdot (T - T_{nom})]$$

[31] $$R_1 = R_{1nom} \cdot [1 + \alpha_{R_1} \cdot (T - T_{nom})]$$

[32] $$I_{cp} = I_{cp_{nom}} \cdot [1 + \alpha_{1_{cp}} \cdot (T - T_{nom})]$$

[33] wherein values of the temperature coefficients α_{kvco}, α_{R_1}, and $\alpha_{I_{cp}}$ are determined so as to enable a change of the loop bandwidth of the frequency synthesizer due to temperature changes to be zero, and wherein the slope

K_{vco}

is a slope of a frequency of the oscillating signal for an input voltage of the voltage controlled oscillator, the current

I_{cp}

is a current of the charge pump, and the resistance

R_1

is one of resistances included in the loop filter.

[34] The present invention also provides method of optimizing a temperature coefficient of a loop bandwidth of a frequency synthesizer, wherein the frequency synthesizer includes a temperature compensated crystal oscillator, a 1/R divider, a voltage controlled oscillator, a 1/N divider, a phase frequency detector, a charge pump, and a loop filter, and wherein when a loop bandwidth of the frequency synthesizer is represented by

[35]
$$BW \approx \frac{I_{cp} \cdot R_1 \cdot K_{vco}}{N}$$

,

[36] values of a temperature coefficient

α_{kvco}

of the slope

K_{vco}

of a frequency of the oscillating signal for an input voltage of the voltage controlled oscillator, a temperature coefficient

α_{R_1}

of a resistance

R_1

included in the loop filter, and a temperature coefficient

$\alpha_{I_{cp}}$

of a current of the charge pump are controlled to enable a temperature coefficient

α_{BW}

of the loop bandwidth to have a minimum value.

Brief Description of the Drawings

[37] FIG. 1 is a block diagram showing a frequency synthesizer.

Best Mode for Carrying Out the Invention

[38] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the attached drawings.

[39] The loop bandwidth BW of the phase locked loop (PLL) affects a performance of the entire system using the frequency synthesizer. In particular, when temperature changes and therefore a value of the loop bandwidth also changes, a delayed locking time and increased phase noises simultaneously affect the system using the frequency synthesizer. Therefore, reducing the influence of the temperature is the core of the present invention.

[40] Values of a slope

K_{vco}

, a resistance

R_1

, and a current

I_{cp}

according to temperature change may be represented by Equation 3.

[41] [Equation 3]

[42] $$K_{vco}=kvco_{nom}\cdot[1+\alpha_{kvco}\cdot(T-T_{nom})]$$

[43] $$R_1=R_{1nom}\cdot[1+\alpha_{R_1}\cdot(T-T_{nom})]$$

[44] $$I_{cp}=I_{cp_{nom}}\cdot[1+\alpha_{1_{cp}}\cdot(T-T_{nom})]$$

[45] Referring to FIG. 3, a slope

K_{vco}

of a frequency of an oscillating signal for an input voltage of the voltage controlled oscillator 10 according to temperature change is determined by a slope temperature co-efficient

α_{Kvco}

. Similarly, a resistance value of the resistance

R_1

in the loop filter 70 according to temperature changes is determined by a resistance temperature coefficient

α_{R_1}

, and a current value of the current

I_{cp}

supplied from the charge pump 60 is determined by a current temperature coefficient

$\alpha_{I_{cp}}$

. Here, the subscript nom means a value in a normal temperature.

[46] Even though the temperature changes, electrical characteristics of the 1/N divider 20 do not change, so that a change in characteristics of the 1/N divider 20 due to temperature changes needs not be considered.

[47] The slope

K_{vco}

of the frequency of the oscillating signal for the input voltage of the voltage controlled oscillator 10 is very sensitive to temperature and has a delta of +/- 20%. Whether the slope

K_{vco}

has a positive value or negative value may be determined when the voltage controlled oscillator 10 is designed.

[48] A change in the resistance value of the resistance

R_1

included in the loop filter 70 according to temperature changes can be predicted according to a manufacturing process, and moreover, the change in the resistance value due to temperature changes is small. The resistance may be manufactured to have the positive slope in which the resistance value increases when the temperature increases or may be manufactured to have the negative slope in which the resistance value decreases when the temperature increases. In general, the resistance is manufactured to

have the positive slope.

[49] The current change due to temperature changes of the current I_{cp} output from the charge pump 60 may be designed to have the positive slope or negative slope.

[50] Referring to Equations 1 to 3, since the loop bandwidth BW of the PLL is obtained by multiplying the temperature coefficient α_{kvco} of the slope K_{vco} of the frequency of the output signal for the input voltage of the voltage controlled oscillator, the temperature coefficient α_{R_1} of the resistance R_1, and the temperature coefficient $\alpha_{I_{cp}}$ of the current I_{cp}, the temperature coefficient α_{BW} of the PLL loop bandwidth is proportionate to a value obtained by multiplying the three temperature coefficients α_{kvco}, α_{R_1}, and

$\alpha_{I_{cp}}$

.

[51] Equation 1 simply represents the loop bandwidth of the frequency synthesizer shown in FIG. 1 and it becomes different according to a practical system. Here, for convenience of description of the present invention, Equation 1 is simply represented. Therefore, a different transfer function may be obtained according to a system.

[52] According to the present invention, in order for the loop bandwidth not to be sensitive to temperature, as described above, the slopes of the temperature coefficients

α_{kvco}

,

α_{R_1}

, and

$\alpha_{I_{cp}}$

which are multiplied to determine temperature characteristics of the loop bandwidth are properly used to implement the temperature coefficient

α_{BW}

of the loop bandwidth to the minimum.

[53] In order to minimize the temperature coefficient

α_{BW}

of the loop bandwidth, the three temperature coefficients

α_{kvco}

,

α_{R_1}

, and

$\alpha_{I_{cp}}$

may be considered as variables. However, since the temperature coefficient

α_{R_1}

of the resistance

R_1

generally has the positive slope, it is assumed that the value of the temperature coefficient

α_{R_1}

of the resistance

R_1

has the positive slope, and the slopes of the rest two temperature coefficients

α_{kvco}

and

$\alpha_{I_{cp}}$

may be adjusted to enable the temperature coefficient

α_{BW}

of the loop bandwidth to be zero.

[54] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the appended claims.

Industrial Applicability

[55] As described above, the method of optimizing a temperature coefficient and the freq uency synthesizer using the method according to the present invention have an advantage of minimizing a loop bandwidth (BW) of a phase locked loop (PLL) although temperature changes.

Claims

[1] A frequency synthesizer comprising:

a temperature compensated crystal oscillator generating a frequency signal;

a 1/R divider dividing the frequency signal by R (R is an integer);

a voltage controlled oscillator generating an oscillating signal in response a DC (direct current) voltage;

a 1/N divider dividing the oscillating signal by N (N is an integer);

a phase frequency detector comparing frequencies and phases of signals output from the 1/R divider and the 1/N divider with each other and generating an up/down signal;

a charge pump outputting a DC voltage responding to the up/down signal; and

a loop filter removing noises included in the DC voltage,

wherein a loop bandwidth of the frequency synthesizer is represented by

$$BW \approx \frac{I_{cp} \cdot R_1 \cdot K_{vco}}{N}$$

,

wherein values of a slope

K_{vco}

, a resistance

R_1

, and a current

I_{cp}

according to temperature changes are represented by

$$K_{vco} = kvco_{nom} \cdot [1 + \alpha_{kvco} \cdot (T - T_{nom})]$$

$$R_1 = R_{1nom} \cdot [1 + \alpha_{R_1} \cdot (T - T_{nom})]$$

$$I_{cp} = I_{cp_{nom}} \cdot [1 + \alpha_{1_{cp}} \cdot (T - T_{nom})]$$

wherein values of the temperature coefficients

α_{kvco}

,

α_{R_1}

, and

$\alpha_{I_{cp}}$

are determined so as to enable a change of the loop bandwidth of the frequency synthesizer due to temperature changes to be zero, and
wherein the slope

K_{vco}

is a slope of a frequency of the oscillating signal for an input voltage of the voltage controlled oscillator, the current

I_{cp}

is a current of the charge pump, and the resistance

R_1

is one of resistances included in the loop filter.

[2] The frequency synthesizer of claim 1, wherein the temperature coefficient

α_{kvco}

of the slope

K_{vco}

of the frequency of the oscillating signal for the input voltage of the voltage controlled oscillator and the temperature coefficient

$\alpha_{I_{cp}}$

of the current

I_{cp}

have the opposite slopes to each other.

[3] The frequency synthesizer of claim 2, wherein the temperature coefficient

α_{R_1}

of the resistance

R_1

included in the loop filter has a positive slope.

[4] A method of optimizing a temperature coefficient of a loop bandwidth of a frequency synthesizer, wherein the frequency synthesizer comprises:

a temperature compensated crystal oscillator generating a frequency signal;

a 1/R divider dividing the frequency signal by R (R is an integer);

a voltage controlled oscillator generating an oscillating signal in response a DC (direct current) voltage;

a 1/N divider dividing the oscillating signal by N (N is an integer);

a phase frequency detector comparing frequencies and phases of signals output from the 1/R divider and the 1/N divider with each other and generating an up/down signal;

a charge pump outputting a DC voltage responding to the up/down signal; and

a loop filter removing noises included in the DC voltage, and

wherein, when the loop bandwidth of the frequency synthesizer is represented by

$$BW \approx \frac{I_{cp} \cdot R_1 \cdot K_{vco}}{N}$$

,

values of a temperature coefficient

α_{kvco}

of the slope

K_{vco}

of a frequency of the oscillating signal for an input voltage of the voltage controlled oscillator, a temperature coefficient

α_{R_1}

of a resistance

R_1

included in the loop filter, and a temperature coefficient

$\alpha_{I_{cp}}$

of a current of the charge pump are controlled to enable a temperature coefficient

α_{BW}

of the loop bandwidth to have a minimum value.

[5] The method of claim 4, wherein the temperature coefficient

α_{kvco}

of the slope

K_{vco}

of the frequency of the oscillating signal for the input voltage of the voltage controlled oscillator and the temperature coefficient

$\alpha_{I_{cp}}$

of the current

I_{cp}

have the opposite slopes to each other.

[6] The method of claim 5, wherein the temperature coefficient

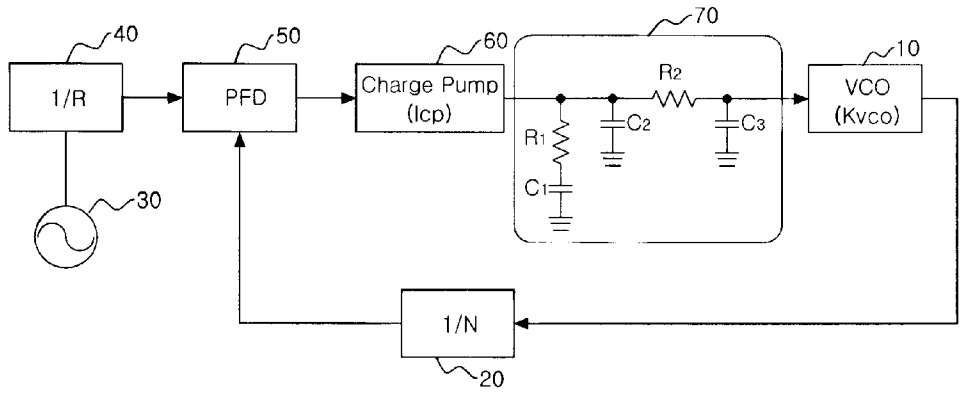
$\alpha_{I_{cp}}$

of the resistance

R_1

has a positive slope.

[Fig. 1]


40
50
60
70
10
1/R
PFD
Charge Pump
(Icp)
R2
VCO
(Kvco)
R1
C2
C3
C1
30
1/N
20

PATENT COOPERATION TREATY

PCT

DECLARATION OF NON-ESTABLISHMENT OF INTERNATIONAL SEARCH REPORT

(PCT Article 17(2)(a), Rules 13*ter*.1(c) and (d) and 39)

Applicant's or agent's file reference	**IMPORTANT DECLARATION**	Date of mailing (*day/month/year*)
S07-430PCT		11 SEPTEMBER 2007 (11.09.2007)
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International Patent Classification (IPC) or both national classification and IPC

H03L 7/16(2006.01)i

Applicant

FCI inc et al

This International Searching Authority hereby declares, according to Article 17(2)(a), that **no international search report will be established** on the international application for the reasons indicated below.

1. ☐ The subject matter of the international application relates to:
   - a. ☐ scientific theories.
   - b. ☐ mathematical theories.
   - c. ☐ plant varieties.
   - d. ☐ animal varieties.
   - e. ☐ essentially biological processes for the production of plants and animals, other than microbiological processes and the products of such processes.
   - f. ☐ schemes, rules or methods of doing business.
   - g. ☐ schemes, rules or methods of performing purely mental acts.
   - h. ☐ schemes, rules or methods of playing games.
   - i. ☐ methods for treatment of the human body by surgery or therapy.
   - j. ☐ methods for treatment of the animal body by surgery or therapy.
   - k. ☐ diagnostic methods practised on the human or animal body.
   - l. ☐ mere presentation of information.
   - m. ☐ computer programs for which this International Searching Authority is not equipped to search prior art.
2. ☒ The failure of the following parts of the international application to comply with prescribed requirements prevents a meaningful search from being carried out:
   ☒ the description ☒ the claims ☐ the drawings
3. ☐ A meaningful search could not be carried out without the sequence listing; the applicant did not, within the prescribed time limit:
   - ☐ furnish a sequence listing on paper complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
   - ☐ furnish a sequence listing in electronic form complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
   - ☐ pay the required late furnishing fee for the furnishing of a sequence listing in response to an invitation under Rule 13ter.1(a) or (b)
4. ☐ A meaningful search could not be carried out without the tables related to the sequence listings; the applicant did not, within the prescribed time limit, furnish such tables in electronic form complying with the technical requirements provided for in Annex C-bis of the Administrative Instructions, and such tables were not available to the International Searching Authority in a form and manner acceptable to it.
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