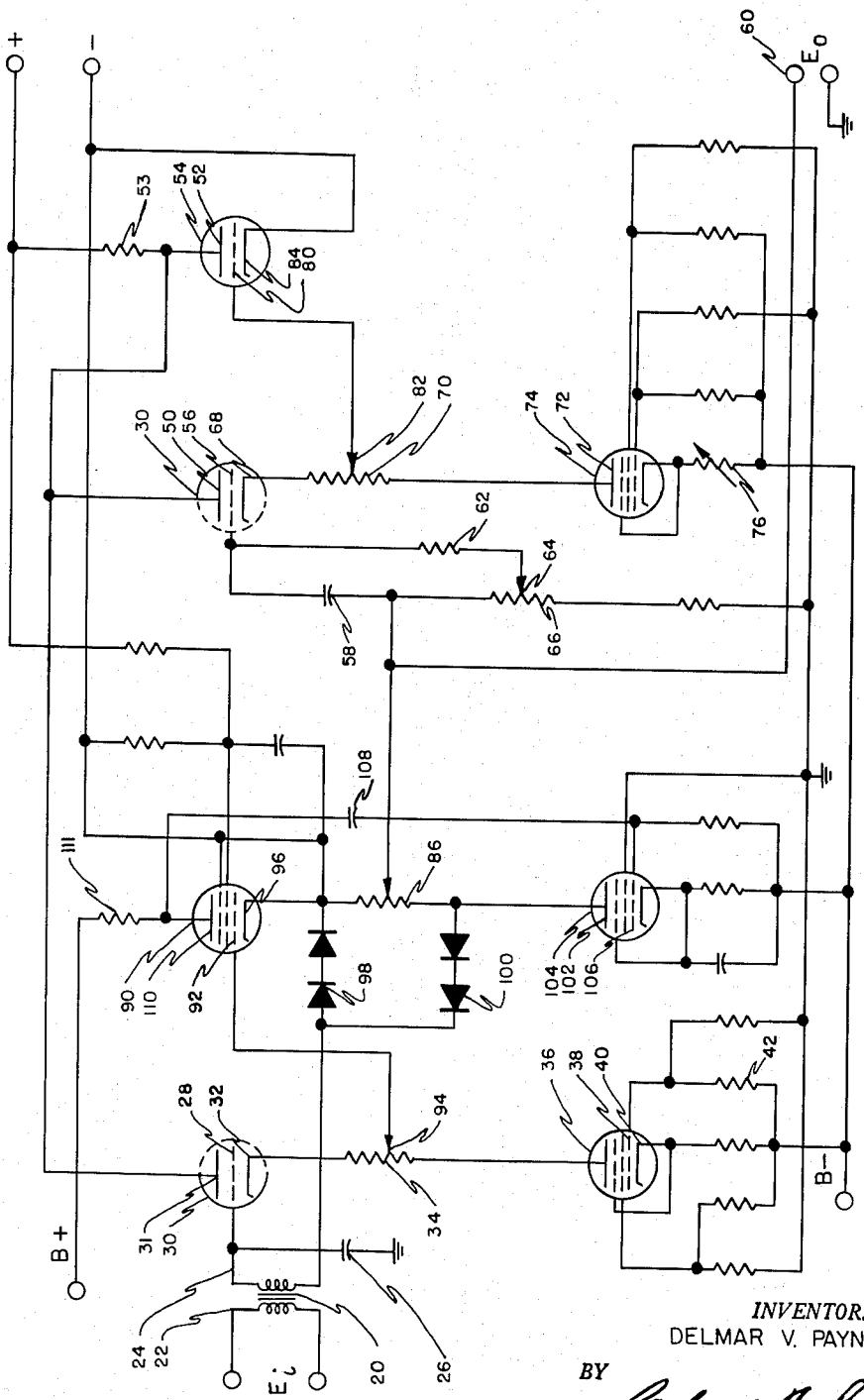
Dec. 17, 1963 D. V. PAYNE 3,114,885

INTEGRATING CIRCUIT

Filed June 6, 1960



INVENTOR.
DELMAR V. PAYNE

BY
Richard J. Sager
ATTORNEY

United States Patent Office 3,114,885 Patented Dec. 17, 1963

3,114,885

INTEGRATING CIRCUIT

Delmar V. Payne, Ferndale, Mich., assignor to The Bendix Corporation, a corporation of Delaware

Filed June 6, 1960, Ser. No. 33,980
10 Claims. (Cl. 328—127)

This invention pertains to a circuit for receiving pulses and integrating these pulses to provide an accumulative voltage. More particularly, this invention pertains to an integrating circuit which is able to hold the accumulated charge on an integrating capacitor with a minimum of decay.

An object of this invention is to provide an integrating circuit wherein an integrating capacitor has its charging plate connected to the grid of a first cathode follower triode in a dual triode tube for controlling current flow from a charging source to the capacitor according to input pulses placed on the charging plate. Since any grid current will cause a change in the charge on the integrating capacitor, it is highly desirable to minimize grid current flow. This is done by connecting a compensating capacitor to the grid of the second cathode follower triode in the dual triode tube so that any grid current in the second triode will result in a corresponding change of the second triode grid voltage. The second triode cathode output is connected to the grid of a third tube which has its plate connected to the plates of the first and second triodes with any variation in second triode grid voltage causing a compensating change in the plate voltages. The cathodes of the two triodes are supplied through resistances from similar current sources and the plates are connected together. Also, the grids are closely adjacent one another so that the grid currents of the first and second triodes tend to be the same, and any grid current results in a change of plate voltage of the two triodes in a compensating manner.

It is a further object of this invention to provide in the circuit of the preceding paragraph a resistance which has one end connected between the compensating capacitor and the grid of the second triode of the dual triode tube, and its other end connected to an output sensitive resistance so that any change in the output will "overcompensate" to correct the leakage resistance in parallel with the integrating capacitor.

These and other objects and advantages will become more apparent when a preferred embodiment of this invention is described in connection with the drawing which shows a schematic diagram of the integrating and compensating circuits.

In the drawing is a transformer 20 having a primary winding 22 across which the input pulses are placed and having a secondary winding 24 which has one leg connected to the charging plate of an integrating capacitor 26 and also to the grid 28 of a triode which is one-half of a dual triode 30 such as a Raytheon tube No. 5755. A cathode 32 of tube 30 is connected to a resistance 34 which is connected to the plate of a pentode 36. The control grid 38 and cathode 40 of pentode 36 are connected by resistance 42 and tube 36 is operated so that it is in the area where change in plate voltage will have a minimum effect on plate current and, therefore, results in a constant current supply to cathode 32.

A plate 31 of tube 30 is connected to plate 50 of the second triode in tube 30, and also connected to plate 52 of triode 54. Grid 56 of the second triode in tube 30 is connected to one plate of capacitor 58, the opposite plate of which is connected to output 60 and resistance 66. Adjustable contact 64 provides an adjustable contact between resistance 62 and resistance 66. The cathode 68 of the second triode in tube 30 is connected to resistor 70 which, in turn, is connected to the plate 72 of a pentode 74 which is similar in construction and function to pentode

36 with the exception that it has its cathode resistance 76 adjustable. Pentode 74 also is operated to provide an essentially constant current to cathode 68.

The grid 80 of tube 54 is connected through an adjustable pointer 82 to resistance 70, and cathode 84 of tube 54 is connected to a negative voltage line and to output 60 through a portion of an output resistance 86. In the operation of the integrator, a series of input pulses accumulate on the upper or charging plate of capacitor 26 and the charge on this plate is supplied according to the input pulses, by means later described, and measured at output 60. However, any current in grid 28 will tend to cause decay of the charge on capacitor 26 and, therefore, it is desirable that the grid 28 current be kept to a minimum. This is done by placing a second triode in the same tube 30 and by maintaining the plates 31, 50 and the cathodes 32, 68 in such a manner that the grid currents of grids 28 and 56 will be approximately the same and controlling the grid 56 current so that it has an average of zero. To accomplish this, a compensating capacitor 58 is placed in the grid 56 circuit so that any grid 56 current will result in a storage of charge on the upper plate of capacitor 58 and a resulting change in voltage of both the capacitor 58 and grid 56. A change in voltage in grid 56 will result in a corresponding change of voltage in cathode 68 and a change of voltage at pointer 82 and grid 80, which will change the potential of plates 52, 50 and 31 in a manner which compensates for any current in grids 28 and 56 to reduce these currents to a minimum. For example, if the current in grids 28 and 56 are such that the charge on upper plate of capacitor 58 becomes positive, cathode 68, pointer 82, and grid 80 will also become more positive, thereby increasing the flow of current in plate 52. This will cause a larger drop in resistance across plate resistor 53 lowering the potential of plates 31, 50 and 52, lowering the electron flow to the plate and increasing the electron flow to grids 28, 56 which opposes, and, therefore, minimizes the existing current flow from positive ions therein.

A certain amount of charge is lost from the charging plate of capacitor 26 due to leakage resistance. This is compensated for by resistor 62 through which charge from the upper plate of capacitor 58 is lost in amounts corresponding to voltage at output 60. Therefore, when the voltage at output 60 is high positive, the charge lost from the upper plate of integrating capacitor 26 through leakage resistance will be relatively high, but the charge lost from the upper plate of compensating capacitor 58 will also be relatively high which causes grids 56 and 80 to go more negative, raising the potential of plates 31, 30 and 52, and attracting more positive ions to grid 28 to raise the charge on capacitor 26.

The apparatus for supplying charge to the upper plate of integrating capacitor 26 in amounts corresponding in sign and magnitude from input pulses will now be described. A pentode 90 has its grid 92 connected to resistance 34 through an adjustable pointer 94. The cathode 96 of pentode 90 is connected to output resistance 86 and to a pair of diodes 98 which, in turn, are connected to secondary 24 of transformer 20. The other end of resistance 86 is connected to a pair of diodes 100 which are connected in an opposite direction from diodes 98 and also connected to secondary 24, and plate 102 of pentode 104. The control grid 106 of pentode 104 is connected through capacitance 108 to the plate 110 of pentode 90.

When an input signal is impressed on secondary 24, grid 28 will change in voltage in a corresponding manner as the charge on capacitor 26 is changed. If the pulse is positive then there will exist a voltage between the lower end of transformer secondary 24 and resistance 86 which is of such polarity and magnitude that diode pair

100 will conduct and diode pair 98 are further cut off. As diode pair 100 conducts, capacitor 26 is charged positive through secondary 24. This results in a change of voltage at pointer 94, although the drop across resistor 34 remains the same since tube 36 supplies substantially constant current, and to the grid 92 of pentode 90. Grid 92 will become more positive, increasing the voltage output 60 in a positive direction so as to maintain the conduction of diodes 100 and thereby supplying current in a positive direction to capacitor 26. When the positive pulse terminates across secondary 24 the voltage at grid 28 will be correspondingly higher but the voltage at cathode 96 will also be higher and, therefore, the potential drop across the diodes 98, 100 will be the same as it was initially and no current flow will take place.

If negative pulses are received, grid 28, cathode 32, pointer 94, grid 92, and cathode 96 will go negative and the current flow through plate 110 will be less, raising the voltage at the plate connection of resistor 111 and raising the voltage of grid 106 to increase current flow through tube 104. Then voltage changes are the result of the conduction of diode pair 98 and the consequent change of charge on capacitor 26 through secondary 24. Again, when the pulse ends, the potential is lowered on either side of diode pair 98 and they will stop conducting.

Adjustment

The pulse integrator circuit above described may be adjusted as follows:

(1) Ground grid 32 and short out capacitor 58.

(2) Adjust pointer 94 along resistance 34 until equal voltages above and below ground appear at each end of resistance 86.

(3) Adjust resistance 86 so that the grid 56 measures zero volts.

(4) Repeatedly remove and replace the ground on grid 28 and adjust the voltage of plate 31 by adjusting pointer 82 until the output voltage 60 does not change from zero volts. Record the cathode to plate voltage of tube 54.

(5) Replace the ground on grid 28 and removed the short across capacitor 58. Adjust resistance 76 until the voltage across tube 54 is the same as that between the recorded voltage in the previous step.

(6) Repeat steps 1–5.

Operation

Briefly, the operation is as follows: An input pulse is received at the primary of transformer 20 and is impressed on the secondary changing the voltage on the anode side of diode pair 98 and the cathode side of diode pair 100. This causes current to flow through the diode pair which is biased on and a consequent change of charge on capacitor 26 through secondary winding 24. The change in charge on capacitor 26 results in a voltage change on the upper plate 24 which produces an almost equal voltage change at pointer 94 and resistor 86 so that the voltage change on diode pairs 98 and 100 is maintained while the pulse is applied. When the pulse terminates, the diodes will stop conducting since the voltage on either side, at grid 28 and across resistance 86, will both be changed in equal amounts and the voltage across the diodes will be the same as it was initially.

Any current in grid 28 will also tend to appear in grid 56 since these are grids of dual triodes in the same tube 30 and the current to cathode 68 was adjusted by adjusting resistor 76 until the grid currents were equal. Any current in grid 56 will result in a charge build-up on the upper plate of capacitor 58, changing the potential of grid 56, and cathode 68, resistance 70 and gird 80 to change the flow of current in tube 54 which will compensate and minimize the grid currents since plate 52 is connected to both plates 31 and 50. Also, resistance 62 is sensitive to output voltage and provides a leakage path for the charge in an amount corresponding to output voltage from the upper plate of capacitor 58 to provide a constant correction for loss of charge due to leakage resistance between the upper plate of capacitor 26 and ground.

Although this invention has been disclosed and illustrated with reference to particular applications, the principles involved are susceptible of numerous other applications which will be apparent to persons skilled in the art. The invention is, therefore, to be limited only as as indicated by the scope of the appended claims.

Having thus described my invention, I claim:

1. An integrator circuit comprising an input means, a dual triode tube having first and second cathode follower triodes in a common gas-tight envelope, integrating capacitor means being connected to said input means and to the grid of said first triode, charging means being connected to the cathode of said first triode and to said integrating capacitor means to supply charge to said capacitor means according to the magnitude of the input pulses, said charging means being controlled by the cathode output of said first cathode follower, output means being connected to said integrating capacitor means so that it is at a potential corresponding to the charge on said integrating capacitor means, compensating capacitor means being connected between said output means and the grid of said second triode, so that the voltage of said second triode grid will vary according to the second triode grid current and output voltage, each of said cathode follower triodes having cathode resistances, means being connected to the second triode cathode resistance to adjust the first and second triode plate voltages in accordance with said second triode cathode resistance voltage to reduce first and second triode grid current.

2. The integrator circuit of claim 1 with current supply means being connected to the cathode resistances of said first and second triodes, said supply means being adjustable relative one another to equalize grid currents in said first and second triodes.

3. The integrator circuit of claim 1 with resistance means being between an output related voltage and the grid of said second triode so that a portion of the charge of said compensating capacitor means may leak off to correct for leakage from said integrating capacitor means.

4. An integrator circuit comprising an input means, first and second multi-element electron devices being contained in a common gas-tight envelope, integrating capacitor means being connected to said input means and to the control grid of said first device, charging means being connected to the output of said first device and to said capacitor means to supply charge to said capacitor means according to the magnitude of said input pulses, said charging means being controlled by the output of said first device, output means being connected to said integrating means so that it is at a potential corresponding to the charge on said integrating capacitor means, compensating capacitor means being connected to the control grid of said second electron device so that the voltage of said second device will vary accordingly to the second device grid current, means being connected to the second device cathode to adjust the first and second device plate voltage to reduce first and second device grid currents.

5. An integrator circuit comprising an input means, first and second multi-element electron devices being contained in a common gas-tight envelope, integrating capacitor means being connected to said input means and to the control grid of said first device, charging means being connected to the output of said first device and to said capacitor means to supply charge to said capacitor means according to the magnitude of said input pulses, said charging means being controlled by the output of said first device, output means being connected to said integrating means so that it is at a potential corresponding to the charge on said intergrating capacitor means, com-

pensating capacitor means being connected between said output means and the control grid of said second electron device so that the voltage of said second device will vary accordingly to the second device grid current, and output voltage, means being connected to the second device cathode to adjust the first and second device plate voltage to reduce first and second device grid currents.

6. The integrator circuit of claim 5 with current supply means being connected to said first and second devices, said supply means being adjustable relative one another to equalize grid currents in said first and second devices.

7. The integrator circuit of claim 5 with resistance means being between an output related voltage and the grid of said second device so that a portion of the charge of said compensating capacitor means may leak off to correct for leakage from said integrating capacitor.

8. An integrator circuit comprising an input means, an integrating capacitor means being connected to said input means to store the input pulses, a dual triode tube having first and second cathode follower triodes each having a plate grid and cathode in a common gas-tight envelope, said capacitor means being connected to the grid of said first triode and being connected to one end of a pair of diode means in parallel, said diode means being connected in opposite directions, a first resistance connecting the other ends of said diode means, current supply means being connected to each end of said first resistance, an electrical output contact being movable along said first resistance, a compensating capacitor being connected between second triode grid and said output contact, a second triode cathode resistor being connected between said second triode cathode and the grid of a third tube means having a plate, a grid and a cathode, the plate of said third tube means being connected to the plates of said first and second triodes so that any current in said second

triode grid will cause a voltage across said compensating capacitor, causing a corresponding change in voltage across said second triode cathode resistor and third tube means grid so that the third tube means plate voltage will change inversely with said change altering the plate voltages of said first and second triodes in a manner to correspondingly change the first and second triode grid currents.

9. The integrator of claim 8 having a first cathode follower triode resistor connected to the cathode of said first cathode follower triode, said current supply means comprising a first pentode having its cathode connected to one end of said first resistance and its control grid connected to said first cathode follower triode resistor so that the grid and cathode potential of said first pentode vary in voltage with the grid of said first cathode follower triode, a second pentode having its plate connected to the outer end of said first resistance and its control grid being coupled to the plate of said first pentode through a capacitance.

10. The integrator of claim 9 with the plate of a third pentode being connected to said first cathode follower triode resistor and the plate of a fourth pentode being connected to said second triode cathode resistor, said third and fourth pentodes each having its control grid coupled to its cathode by a resistor.

References Cited in the file of this patent

UNITED STATES PATENTS

2,468,687	Schmitt	July 9, 1945
2,705,282	Parode et al.	Dec. 9, 1952
2,710,915	Young	Dec. 9, 1952

FOREIGN PATENTS

818,104	Great Britain	Aug. 12, 1959