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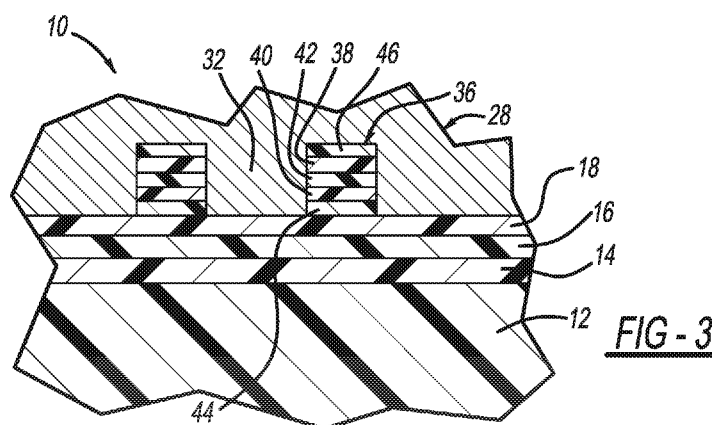
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(54) Title: WRAP AROUND GATE FIELD EFFECT TRANSISTOR (WAGFET)



(57) Abstract: A field effect transistor (FET) including a substrate, a plurality of semiconductor epitaxial layers deposited on the substrate, and a heavily doped gate layer deposited on the semiconductor layers. The FET also includes a plurality of castellation structures formed on the heavily doped gate layer and being spaced apart from each other, where each castellation structure includes at least one channel layer. A gate metal is deposited on the castellation structures and between the castellation structures to be in direct electrical contact with the heavily doped gate layer. A voltage potential applied to the gate metal structure modulates the at least one channel layer in each castellation structure from an upper, lower and side direction.



## WRAP AROUND GATE FIELD EFFECT TRANSISTOR (WAGFET)

## BACKGROUND

## Field

**[0001]** This invention relates generally to a wrap around gate field effect transistor (WAGFET) and, more particularly, to a WAGFET that includes a plurality of three-dimensional castellation structures each having one or more channels layers deposited on a heavily doped layer, where gate metal is deposited on the castellation structures and between the castellation structures to be in direct electrical contact with the heavily doped gate layer so as to modulate the channel layer from all directions.

## Discussion

**[0002]** Field-effect transistors (FET) are well known in the transistor art, and come in a variety of well known types, such a HEMT, MOSFET, MISFET, FinFET, etc., and can be integrated as horizontal devices or vertical devices. A typical FET will include various semiconductor layers, such as silicon, gallium arsenide (GaAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), indium phosphide (InP), etc. Sometimes the semiconductor layers are doped with various impurities, such as boron, to increase the population of carriers in the layer, where the higher the doping level of the layer the greater the conductivity of the particular semiconductor material. An FET will also include a source terminal, a drain terminal and a gate terminal, where one or more of the semiconductor layers is designated a channel layer and is in a electrical contact with the source and drain terminals. An electrical potential provided to the source terminal allows electrical carriers, either N-type or P-type, to flow through the channel layer to the drain terminal. An electric signal applied to the gate terminal creates an electrical field that modulates the carriers in the channel layer, where a small change in the gate voltage can cause a large variation in the population of carriers in the channel layer to change the current flow from the source terminal to the drain terminal.

**[0003]** It is known in the art to provide an FET that includes spaced apart castellation structures including one or more channel layers all deposited on a common base structure. In these types of castellated FETs, a

common gate metal is deposited on the base structure so that it encloses all of the castellation structures, particularly tops of the castellation structures and sides of the castellation structures. In this type of configuration, the electric field generated by the gate terminal to modulate the channel layer or layers is applied to not only the top of the channel layer, but also to the sides of the channel layer, which improves the amplification of the current flow.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0004]** Figure 1 is an isometric view of a wrap-around field effect transistor (WAGNET);

**[0005]** Figure 2 is an isometric view of the WAGFET shown in figure 1 with a gate terminal removed; and

**[0006]** Figure 3 is a cut-away, cross-sectional profile view of the WAGFET shown in figure 1 through line 3-3.

#### DETAILED DESCRIPTION OF THE EMBODIMENTS

**[0007]** The following discussion of the embodiments of the invention is directed to a WAGFET including a plurality of castellation structures and a heavily doped gate layer, where gate metal is deposited on the castellation structures and between the castellation structures to be in direct electrical contact with the heavily doped gate layer so as to modulate the channel layer from all directions, where the discussion is merely exemplary in nature, and is in no way intended to limit the invention or its applications or uses.

**[0008]** Figure 1 is an isometric view of a WAGFET 10 that provides modulation of one or more channel layers as will be described in detail below. The WAGFET 10 includes a substrate 12 that is made of any suitable material, for example, SiC, Sapphire, GaN, AlN, Si, GaAs, etc. In this non-limiting example, the substrate 12 is a GaAs substrate. A number of semiconductor layers are then grown on the substrate 12 as epitaxial layers to a desired layer thickness for the particular FET design. For example, in this non-limiting embodiment, a buffer layer 14 is grown on the substrate 12 and an InGaAs barrier layer 16 is grown on the buffer layer 14. A heavily doped gate layer 18 is grown on the barrier layer 16, and is a pseudo-conductive

layer that provides a modulation signal to a channel layer, as will be described in detail below. The gate layer 18 can be any suitable semiconductor material, such as GaAs in this non-limiting example, having any suitable thickness, and being doped with any suitable impurity or dopant that provides a high number of N-type or P-type carriers. Suitable and well known patterning and metal deposition steps are employed to deposit a source terminal 24, a drain terminal 26 and a gate terminal 28 on the gate layer 18, where the gate terminal 28 includes a top portion 30 and side portions 32 for reasons that will become apparent from the discussion below.

10           **[0009]**           Figure 2 is an isometric view of the WAGFET 10 with the gate terminal 28 removed showing a plurality of gate castellation structures 36. Figure 3 is a cut-away cross-sectional view of the WAGFET 10 through line 3-3 of figure 1. In this embodiment, the WAGFET 10 includes two of the castellation structures 36. However, as would be well understood by those skilled in the art, such a castellated FET of the type described herein would include many of the castellation structures 36 forming a castellated gate. Each castellation structure 36 includes two channel layers, namely, an upper channel layer 38 and a lower channel layer 40, separated by a semiconductor spacer layer 42, where the channel layers 38 and 40 may be quantum well structures, for example, alternating layers of GaAs and AlAs. Although the castellation structures 36 include the two channel layers 38 and 40, this is by way of a non-limiting example in that the castellated structures 36 may only employ a single channel layer, or more than two channel layers. Further, a second semiconductor spacer layer 44 is provided between the lower channel layer 40 and the gate layer 18. A semiconductor cap layer 46 is grown on the upper channel layer 38 and insulates the upper channel layer 38 from the gate terminal 28. The spacer layers 42 and 44 and the cap layer 46 can be made of any suitable semiconductor material and have any suitable thickness for the purposes described herein. The side portion 32 of the gate terminal 28 encloses sides of the castellation structures 36 and is in electrical contact with the channel layers 38 and 40.

**[0010]** As is apparent, in this configuration, the gate terminal 28 is formed on top of each of the castellation structures 36 and around the sides of each of the castellation structures 36 so that a voltage potential from the gate terminal 28 is provided to sides and the top of the channel layers 38 and 40. Further, the gate terminal 28 is in electrical contact with the gate layer 18 so that the gate layer 18 is at the same potential as the terminal 28, which causes a current flow therethrough that generates an electric field applied to a bottom of the channel layers 38 and 40. The field effect from the upper, lateral and lower surfaces of the castellation structures 36 provides a more uniform channel flow in each of the channel layers 36 and 40 in each of the castellation structures 36. In other words, applying a modulation signal to all sides of the channel layers 38 and 40, provides a more uniform modulation of the electric field, which allows the WAGFET 10 to operate with higher linearity to amplify signals with different strengths. The modulating signals from the gate terminal 28 and the heavily doped gate layer 18 operate to populate the channel layers 38 and 40 in a uniform manner so that the performance of the channel layers 38 and 40 is improved. In this manner, the gate layer 18 can be grown on the base layers in the same manner as the castellation structures 36, where the gate terminal 28 is then deposited on top of the castellation structures 36, and where the gate layer 18 will ultimately act as a suitable conductor.

**[0011]** The foregoing discussion discloses and describes merely exemplary embodiments of the present invention. One skilled in the art will readily recognize from such discussion and from the accompanying drawings and claims that various changes, modifications and variations can be made therein without departing from the spirit and scope of the invention as defined in the following claims.

## CLAIMS

What is Claimed is:

1. A semiconductor device comprising:
  - a substrate;
  - a plurality of semiconductor layers deposited on the substrate;
  - a heavily doped gate layer deposited on the semiconductor
- 5 layers;
  - a plurality of castellation structures formed on the heavily doped layer and being spaced apart from each other, each castellation structure including at least one channel layer; and
  - a gate metal structure formed over the plurality of castellation
- 10 structures so that gate metal is deposited on the castellation structures and between the castellation structures to be in direct electrical contact with the heavily doped gate layer, wherein a voltage potential applied to the gate metal structure modulates the at least one channel layer in each castellation structure from an upper, lower and side direction.
2. The semiconductor device according to claim 1 wherein each castellation structure includes two channel layers separated by a spacer layer.
3. The semiconductor device according to claim 1 wherein each castellation structure includes a spacer layer between the at least one channel layer and the heavily doped layer.
4. The semiconductor device according to claim 1 wherein each castellation structure includes a cap layer on top of the at least one channel layer.
5. The semiconductor device according to claim 1 wherein the heavily doped layer is a heavily doped N-type GaAs layer.

6. The semiconductor device according to claim 1 wherein the at least one channel layer in each castellation structure is a quantum well structure.

7. The semiconductor device according to claim 1 wherein the substrate is a GaAs substrate.

8. The semiconductor device according to claim 1 wherein the semiconductor device is a field effect transistor.

9. A field effect transistor (FET) comprising:  
a substrate;  
a plurality of semiconductor layers deposited on the substrate;  
a heavily doped gate layer deposited on the semiconductor  
5 layers;

a plurality of castellation structures formed on the heavily doped layer and being spaced apart from each other, each castellation structure including an upper channel layer, a lower channel layer, a first spacer layer positioned between the upper and lower channel layers, a second spacer  
10 layer positioned between the lower channel layer and the heavily doped gate layer, and a cap layer positioned on top of the upper channel layer; and

a gate metal structure formed over the plurality of castellation structures so that gate metal is deposited on the castellation structures and between the castellation structures to be in direct electrical contact with the  
15 heavily doped gate layer, wherein a voltage potential applied to the gate metal structure modulates the channel layers in each castellation structure from an upper, lower and side direction.

10. The FET according to claim 9 wherein the heavily doped layer is a heavily doped N-type GaAs layer.

11. The FET according to claim 9 wherein the at least one channel layer in each castellation structure is a quantum well structure.

12. The FET according to claim 9 wherein the substrate is a GaAs substrate.

13. A method for fabricating a semiconductor device comprising:  
providing a substrate;  
epitaxially growing a plurality of semiconductor layers deposited on the substrate;

5 epitaxially growing a heavily doped gate layer on the semiconductor layers;

forming a plurality of castellation structures on the heavily doped layer and being spaced apart from each other, where each castellation structure includes at least one channel layer; and

10 forming a gate metal structure over the plurality of castellation structures so that gate metal is deposited on the castellation structures and between the castellation structures to be in direct electrical contact with the heavily doped gate layer, wherein a voltage potential applied to the gate metal structure modulates the at least one channel layer in each castellation  
15 structure from an upper, lower and side direction.

14. The method according to claim 13 wherein forming a plurality of castellation structures includes forming castellation structures including two channel layers separated by a spacer layer.

15. The method according to claim 13 wherein forming a plurality of castellation structures includes forming castellation structures including a spacer layer between the at least one channel layer and the heavily doped layer.

16. The method according to claim 13 wherein forming a plurality of castellation structures includes forming castellation structures including a cap layer on top of the at least one channel layer.

17. The method according to claim 13 wherein the heavily doped layer is a heavily doped N-type GaAs layer.

18. The method according to claim 13 wherein forming a plurality of castellation structures includes forming castellation structures where the at least one channel layer is a quantum well structure.

19. The method according to claim 13 wherein providing a substrate includes providing a GaAs substrate.

20. The method according to claim 13 wherein the semiconductor device is a field effect transistor.

AMENDED CLAIMS  
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What is Claimed:

1. A semiconductor device comprising:  
a substrate;  
a plurality of semiconductor layers deposited on the substrate;  
a heavily doped gate layer deposited on the semiconductor  
5 layers;  
a plurality of castellation structures formed on the heavily doped  
layer and being spaced apart from each other, each castellation structure  
including two channel layers separated by a semiconductor spacer layer that  
is in contact with both of the channel layers; and  
10 a gate metal structure formed over the plurality of castellation  
structures so that gate metal is deposited on the castellation structures and  
between the castellation structures to be in direct electrical contact with the  
heavily doped gate layer, wherein a voltage potential applied to the gate metal  
structure modulates the at least one channel layer in each castellation  
15 structure from an upper, lower and side direction.
2. Cancelled.
3. The semiconductor device according to claim 1 wherein each  
castellation structure includes a semiconductor spacer layer between a lower  
one of the two channel layers and the heavily doped layer so that the  
semiconductor spacer layer is in contact with the lower channel layer and the  
heavily doped layer.
4. The semiconductor device according to claim 1 wherein each  
castellation structure includes a cap layer on top of an upper one of the two  
channel layers.
5. The semiconductor device according to claim 1 wherein the  
heavily doped layer is a heavily doped N-type GaAs layer.

6. The semiconductor device according to claim 1 wherein the two channel layers in each the castellation structures are quantum well structures.

7. The semiconductor device according to claim 1 wherein the substrate is a GaAs substrate.

8. The semiconductor device according to claim 1 wherein the semiconductor device is a field effect transistor.

9. A field effect transistor (FET) comprising:  
a substrate;  
a plurality of semiconductor layers deposited on the substrate;  
a heavily doped gate layer deposited on the semiconductor  
5 layers;

a plurality of castellation structures formed on the heavily doped layer and being spaced apart from each other, each castellation structure including an upper channel layer, a lower channel layer, a first semiconductor spacer layer positioned between the upper and lower channel layers so that  
10 the first spacer layer is in contact with both the upper and lower channel layers, a second semiconductor spacer layer positioned between the lower channel layer and the heavily doped layer so that the second spacer layer is in contact with the lower channel layer and the heavily doped gate layer, and a cap layer positioned on top of the upper channel layer; and

15 a gate metal structure formed over the plurality of castellation structures so that gate metal is deposited on the castellation structures and between the castellation structures to be in direct electrical contact with the heavily doped gate layer, wherein a voltage potential applied to the gate metal structure modulates the channel layers in each castellation structure from an  
20 upper, lower and side direction.

10. The FET according to claim 9 wherein the heavily doped layer is a heavily doped N-type GaAs layer.

11. The FET according to claim 9 wherein the upper and lower channel layers in each castellation structure are quantum well structures.
12. The FET according to claim 9 wherein the substrate is a GaAs substrate
13. A method for fabricating a semiconductor device comprising:  
providing a substrate;  
epitaxially growing a plurality of semiconductor layers deposited on the substrate;  
5 epitaxially growing a heavily doped gate layer on the semiconductor layers;  
forming a plurality of castellation structures on the heavily doped layer and being spaced apart from each other, each castellation structure including two channel layers separated by a semiconductor spacer layer that  
10 is in contact with both of the channel layers; and  
forming a gate metal structure over the plurality of castellation structures so that gate metal is deposited on the castellation structures and between the castellation structures to be in direct electrical contact with the heavily doped gate layer, wherein a voltage potential applied to the gate metal  
15 structure modulates the at least one channel layer in each castellation structure from an upper, lower and side direction.
14. Cancelled.
15. The method according to claim 13 wherein forming a plurality of castellation structures includes forming castellation structures including a semiconductor spacer layer between a lower one of the channel layers and the heavily doped layer so that the semiconductor spacer layer is in contact with the lower channel layer and the heavily doped layer.
16. The method according to claim 13 wherein forming a plurality of castellation structures includes forming castellation structures including a cap layer on top of an upper one of the channel layers.

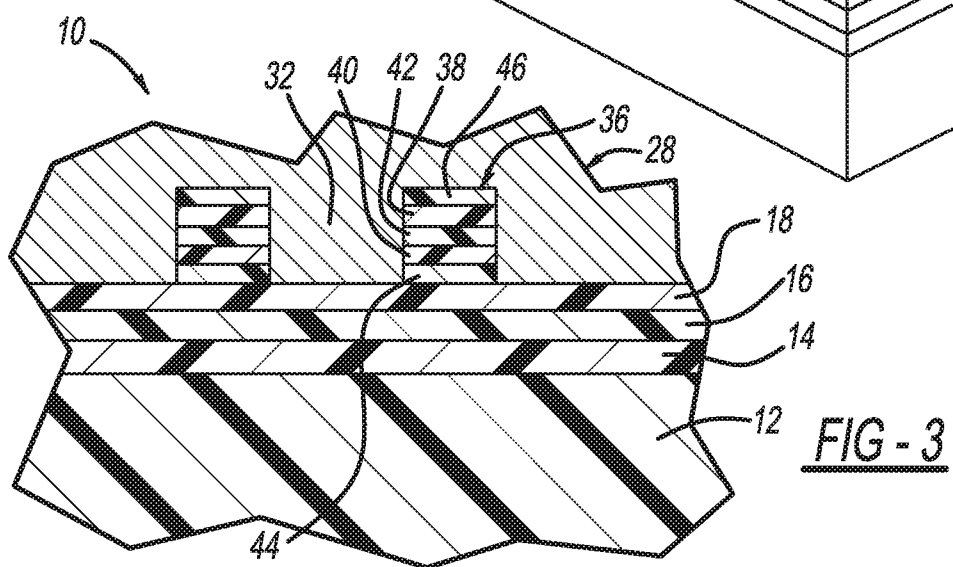
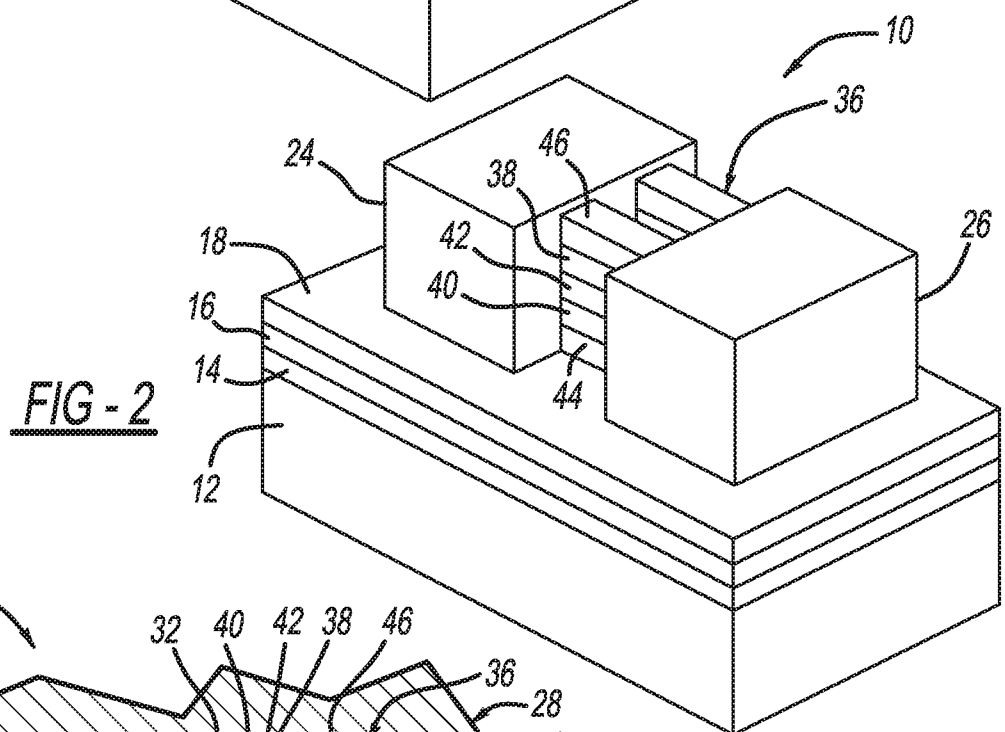
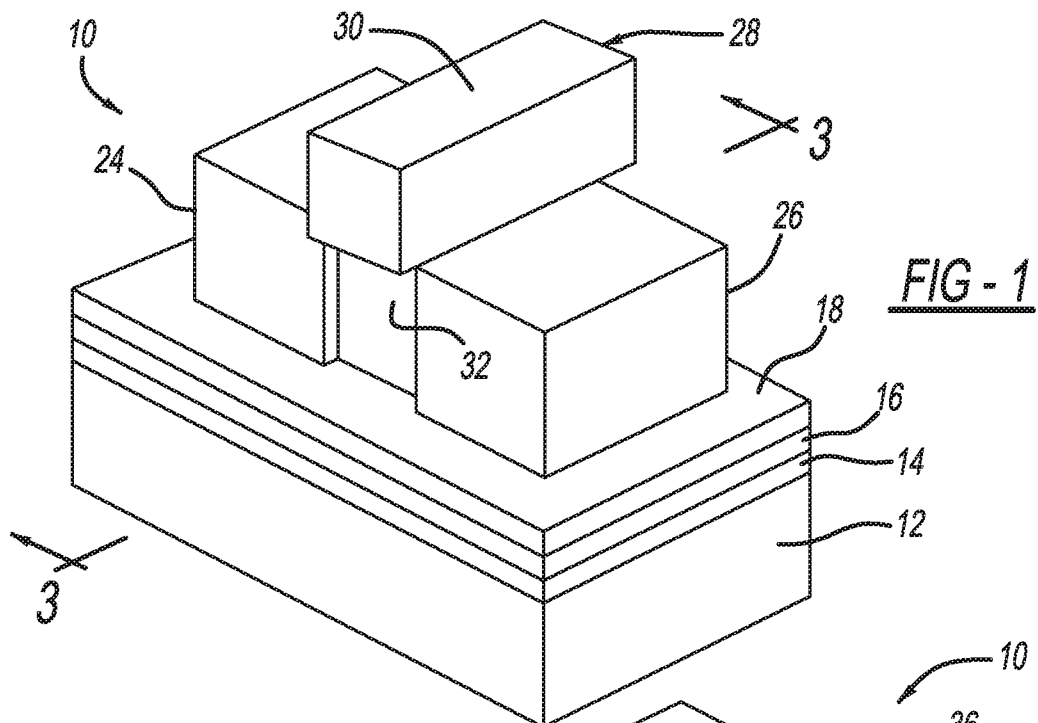
17. The method according to claim 13 wherein the heavily doped layer is a heavily doped N-type GaAs layer.

18. The method according to claim 13 wherein forming a plurality of castellation structures includes forming castellation structures where the two channel layers are quantum well structures.

19. The method according to claim 13 wherein providing a substrate includes providing a GaAs substrate.

20. The method according to claim 13 wherein the semiconductor device is a field effect transistor.

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# INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2017/030765

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| <b>A. CLASSIFICATION OF SUBJECT MATTER</b><br>INV. H01L29/06 H01L29/778 H01L21/331<br>ADD.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                               |                       |
| According to International Patent Classification (IPC) or to both national classification and IPC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                               |                       |
| <b>B. FIELDS SEARCHED</b><br>Minimum documentation searched (classification system followed by classification symbols)<br>H01L                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                               |                       |
| Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                               |                       |
| Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)<br>EPO-Internal, WPI Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                               |                       |
| <b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                               |                       |
| Category*                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Citation of document, with indication, where appropriate, of the relevant passages                                            | Relevant to claim No. |
| X                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | US 2015/123215 A1 (OBRADOVIC BORNA J [US] ET AL) 7 May 2015 (2015-05-07) paragraph [0019] - paragraph [0062]; figure 1A       | 1-20                  |
| A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | -----<br>US 2016/049504 A1 (RENALDO KAREN M [US] ET AL) 18 February 2016 (2016-02-18) paragraph [0046]; figure 1<br>-----     | 1-20                  |
| <div style="display: flex; justify-content: space-between; align-items: center;"> <div style="display: flex; align-items: center;"> <input type="checkbox"/> Further documents are listed in the continuation of Box C.         </div> <div style="display: flex; align-items: center;"> <input checked="" type="checkbox"/> See patent family annex.         </div> </div>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                                                               |                       |
| * Special categories of cited documents :                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                               |                       |
| <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier application or patent but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </div> <div style="width: 45%;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&amp;" document member of the same patent family</p> </div> </div> |                                                                                                                               |                       |
| Date of the actual completion of the international search<br><br><div style="text-align: center; font-size: 1.2em;">30 June 2017</div>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Date of mailing of the international search report<br><br><div style="text-align: center; font-size: 1.2em;">10/07/2017</div> |                       |
| Name and mailing address of the ISA/<br>European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040,<br>Fax: (+31-70) 340-3016                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Authorized officer<br><br><div style="text-align: center; font-size: 1.2em;">Diaz Alvarez, C</div>                            |                       |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s) | Publication<br>date |
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|                                           |                     | US 2016315152 A1           | 27-10-2016          |
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