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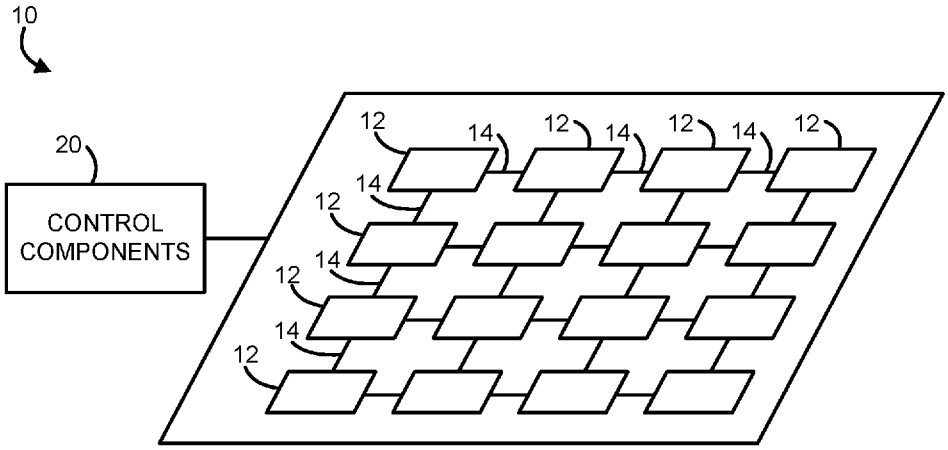

FIG. 1

(57) Abstract: Technologies for resource-efficient quantum error correction are disclosed. A quantum computer may include physical gate qubits, capable of general quantum gate operations such as single-qubit operations and nearest-neighbor two-qubit operations. Each physical qubit gate may be controllably coupled to a quantum memory. The quantum memory may have a lower per-gate error rate than the physical qubit gates as well as a lower per-qubit cost. Because errors accrue at a lower rate in the quantum memory, the physical gate qubits may be able to perform error correction for a large number of logical qubits in the quantum memory, even if the physical gate qubits have an error rate relatively close to an error threshold.

WO 2020/180902 A1

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TECHNOLOGIES FOR RESOURCE-EFFICIENT QUANTUM ERROR CORRECTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefit of U.S. Provisional Application No. 62/813,107, entitled "Technologies for Resource-Efficient Quantum Error Correction" and filed on March 3, 2019, the entirety of which is hereby incorporated by reference.

BACKGROUND

[0002] Quantum computing promises advances in solving problems that cannot be addressed with a classical computer, such as performing specific algorithms to efficiently solve certain problems, including, for example, factoring large numbers and performing simulations of large quantum systems. Quantum computers are susceptible to errors from sources such as unwanted interaction with the environment, but those errors can be corrected with quantum error correction techniques.

[0003] Quantum error correction techniques can be used to allow imperfect systems to implement quantum computing tasks with lower error rates than the error rate of a given physical gate qubit. However, there is a large overhead required to implement this quantum error correction, such as 1,000 to 10,000 physical gate qubits for each error-corrected logical qubit.

SUMMARY

[0004] According to one aspect of the disclosure, a system for resource-efficient quantum error correction comprises a plurality of physical gate qubits, wherein each of the plurality of physical gate qubits has an associated gate error rate; a quantum memory, wherein the quantum memory has an associated idle error rate, wherein the idle error rate of the quantum memory is less than the gate error rate of each of the plurality of physical gate qubits; and control components configured to perform an operation on a logical qubit using the plurality of physical gate qubits; transfer the logical qubit from the plurality of physical gate qubits to the quantum memory; store the logical qubit in the quantum memory for a time period based on the idle error rate of the quantum memory; transfer the logical qubit to the plurality of physical gate qubits; and perform a quantum error correcting code on the logical qubit using the plurality of physical gate qubits.

[0005] In some embodiments, the control components are further configured to sequentially perform an operation on each of a plurality of logical qubits using the plurality of physical gate qubits while the rest of the plurality of logical qubits are stored in the quantum

memory; and sequentially perform the quantum error correcting code on each of the plurality of logical qubits while the rest of the plurality of logical qubits are stored in the quantum memory, wherein to sequentially perform the quantum error correcting code on each of the plurality of logical qubits comprises to transfer the corresponding logical qubit of the plurality of logical qubits from the quantum memory to the physical gate qubits; perform the quantum error correcting code on the corresponding logical qubit of the plurality of logical qubits using the plurality of physical gate qubits; and transfer the corresponding logical qubit of the plurality of logical qubits from the physical gate qubits to the quantum memory.

[0006] In some embodiments, to sequentially perform the quantum error correcting code on each of the plurality of logical qubits comprises to determine, for each of the plurality of logical qubits, an error parameter based on (i) the number of operations performed on the corresponding logical qubit while loaded in the physical gate qubits and (ii) the amount of time the corresponding logical qubit was stored in the quantum memory; determine, for each of the plurality of logical qubits, whether the corresponding error parameter is greater than a threshold value; and perform, for each of the plurality of logical qubits, the quantum error correcting code based on a determination that the corresponding error parameter is greater than the threshold value.

[0007] In some embodiments, the quantum error correcting code is a surface code.

[0008] In some embodiments, the quantum error correcting code is a Gottesman-Kitaev-Preskill (GKP) code.

[0009] In some embodiments, the quantum error correcting code is a bosonic mode code.

[0010] In some embodiments, the quantum error correcting code is a biased error quantum error correction code.

[0011] In some embodiments, to store the logical qubit in the quantum memory comprises to store the logical qubit in a plurality of physical memory qubits in the quantum memory, wherein the control components are further configured to perform single-qubit operations on the physical memory qubits.

[0012] In some embodiments, the plurality of physical gate qubits comprises a plurality of transmon qubits.

[0013] In some embodiments, the plurality of physical gate qubits comprises a plurality of fluxonium qubits.

[0014] In some embodiments, to store the logical qubit in the quantum memory comprises to store the logical qubit in a plurality of modes of a superconducting three-dimensional cavity.

[0015] In some embodiments, to store the logical qubit in the quantum memory comprises to store the logical qubit in a plurality of modes of a superconducting two-dimensional cavity with a high kinetic inductance.

[0016] In some embodiments, to store the logical qubit in the quantum memory comprises to store the logical qubit in a state of an electron spin or nuclear spin.

[0017] In some embodiments, to store the logical qubit in the quantum memory comprises to store the logical qubit in a plurality of modes of a nanomechanical resonator.

[0018] In some embodiments, the control components are further configured to simultaneously perform an operation on each of a plurality of logical qubits loaded in the plurality of physical gate qubits.

[0019] In some embodiments, the control components are further configured to perform a non-error-correcting operation on a first logical qubit of the plurality of logical qubits while simultaneously performing the quantum error correcting code on a second logical qubit of the plurality of logical qubits.

[0020] In some embodiments, to store the logical qubit in the quantum memory for the time period based on the idle error rate of the quantum memory comprises to store the logical qubit in the quantum memory based on the idle error rate of the quantum memory, the gate error rate of each of the plurality of physical gate qubits, and a transfer error rate associated with transfer of the logical qubit between the plurality of physical gate qubits and the quantum memory.

[0021] According to one aspect of the disclosure, a method of storing qubits in a quantum error corrected memory comprises performing an operation on a logical qubit using a plurality of physical gate qubits, wherein each of the plurality of physical gate qubits has an associated gate error rate; transferring the logical qubit from the plurality of physical gate qubits to a quantum memory; storing the logical qubit in the quantum memory for a time period based on an idle error rate of the quantum memory, wherein the idle gate error rate is less than the gate error rate of each of the plurality of physical gate qubits; transferring the logical qubit to the plurality of physical gate qubits; and performing a quantum error correcting code on the logical qubit using the plurality of physical gate qubits.

[0022] In some embodiments, the method may further include sequentially performing an operation on each of a plurality of logical qubits using the plurality of physical gate qubits while the rest of the plurality of logical qubits are stored in the quantum memory; and sequentially performing the quantum error correcting code on each of the plurality of logical qubits while the rest of the plurality of logical qubits are stored in the quantum memory, wherein sequentially performing the quantum error correcting code on each of the plurality of

logical qubits comprises transferring the corresponding logical qubit of the plurality of logical qubits from the quantum memory to the physical gate qubits; performing the quantum error correcting code on the corresponding logical qubit of the plurality of logical qubits using the plurality of physical gate qubits; and transferring the corresponding logical qubit of the plurality of logical qubits from the physical gate qubits to the quantum memory.

[0023] In some embodiments, sequentially performing the quantum error correcting code on each of the plurality of logical qubits comprises determining, for each of the plurality of logical qubits, an error parameter based on (i) the number of operations performed on the corresponding logical qubit while loaded in the physical gate qubits and (ii) the amount of time the corresponding logical qubit was stored in the quantum memory; determining, for each of the plurality of logical qubits, whether the corresponding error parameter is greater than a threshold value; and performing, for each of the plurality of logical qubits, the quantum error correcting code based on a determination that the corresponding error parameter is past the threshold value.

[0024] In some embodiments, the quantum error correcting code is a surface code.

[0025] In some embodiments, the quantum error correcting code is a Gottesman-Kitaev-Preskill (GKP) code.

[0026] In some embodiments, the quantum error correcting code is a bosonic mode code.

[0027] In some embodiments, the quantum error correcting code is a biased error quantum error correction code.

[0028] In some embodiments, storing the logical qubit in the quantum memory comprises storing the logical qubit in a plurality of physical memory qubits in the quantum memory, the method further comprising performing single-qubit operations on the physical memory qubits.

[0029] In some embodiments, performing the operation on the logical qubit using the plurality of physical gate qubits comprises performing the operation on the logical qubit using a plurality of transmon qubits.

[0030] In some embodiments, performing the operation on the logical qubit using the plurality of physical gate qubits comprises performing the operation on the logical qubit using a plurality of fluxonium qubits.

[0031] In some embodiments, storing the logical qubit in the quantum memory comprises storing the logical qubit in a plurality of modes of a superconducting three-dimensional cavity.

[0032] In some embodiments, storing the logical qubit in the quantum memory comprises storing the logical qubit in a plurality of modes of a superconducting two-dimensional cavity with a high kinetic inductance.

[0033] In some embodiments, storing the logical qubit in the quantum memory comprises storing the logical qubit in a state of an electron spin or nuclear spin.

[0034] In some embodiments, storing the logical qubit in the quantum memory comprises storing the logical qubit in a plurality of modes of a nanomechanical resonator.

[0035] In some embodiments, the method may further include simultaneously performing an operation on each of a plurality of logical qubits loaded in the plurality of physical gate qubits.

[0036] In some embodiments, the method may further include performing a non-error-correcting operation on a first logical qubit of the plurality of logical qubits while simultaneously performing the quantum error correcting code on a second logical qubit of the plurality of logical qubits.

[0037] In some embodiments, storing the logical qubit in the quantum memory for the time period based on the idle error rate of the quantum memory comprises storing the logical qubit in the quantum memory based on the idle error rate of the quantum memory, the gate error rate of each of the plurality of physical gate qubits, and a transfer error rate associated with transfer of the logical qubit between the plurality of physical gate qubits and the quantum memory.

[0038] According to one aspect of the disclosure, a resource-efficient quantum error correction assembly comprises a quantum memory comprising a plurality of memory qubits having an associated idle error rate; and a quantum error correction circuit comprising a plurality of gate qubits having an associated error correction error rate, the idle error rate being less than the error correction error rate; wherein the quantum error correction circuit is configured to periodically perform a quantum error correction code on the plurality of memory qubits with a time period based on a ratio of the error correction error rate and the idle error rate.

[0039] In some embodiments, quantum error correcting operations comprise a surface code.

[0040] In some embodiments, quantum error correcting operations comprise a surface code having a code distance and the time period is based on a time when the numbers of idle errors is comparable to the code distance.

[0041] In some embodiments, the quantum error correcting code is a Gottesman-Kitaev-Preskill (GKP) code.

[0042] In some embodiments, the quantum error correcting code is a bosonic mode code.

[0043] In some embodiments, the quantum error correcting code is a biased error quantum error correction code.

[0044] In some embodiments, the plurality of memory qubits is a first logical qubit; the error correction circuit is associated with a plurality of logical qubits including the first logical qubit; and each logical qubit of the plurality of logical qubits has error correction code performed thereon periodically by the error correction code.

[0045] In some embodiments, the error correction circuit performs the error correction code sequentially on each of the logical qubits.

[0046] In some embodiments, the number of memory qubits in each logical qubit is based on the code distance, the idle error rate and the error correction error rate.

[0047] In some embodiments, the plurality of gate qubits of the error correction circuit is further configured to perform logical operations.

[0048] In some embodiments, the logical operations are fault-tolerant logical operations.

[0049] In some embodiments, the quantum memory is a random access quantum memory.

[0050] In some embodiments, the quantum memory comprises a superconducting three-dimensional cavity having a plurality of modes.

[0051] In some embodiments, the quantum memory comprises a plurality of electron spin states nuclear spin states.

[0052] In some embodiments, the quantum memory comprises a nanomechanical resonator having a plurality of modes.

[0053] In some embodiments, the plurality of gate qubits comprises a plurality of transmon qubits.

[0054] According to one aspect of the disclosure, a quantum computer comprises any of the resource-efficient quantum error correction assemblies described above.

[0055] According to one aspect of the disclosure, a quantum repeater comprises any of the resource-efficient quantum error correction assemblies described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0056] The concepts described herein are illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. Where considered appropriate,

reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0057] FIG. 1 is a schematic diagram of a quantum computer component with error-correction;

[0058] FIG. 2 is a schematic diagram of the quantum computer component of FIG. 1 with long-lived quantum memories;

[0059] FIG. 3 is a schematic diagram of a quantum computer that includes the quantum computer component with long-lived quantum memories of FIG. 2; and

[0060] FIG. 4 is a flow chart of a method of operating the quantum computer of FIG. 3.

DETAILED DESCRIPTION OF THE DRAWINGS

[0061] While the concepts of the present disclosure are susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and will be described herein in detail. It should be understood, however, that there is no intent to limit the concepts of the present disclosure to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives consistent with the present disclosure and the appended claims.

[0062] References in the specification to "one embodiment," "an embodiment," "an illustrative embodiment," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may or may not necessarily include that particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to effect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described. Additionally, it should be appreciated that items included in a list in the form of "at least one A, B, and C" can mean (A); (B); (C): (A and B); (B and C); (A and C); or (A, B, and C). Similarly, items listed in the form of "at least one of A, B, or C" can mean (A); (B); (C): (A and B); (B and C); (A and C); or (A, B, and C).

[0063] In the drawings, some structural or method features may be shown in specific arrangements and/or orderings. However, it should be appreciated that such specific arrangements and/or orderings may not be required. Rather, in some embodiments, such features may be arranged in a different manner and/or order than shown in the illustrative figures. Additionally, the inclusion of a structural or method feature in a particular figure is not meant to imply that such feature is required in all embodiments and, in some embodiments, may not be included or may be combined with other features.

[0064] Referring now to FIG. 1, an illustrative quantum computer component 10 includes several physical gate qubits 12 connected by qubit couplers 14. In the illustrative embodiment, the physical gate qubits 12 are a type of charge qubit called a transmission-line shunted plasma oscillation qubit, or transmon. In other embodiments, the physical gate qubits 12 may be any suitable physical gate qubit capable of performing the functions described herein, such as an electron spin on helium qubit, an atomic electron spin qubit, a nuclear spin qubit, a trapped ion qubit, a superconducting charge qubit, a superconducting flux qubit, a superconducting phase qubit, a quantum dot, a nanomechanical system, a fluxonium qubit, etc. The physical gate qubits 12 are capable of performing the single and multi-qubit gates necessary to perform general quantum computing tasks. For example, in the illustrative embodiment, each physical gate qubit 12 is capable of single-qubit operations such as single-qubit initialization, single-qubit rotations, and single-qubit measurement. Each physical gate qubit 12 in the illustrative embodiment is further capable of two-qubit interactions with neighboring physical gate qubits 12, such as a controlled-NOT (CNOT) gate and a swap operation. It should be appreciated that, in some embodiments, some or all of the physical gate qubits 12 may be able to interact with ancilla qubits (not shown), which may facilitate performing certain operations on a logical qubit represented by the physical gate qubits 12, as discussed in more detail below.

[0065] A relatively small grid of 16 physical gate qubits 12 in a four by four grid is shown in FIG. 1 in the interest of clarity. However, it should be appreciated that the quantum computer component 10 may include many more qubits, such as 900 physical gate qubits 12 in an array of 30 by 30, or any number of qubits up to, e.g, 10^6 arranged in a square, rectangular, or other grid pattern. It should be also appreciated that, while the physical gate qubits 12 may be physically laid out in a grid or grid-like pattern in some embodiments, the grid pattern is shown merely to indicate the nearest-neighbor interactions that are possible in the illustrative embodiment. More generally, the physical gate qubits 12 may be arranged in any suitable pattern or distribution, and the interactions possible between physical gate qubits 12 may not necessarily be limited to nearest-neighbor.

[0066] The qubit couplers 14 are configured to allow adjacent physical gate qubits 12 to interact. The physical implementation of the qubit couplers 14 will depend on the particular embodiments of the physical gate qubits 12. For example, if the physical gate qubits 12 are embodied as transmons, the qubit couplers 14 may be parametric Josephson couplers. If the physical gate qubits 12 are trapped ions, the qubit couplers 14 may be a system of lasers and other electronics capable of modulating the interaction between two physical gate qubits 12, including by physical movement of the physical gate qubits 12.

[0067] Operations on the physical gate qubits 12 will always have a chance of resulting in an error in the state of the physical gate qubits 12 after the operation. Each physical gate qubit 12 may have an associated gate error rate, and the gate error rate of the physical gate qubits 12 may be different. As used herein, unless noted otherwise, a gate error rate refers to a probability of some kind of an error that may occur in association with performing a gate on physical gate qubits 12. For example, a gate error rate may refer to a probability that a CNOT operation is followed by a random Pauli operator applied to one or both of the physical gate qubits 12 involved in the CNOT operation. It should be appreciated that, in various embodiments, the gate error rate may refer to different types of errors, such as a specific Pauli operator. Of course, in addition to errors caused during multi-qubit gates, the physical gate qubits 12 will be subject to some amount of errors in single-qubit operations, such as single-qubit rotations, measurement, and preparation.

[0068] In the illustrative embodiment, the physical gate qubits 12 are used to represent one or more logical qubits using a surface code, a type of error correcting code. Additionally or alternatively, in some embodiments, the physical gate qubits 12 may be used to implement a different type of error correction, such as a Steane code, a quantum low density parity check (LDPC) code, a Gottesman-Kitaev-Preskill (GKP) code, a multiple bosonic mode code, a biased error code, etc. The error correcting code may have a threshold for how high the gate error rate can be while still permitting error correction, such as 1% for a surface code. If the gate error gate is below the threshold by any amount, the error correcting code can be used to correct errors, although if the gate error is close to the threshold, the amount of resources required to implement the error correcting code may be large. The amount of error for performing a logic gates of a given physical gate qubit 12 (or physical gate qubits 12 for a multi-qubit gate) may be less than the error threshold for the error correcting code being implemented. For example, for a surface code with a 1% error threshold, the error rate for performing gates on the physical gate qubits 12 may be 0.1%. Of course, in some embodiments, the error rate for performing gates on the physical gate qubits 12 may be more or less than 0.1%, such as any error rate from 2% to 10^{-6}. It should be appreciated that, for a given error threshold of the surface code and the error rate for performing gates on the physical gate qubits 12, the resilience of the logical qubit to errors will depend on the number of physical gate qubits 12 used to represent the logical qubit.

[0069] It should be appreciated that, by manipulation of the physical gate qubits 12, the state of the logical qubit manipulated. The logical qubit may undergo, e.g., single-qubit operations such as a $Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$ operation, an $X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$ operation, or a Hadamard

operation $H=\frac{1}{\sqrt{2}}\begin{pmatrix}1 & 1\\ 1 & -1\end{pmatrix}$ by either manipulation of the physical gate qubits 12 or by implementing gates in the classical control software without any manipulation of the physical gate qubits 12. The logical qubits may undergo additional single-qubit operations such as $S=\begin{pmatrix}1 & 0\\ 0 & i\end{pmatrix}$ or $T=\begin{pmatrix}1 & 0\\ 0 & e^{i\pi/4}\end{pmatrix}$, also called the $\pi/8$ gate, by interacting with suitably-prepared ancilla qubits (not shown). Two-qubit gates between logical qubits is discussed in more detail below in regard to FIG. 3.

[0070] The quantum computer component 10 also includes control components 20. The control components 20 are capable of controlling the physical gate qubits 12 and the qubit couplers 14 shown in FIG. 1 and are capable of performing classical computing tasks, such as determining when error correction is required, what quantum gate operation should be performed, keeping track of gates implemented by software, etc. For example, if the physical gate qubits 12 are embodied as transmons, the control components 20 may be capable of controlling various current or voltage levels, applied magnetic fields, electromagnetic pulses applied to the physical gate qubits 12, etc. If the physical gate qubits 12 are embodied as trapped ions, the control components 20 may be capable of controlling a system of lasers and other electronics capable of modulating the interaction between two physical gate qubits 12, including by physical movement of the physical gate qubits 12. The control components 20 may be embodied as any suitable hardware or software capable of performing the functionality described herein, such as a classical computer, firmware, software, amplifiers, voltage sources, etc. In some embodiments, the control components 20 may compose or otherwise form a part of a quantum error correction circuit that is configured to perform or control the quantum error correction techniques described herein.

[0071] Referring now to FIG. 2, the quantum computer component 10 may further include a quantum memory 16 coupled to each physical gate qubit 12 through a memory qubit coupler 18. (The quantum memories 16 are omitted in FIG. 1 in the interest of clarity, but may be present in embodiments of the quantum computer component 10 shown in FIG. 1.) The quantum memory 16 may include one or more physical memory qubits. In the illustrative embodiment, each quantum memory 16 is a multi-mode quantum memory with a relatively long lifetime. For example, in the illustrative embodiment, each quantum memory 16 may be a multi-mode 3-D superconducting resonator, as described in U.S. patent application publication no. 2019/0288367 by Schuster *et al.*, entitled "TECHNOLOGIES FOR LONG-LIVED 3D MULTIMODE MICROWAVE CAVITIES," the entirety of which is incorporated by reference. Such a quantum memory 16 may have a large number of modes, such as 1,000 modes, each capable of operation as a physical memory qubit. In other embodiments, the quantum memories

16 may be a different type of quantum memory, such as a spin qubit, a photonic qubit, a nuclear qubit, a nanomechanical system, a two-dimensional multimode resonator, etc. For example, in some embodiments, a quantum memory may be embodied as one or more two-dimensional multimode resonators created with thin and narrow wires of a superconducting material with a high kinetic inductance. Such a resonator would have a slow effective speed of light and, as a result, a short effective wavelength. The short wavelength would permit resonators in small volumes far below the vacuum wavelength. Additionally, such resonators could have a meandering structure without significantly reducing the inductance. The memory qubit couplers 18, similar to the qubit couplers 14, are configured to allow physical gate qubits 12 to interact with the physical memory qubits in the corresponding quantum memory 16. In particular, the memory qubit couplers 18 are configured to swap the quantum state of the physical gate qubit 12 with the quantum state of a physical memory qubit in the quantum memory 16. The memory qubit couples 18 may swap the quantum state of the physical gate qubit 12 with the quantum state of any of the physical memory qubits in the quantum memory 16, allowing the quantum memory 16 to act as a random access memory, similar to a random access memory of a classical computer. The physical implementation of the memory qubit couplers 18 will depend on the particular embodiments of the physical gate qubits 12. For example, if the physical gate qubits 12 are embodied as transmons, the memory qubit couplers 18 may be parametric Josephson couplers.

[0072] The idle error rate of the quantum memory 16 refers to the probability of a single-qubit error in a unit of time associated with the physical gate qubits 12, such as the amount of time it takes to perform a multi-qubit operation on the physical gate qubits 12. For example, the idle error rate of the quantum memory 16 may refer to the probability that a random Pauli matrix is applied to any given qubit stored in the quantum memory in the time it takes to perform a multi-qubit operation on the physical gate qubits 12. In the illustrative embodiment, the quantum memory 16 is embodied as a 3-D superconducting resonator with qubits stored as electromagnetic modes in the resonator, with a per-gate idle error rate of, e.g., 10^{-6}. In other embodiments, the per-gate idle error rate may be other values, such as any value from 10^{-3} to 10^{-6}. It should be appreciated that, in some embodiments, each mode of a multi-mode quantum memory 16 may have a different error rate. An idle error rate of a quantum memory 16 may refer to a maximum error rate of the modes supported by the quantum memory 16, an average error rate of the modes supported by the quantum memory 16, or an error rate of a particular mode of the quantum memory 16. There may be an additional error rate associated with querying the quantum memory 16, such as storing a logical qubit from the physical gate

qubits 12 to the quantum memory 16 or loading a logical qubit from the quantum memory 16 to the physical gate qubits 12. The query error rate for such a transfer may be, e.g., 0.1%.

[0073] In the illustrative embodiment, the quantum memory 16 can store qubits but cannot otherwise manipulate them. In other embodiments, such as when the quantum memory 16 is a nuclear spin, the quantum memory 16 may be able to perform certain operations on qubits stored in the quantum memory, such as single-qubit gates, measurement, or two-qubit gates with only one other qubit.

[0074] It should be appreciated that the lower error rate of the quantum memories 16 may permit the quantum computer component 10 to concurrently maintain a larger number of error-corrected logical qubits than can be loaded into the physical gate qubits 12 at any one time. For example, if the per-gate error rate is 0.1% for the physical gate qubits and the per-gate error rate for idle qubits in the quantum memory 16 is 10^{-6}, error correction will have to be performed on the qubits in the quantum memory 16 approximately one thousand times less often than if the qubits stored in the quantum memory 16 were subject to the same error rate as the physical gate qubits 12. Such an approach allows for implementation of a quantum computer component 10 that has access to a large number of logical qubits with a relatively small number of physical gate qubits 12. Additionally, the per-qubit cost of the quantum memory 16 may be significantly lower than the per-qubit cost of the gate qubits. For example, a single quantum memory 16 made up of a single 3-D resonator may be able to store 1,000 qubits, while a single physical qubit 12 can only store one qubit.

[0075] In the illustrative embodiment, the error correcting code may be performed on the physical gate qubits 12 to correct any errors in the logical qubit. The error correcting code may be performed by performing single- and two-qubit gates and measurements on some or all of the physical gate qubits 12. The particular operations to be performed will depend on the error correcting code that is being used. The error correcting code may be performed continuously, continually, periodically, or when certain conditions are met. The conditions may be, e.g., when an error parameter reaches a certain threshold. An error parameter could be any parameter than indicates a likelihood of an error in a logical qubit. For example, an error parameter could be embodied as a sum of all errors accumulated by individual operations (i.e., three operations performed with a gate error rate of 0.1% could be represented by an error parameter of 0.3%). An error parameter could also be embodied as a probability of an unrecoverable error in the physical qubits 12 such that the value of the logical qubit cannot be corrected. An error parameter could also be embodied as a probability of an error in an individual physical qubit 12. An error parameter can represent errors from more than one source, such as from a gate error, an idle error in the physical qubit 12, an idle error in the

quantum memory 16, a transfer error to or from the quantum memory 16, etc. More generally, the calculation of an error parameter may depend on the particular error correcting code, the types of errors present in a given system, the number of physical gate qubits 12 used to represent a logical qubit, etc. The threshold used to determine when error correction is to be performed may also depend on the particular error correcting code, the types of errors present in a given system, the number of physical gate qubits 12 used to represent a logical qubit, a desired error rate of the logical qubits, etc.

[0076] It should be appreciated that the quantum computer component 10 may include control components 20 similar to those described in regard to FIG. 1 capable of controlling quantum memories 16 and the memory qubit couplers 18. The control components 20 are omitted from FIG. 2 in the interest of clarity.

[0077] Referring now to FIG. 3, a quantum computer 30 may include several quantum computer components 10. The illustrative quantum computer 30 includes 32 quantum computer components 10, one of which is labeled as such in FIG. 3. As noted above, each quantum computer component 10 may be able to represent one or more logical qubits in its physical gate qubits 12. The quantum computer 30 may then be able to represent several logical qubits, such as one logical qubit in each of 32 quantum computer components 10.

[0078] The quantum computer 30 is able to perform two-qubit gates between the logical qubits represented in different quantum computer components 10. In the illustrative embodiment, the quantum computing components 10 may be arranged in a grid, such as a four by eight grid shown in FIG. 3. In such an embodiment, physical gate qubits 12 in one quantum computer component 10 are able to interact with adjacent physical gate qubits 12 in the adjacent quantum computer component 10. It should be appreciated, however, that such an arrangement is merely one possibility, and the particular configuration may depend on the underlying physical gate qubits 12 used and the capabilities of those qubits. For example, the quantum computer 30 may include a different number of quantum computing components 10, such as any number from 2 to 128. It also should be appreciated that, in the illustrative embodiment, the configuration of the quantum computer 30 shown in FIG. 3 is a grid of 16 by 32 physical gate qubits 12. While the quantum computer 30 may separate the physical gate qubits 32 into blocks of quantum computing components 10, each of which represents a logical qubit, the quantum computer 30 may control the physical gate qubits 12 to operate in a different manner in different circumstances. For example, the quantum computer 30 may use a grid of 100 by 100 physical gate qubits 12 to represent 25 logical qubits, each corresponding to a grid of 20 by 20 physical gate qubits 12, and then the quantum computer 30 may use the same grid of 100 by 100 physical gate qubits 12 to represent 4 logical qubits, each corresponding to a grid of 50 by

50 physical gate qubits 12. It should be appreciated that using a larger number of physical gate qubits 12 will lead to better error protection at a cost of fewer logical qubits. Although shown as a grid 16 by 32 physical gate qubits 12, the quantum computer 30 may be include a grid of a different number of physical gate qubits 12, such as 120 by 240. More generally, the quantum computer 30 may include any number of physical gate qubits 12 that are able to perform nearest-neighbor interaction, such as any number from 2 to 10^6.

[0079] The approach to executing gates between logical qubits represented in different quantum computing components 10 may depend on the error correcting code used. For example, with a surface code, the quantum computer 30 may perform two-qubit gates between logical gates by performing a topological braid transformation that provides the logical CNOT operation in the logical qubits represented in the surface code. Interactions can also be done between logical qubits present in the same quantum computing component 10, such as between a first logical qubit present in the physical gate qubits 12 and a second logical qubit present in the quantum memory 16 of a selected quantum computing component 10. Such an interaction can be done by swapping the first logical qubit present in the physical gate qubits 12 of the selected quantum computing component 10 with the logical qubit in an adjacent quantum computing component 10, bringing the second logical qubit into the physical gate qubits 12 of the selected quantum computing component 10, and then interacting the two logical qubits present in the selected quantum computing component 10 and the adjacent quantum computing component 10. It should be appreciated that, in this way, any logical qubit in the quantum computer 30 can interact with any other logical qubit in the quantum computer 30. In analogy to a classical computer, the physical gate qubits 12 act as the classical processor, able to perform general computing tasks, and the quantum memory 16 acts as the classical memory, storing data that can be loaded into the processor.

[0080] As discussed above in regard to FIG. 2, it should be appreciated that, in addition to hardware to implement the quantum computing components 10, the quantum computer 30 may include control hardware and software capable of controlling the hardware shown in FIG. 3 and capable of performing classical computing tasks, such as determining when error correction is required, what quantum gate operation should be performed, keeping track of gates implemented by software, etc. The classical control hardware and software is not shown in FIG. 3 in the interest of clarity.

[0081] Referring now to FIG. 4, in use, the quantum computer 30 may perform a method 40 for performing quantum computing tasks. The method 40 begins in block 42, in which the quantum computer 30 loads target logical qubits from the quantum memory 16 into the physical gate qubits 12. Of course, in some instances, the target logical qubits may already

be present in the physical gate qubits 12, and no loading from the quantum memory 16 may be required.

[0082] In block 44, in which the quantum computer 30 performs an operation on the logical qubits using the physical gate qubits 12, such as a single- or multi-qubit gate. As discussed in more detail above, the operations on the logical qubits may be performed by performing single- and multi-qubit gates on the physical gate qubits 12, and the particular approach to performing operations on the logical qubits may depend on the particular implementation of an error correcting code.

[0083] In block 46, the quantum computer 30 determines whether error correction is required. The quantum computer 30 may determine whether error correction is required for the logical qubits present in some or all of the physical gate qubits 12 and/or may determine whether error correction is required for the logical qubits present in some or all of the quantum memory 16. An error correction may be required when an error parameter has reached a threshold value or will reach a threshold value by the time error correction can be performed. For example, multiple logical qubits in the quantum memory 16 may have a similar value for an error parameter that is slightly below the threshold. If the quantum computer 30 waits to perform error correction until the error parameters for all of those logical qubits are past the threshold, the errors will continue to accumulate past the error threshold for some of the logical qubits while the other logical qubits are having their errors corrected. It should be appreciated that, in some embodiments, the quantum computer 30 may determine that error correction is required for all of the logical qubits, and error correction may then be performed on each of the logical qubits in the quantum computer 30. In other embodiments, the quantum computer 30 may determine that error correction is only required for a subset of the logical qubits, and logical operations may be performed on some logical qubits in the physical gate qubits 12 of the quantum computer 30 at the same time that error correction operations are being performed on other logical qubits in the physical gate qubits 12 of the quantum computer 30.

[0084] In block 48, if the quantum computer 30 determines that error correction should not be performed, the method 400 loops back to block 42, in which the quantum computer 30 loads a target logical qubit from the quantum memory 16 into the physical gate qubits 12. If the quantum computer 30 determines that error correction should be performed, the method 400 proceeds to block 50. In block 50, the quantum computer 30 performs error correction on some or all of the logical qubits present in the physical gate qubits 12.

[0085] In block 52, the quantum computer determines whether additional error correction is required, such as on logical qubits present in the quantum memory 16. If the quantum computer determines that additional error is not required, the method 400 loops back

to block 42, in which the quantum computer 30 loads a target logical qubit from the quantum memory 16 into the physical gate qubits 12. If the quantum computer determines that additional error is required, the quantum computer 30 loads the next logical qubit selected for error correction from the quantum memory 16 into the physical gate qubits 12 in block 54, storing the logical qubit previously present in the physical gate qubits 12 in the quantum memory 16. The method 400 then loops back to block 50 to perform error correction on the logical qubit loaded into the physical gate qubits 12.

[0086] It should be appreciated that, in some embodiments, the quantum computer 30 may not be able to perform large-scale quantum computing tasks without error. For example, in some embodiments, all of the physical gate qubits 12 may have a gate error rate that is below the threshold for an error correcting code, but the quantum computer 30 may not have enough physical gate qubits 12 to correct errors in a logical qubit represented by the physical gate qubits 12 at an acceptably low error level. Such a quantum computer 30 may still perform complex quantum computing tasks suitable for, e.g., testing and/or simulation. In some embodiments, the quantum computer 30 may be incorporated into a quantum repeater, allowing for long-distance quantum communication such as quantum cryptography.

WHAT IS CLAIMED IS:

1. A system for resource-efficient quantum error correction, the system comprising:

a plurality of physical gate qubits, wherein each of the plurality of physical gate qubits has an associated gate error rate;

a quantum memory, wherein the quantum memory has an associated idle error rate, wherein the idle error rate of the quantum memory is less than the gate error rate of each of the plurality of physical gate qubits; and

control components configured to:

perform an operation on a logical qubit using the plurality of physical gate qubits;

transfer the logical qubit from the plurality of physical gate qubits to the quantum memory;

store the logical qubit in the quantum memory for a time period based on the idle error rate of the quantum memory;

transfer the logical qubit to the plurality of physical gate qubits; and

perform a quantum error correcting code on the logical qubit using the plurality of physical gate qubits.

2. The system of claim 1, wherein the control components are further configured to:

sequentially perform an operation on each of a plurality of logical qubits using the plurality of physical gate qubits while the rest of the plurality of logical qubits are stored in the quantum memory; and

sequentially perform the quantum error correcting code on each of the plurality of logical qubits while the rest of the plurality of logical qubits are stored in the quantum memory,

wherein to sequentially perform the quantum error correcting code on each of the plurality of logical qubits comprises to:

transfer the corresponding logical qubit of the plurality of logical qubits from the quantum memory to the physical gate qubits;

perform the quantum error correcting code on the corresponding logical qubit of the plurality of logical qubits using the plurality of physical gate qubits; and

transfer the corresponding logical qubit of the plurality of logical qubits from the physical gate qubits to the quantum memory.

3. The system of claim 2, wherein to sequentially perform the quantum error correcting code on each of the plurality of logical qubits comprises to:

determine, for each of the plurality of logical qubits, an error parameter based on (i) the number of operations performed on the corresponding logical qubit while loaded in the physical gate qubits and (ii) the amount of time the corresponding logical qubit was stored in the quantum memory;

determine, for each of the plurality of logical qubits, whether the corresponding error parameter is greater than a threshold value; and

perform, for each of the plurality of logical qubits, the quantum error correcting code based on a determination that the corresponding error parameter is greater than the threshold value.

4. The system of any of claims 1-3, wherein the quantum error correcting code is a surface code.

5. The system of any of claims 1-3, wherein the quantum error correcting code is a Gottesman-Kitaev-Preskill (GKP) code.

6. The system of any of claims 1-3, wherein the quantum error correcting code is a bosonic mode code.

7. The system of any of claims 1-3, wherein the quantum error correcting code is a biased error quantum error correction code.

8. The system of any of claims 1-3, wherein to store the logical qubit in the quantum memory comprises to store the logical qubit in a plurality of physical memory qubits in the quantum memory,

wherein the control components are further configured to perform single-qubit operations on the physical memory qubits.

9. The system of any of claims 1-3, wherein the plurality of physical gate qubits comprises a plurality of transmon qubits.

10. The system of any of claims 1-3, wherein the plurality of physical gate qubits comprises a plurality of fluxonium qubits.

11. The system of any of claims 1-3, wherein to store the logical qubit in the quantum memory comprises to store the logical qubit in a plurality of modes of a superconducting three-dimensional cavity.

12. The system of any of claims 1-3, wherein to store the logical qubit in the quantum memory comprises to store the logical qubit in a plurality of modes of a superconducting two-dimensional cavity with a high kinetic inductance.

13. The system of any of claims 1-3, wherein to store the logical qubit in the quantum memory comprises to store the logical qubit in a state of an electron spin or nuclear spin.

14. The system of any of claims 1-3, wherein to store the logical qubit in the quantum memory comprises to store the logical qubit in a plurality of modes of a nanomechanical resonator.

15. The system of any of claims 1-3, wherein the control components are further configured to simultaneously perform an operation on each of a plurality of logical qubits loaded in the plurality of physical gate qubits.

16. The system of claim 15, wherein the control components are further configured to perform a non-error-correcting operation on a first logical qubit of the plurality of logical qubits while simultaneously performing the quantum error correcting code on a second logical qubit of the plurality of logical qubits.

17. The system of any of claims 1-3, wherein to store the logical qubit in the quantum memory for the time period based on the idle error rate of the quantum memory comprises to store the logical qubit in the quantum memory based on the idle error rate of the quantum memory, the gate error rate of each of the plurality of physical gate qubits, and a transfer error rate associated with transfer of the logical qubit between the plurality of physical gate qubits and the quantum memory.

18. A method of storing qubits in a quantum error corrected memory, the method comprising:

performing an operation on a logical qubit using a plurality of physical gate qubits, wherein each of the plurality of physical gate qubits has an associated gate error rate;

transferring the logical qubit from the plurality of physical gate qubits to a quantum memory;

storing the logical qubit in the quantum memory for a time period based on an idle error rate of the quantum memory, wherein the idle gate error rate is less than the gate error rate of each of the plurality of physical gate qubits;

transferring the logical qubit to the plurality of physical gate qubits; and

performing a quantum error correcting code on the logical qubit using the plurality of physical gate qubits.

19. The method of claim 18, further comprising:

sequentially performing an operation on each of a plurality of logical qubits using the plurality of physical gate qubits while the rest of the plurality of logical qubits are stored in the quantum memory; and

sequentially performing the quantum error correcting code on each of the plurality of logical qubits while the rest of the plurality of logical qubits are stored in the quantum memory,

wherein sequentially performing the quantum error correcting code on each of the plurality of logical qubits comprises:

transferring the corresponding logical qubit of the plurality of logical qubits from the quantum memory to the physical gate qubits;

performing the quantum error correcting code on the corresponding logical qubit of the plurality of logical qubits using the plurality of physical gate qubits; and

transferring the corresponding logical qubit of the plurality of logical qubits from the physical gate qubits to the quantum memory.

20. The method of claim 19, wherein sequentially performing the quantum error correcting code on each of the plurality of logical qubits comprises:

determining, for each of the plurality of logical qubits, an error parameter based on (i) the number of operations performed on the corresponding logical qubit while loaded in the physical gate qubits and (ii) the amount of time the corresponding logical qubit was stored in the quantum memory;

determining, for each of the plurality of logical qubits, whether the corresponding error parameter is greater than a threshold value; and

performing, for each of the plurality of logical qubits, the quantum error correcting code based on a determination that the corresponding error parameter is past the threshold value.

21. The method of any of claims 18-20, wherein the quantum error correcting code is a surface code.

22. The method of any of claims 18-20, wherein the quantum error correcting code is a Gottesman-Kitaev-Preskill (GKP) code.

23. The method of any of claims 18-20, wherein the quantum error correcting code is a bosonic mode code.

24. The method of any of claims 18-20, wherein the quantum error correcting code is a biased error quantum error correction code.

25. The method of any of claims 18-20, wherein storing the logical qubit in the quantum memory comprises storing the logical qubit in a plurality of physical memory qubits in the quantum memory,

the method further comprising performing single-qubit operations on the physical memory qubits.

26. The method of any of claims 18-20, wherein performing the operation on the logical qubit using the plurality of physical gate qubits comprises performing the operation on the logical qubit using a plurality of transmon qubits.

27. The method of any of claims 18-20, wherein performing the operation on the logical qubit using the plurality of physical gate qubits comprises performing the operation on the logical qubit using a plurality of fluxonium qubits.

28. The method of any of claims 18-20, wherein storing the logical qubit in the quantum memory comprises storing the logical qubit in a plurality of modes of a superconducting three-dimensional cavity.

29. The method of any of claims 18-20, wherein storing the logical qubit in the quantum memory comprises storing the logical qubit in a plurality of modes of a superconducting two-dimensional cavity with a high kinetic inductance.

30. The method of any of claims 18-20, wherein storing the logical qubit in the quantum memory comprises storing the logical qubit in a state of an electron spin or nuclear spin.

31. The method of any of claims 18-20, wherein storing the logical qubit in the quantum memory comprises storing the logical qubit in a plurality of modes of a nanomechanical resonator.

32. The method of any of claims 18-20, further comprising simultaneously performing an operation on each of a plurality of logical qubits loaded in the plurality of physical gate qubits.

33. The method of any of claims 18-20, further comprising performing a non-error-correcting operation on a first logical qubit of the plurality of logical qubits while simultaneously performing the quantum error correcting code on a second logical qubit of the plurality of logical qubits.

34. The method of any of claims 18-20, wherein storing the logical qubit in the quantum memory for the time period based on the idle error rate of the quantum memory comprises storing the logical qubit in the quantum memory based on the idle error rate of the quantum memory, the gate error rate of each of the plurality of physical gate qubits, and a transfer error rate associated with transfer of the logical qubit between the plurality of physical gate qubits and the quantum memory.

35. A resource-efficient quantum error correction assembly comprising:

a quantum memory comprising a plurality of memory qubits having an associated idle error rate; and

a quantum error correction circuit comprising a plurality of gate qubits having an associated error correction error rate, the idle error rate being less than the error correction error rate;

wherein the quantum error correction circuit is configured to periodically perform a quantum error correction code on the plurality of memory qubits with a time period based on a ratio of the error correction error rate and the idle error rate.

36. The resource-efficient quantum error correction assembly of claim 35, wherein quantum error correcting operations comprise a surface code.

37. The resource-efficient quantum error correction assembly of claim 35, wherein quantum error correcting operations comprise a surface code having a code distance and the time period is based on a time when the numbers of idle errors is comparable to the code distance.

38. The resource-efficient quantum error correction assembly of claim 35, wherein the quantum error correcting code is a Gottesman-Kitaev-Preskill (GKP) code.

39. The resource-efficient quantum error correction assembly of claim 35, wherein the quantum error correcting code is a bosonic mode code.

40. The resource-efficient quantum error correction assembly of claim 35, wherein the quantum error correcting code is a biased error quantum error correction code.

41. The resource-efficient quantum error correction assembly of claim 35, wherein:

the plurality of memory qubits is a first logical qubit;

the error correction circuit is associated with a plurality of logical qubits including the first logical qubit; and

each logical qubit of the plurality of logical qubits has error correction code performed thereon periodically by the error correction code.

42. The resource-efficient quantum error correction assembly of claim 41, wherein the error correction circuit performs the error correction code sequentially on each of the logical qubits.

43. The resource-efficient quantum error correction assembly of claim 41, wherein the number of memory qubits in each logical qubit is based on the code distance, the idle error rate and the error correction error rate.

44. The resource-efficient quantum error correction assembly of any of claims 35-43 wherein the plurality of gate qubits of the error correction circuit is further configured to perform logical operations.

45. The resource-efficient quantum error correction assembly of claim 44 wherein the logical operations are fault-tolerant logical operations.

46. The resource-efficient quantum error correction assembly of any of claims 35-43, wherein the quantum memory is a random access quantum memory.

47. The resource-efficient quantum error correction assembly of any of claims 35-43, wherein the quantum memory comprises a superconducting three-dimensional cavity having a plurality of modes.

48. The resource-efficient quantum error correction assembly of any of claims 35-43, wherein the quantum memory comprises a plurality of electron spin states nuclear spin states.

49. The resource-efficient quantum error correction assembly of any of claims 35-43, wherein the quantum memory comprises a nanomechanical resonator having a plurality of modes.

50. The resource-efficient quantum error correction assembly of any of claims 35-43, wherein the plurality of gate qubits comprises a plurality of transmon qubits.

51. A quantum computer comprising the resource-efficient quantum error correction assembly of any of claims 35-50.

52. A quantum repeater comprising the resource-efficient quantum error correction assembly of any of claims 35-50.

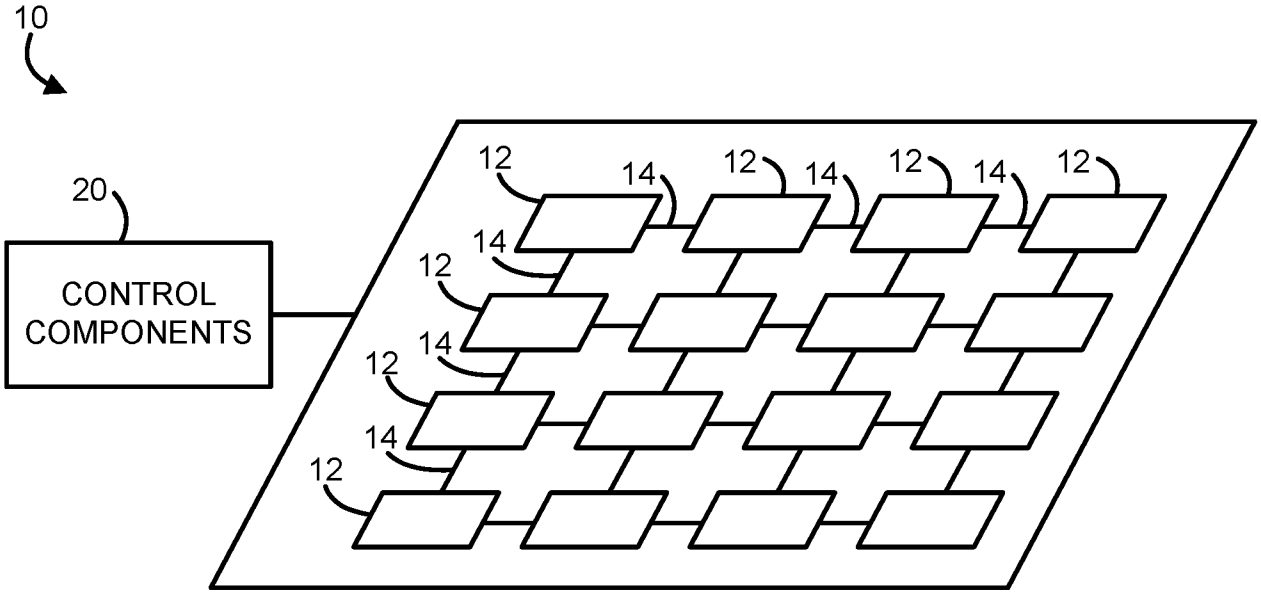

FIG. 1

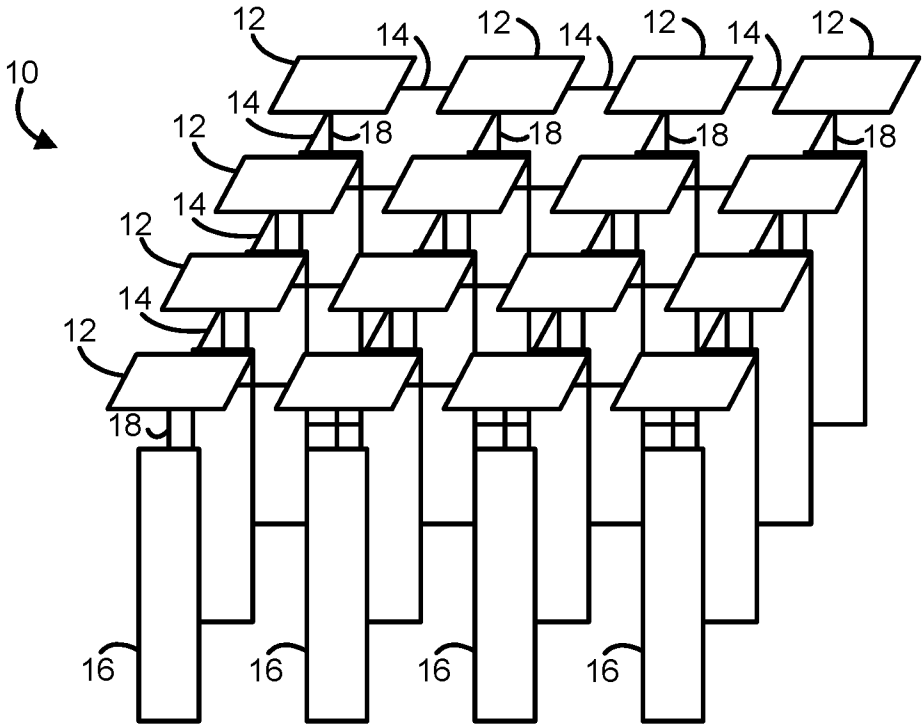

FIG. 2

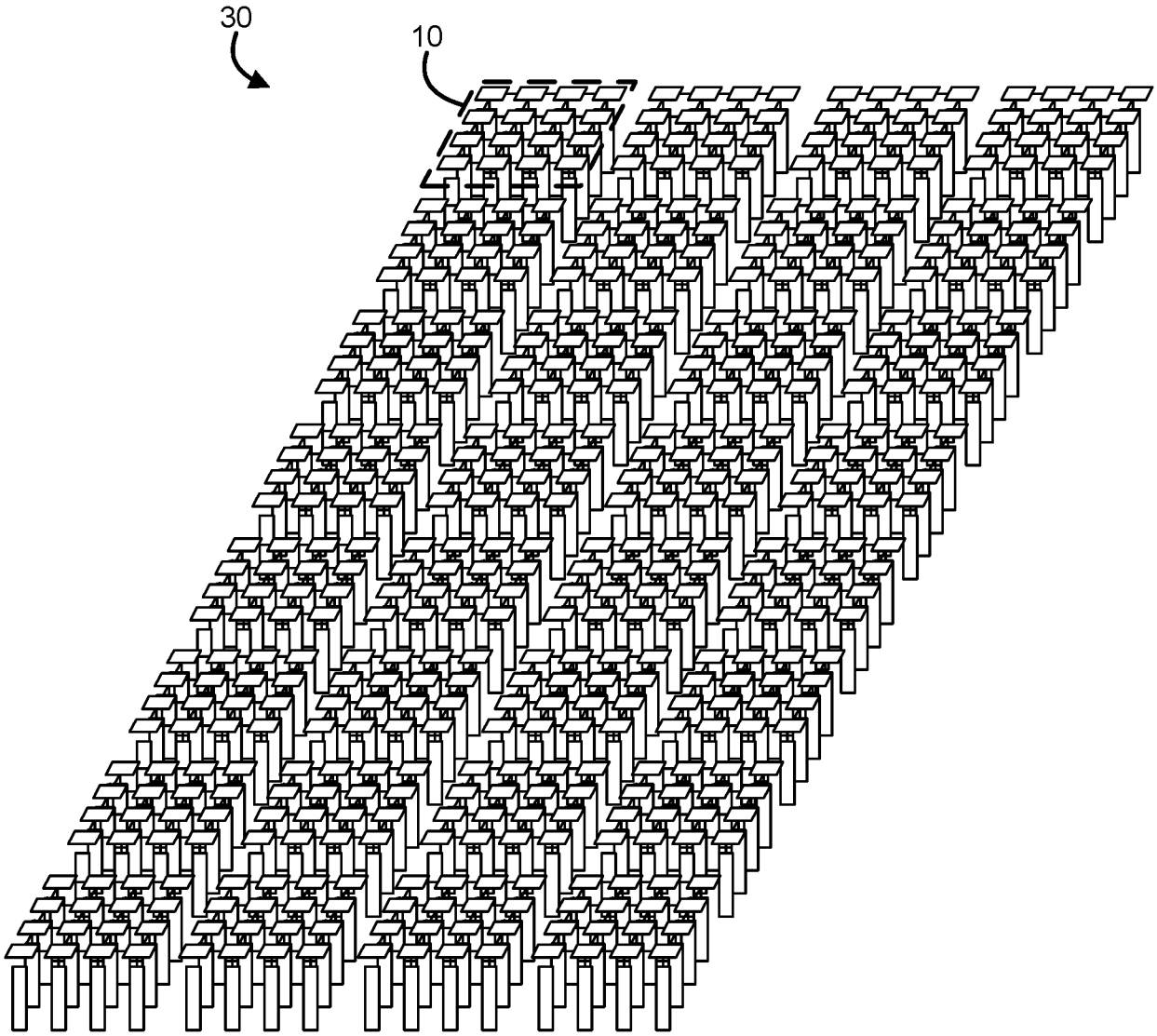

FIG. 3

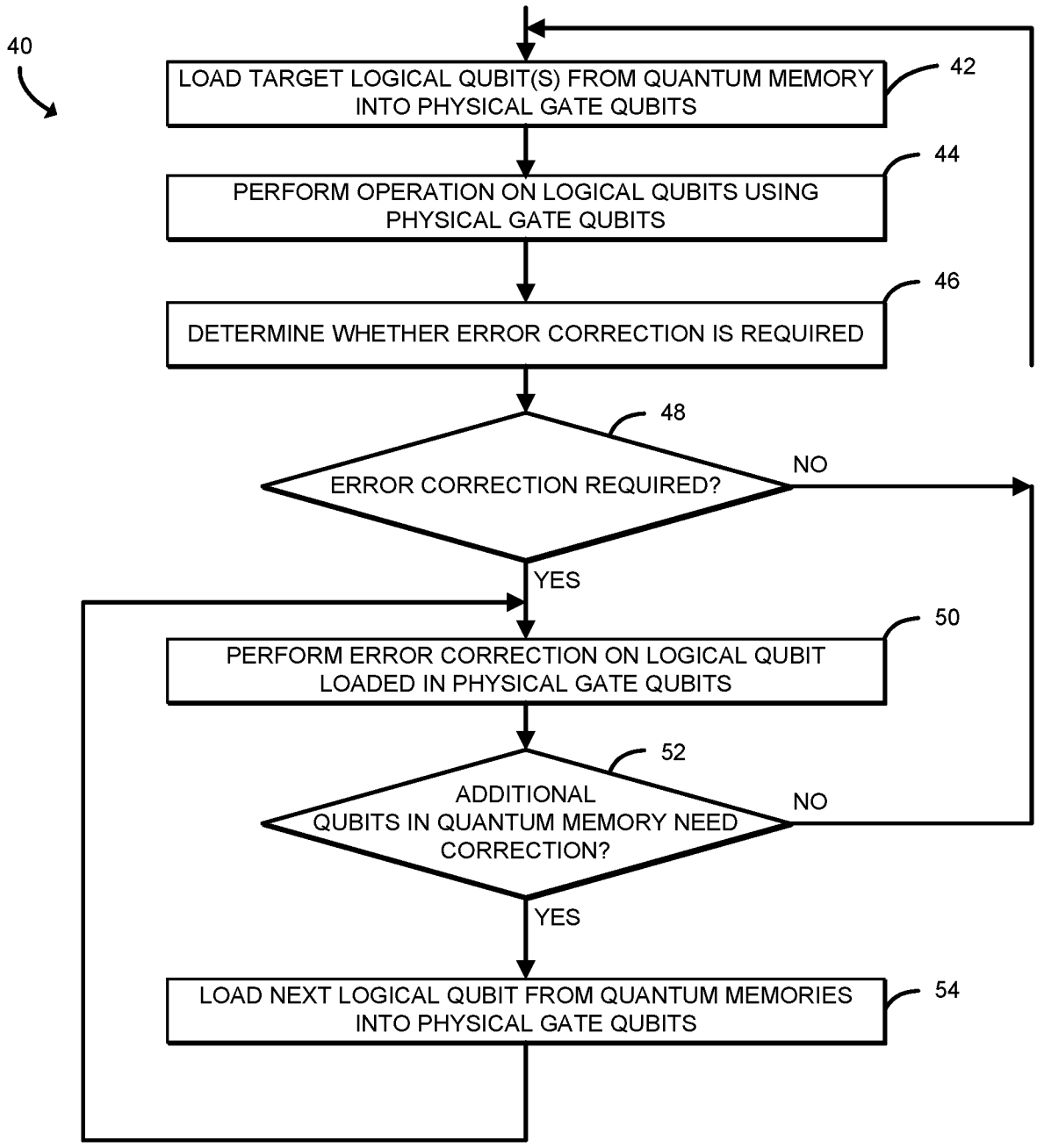
40
LOAD TARGET LOGICAL QUBIT(S) FROM QUANTUM MEMORY INTO PHYSICAL GATE QUBITS
42
PERFORM OPERATION ON LOGICAL QUBITS USING PHYSICAL GATE QUBITS
44
DETERMINE WHETHER ERROR CORRECTION IS REQUIRED
46
ERROR CORRECTION REQUIRED?
48
NO
YES
PERFORM ERROR CORRECTION ON LOGICAL QUBIT LOADED IN PHYSICAL GATE QUBITS
50
ADDITIONAL QUBITS IN QUANTUM MEMORY NEED CORRECTION?
52
NO
YES
LOAD NEXT LOGICAL QUBIT FROM QUANTUM MEMORIES INTO PHYSICAL GATE QUBITS
54

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/020851

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G06F 11/10; G06N 99/00; H01L 27/18; H01L 29/15; H01L 39/02 (2020.01)
CPC - G06N 10/00; G06F 11/10; G06N 20/00; H01L 27/18; H01L 39/02 (2020.05)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 257/14; 257/31; 714/758; 977/933 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/0185576 A1 (HOLLENBERG et al) 07 August 2008 (07.08.2008) entire document	1-50
A	US 2014/0365843 A1 (ALCATEL-LUCENT USA INC.) 11 December 2014 (11.12.2014) entire document	1-50
A	LEVY et al. "Implications of electronics constraints for solid-state quantum error correction and quantum circuit failure probability." In: New Journal of Physics. 16 August 2011 (16.08.2011) Retrieved on 27 April 2020 (27.04.2020) from <https://arxiv.org/ftp/arxiv/papers/1105/1105.0682.pdf> entire document	1-50
A	US 2016/0125311 A1 (NEWSOUTH INNOVATIONS PTY LIMITED et al) 05 May 2016 (05.05.2016) entire document	1-50
A	US 2012/0159272 A1 (PESETSKI et al) 21 June 2012 (21.06.2012) entire document	1-50
A	US 2016/0191077 A1 (KABUSHIKI KAISHA TOSHIBA) 30 June 2016 (30.06.2016) entire document	1-50

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2020	19 JUN 2020
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Authorized officer Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/020851

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 51, 52
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.