(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 January 2013 (03.01.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/002884 A1

(51) International Patent Classification:
G11C 5/02 (2006.01) *G11C 11/40* (2006.01)
G11C 5/06 (2006.01) *H01L 27/108* (2006.01)

(21) International Application Number:
PCT/US2012/034431

(22) International Filing Date:
20 April 2012 (20.04.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/169,864 27 June 2011 (27.06.2011) US

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **WANG, Yih** [—/US]; 12527 NW Forest Spring Lane, Portland, Oregon 97229 (US). **WEBB, M. Clair** [US/US]; 20180 SW Inglis Drive, Aloha, Oregon 97007 (US). **LINDERT, Nick** [US/US]; 5282 NW 140th Ave, Portland, Oregon 97229 (US). **SIVAKUMAR, Swaminathan** [US/US]; 12600 SW Crescent Street, #406, Beaverton, Oregon 97005 (US). **ZHANG, Kevin X.** [US/US]; 1807 NW Pentland Street, Portland, Oregon 97229 (US). **SOMASEKHAR, Dinesh** [IN/US]; 621 NW 112th Avenue, Portland, Oregon 97229 (US).

(74) Agents: **VINCENT, Lester J.** et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 1279 Oakmead Parkway, Sunnyvale, California 94085-4040 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

[Continued on next page]

(54) Title: 6F^2 DRAM CELL

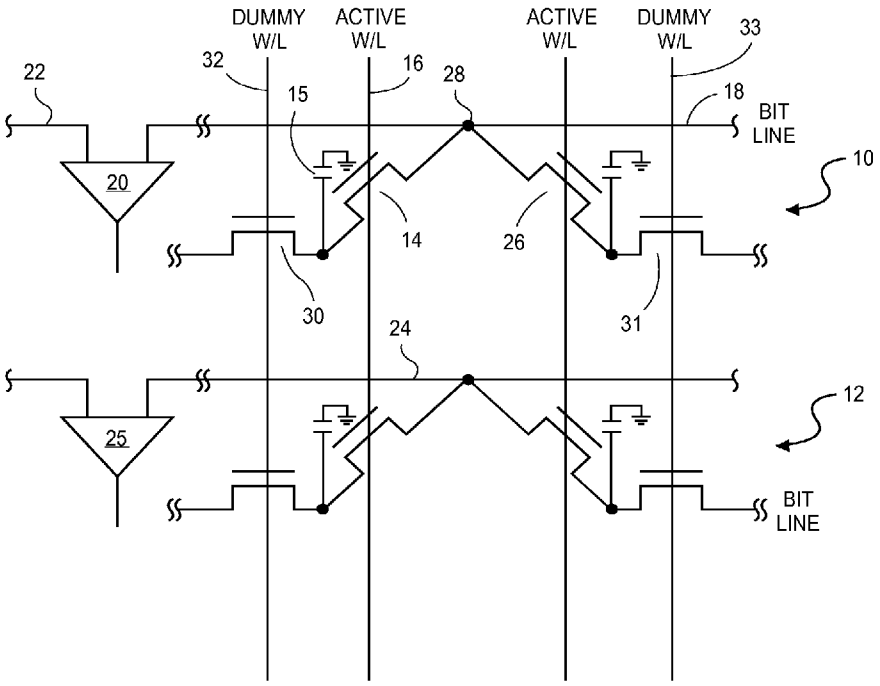


FIG. 1

(57) Abstract: A 6F^2 DRAM cell with paired cells is described. In one embodiment the cell pairs are separated by n-type isolation transistors having gates defining dummy word lines. The dummy word lines are fabricated from a metal with a work function favoring p-channel devices.

WO 2013/002884 A1

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

$6F^2$ DRAM Cell

FIELD OF THE INVENTION

The invention relates to dynamic random access memory (DRAM) cells.

PRIOR ART

Integrated circuit transistors are often isolated from one another with oxide regions. Two common techniques for forming these regions are: (i) the local oxidation of silicon (LOCOS) using openings in a silicon nitride layer, and (ii) shallow trench isolation (STI) where shallow trenches are filled with oxide. Neither is easily scaled and careful layout is required to realize DRAM cells with an area of 8F2 or smaller.

U.S. Patent 6,545,904 describes a 6F2 DRAM cell where isolation is obtained from a combination of isolation transistors and STI. The gate oxide in the isolation transistors is thicker than the oxides used in the DRAM access transistors providing greater isolation.

P+ polysilicon gates for n-channel access transistors and isolation transistors are suggested as another method to achieve 6F2 DRAM cells. See "Data Retention Time in DRAM with WSix/P+ ply-Si Gate NMOS Cell Transistors," by Hiroshi Kiuirai et al. Electronic Devices Meeting, 2001, IEDM Technical Digest International, beginning at page 395. Another technique for 6F2 DRAM cells in a bit-line overcapacitor cell using LOCOS and isolation transistors is described in "Fully Self-Aligned 6F2 Cell Technology for Low Cost 1Gb DRAM," by Masami Aoki et al. 1996 Symposium on VLSI Technology Digest of Technical Papers, beginning on page 22.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an electrical schematic illustrating paired dynamic random access memory (DRAM) cells laid out in accordance with one embodiment of the present description.

Figure 2 is a plan view of the cell pairs showing their contacts to overlying bit lines and overlying capacitors.

Figure 3 is a cross-sectional, elevation view of a capacitor contact and overlying capacitor taking generally through section lines 3-3 of Figure 2.

Figure 4 is a cross-sectional, elevation view of a metal word line forming a gate for an access transistor taken generally taken through section line 4-4 of Figure 2.

Figure 5 is a cross-sectional, elevation view illustrating the contact to a bit line from an underlying source/drain region of an access transistor.

Figure 6 is a plan view showing angled diffusions used in another embodiment where a 6F2 cell is realized without isolation transistors.

DETAILED DESCRIPTION

In the following description 6F2 DRAM cells are described. Numerous specific details are set forth in order to provide a thorough understanding of the cells and their use in an array such as the capacitor contact structure of Figure 3. It will be apparent to one skilled in the art that these specific details are but one way to achieve the claimed memory. In other instances, well-known processes for fabricating DRAM cells are not described in detail in order not to unnecessarily obscure the present invention.

The described cells are particularly useful for embedded DRAMs since they are compatible with logic CMOS technology.

In Figure 1, two pairs of cells 10 and 12 are illustrated. Each cell comprises an access transistor and capacitor such as transistor 14 and capacitor 15. A source/drain region of the access transistor 14 is connected to an overlying bit line 18 by contact 28. One cell in each pair of cells is accessed by the potential on word line 16. Each bit line is connected to one input of a sense amplifier such as sense amp 20; the other input of sense amp 20 is connected to a bit line 22 extending over another portion of a DRAM array. Similarly, the pair of cells 12 is connected to a bit line 24 providing one input to the sense amp 25.

The channel regions of the access transistors 14 and 26 are angled with respect to the bit lines and word lines. As will be seen in Figure 2 this reduces the horizontal dimension of the cell pairs and more readily facilitates a single contact 28 to the overlying bit line 18 for a cell pair.

Isolation between each cell pair and its neighboring cell pairs (along a given bit line) is obtained through isolation transistors, such as transistors 30 and 31 of Figure 1. The gates of these transistors define dummy word lines such as lines 32 and 33 of Figure 1. These dummy word lines are fabricated in a replacement gate process from a metal with a work function favoring a p-type device even though the source/drain regions for the transistors 30 and 31, as well as the source/drain regions of the access transistors 14 and 26, are all n-type regions. The access transistors have metal gates with a work function favoring n-type devices. The cells for the layout of Figure 2 have an effective area of 6F2 and are fabricated with a logic-based fabrication process.

(F is defined as one-half the minimum pitch, with minimum pitch being the minimum line width plus the width of a space immediately adjacent the line on one side of the line and the next adjacent line in a repeated pattern. For the layout of Figure 2, bit lines are in a horizontal direction and word lines are in a vertical direction. The bit lines are on a 2F half-metal pitch. Each cell's horizontal dimension is on a 1.5 gate pitch or 3F half-gate pitch. This yields a cell area of 6F2.)

The layout of Figure 2 can be fabricated on a bulk silicon substrate or on a silicon-on-insulator (SOI) substrate. In one embodiment serpentine shaped fin-like, semiconductor bodies 40, 41 and 42 are etched from a p-type bulk silicon substrate, each of the bodies 40, 41 and 42 are generally parallel to an adjacent bit line such as bit lines 43, 44 and 45, respectively. The continuous bodies, such as body 42, include "lambda" shaped segments formed at, for instance, the regions 48 of body 42. The bodies 40, 41 and 42 include the n-type source/drain regions for both the access transistors and isolation transistors as well as the channel regions for these transistors. It should be noted that while raised bodies are used in a tri-gate process for one embodiment, this is not necessary to the layout, for instance the source/drain and the channel regions defined therebetween can be formed directly in a bulk silicon.

STI regions are formed in the horizontal direction between the lines 40, 41 and 42. And as mentioned, vertical isolation between cells pairs is provided by the isolation transistors which are defined at the intersection of the semiconductor bodies and the vertically disposed dummy word lines such as dummy word lines 52 and 53 of Figure 2. Each pair of cells is isolated from a neighboring pair of cells along a given silicon body, such as body 40, by isolation transistors disposed on opposite sides of the cell pairs. Each of the isolation transistors includes a source/drain region such as regions 72 and 74 with a channel region defined therebetween. The access word lines, such as word lines 50 and 51, are formed between the dummy word lines 52 and 53 defining gates for the access transistors.

The generally horizontally disposed bit lines, such as bit lines 43, 44 and 45 are metal lines formed in, for instance, a metal 1 layer disposed above the substrate generally perpendicular to the word lines. All the access transistors associated with a given bit line (e.g. the access transistors formed along body 40 for bit line 43) have via contacts, such as contacts 60 and 61, so that a source/drain region from each access transistor in a pair of access transistors is connected to the bit line through a single via contact. Consequently the access transistor with the source/drain regions 63 and 64 (defining the angled channel region 65) as well as the access transistor with the source/drain regions 66 and 68 (defining the angled channel region 70) are connected to the word line 43 through the common via contact 61.

The other source/drain region of each access transistors is connected to a capacitor by a contact via, such as contacts 75 and 76. As will be seen best from Figure 3, the capacitor over bit line (COB) layout facilitates the 6F2 cell size and also eliminates the need for substrate level processing steps not necessarily compatible with a logic process that would otherwise be needed where substrate regions are used in the formation of a capacitor.

All the source/drain regions for the layout of Figure 2 are n+ regions. Consequently, both the access transistors and isolation transistors are n channel devices. However, the metal lines

defining the gates for the isolation transistors comprise a material favoring a p-type device, more specifically a metal with a work function between approximately 4.8 to 5.1 eV. In contrast, the access word lines defining the gates of the access transistors are fabricated from a metal with a work function favoring n-type devices, more specifically a metal with a work function between approximately 4.0 to 4.2 eV.

In one embodiment, the dummy word lines are maintained at a potential less than zero volts (relative to zero volts of the substrate). Also, the access word lines, when not selecting a column of access transistors, are maintained at this same potential of less than zero volts. Word line selection which may be used for the layout of Figure 2 is described in "NOR Word Line Selection," Application No. 12/928,989, filed 12/20/2010, and "NAND Logic Word Line Selection," Application No. 12/928,949, filed 12/20/2010. A hierarchical DRAM sensing arrangement that may be used with the array of Figure 2 is described in "Hierarchical DRAM Sensing," Application No. 12/928,948, filed 12/20/2010. All three of the above-referenced applications are assigned to the assignee of the present application.

In Figure 3 a capacitor and via contact for a single DRAM cell is shown in a cross-sectional view. A semiconductor substrate 81 includes an integral body having a source/drain region beneath the via contact 86. Contact 86 is surrounded by an insulator, sometimes referred to as the 0 level interlayer dielectric (ILD). In the first level ILD the via contact comprises the plug 87 (for instance a tungsten plug) extending from the contact 86 to the damascene copper inlay 88. Note there is an opening formed through the etchant stop layers 85 which separates each of the ILD layers for contact to an underlying layer. Again in the second ILD, the via contact comprises a plug 91 with an overlying damascene copper inlay 90. The capacitor is formed in the ILD layers 3 and 4 for the illustrated embodiment. It includes a first plate 92 which makes contact with the underlying inlay 90. An insulator 93 insulates the plate 92 from the inner, second, plate 94. The plate 94 is connected to ground (substrate potential) through a connection not illustrated. Note that at each higher ILD level the line spacing increases. However, there is sufficient spacing between the capacitors for the illustrated embodiment to allow the fabrication of the cells within the 6F2 area for this COB cell. The fabrication of the capacitor is described in co-pending Application Serial No. 13/041,170, assigned to the assignee of the present application.

Figure 4, taken through section line 4-4 of Figure 2, shows a semiconductor body, such as body 41 of Figure 2, and an overlying metal word line 50 insulated from the body as is typically the case with field-effect transistors. In one process for fabricating the array of Figure 2, the word lines are initially formed from a sacrificial polysilicon layer and then after the source/drain regions for the transistors are doped in alignment with the sacrificial gate, a replacement gate

process is used to replace the polysilicon with the metal word line. For Figure 4 the metal word line 50 is one that has a work function favoring n-channel devices.

Figure 5, taken through section line 5-5 of Figure 2, shows a contact from an overlying bit line 43 to a semiconductor body 40 which is a source/drain region. This bit line is formed in the first metal layer. A contact 100 connects the bit line 43 and plug 101 to the body 40 (source/drain region) disposed between the two access transistors in the paired cell layout of Figure 2. Once again an ILD 0 is shown along with an etchant stop layer 85.

Figure 6 is an alternate layout where the DRAM COB cells are organized as linear pairs without the dummy word lines. A single cell is shown within the regions 130. A pair of cells is formed in each of the diffusion zones 120. (Note that not all the diffusion zones 120 are shown.) The cells are paired in a linear arrangement without the serpentine body of Figure 2. STI is used between each of the diffusions. All the diffusions for the cells occur at the same angle relative to the principal angles of the wafer. Consequently, a wafer is positioned in the same off-axis orientation for both channel implants and source/drain implants.

All the word lines shown in Figure 6, specifically lines 105, 106, 107, 108 and 109 are access word lines. A word line is positive when selected and maintained at a negative potential when deselected. Bit lines are not shown but are disposed horizontally across the bit line contacts 110. Each cell pair shares a bit line contact 110 disposed midway between its cells.

As can be seen from the rectangular block 112, a cell has an area equal to 6F2, 3F of which runs in the word line direction for this embodiment and 2F extends from word line to word line such as from word lines 105 to 106.

Thus, DRAM layouts have been described where the cells are paired using a common bit line contact and where the cells have an area equal to 6F2.

CLAIMS

What is claimed is:

1. A DRAM array comprising:

a pair of cells, each cell comprising an access transistor having n-type source/drain regions defining a channel region, and a capacitor, one source/drain region of each access transistor in a first pair of cells being connected to a common via contact providing a connection to a bit line, the other source/drain region of each access transistor being separated from other source/drain regions of access transistors of adjacent pairs of cells by common channel regions defined by the n-type source/drain regions;

access word lines extending generally perpendicular to the bit line, each access word line extending over a channel region of an access transistor, the access word lines comprising a material with a work function favoring n-channel devices; and

dummy word lines extending generally perpendicular to the bit line, each dummy word line extending over one of the common channel regions, the dummy word lines comprise a material with a work function favoring p-channel devices.

2. The array of claim 1, wherein the work function for the dummy word lines is approximately 4.8 – 5.1 eV.

3. The array of claim 1, wherein the dummy word is coupled to a negative potential with respect to a substrate potential.

4. The array of claim 3, including via contacts connected to the other source/drain regions of the access transistors for providing a connection to overlying capacitors.

5. The array of claim 4, wherein the bit line is a metal line disposed above the pairs of cells in the array.

6. The array of claim 5, wherein the capacitors are disposed above the bit lines.

7. The array of claim 1, wherein the channel regions of the access transistors are angled with respect to their source/drain regions.

8. The array of claim 6, wherein the channel regions of the access transistors are angled with respect to their source/drain regions.

9. The array of claim 7, wherein the source/drain regions, access transistor channel regions, and common channel regions are formed from a continuous serpentine-shaped semiconductor body disposed generally perpendicular to the word lines.

10. The array of claim 8, wherein the source/drain regions, access transistor channel regions, and common channel regions are formed from a continuous serpentine-shaped semiconductor body disposed generally perpendicular to the word lines.

11. The array of claim 10, wherein each cell has an area of approximately $6F^2$.

12. A DRAM array comprising:

a pair of cells, each cell comprising an access transistor having n-type source/drain regions defining a channel region, and a capacitor, one source/drain region of each access transistor in a first pair of cells being connected to a common via contact providing a connection to a bit line;

access word lines extending generally perpendicular to the bit line, each access word line extending over a channel region of an access transistor, the access word lines comprising a material with a work function favoring n-channel devices; and

wherein the channel regions of the access transistors are angled with respect to their source/drain regions.

13. The DRAM of claim 12, wherein the access word lines are maintained at a negative potential with respect to a substrate potential when the access word line is deselected.

14. The DRAM of claim 13, wherein the access word lines are fabricated from a metal having a work function of between approximately 4.0 to 4.2 eV.

15. The DRAM of claim 12, wherein the other source/drain region of each access transistor are separated from other source/drain regions of access transistors of adjacent pairs of cells by common channel regions defined by n-type source/drain regions, and including dummy word lines extending generally perpendicular to the bit line, each dummy word line extending over one of the common channel regions, the dummy word lines comprise a material with a work function favoring p-channel devices.

16. The array of claim 15, wherein the work function for the dummy word lines is approximately 4.8 – 5.1 eV.

17. The array of claim 16, including via contacts connected to the other source/drain regions of the access transistors for providing a connection to overlying capacitors.

18. The array of claim 17, wherein the bit line is a metal line disposed above a substrate.

19. The array of claim 18, wherein the capacitors are disposed above the bit lines.

20. A DRAM array comprising:

a pair of cells, each cell comprising an access transistor having n-type source/drain regions defining a channel region, and a capacitor, one source/drain region of each access transistor in a first pair of cells being connected to a common via contact providing a connection to a bit line;

access word lines extending generally perpendicular to the bit line, each access word line extending over a channel region of an access transistor, the access word lines comprising a material with a work function favoring n-channel devices; and

wherein the word lines are maintained at a negative potential with respect to a substrate potential when the access word line is deselected.

21. The DRAM of claim 20, wherein each pair of cells is disposed in a common diffusion zone.

22. The DRAM of claim 21, wherein each of the diffusion zones are separated by shallow trench isolation.

23. The DRAM of claim 21, wherein each diffusion zone is angled at the same angle with respect to the access word lines.

24. The DRAM of claim 23, wherein the common via contact for each pair of cells is located approximately midway in each diffusion zone.

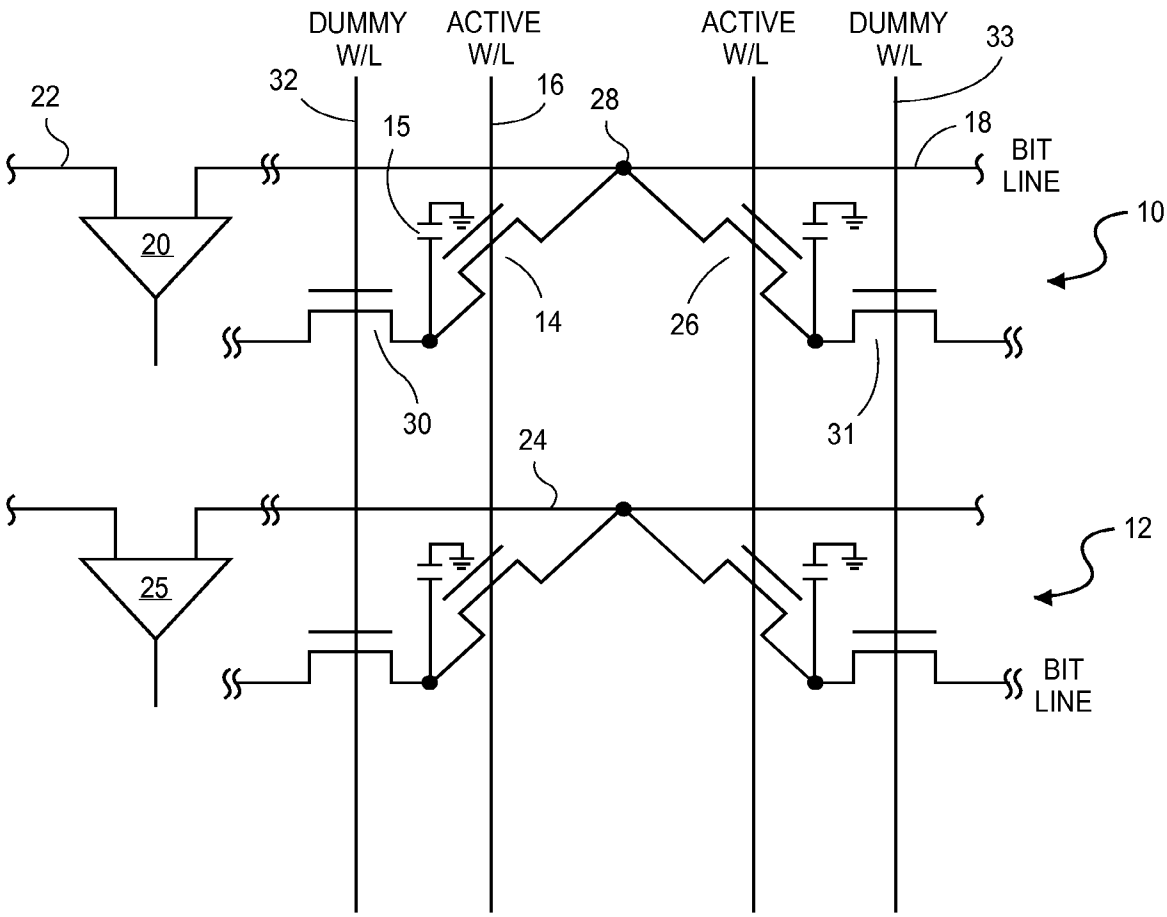

DUMMY W/L
ACTIVE W/L
ACTIVE W/L
DUMMY W/L
33
32
16
28
22
15
18
BIT LINE
10
20
14
26
30
31
24
12
25
BIT LINE

FIG. 1

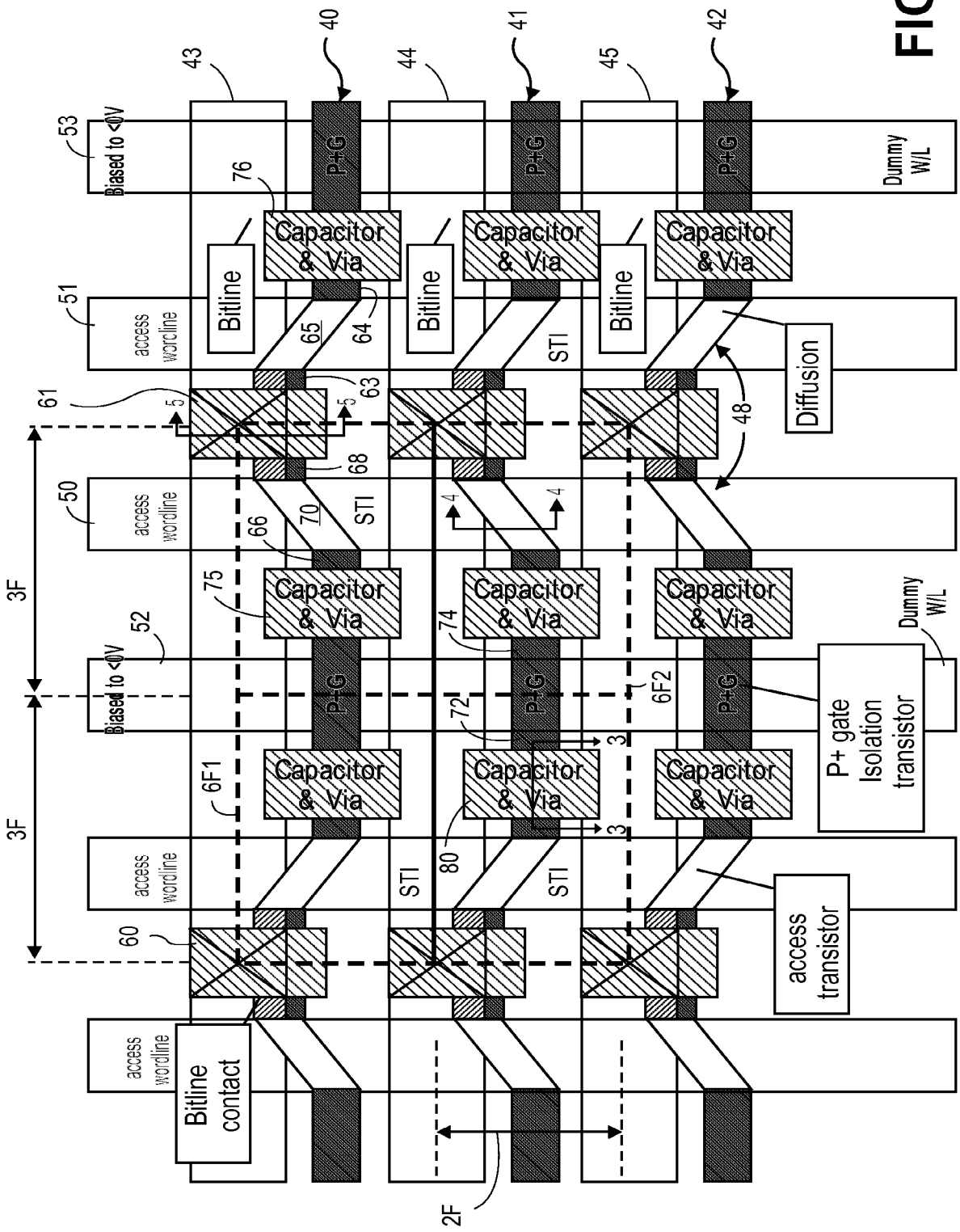

Biased to <0V
Biased to <0V
Dummy W/L
Dummy W/L
P+G
Capacitor & Via
Bitline
access wordline
STI
Diffusion
P+ gate Isolation transistor
access transistor
Bitline contact
3F
3F
2F
6F1
6F2
40
41
42
43
44
45
48
50
51
52
53
60
61
63
64
65
66
68
70
72
74
75
76
80

FIG. 2

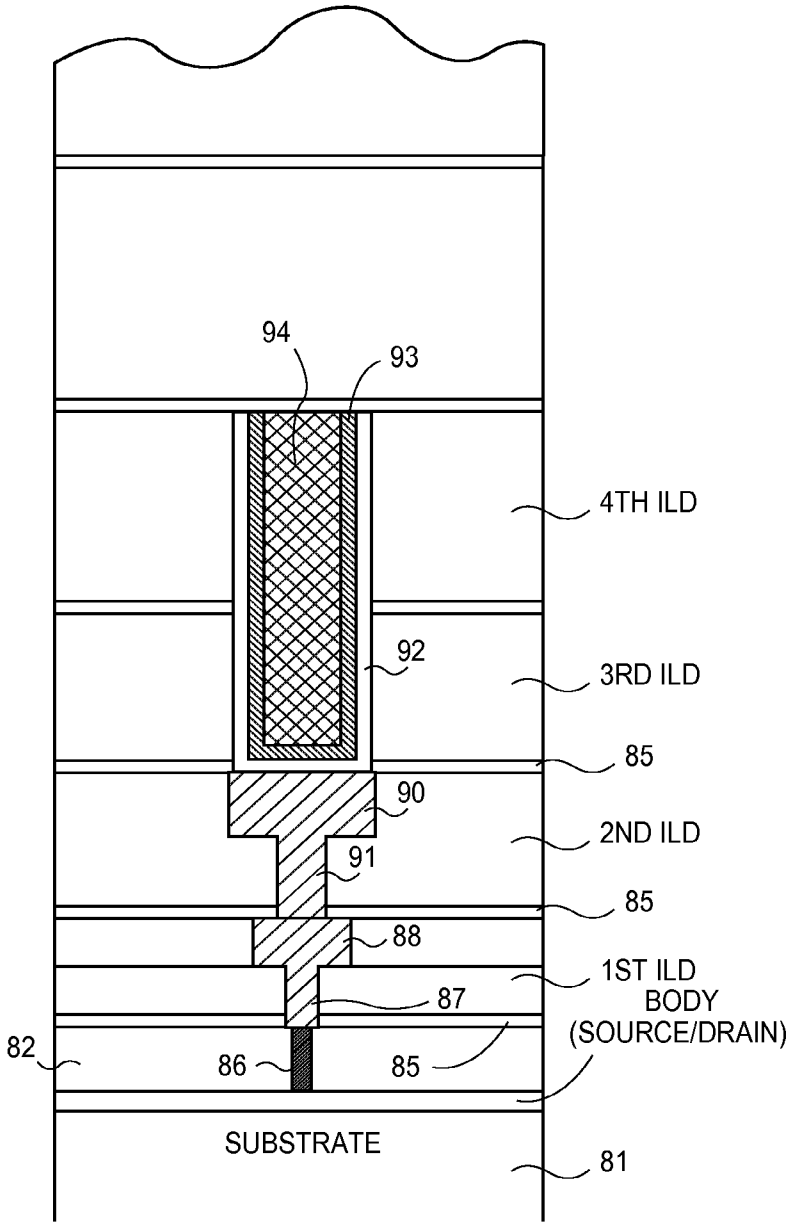

94
93
4TH ILD
92
3RD ILD
85
90
2ND ILD
91
85
88
1ST ILD
BODY
(SOURCE/DRAIN)
87
82
86
85
SUBSTRATE
81

FIG. 3

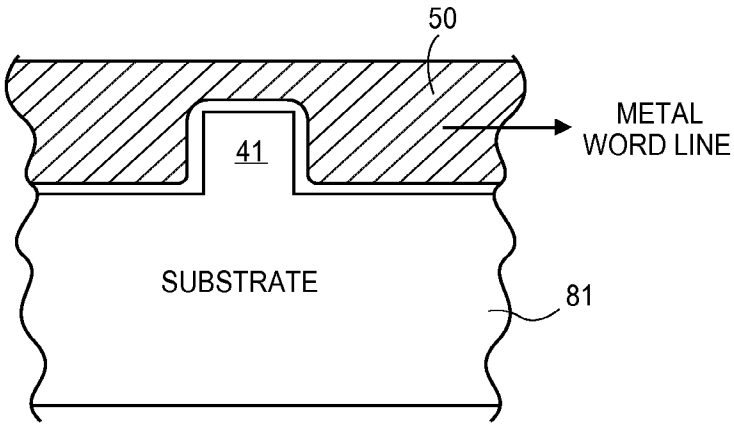

50
METAL
WORD LINE
41
SUBSTRATE
81

FIG. 4

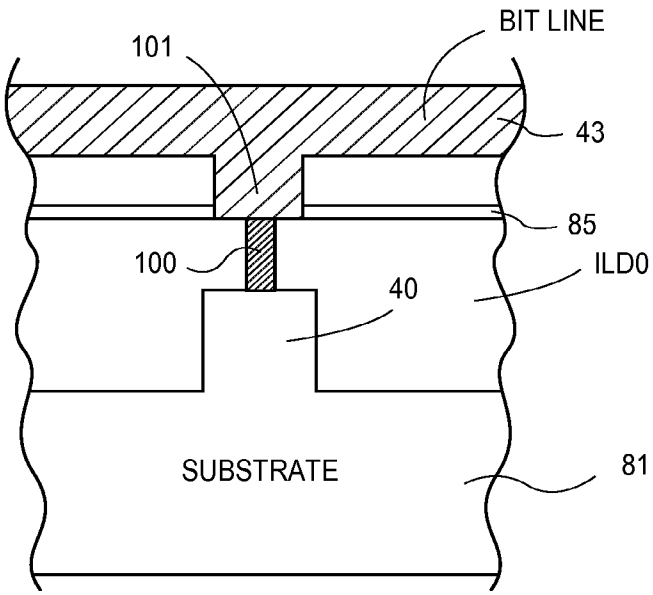

BIT LINE
101
43
85
100
ILD0
40
SUBSTRATE
81

FIG. 5

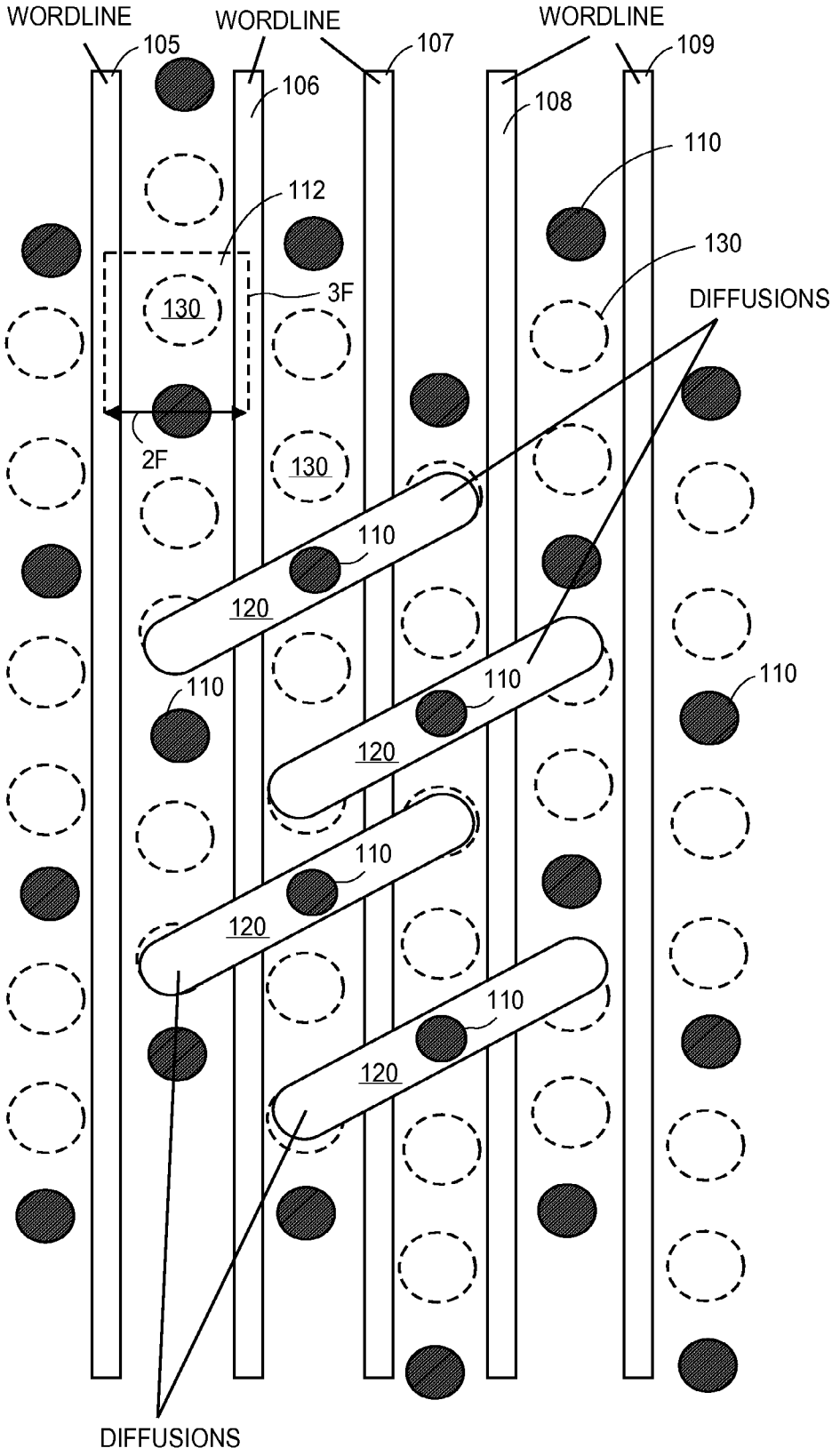

WORDLINE
WORDLINE
WORDLINE
105
106
107
108
109
110
112
130
3F
DIFFUSIONS
2F
120
DIFFUSIONS

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/034431

A. CLASSIFICATION OF SUBJECT MATTER

G11C 5/02(2006.01)i, G11C 5/06(2006.01)i, G11C 11/40(2006.01)i, H01L 27/108(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 5/02; H01L 23/52; H01L 21/336; H01L 21/70; H01L 29/94; G06F 17/30; G06Q 10/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:Dram,separat*,region*,cell,transistor,word,line,wordline,bit,bitline

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006-0252206 A1 (Micron Technology, Inc.) 09 November 2006 See Paragraphs [0033]-[0037] and Figures 4A-4B.	1-24
A	US 2007-0228433 A1 (Micron Technology, Inc.) 04 October 2007 See Paragraphs [0040]-[0049] and Figures 9A-9B.	1-24
A	US 7902611 B1 (RAHIM IRFAN et al.) 08 March 2011 See Paragraphs [0039]-[0080] and Figure 2.	1-24
A	US 2006-0004607 A1 (PHILIP MARSHALL et al.) 05 January 2006 See Paragraphs [0123]-[0161] and Figures 32-33.	1-24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 OCTOBER 2012 (29.10.2012)	**29 OCTOBER 2012 (29.10.2012)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Son, June Young

Telephone No. 82-42-481-5720

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2012/034431

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006-0252206 A1	09.11.2006	US 2004-0042256 A1	04.03.2004
		US 2005-0041457 A1	24.02.2005
		US 7149109 B2	12.12.2006
		US 7224024 B2	29.05.2007
		US 7323380 B2	29.01.2008
US 2007-0228433 A1	04.10.2007	CN 101410961 A	15.04.2009
		CN 101410963 A	15.04.2009
		CN 101410963 B	30.03.2011
		CN 101416288 A	22.04.2009
		CN 101416317 A	22.04.2009
		EP 2002468 A1	17.12.2008
		EP 2002469 A1	17.12.2008
		EP 2002470 A2	17.12.2008
		EP 2008309 A1	31.12.2008
		JP 2009-532903 A	10.09.2009
		JP 2009-532904 A	10.09.2009
		JP 2009-532905 A	10.09.2009
		JP 2009-532907 A	10.09.2009
		KR 10-2009-0005149 A	12.01.2009
		KR 10-2009-0006169 A	14.01.2009
		KR 10-2009-0007393 A	16.01.2009
		KR 10-2009-0007397 A	16.01.2009
		TW I344181B	21.06.2011
		TW 200802617 A	01.01.2008
		TW 200802627 A	01.01.2008
		TW 200805509 A	16.01.2008
		US 2007-0228491 A1	04.10.2007
		US 2007-0231980 A1	04.10.2007
		US 2007-0231985 A1	04.10.2007
		US 2007-0232007 A1	04.10.2007
		US 2009-0155966 A1	18.06.2009
		US 2010-0330759 A1	30.12.2010
		US 7425491 B2	16.09.2008
		US 7491995 B2	17.02.2009
		US 8062949 B2	22.11.2011
		US 8119484 B2	21.02.2012
		WO 2007-114927 A1	11.10.2007
		WO 2007-120492 A1	25.10.2007
		WO 2007-120493 A1	25.10.2007
		WO 2007-136461 A2	29.11.2007
		WO 2007-136461 A3	29.11.2007
US 7902611 B1	08.03.2011	None	
US 2006-0004607 A1	05.01.2006	US 2004-0044548 A1	04.03.2004