(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
19 December 2024 (19.12.2024)

WIPO | PCT

(10) International Publication Number
WO 2024/255935 A1

(51) International Patent Classification:
H03K 19/0948 (2006.01) *H03K 3/03* (2006.01)
H03K 19/20 (2006.01)

(21) International Application Number:
PCT/CZ2023/000029

(22) International Filing Date:
16 June 2023 (16.06.2023)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE** [CZ/CZ]; Technická 2, 166 27 Praha (CZ).

(72) Inventors: **BĚLOHOUBEK, Jan**; Do Vrchu 1390, 332 02 Starý Plzenec (CZ). **LORENCZ, Róbert**; Pátecká 1384, 290 01 Poděbrady (CZ).

(74) Agent: **DANĚK, Vilém** et al.; Vinohradská 17, 120 00 Praha 2 (CZ).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report (Art. 21(3))*

(54) Title: LOW FLICKER NOISE NEAR-THRESHOLD CMOS INVERTER

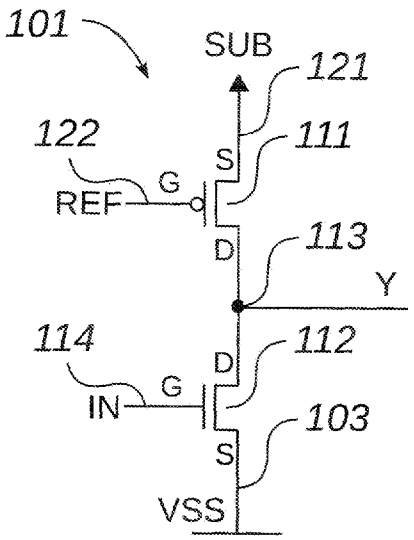


Fig. 4

(57) Abstract: The design of a near-threshold inverter suppressing the flicker noise is disclosed. The inverter is operated near the threshold, and thus its operation point, determined by the connection to the near-threshold region, suppresses the flicker noise floor effectively for short-channel CMOS devices. Two variants of the connection are possible: one with the static pull-up PMOS network, and another with a static pull-down NMOS network. The part, which is chosen to be static reduces its contribution to the flicker noise more significantly.

WO 2024/255935 A1

Title: Low Flicker Noise Near-Threshold CMOS Inverter

TECHNICAL FIELD

[0001] The disclosed invention of a low flicker noise near-threshold CMOS inverter relates to the flicker noise suppression in CMOS, and represents the CMOS structure decreasing the flicker noise in general, and to low-noise CMOS ring oscillators utilizing the disclosed low flicker noise near-threshold CMOS inverter in particular. Thus, the present invention also relates to the implementation of the CMOS inverter into control gate and ring oscillator.

BACKGROUND ART

[0002] Complementary metal-oxide-semiconductor (CMOS) ring oscillators are widely used in True Random Number Generators (TRNG), Physical Unclonable Functions (PUF), or Phase Locked Loop (PLL) circuits. The ring oscillators are typically based on the CMOS inverter structure.

[0003] As a device's size scales down, the inverter dimensions become smaller, and noise in ring oscillators becomes more important. The flicker noise is caused by impurities in the semiconductor device channel, and variations in charge trapping. The flicker noise could also be increased by semiconductor degradation caused e.g. by aging or ionizing radiation.

[0004] The flicker noise is significant, and it dominates over white (temperature) noise in lower frequencies for upstream CMOS technology nodes. Flicker noise commonly dominates over white noise up to tens of Mhz and its significance increases for recent technology nodes, as reported e.g. in the patent US10295583B2. The flicker noise in the ring oscillator translates into phase noise or jitter.

[0005] In cryptographic primitives, high entropy, and/or long-term stability is a common requirement. It is advantageous to strengthen high entropy lower amplitude noise source – represented by white noise – beside lower entropy burst noise source – represented by a flicker noise.

[0006] The standard method of flicker noise elimination is high current insertion e.g. by extending the transistor channel, as reported in the document ABIDI, Assad A. Phase noise and jitter in CMOS ring oscillators. IEEE journal of solid-state circuits, 2006, 41.8: 1803-1816.

[0007] Another option used for flicker noise suppression is the connection employing the resistor degeneration effect disclosed in the patent EP2609681B1.

[0008] The flicker noise drain to source voltage and the gate bias dependence is negligible for long-channel NMOS transistors, however, the significant gate bias dependence of the flicker noise has been reported for PMOS devices, and for short-channel devices in general, as reported in the document CHANG, Jimmin; ABIDI, A. A.; VISWANATHAN, C. R. Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures. IEEE Transactions on Electron Devices, 1994, 41.11: 1965-1971.

[0009] The existing solutions used to diminish the flicker noise provide the flicker suppression for a cost of increased area and/or increased power consumption. This might be problematic, especially in low-power design.

SUMMARY OF THE INVENTION

[0010] The above disadvantages are suppressed by the circuit structure that decreases the flicker noise by choosing the operating point of the CMOS inverter circuit in the near-threshold region for the switching device and near the saturation region for the static pull-up or pull-down device respectively. The operating point is chosen in such a way, that the flicker noise is decreased significantly. The choice of the operating point in the region with a low flicker level is problematic due to CMOS's complementary nature, where only PMOS or NMOS flicker noise contribution is suppressed ideally, however, the disclosed connection represents a highly efficient way to limit flicker noise contribution from both PMOS and NMOS.

[0011] The inverter circuit comprises semi-standard connections of PMOS and NMOS transistors. One of the complementary parts serves as a static pull-up or pull-down network respectively, while the other part as a dynamic switching part.

[0012] The NMOS transistor is connected by its source terminal to the inverter ground node VSS and by the drain terminal to the inverter output. The gate terminal of the NMOS transistor is the inverter input node. The PMOS transistor drain terminal is connected to the inverter output node, but its source terminal is connected to the SUB node. The PMOS gate terminal is connected to the REF node.

[0013] The SUB node voltage V(SUB) is chosen in such a way, that it is lower than circuit nominal supply voltage V(VDD), but higher than the threshold voltage of the PMOS transistor V(THP): V(VDD) >> V(SUB) > V(THP).

[0014] The REF node voltage is chosen in such a way, that it is lower than the V(SUB) voltage: V(SUB) > V(REF). Typically, V(REF) ≈ 0.5 * V(SUB).

[0015] Complementary structure is also possible: The NMOS inverter is connected by its source terminal to the inverter ground node VSS and by the drain terminal to the inverter output. The gate terminal of the NMOS is connected to the REF node. The PMOS inverter drain terminal is connected to the inverter output node, its source terminal is connected to the SUB node. The PMOS gate terminal is the inverter input node.

[0016] In the complementary case, the SUB node voltage V(SUB) is chosen in such a way, that it is lower than circuit nominal supply voltage V(VDD), but higher than the threshold voltage of the PMOS transistor V(THP): V(VDD) >> V(SUB) > V(THP).

[0017] The REF node voltage is chosen in such a way, that it is lower than the threshold voltage of the NMOS transistor V(THN: V(REF) < V(THN). Typically, V(REF) ≈ 0.5 * V(THN).

[0018] The advantages of the disclosed solution embodiment are, that it has a simple structure without additional components such as resistors decreasing the occupied

circuit area, or that a high mismatch could be achieved when sizes of PMOS and NMOS transistors are chosen close to the lower technology limit.

[0019] The property of the disclosed solution embodiment is that the near-threshold operation decreases the oscillation frequency – high oscillation frequencies could not be achieved, however short rings could be used for higher frequencies leading to small area footprint, while the disadvantage of the disclosed solution embodiment is, the lower noise immunity in the near-subthreshold region.

[0020] In one embodiment of the invention, the Low Flicker Noise Near-Threshold CMOS Inverter comprises a semi-standard connections of PMOS transistor and NMOS transistor, where the NMOS transistor is connected by its source terminal S to the ground VSS node, and by its drain terminal D to the inverter output Y, while the PMOS transistor drain terminal D is connected to the inverter output Y.

[0021] It is essential that the gate terminal G of the NMOS transistor is connected to the inverter input IN, and the source terminal S of the PMOS transistor is connected to the SUB node, and the PMOS transistor gate terminal G is connected to the REF node. Alternatively, the gate terminal G of the PMOS transistor is connected to the inverter input IN node, and the source terminal S of the PMOS transistor is connected to the SUB node, and the NMOS transistor gate terminal G is connected to the REF node.

[0022] It is also possible that the inverter is configured is such a way that multiple transistors of the same type are connected in parallel or in series to the PMOS transistor or NMOS transistor, while their gate terminals G are connected to REF node and/or IN node respectively.

[0023] Furthermore, the invention also relates to a control gate comprising the CMOS inverter structure according to this invention.

[0024] Advantageously, the control gate is configured in such a way that typically two, but at least one of the gate terminals G of PMOS and NMOS transistors placed in parallel or in series to the transistors in the inverter structure are bonded together

creating a second input of the control gate, where the control gate implements a basic logic function, typically NAND.

[0025] Furthermore, the invention relates to a ring oscillator comprising an odd number of three or more inverters according to this invention, which are connected in the ring in such a way that the output Y of one of inverters in the ring is the output of the ring oscillator OUT.

[0026] Moreover, the invention also relates to a ring oscillator comprising an even number of two or more inverters according to this invention and one control gate provided with the inverters and connected in the ring, wherein the output of one of inverters or the output of the control gate in the ring is the output of the ring oscillator OUT, and one of the control gate inputs is connected to the output of one of inverter outputs in the ring, and the second input of the control gate is the enable signal ENA of the ring oscillator.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The standard embodiment of the inverter-based ring oscillator is shown in Fig. 1, while Fig. 2 illustrates the embodiment of the standard inverter-based ring oscillator with the incorporated control signal. Fig. 3 illustrates the structure of the CMOS inverter, while Fig. 4 discloses the principle of the disclosed solution. Fig. 5 gives an example of how the disclosed solution could be incorporated into a standard digital design. Fig. 6 describes how the operation point of CMOS devices in the disclosed inverter is limited in a particular case.

[0028] Fig. 5 illustrates, how the disclosed solution could be incorporated into a standard CMOS digital design represented by a counter 302 in the VDD domain characterized by the nominal supply voltage provided through the VDD node 102. The counter 302 is connected by its input to the output 303 of the comparator 301 in the VDD domain. The comparator 301 inputs are reference input REF 122 and inverter-based ring oscillator 120 output OUT 102 located in the SUB supply voltage domain

characterized by a near-threshold supply voltage provided through the SUB node 121. Both supply domains have a common ground VSS node 103.

[0029] Fig. 6 describes how the limited operation point of CMOS devices in the disclosed inverter limits the flicker noise RMS in a particular realization of the disclosed inverter in the sky130 technology.

DETAILED DESCRIPTION OF THE INVENTION

[0030] The inverter-based ring oscillator 120 comprises an odd count of inverters 101 chained in the ring in a standard way, following the structure of the ring oscillator 100 or 200 in Fig. 1, or Fig. 2 respectively, where the output of the first is connected to the input of another, and one of the inverter outputs is the output of the ring oscillator OUT node 102.

[0031] The inverter 101 is the disclosed solution shown in Fig. 4 with the operating point chosen near the threshold region compared to the standard CMOS inverter in Fig. 3. The disclosed inverter operation region reduction is shown in Fig. 6. The disclosed Inverter 101 is composed of a PMOS transistor 111 connected by its source terminal S to the SUB node 121, by its gate terminal G to the reference input REF 122, and by its drain terminal D to the inverter output Y 113, and by an NMOS transistor 112 connected by its drain terminal D to the inverter output Y 113, by its gate terminal G to the inverter input IN 114, and by its source terminal S to the ground VSS node 103.

INDUSTRIAL UTILIZATION

[0032] The disclosed solution has good industrial applicability, for example, in the creation of cryptographic primitives like ring-oscillator-based random number generators (TRNGs) or physically unclonable functions (PUFs), especially in low-power application-specific integrated circuits (ASICs).

CLAIMS

1. A Low Flicker Noise Near-Threshold CMOS Inverter (101) comprising a semi-standard connections of PMOS transistor (111) and NMOS transistor (112), where the NMOS transistor (112) is connected by its source terminal S to the ground VSS node (103), and by its drain terminal D to the inverter output Y (113), while the PMOS transistor (111) drain terminal D is connected to the inverter output Y (113), **characterized in that**

the gate terminal G of the NMOS transistor (112) is connected to the inverter input IN (114), and the source terminal S of the PMOS transistor (111) is connected to the SUB node (121), and the PMOS transistor (111) gate terminal G is connected to the REF node (122),

or

the gate terminal G of the PMOS transistor (111) is connected to the inverter input IN node (114), and the source terminal S of the PMOS transistor (111) is connected to the SUB node (121), and the NMOS transistor (112) gate terminal G is connected to the REF node (122).

2. The inverter according to claim 1, wherein multiple transistors of the same type are connected in parallel or in series to the PMOS transistor (111) or NMOS transistor (112), while their gate terminals G are connected to REF node (122) and/or IN node (114) respectively.

3. A control gate (201) comprising CMOS inverter according to claim 1 or 2, wherein typically two, but at least one of the gate terminals G of PMOS and NMOS transistors placed in parallel or in series to the transistors in the inverter structure are bonded together creating a second input of the control gate (201).

4. A ring oscillator (100) comprising an odd number of three or more inverters (101) according to claim 1 or 2 connected in the ring, wherein the output Y (113) of one of inverters in the ring is the output of the ring oscillator OUT (102).

5. A ring oscillator (200) comprising an even number of two or more inverters (101) and one control gate (201) according to any of claims 1 to 4 connected in the ring, wherein the output of one of inverters (101) or the output of the control gate (201) in the ring is the output of the ring oscillator OUT (102), and one of the control gate (201) inputs is connected to the output of one of inverter (101) outputs in the ring, and the second input of the control gate (201) is the enable signal ENA (202) of the ring oscillator.

LIST OF REFERENCE MARKS

100 – standard inverter-based ring oscillator
101 – CMOS inverter circuit
102 – ring oscillator OUT
103 – ground VSS node
111 – PMOS transistor
112 – NMOS transistor
113 – inverter output Y
114 – inverter input IN
120 – inverter-based ring oscillator employing disclosed inverters
121 – SUB node
122 – REF node
200 – standard ring oscillator with ENA control signal
201 – ring oscillator control gate
202 – enable signal ENA
301 – comparator in the VDD domain
302 – counter in the VDD domain
303 – output of the comparator

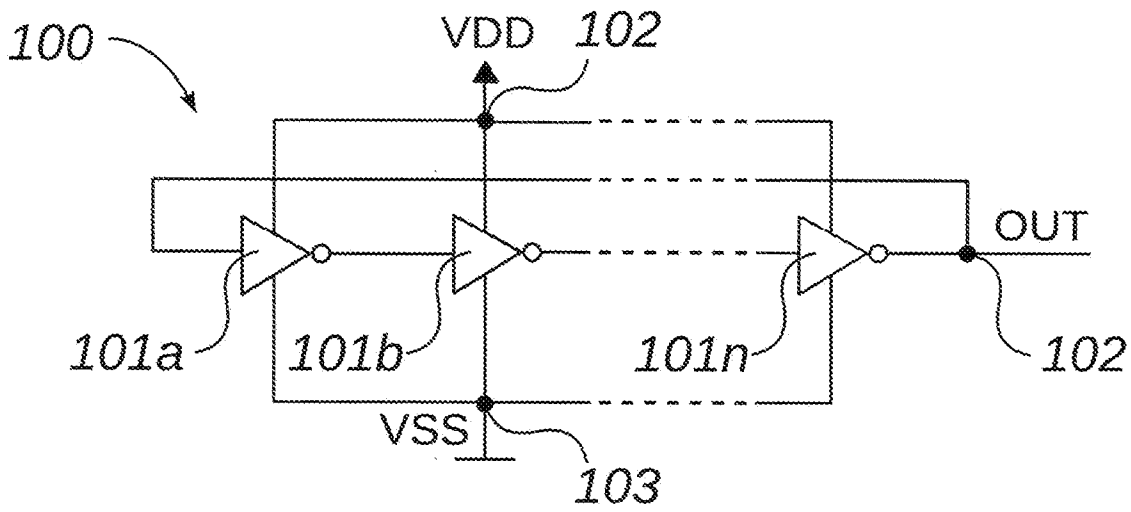

100
VDD
102
OUT
101a
101b
101n
102
VSS
103

Fig. 1

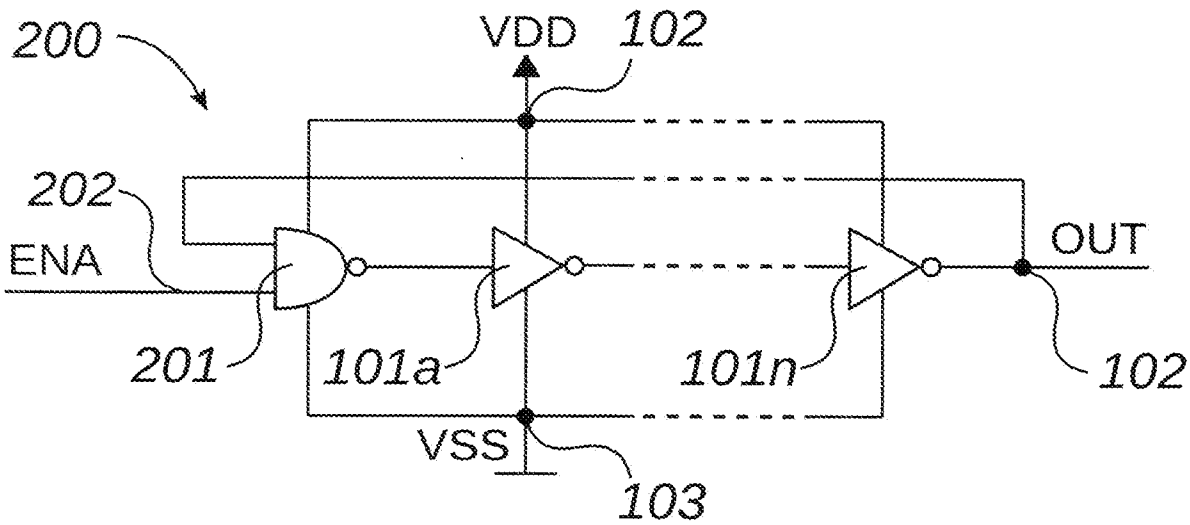

200
VDD
102
202
ENA
OUT
201
101a
101n
102
VSS
103

Fig. 2

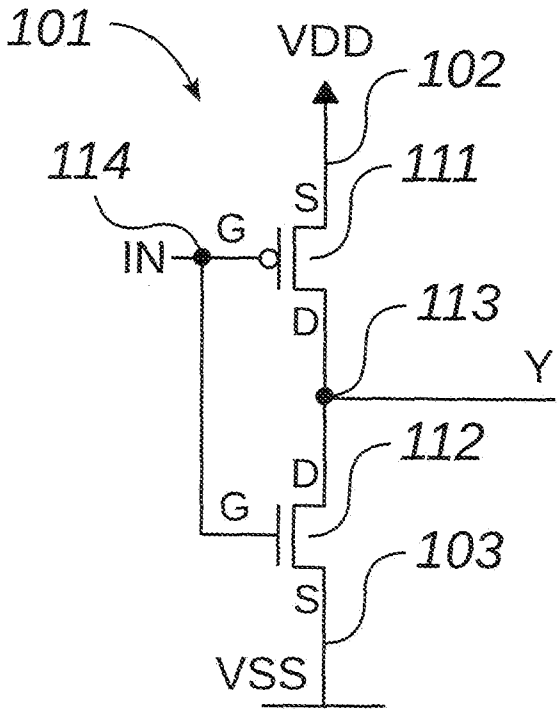

101
VDD
102
114
111
S
G
IN
D
113
Y
112
D
G
103
S
VSS

Fig. 3

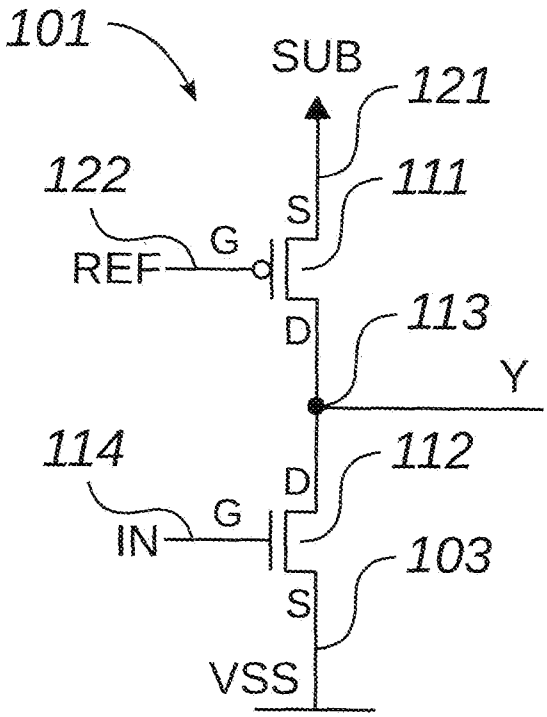

101
SUB
121
122
111
S
G
REF
D
113
Y
114
112
D
G
IN
103
S
VSS

Fig. 4

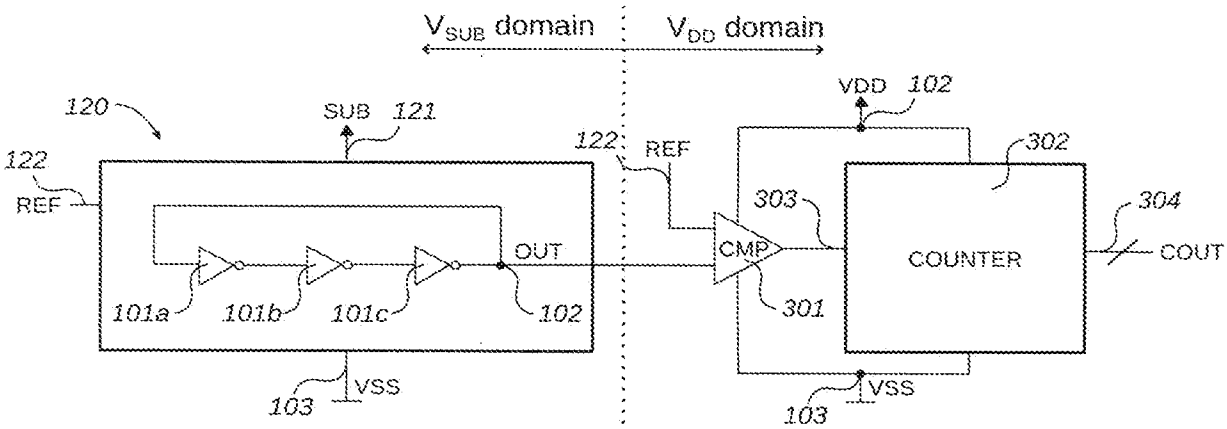
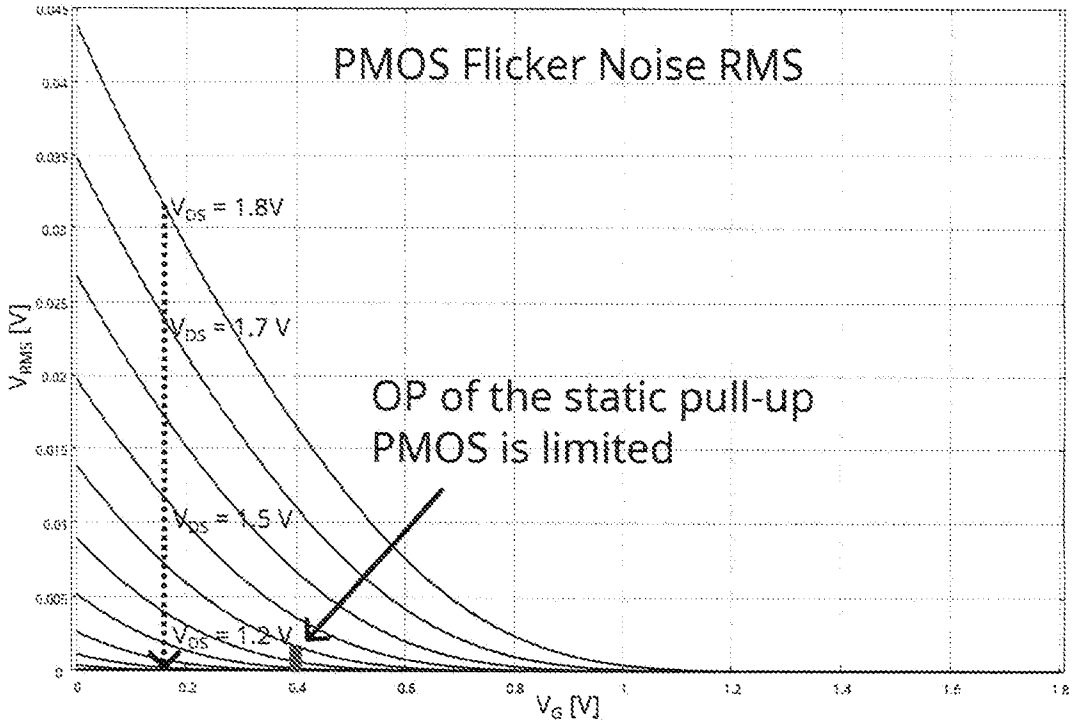

V_{SUB} domain
V_{DD} domain
120
SUB
121
122
REF
OUT
101a
101b
101c
102
103
VSS
122
REF
VDD
102
302
303
304
CMP
COUNTER
COUT
301
103
VSS

Fig. 5


PMOS Flicker Noise RMS
V_{DS} = 1.8V
V_{DS} = 1.7 V
V_{DS} = 1.5 V
V_{DS} = 1.2 V
OP of the static pull-up PMOS is limited
V_{RMS} [V]
V_G [V]

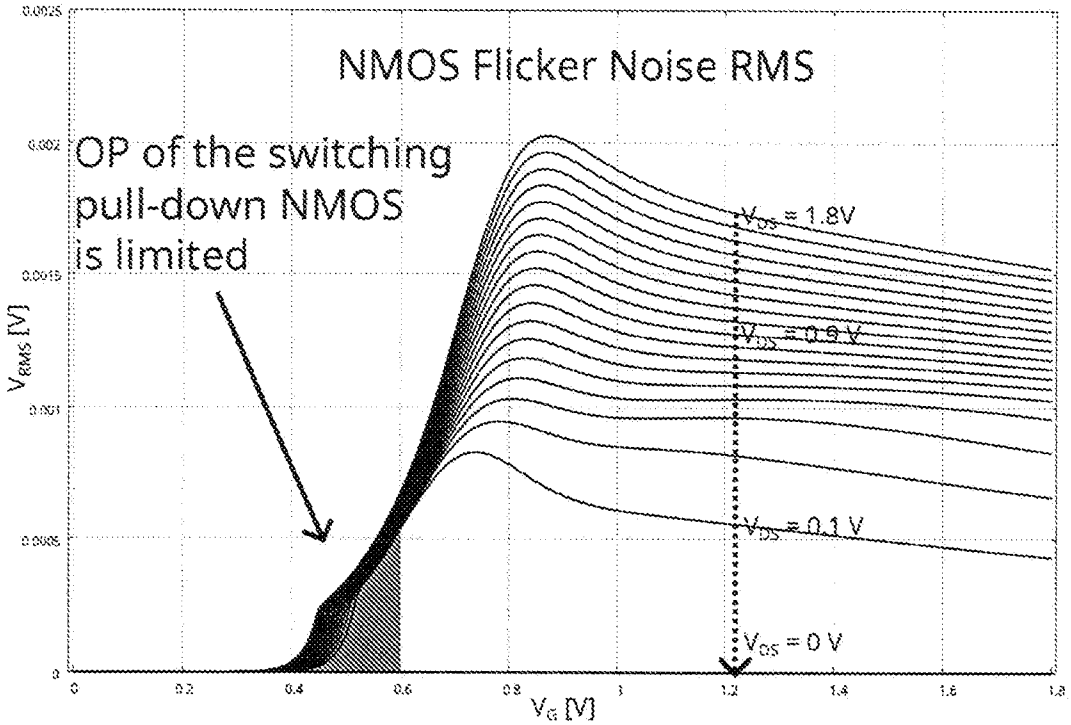

NMOS Flicker Noise RMS
OP of the switching pull-down NMOS is limited
V_{DS} = 1.8V
V_{DS} = 0.9 V
V_{DS} = 0.1 V
V_{DS} = 0 V
V_{RMS} [V]
V_G [V]

Fig. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/CZ2023/000029

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K19/0948 H03K19/20 H03K3/03
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SINGHAI SHREY ET AL: "Process Sensor Using Current-Steering Logic Inverter based Ring Oscillator", 2022 IEEE 19TH INDIA COUNCIL INTERNATIONAL CONFERENCE (INDICON), IEEE, 24 November 2022 (2022-11-24), pages 1-5, XP034297071, DOI: 10.1109/INDICON56171.2022.10039927 [retrieved on 2023-02-16] Section III.A.; figures 4,6	1-5

-/--

[x] Further documents are listed in the continuation of Box C.

[ ] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2023	10/01/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Martínez Martínez, J

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/CZ2023/000029

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	NG H-T ET AL: "CMOS CURRENT STEERING LGOIC FOR LOW-VOLTAGE MIXED-SIGNAL INTEGRATEDCIRCUITS", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 5, no. 3, 1 September 1997 (1997-09-01), pages 301-308, XP000701407, ISSN: 1063-8210, DOI: 10.1109/92.609873 Section II.; figure 3 -----	1-5

1