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(54) Title: MODEM FOR DATA TRANSMISSION OVER HIGH VOLTAGE DISTRIBUTION LINES

(57) Abstract: Modem for data transmission over high voltage distribution lines comprises a block (JADRO) that contains at least two serial communication ports (UART) and at least two ports (I/O) accessible via a connector (PK). The block (JADRO) further comprises a gate array (FPGA), an input analog-digital converter (AD) and an output digital-analog converter (DA). To the gate array (FPGA) a circuit (CPLD) is connected for booting firmware in the memory (RAM) to ensure the required function of the gate array (FPGA) after turning on of the power supply. The circuit (CPLD) is designed to ensure data protection and to check data handling for correctness. The memory (RAM) is connected to the gate array (FPGA) to ensure the entire operation of the gate array (FPGA) program. A memory (FLASH) is also connected to the gate array (FPGA) for saving of internal data. The gate array (FPGA) is equipped with an internal processor (ALU) and has such an internal hardware structure to be able to use the processor (ALU) for the control of processing, reception and transmission of data.
Modem for data transmission over high voltage distribution lines

Technical Field

The present invention relates to a modem for data transmission over high voltage distribution lines. This modem may either work as the master modem of a central unit, or the modem of a slave unit and enables bidirectional data communication between the master modem of the central unit and the modem of at least one slave unit over the power distribution grid, i.e. over high-voltage metallic lines.

Background Art

The high voltage distribution lines according to this application are distribution lines having voltage up to 35kV.

At present data are transmitted over the high-voltage power distribution grid rather sporadically, and generally over high-voltage cable lines only, namely in smally areas (Prague) only. A great majority of high-/low-voltage distribution lines are not used for any communication, which mainly holds good for older designs of distribution lines. High-frequency radio devices (GPRS) are mostly used for remote control of new HV/LV transformer stations. Practice has shown that this type of communication is rather vulnerable with regard to frequent communication failures, network overloading in some time periods, problems of the electronic equipment caused by atmospheric discharges (lightning), insufficient signal coverage of some places, dependence on the operator etc.

The Power Line Communication technology, hereinafter the PLC technology only, generally uses the band from 500 kHz to 100 MHz (most frequently 2 MHz to 30 MHz) for transmission over HV lines. This is the case of broadband communication (referred to as BPL = Broadband over Power Line). The effort to transmit as many data as possible in a short time interval makes it necessary to use higher transmission frequencies in a broadband manner with several carrier frequencies.
Communication over power grid lines has several problematic characteristics that considerably impair, or limit propagation of the high-frequency signal.

1. Transmission loss characteristic of power lines.
There is a general rule that the higher is the transmission frequency, the higher is the line loss with regard to the transmitted signal. The loss characteristic of power lines is equal to approx. 3 dB from 10 kHz to approx. 150 kHz. Then, it gradually increases to approx. 21 dB at the frequency of 1 MHz and at higher frequencies the loss characteristic is in the range from 22 to 75 dB. This means that for bigger distances of transmission points the signal must be amplified with an inserted repeater, or even more repeaters, which is usually quite complicated or problematic and significantly increases the system costs.

2. Power lines behave like an antenna.
It is just the frequency band of 2 MHz to 30 MHz that is used by a considerably high number of radio services, see fig. 3. As during communication the lines emit power, undesired blocking of some important radio services may occur in the vicinity of the lines. Therefore, the output of BPL equipment must be restricted to certain limits and some frequencies even need to be omitted (by means of band suppression filters). With respect to these issues the approach of individual countries to the implementation of BPL communication in the above mentioned frequency bands manifests variable degrees of strictness and some countries have completely prohibited the use of this technology in their territory.

Disclosure of Invention

The above mentioned shortcomings are significantly eliminated by a modem for data transmission over high voltage distribution lines the principle of which is that it comprises a block that includes at least two serial communication ports and at least two binary, input/output ports accessible by means of a connector, an input analog-digital converter and an output digital-analog converter, a gate array to which a circuit for firmware booting into the memory via the inner structure of the gate array is connected to ensure the required function of the gate array after
turning the power supply on. The circuit is also designed to ensure data protection and to check data handling for correctness. A memory is connected to the gate array to ensure the entire run of the gate array program and a memory for saving accepted data is also connected to the gate array. The internal hardware structure of the gate array makes it possible to use an internal processor for the control of processing, reception and transmission of data.

The modem according to the invention may work as the master modem of a central unit, or as the modem of a slave unit. Such modems support bidirectional data communication between the master modem of the central unit and the modem of at least one slave unit over the power distribution grid, i.e. over high-voltage metallic lines.

It is convenient if for data transmission over high voltage lines the outputs of the internal processor are internally connected to 1 to n blocks of turbo encoders and preambles arranged in the gate array, preparing data for transmission and connection of the required preamble to the data packet to synchronize the receiving side of the modem.

The outputs of the 1 to n blocks of the turbo encoders and preambles are preferably internally connected to 1 to n blocks of digital modulators arranged in the gate array for processing of data supplied from the blocks of the turbo encoders and preamble, to modulate individual carrier frequencies with the data supplied from the blocks of the turbo encoders and preamble.

The outputs of the 1 to n blocks of the digital modulators are preferably internally connected to a digital mixer block arranged in the gate array to sum up all data from the digital modulator blocks and to supply this sum to the digital-analog converter.

The output of the digital mixer is preferably connected, via the output of the gate array, to the input of the digital-analog converter, converting the digital data of the completed signal to an analog signal and supplying it to an active low-pass filter.
The output of the digital-analog converter is also preferably connected to the input of an active output low-pass filter suppressing the higher harmonics of the analog signal provided by the converter, which are created by quantizing of the converter, while the output of the low-pass filter is connected to the input of the terminal power stage.

The output of the low-pass filter is preferably connected to a discrete terminal power stage amplifying the output PLC analog signal while the terminal power stage is further connected to an impedance adapting element.

The outputs of the impedance adapting element ensuring suitable connection to the high-voltage transmission grid are preferably switched from the block of the binary output ports via a connector while one of the outputs of the impedance adapting elements is subsequently connected to a high-voltage separating coupler.

The input of the high-voltage separating coupler ensuring safe, galvanically separated coupling of the modem to the high-voltage transmission grid, which comprises of a separating coupling transformer and a coupling capacitor, is preferably connected to a differential input transformer.

The output of the differential input transformer ensuring symmetrizing of the input analog signal for processing by the differential input is preferably connected to the input of an active input low-pass filter suppressing higher harmonics of the input signal to avoid distortion of the amplitude of the basic transmission frequencies.

The output of the active input low-pass filter is preferably connected to the block via a connector and to the input of the analog-digital converter, which is part of the block.
In a preferred embodiment, the output of the analog-digital converter converting the analog input signal to digital data is connected, via an input of the gate array, to the input of a data decimation filter block arranged in the gate array.

The output of the data decimation filter block reducing the data volume by treating them with the decimation function is preferably internally connected to the inputs of 1 to n blocks of digital mixers with a digital low-pass filter arranged in the gate array.

The outputs of the 1 to n blocks of digital mixers and digital low-pass filters ensuring digital demodulation of data are preferably internally connected to the inputs of 1 to n blocks of synchronizer and detector frames arranged in the gate array.

The outputs of the 1 to n synchronizer and detector frame blocks preparing data for further processing are preferably internally connected to the inputs of 1 to n blocks of turbo decoders arranged in the gate array.

The outputs of the 1 to n blocks of turbo decoders are preferably internally connected to an internal processor used in the gate array, for further processing, e.g. their saving in the memory, processing of commands etc.

The described design represents a system using gate arrays that makes it possible to provide a unique solution of using the PLC technology in a lower transmission band of 30 kHz to 145 kHz in such a way that the modulation and demodulation will ensure transmission of the required data volume approximating the real transmission capabilities of the BPL technology, even with the use of a lower frequency band. Transmissions over high-voltage power distribution lines are subject to the condition of transmission of higher data volumes to cover the future needs of introduction of the AMM (Advanced Metering Management) system in the low-voltage distribution areas of HV/LV transformer stations supplied from this high-voltage distribution grid. Data accumulated in individual HV/LV distribution transformer stations must be transmitted over the high-voltage
distribution grid to a central master unit ensuring further connection to a superior control system, e.g. SCADA in UHV/HV switching stations.

The above mentioned frequently band mainly comprises the delimited CENELEC frequency band A,B,C,D (9 kHz to 148.5 kHz) for PLC communication transmission for European countries. This long wave band is mainly intended for naval communication. This frequency band does not exhibit any interference with terrestrial transmitters or amateur radio service. Also, the output of a PLC transmitter, which is defined by the ČSN EN 50065 standard, is not able to interfere with long-wave naval telecommunication.

The use of gate arrays provides a quick and efficient way of conversion between individual modulations and transmission method by re-programming of the gate arrays. Thus, a single device can be used for all known ways of modulation and methods of PLC signal transmission. Individual transmission methods can also be created. The unquestionable benefits are as follows:

- One circuit design for more applications (high versatility)
- Simpler verification of electromagnetic compatibility
- High reliability
- High and steady product quality level
- Simple changing of the product character consisting in its re-programming

**Brief Description of Drawings**

Fig. 1 shows a wiring diagram of the transmission part of a modem according to the invention for transmission of data over high-voltage lines.

Fig. 2 shows a basic wiring diagram of the receiving part of a modem according to the invention for transmission of data over high-voltage lines.

Fig. 3 illustrates the use of the radio band in the frequency range of 0 to 30 MHz.
Description of preferred embodiments

Fig. 1 shows a wiring diagram of the transmission part of a modem according to the invention. The modem uses integration of a gate array in the PLC modem structure, which principally comprises of a core block (JADRO), which has at least two UART serial ports and at least two binary input/output (IO) port. In a preferred embodiment there are at least four serial communication ports and at least eight binary IO ports. The core block (JADRO) comprises of the entire FPGA gate array to which a CPLD circuit is connected that boots the firmware to the RAM memory to ensure the required function of the FPGA gate array after turning on of the power supply. The CPLD circuit takes care of data protection and checks data handling for correctness. Further, a RAM memory that ensures the entire run of the program of the FPGA gate array and a FLASH memory where internal data are saved are connected to the FPGA gate array. The internal hardware of the FPGA gate array is arranged in such a way that among other things it comprises the internal processor ALU. The processor ALU controls, processes, transmits and receives data. From the processor the transmitted data are supplied to the block of turbo encoders and preamble TK+P-n arranged in the gate array. The task of this block of turbo encoders and preamble TK+P-n is to prepare the data for transmission and to connect the required preamble to the data packet so that the receiving side can be synchronized. There may be more these blocks TK+P-n, in a particular embodiment e.g. eight, depending on the required width of the transmission channel, or based on the operator's requirements. From the block TK+P-n the data are supplied to the multi-channel modulator blocks DM-n arranged in the gate array, consisting of n individual digital modulators depending on the number of carrier frequencies. In the multi-channel modulator blocks DM-n the data of all the channels are modulated by the carrier frequencies and summarised in one output. The above mentioned output is connected to the digital-analog converter DA.

From the digital-analog converter DA the analog signal is directed to the input of an active output low-pass filter ADP-VYS. The purpose of the active output low-pass filter ADP-VYS is to suppress the higher harmonics produced by quantizing
of the DA converter. The output of the low-pass filter DP-VYS is connected to the input of a terminal power stage KVS. The purpose of the terminal power stage KVS is to amplify the output PLC signal and to adapt the impedance of the output for the connection to the high-voltage distribution grid. The output of the terminal power stage KVS is connected to a high-voltage coupler VN-VC that guarantees safe, galvanically separated coupling of the modem to the transmission media (high-voltage grid) and comprises of a coupling separating transformer VT and a coupling capacitor VC.

Reception of the PLC signal from the high-voltage distribution grid is illustrated in fig. 2 while the signal is received via the high-voltage coupler VN-VC, which comprises of a coupling capacitor VC and a coupling separating transformer VT and common protective elements for high voltage. The output of the high-voltage coupler (VN-VC) is connected to a differential input transformer DVT that provides symmetrical analog signal for the input amplifier of an active low-pass filter ADP-VST connected in a differential manner, the task of which is to remove the signals of higher frequencies, mainly the higher frequencies, which might deform the amplitude of the main carrier frequency. The output of the active input low-pass filter ADP-VST is preferably connected to the CORE block (JADRO) via a connector PK to the input of the analog-digital converter AD, which is part of the block JADRO. The converter with a high sampling frequency very precisely converts the analog signal to digital data. As the volume of these data is high, the data are processed in the data decimation filter block CIC. Then, the data treated this way are supplied to 1 to n digital mixer blocks S+DP-n with digital low-pass filters. Together with 1 to n synchronizer and detector frame blocks RSD-n and 1 to n turbo decoder blocks TDC-n performing synchronization, demodulation and turbo decoding of data. Finally, the data are supplied to the internal processor ALU, where they are further processed and saved in the FLASH memory.

The processor unit ALU is connected to the internal UART block created in the gate array, which ensures external communication over serial lines. The UART block is an internal part of the FPGA gate array. The UART block is further connected to a connector PK of the block JADRO.
The master unit is equipped with software for communication in the master mode with one or more slave units, i.e. for sending commands and data to the slave units and receiving answers and data back from the slave units over the high-voltage distribution grid, further processing data, saving them temporarily and sending them to a superior system, e.g. SCADA.

The slave unit is equipped with software for communication with the master central unit in the slave mode, i.e. receiving commands and data from the central master unit and sending answers and data back to the central master unit over high-voltage lines, further processing data and monitoring the HV/LV distribution transformer station and the AMM (Advanced Metering Management) system if it is introduced.

The distribution area of one transformer is equipped with the AMM (Advanced Metering Management) system of remote reading of data of consumption point meters. These consumption places are handled by the slave unit of the transformer station of the area. Besides this activity the slave unit also carries out activities in the entire transformer station. It operates the summary electricity meter, monitors the status of individual devices of the transformer station, checks the state of the outgoing supply branches, controls some activities in the transformer station based on commands, or automatically in accordance with a schedule. It sends all accumulated data, commands, statuses, error states or emergency states of the entire transformer station over high-voltage lines to the control modem of the central unit. This is guaranteed by the modem of the slave unit of the device for data transmission over high-voltage lines.

Industrial Applicability

The modem for data transmission over high-voltage distribution lines is part of an integral system for administration, monitoring and collection of data of the distribution area of one transformer station of the UHV/HV distribution grid. The control modem of the central unit is installed in one UHV/HV transformer station of
the distribution grid at the HV side. The modem of the slave unit is installed in a HV/LV distribution transformer station. The modems ensure transport of all data from one or several slave units to the master system or vice versa, over high-voltage power distribution lines.

List of reference marks

AD - analog-digital converter block
ADP-VST - input active low-pass filter block
ADP-VYS - output active low-pass filter block
ALU - processor block
CIC - data decimation filter block
CPLD - „complex programmable logic device (CPLD)” circuit block
DA - digital-analog converter block
DM -1 to n - digital modulator block 1 to n
DVT - differential input transformer block
FLASH - FLASH type memory block
FPGA - „/field-programmable gate array (FPGA)” circuit block
IC - impedance adapting element block
I/O - block of input and output binary lines
KVS - terminal power stage block
PK - connector
RAM - SRAM type memory block
RSD -1 to n - synchronizer and detector frame block 1 to n
SM - digital mixer blocks
S+DP-1 to n - digital mixer and low-pass filter block 1 to n
TDC -1 to n - turbo decoder block 1 to n
TK+P -1 to n - block of circuits of turbo encoders + preambles 1 to n
UART - UART serial interface block
VN-VC - high-voltage separating coupler block
VT - coupling transformer block
VC - coupling capacitor block
Claims

1. A modem for data transmission over high voltage distribution lines, characterized in that it comprises a block (JADRO) that contains at least two serial communication ports (UART) and at least two ports (I/O) accessible via a connector (PK), the block (JADRO) further comprises a gate array (FPGA), an input analog-digital converter (AD) and an output digital-analog converter (DA), to the gate array (FFGA) a circuit (CPLD) is connected for booting firmware in a memory (RAM) to ensure the required function of the gate array (FPGA) after turning on of the power supply, while the circuit (CPLD) is designed to ensure data protection and to check data handling for correctness, further the memory (RAM) is connected to the gate array (FPGA) to ensure the entire operation of the gate array (FPGA) program, and a memory (FLASH) is also connected to the gate array (FPGA) for saving of internal data, while the gate array (FPGA) is equipped with an internal processor (ALU) and has such an internal hardware structure to be able to use the processor (ALU) for the control of processing, reception and transmission of data.

2. The modem in accordance with claim 1, characterized in that the outputs of the internal processor (ALU) are internally connected to 1 to n blocks of turbo encoders and preambles (TK+P-n) arranged in the gate array (FPGA) for preparation of data for transmission and connection of the required preamble to the data packet.

3. The modem in accordance with claim 2, characterized in that the outputs of the 1 to n blocks of the turbo encoders and preambles are internally connected to 1 to n blocks (DM-n) of digital modulators arranged in the gate array (FPGA) for processing of data supplied from the blocks of the turbo encoders and preambles (TK+P-n), to modulate individual carrier frequencies with the data supplied from the blocks of turbo encoders and preambles (TK+P-n).
4. The modem in accordance with claim 3, **characterized in that** the outputs of the 1 to n blocks of digital modulators (DM-n) are internally connected to a digital mixer block (SM) arranged in the gate array (FPGA) to sum up all data from the digital modulator blocks (DM-n) and to supply this sum to the digital-analog converter (DA).

5. The modem in accordance with any of claims 1 to 4, **characterized in that** the output of the digital mixer (SM) is connected, via the output of the gate array (FPGA) to the input of the digital-analog converter (DA) for conversion of the digital data of the complete signal to the analog signal.

6. The modem in accordance with any of claims 1 to 5, **characterized in that** the output of the digital-analog converter (DA) is connected to the input of an active output low-pass filter (ADP-VYS) suppressing the higher harmonics of the analog signal provided by the converter (DA), which are created by quantizing of the converter (DA), while the output of the low-pass filter (ADP-VYS) is connected to the input of the terminal power stage (KVS).

7. The modem in accordance with claim 6, **characterized in that** the output of the low-pass filter (ADP-VYS) is connected to a discrete terminal power stage (KVS) for power amplification of the output analog PLC signal while the terminal power stage (KVS) is further connected to an impedance adapting element (IC).

8. The modem in accordance with any of claims 1 to 7, **characterized in that** the outputs of the impedance adapting element (IC) ensuring optimum connection to the high-voltage transmission grid are switched from the ports (I/O) via a connector (PK) while one of the outputs of the impedance adapting element (IC) is subsequently connected to a high-voltage separating coupler (VN-VC).

9. The modem in accordance with claim 8, **characterized in that** the input of the high-voltage separating coupler (VN-VC) ensuring safe, galvanically separated coupling of the modem to the high-voltage transmission grid, which comprises of a
separating coupling transformer (VT) and a coupling capacitor (VC), is connected to a differential input transformer (DVT).

10. The modem in accordance with claim 9, characterized in that the output of the differential input transformer (DVT) ensuring symmetrizing of the input analog signal for processing by the differential input of the operating amplifier is connected to the input of an active input low-pass filter (ADP-VST) suppressing higher harmonics of the input signal.

11. The modem in accordance with any of claims 1 to 10, characterized in that the output of the active input low-pass filter (ADP-VST) is connected to the block (JADRO) via a connector (PK) and to the input of the analog-digital converter (AD), which is part of the block (JADRO).

12. The modem in accordance with any of claims 1 to 11, characterized in that the output of the analog-digital converter (AD) converting the analog input signal to digital data is connected, via an input of the gate array (FPGA), to the input of a data decimation filter block (CIC) arranged in the gate array (FPGA).

13. The modem in accordance with any of claims 1 to 12, characterized in that the output of the data decimation filter block (CIC) reducing the data volume by treating them with the decimation function is internally connected to the inputs of 1 to n blocks of digital mixers (S+DP-n) with a digital low-pass filter arranged in the gate array (FPGA).

14. The modem in accordance with any of claims 1 to 13, characterized in that the outputs of the 1 to n blocks of digital mixers and digital low-pass filters (S+DP-n) ensuring digital demodulation of data are internally connected to the inputs of 1 to n blocks of synchronizer and detector frames (RSD-n) arranged in the gate array (FPGA).

15. The modem in accordance with any of claims 1 to 14, characterized in that the outputs of the 1 to n synchronizer and detector frame blocks (RSD-n) for
treatment of data for further processing are internally connected to the inputs of 1 to n turbo decoder blocks (TDC-n) arranged in the gate array (FPGA).

16. The modem in accordance with any of claims 1 to 14, characterized in that the outputs of the 1 to n turbo decoder blocks (TDC-n) are internally connected to an internal processor (ALU) used internally in the gate array (FPGA) for further processing or for their saving in the memory (FLASH), or processing of commands.
INTERNATIONAL SEARCH REPORT

INTERNATIONAL APPLICATION

PCT/CZ2015/000138

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04B3/54
ADD.

According to International Patent Classification (IPC) or both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database consulted during the international search (name of database and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>Wo 2008/011889 AI (SI EMENS AG [DE]; BREKKE ENDRE [NO]; HORTEN VEGARD [NO]; STEIEN VIDAR) 31 January 2008 (2008-01-31) the whole document</td>
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