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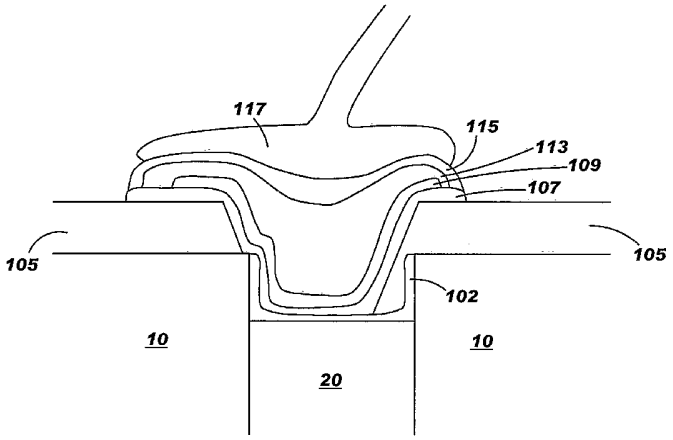
(54) Title: I/O SITES FOR PROBE TEST AND WIRE BOND



(57) Abstract: A method of forming an input-output (I/0) structure is described, wherein a substrate having copper conductive feature (20) exposed at the bottom of a recess (25) in a first dielectric layer (10) is covered by a first conductive barrier (102) that is selectively formed in the recess (25). A second dielectric (105), preferably an organic polymer such as polyimide, is formed over the substrate surface and a second recess (27) is formed in the second dielectric (105) so that at least a portion of the first conductive barrier (102) is exposed. A second conductive barrier (107) is conformally deposited, followed by conformal deposition of a seed layer (109), where both are deposited under a vacuum to ensure adhesion of the seed layer (109) to the second conductive barrier (107). The seed layer (107) is selectively removed external to the recess (27), followed by plating of a nickel-containing metal (113) and then a noble metal (115), which will plate on the remaining portion of the seed layer (107) in the recess (27), but not on the second barrier layer (107). The second barrier layer (107) is removed from the exposed field areas by a low bias power RIE. The invention provides a low-cost method of forming an I/0 structure for both probe test and wire bond without damage to underlying devices and reduced chip real estate.

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I/O Sites for Probe Test and Wire Bond

Technical Field

The present invention relates generally to semiconductor manufacturing, and more particularly, to a process for fabricating an input/output (I/O) site used in packaging integrated circuit (IC) chips.

Background Art

In the fabrication of semiconductor devices, metal lines are often embedded in dielectric layers in a multilevel structure, particularly in the latter stage ("back end of the line" or "BEOL") of the fabrication process. The final layer containing metal lines (sometimes referred to in the art as the terminal via or TV layer) will have metal pads fabricated in contact with the metal lines, in a process sometimes referred to as "far back end of the line", or "far BEOL". The majority of IC chips use aluminum (Al) to form the interconnects, but more recently copper (Cu) is used. Cu has the advantage of lower resistivity, but has the disadvantage that it requires oxidation/diffusion barriers. The metal pads are typically used as bonding sites to connect a chip with other system components, such as another level of interconnect. Common connections include wire bond and solder bumps. Although there is much interest in reducing the size of all elements of IC chips, bond pads are increasingly difficult to shrink, and in some instances, the area of bond pads is increasing. Since the yield (i.e., the percentage of good chips versus all chips on a given wafer or substrate) is inversely related to the size of the chip, particularly in logic chips, the larger the chip area, the greater the chance for damage, for example, by deposition of a contaminating particle.

Wire bonding is well-known in the art and used in the majority of IC chips, but disadvantages include a limited density of interconnect sites and the possibility of mechanical damage to the chip at the site of the bond. Most current semiconductor fabrication facilities commonly known in the industry use an aluminum pad which is used for both wire bond and circuit testing. Metal pads are primarily composed of aluminum (Al), which typically will have an oxide layer formed over the surface because of the reactivity of aluminum.

Prior to wire bonding, circuit testing is performed by pushing a set of test probes against critical conductive points on the top layer. The surface oxide must be broken through (often by a technique known as "scrubbing") in order to form a good contact between the test probe and the pad metal. Thus the surface of the bond pad will be scored or damaged. In some cases, the pad may be pierced by the probe.

A wire, which is often gold (Au) having a trace amount of silicon for rigidity, will be attached to the aluminum pad, which has an oxidized surface, using techniques known in the art, such as thermosonic bonding. In thermosonic bonding, the tip of the gold wire is melted to form a ball after it is extruded through a capillary. The ball is then forced down onto the bond pad, causing the ball to deform, and an ultrasonic force is introduced to complete the bond. The down force and the ultrasonic force are not always enough to overcome the damage introduced by the testers, which would lead to a bond failure. Thus, pads tend to be made larger in area, to allow separate probe and wire bond sites on the pad.

Another problem in forming wire bonds between gold and aluminum is that gold forms intermetallics with aluminum that can reduce the reliability of the bond.

Damage to the underlying substrate and devices is yet another problem with current integrated circuits. Particularly in integrated circuits using Cu metallization, low-k dielectrics may be employed which are soft and sensitive to damage by pressure. Therefore, particularly in the case of soft low-k dielectrics, the chip is subjected to potential mechanical damage. Thus, there is often a requirement that the area under the bond pad be left devoid of devices, which also increases the total size of the chip.

Nickel/gold bond pads have been introduced, since gold is a noble metal, which will not readily oxidize, so that the bonding of gold wire to a gold pad is relatively simple compared to bonding gold to aluminum (for example, see U.S. 6,534,863, the contents of which are hereby incorporated in its entirety by reference). Bonding forces have been successfully been reduced to between 30-50% without bond failure. However, the process disclosed in U.S. 6,534,863 is typically performed using semiconductor processing equipment that have stringent cleanliness requirements, and therefore is costly. It would be advantageous to provide a method of forming an I/O pad that has a noble metal surface using less expensive equipment and processes, such as those available in packaging facilities.

It would therefore be desirable to form an I/O pad that has a noble metal to allow low bonding forces for both probe testing and wire bond without damage to underlying substrate, which reduces real estate requirements, and reduces costs.

Bearing in mind the problems and deficiencies of the prior art, it is therefore an object of the present invention to provide an I/O site for copper interconnects having a noble metal surface, capable of forming a reliable wire bond after probe testing and with minimal or no damage to the underlying substrate. It is another object of the present invention to provide an I/O site that has reduced area requirements, and removes the requirement that the underlying substrate be devoid of devices. It is yet another object of the present invention to provide a method for forming such an I/O site that reduces costs of manufacturing. Still other objects and advantages of the invention will in part be obvious and will in part be apparent from the specification.

Disclosure of Invention

A method of forming an input-output (I/O) structure is described, wherein a substrate having a copper conductive feature (e.g. an interconnect) exposed at the bottom of a recess in a first dielectric layer, such as an oxide or nitride, is covered by a first conductive barrier, such as TiW, TiN or TaN, more preferably TiW, that is selectively formed in the recess to cover the surface of the copper. A second dielectric layer is formed over the substrate surface, which preferably contains an organic polymer, such as a polyimide, and a second recess is formed in the second dielectric so that at least a portion of the first conductive barrier at the bottom of the recess is exposed. A second conductive barrier, such as TiW, is conformally deposited, followed by conformal deposition of a seed layer, preferably CrCu/Cu, where both layers are deposited under a vacuum to ensure adhesion of the CrCu/Cu seed layer to the second conductive barrier. The second conductive barrier is preferably chosen to be self-passivating when exposed to a source of oxygen. The seed layer is selectively removed external to the recess in the second dielectric (e.g. polyimide), followed by selective plating (e.g. electro- or electroless) of a nickel-containing metal on the seed layer, followed by selective plating of a noble metal on the nickel-containing layer. The plating will occur selectively because of the self-passivating nature of the second conductive barrier layer. The noble metal is preferably gold. The exposed field areas of the second barrier layer are removed by a low bias power RIE.

The advantages realized by the above invention relative to current approaches includes lower cost since the invention can be practiced using lower cost packaging tools and processes compared to semiconductor processing tools and processes. The resulting I/O

structure provides a common site for both probe test and wire bond, without damage to underlying devices and reduced chip real estate.

Brief Description of Drawings

The present invention will now be described in more detail by referring to the drawings that accompany the present application, which are not necessarily drawn to scale. It is noted that in the accompanying drawings like reference numerals are used for describing like and corresponding elements thereof.

Fig. 1 illustrates a cross-section view of a starting structure for the present invention, comprising a substrate having a copper interconnect exposed in a recess formed in a dielectric.

Fig. 2 illustrates a cross-section view of the structure at an intermediate step of the invention.

Fig. 3 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 4 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 5 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 6 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 7 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 8 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 9 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 10 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 11 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 12 illustrates a cross-section view the structure at an intermediate step of the invention.

Fig. 13 illustrates a cross-section view the structure according to the invention, including a wirebond.

Fig. 14A illustrates a plan view of an prior art I/O pad.

Fig. 14B illustrates a plan view of an I/O pad formed according to the present invention.

Best Mode of Carrying Out The Invention

In accordance with the invention, an I/O site having a noble metal surface and a method for forming the I/O site that can be implemented at relatively low cost, is described. The I/O site of the present invention is particularly suitable for both probe testing and wire bond. In the following description of the preferred embodiments of the invention, it will be appreciated that this is intended as an example only, and that the invention may be practiced with a variety of substrates and metals. Reference is made to the drawings to illustrate the method according to the present invention, which are not necessarily drawn to scale.

Referring to FIG. 1, a substrate 5 is provided that includes a back-end-of-the-line (BEOL) structure including a metal conductor 20, such as aluminum (Al), copper (Cu) or the like, having a surface exposed in a recess 25 of an first dielectric layer 10. For example, such a structure may be a BEOL wherein the metal conductor 20 is formed as an interconnect structure. The recess is formed using processes including, but not limited to, lithographic and etch processes as known in the art. The recess is formed at the desired location of the I/O pad, and typically has a width in the range of 50-140 μm, for example, a rectangular shape of dimensions 52 μm by 140 μm. The depth of the recess may be in the range 0.4 to about 4.0 μm, and more preferably from about 0.6-0.8 μm. The dielectric layer 10 may be comprised of multiple layers (not shown, for clarity) of dielectric material, such as silicon dioxide (SiO_2), silicon nitride (SiN_x), SiCOH, and other suitable dielectrics. The dielectric is preferably a low-k dielectric such as SiCOH, SiLK® from Dow Chemical, or other low modulus materials.

According to the present invention, as shown in FIG. 2, a first electrically conductive barrier layer 102 is formed conformally over the surface of the substrate 5. The conductive barrier layer 102 is preferably TiW, but may also be formed from materials such as TaN, TiN,

or other electrically conductive materials that serve as a diffusion barrier and an adhesion promoter. The thickness of the barrier layer 102 is preferably thin for ease of manufacturability and for good electrical conductivity to the interconnect 20, but sufficiently thick to act as a barrier to diffusion of metal into an overlying material. The thickness of the barrier layer 102 is preferably at least about 350 Å, and not more than about 500 Å. The barrier layer 102 may be deposited by methods known in the art, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), ionized physical vapor deposition (IPVD), atomic layer deposition (ALD), etc., and preferably by CVD.

The barrier layer 102 is next removed from the surface of the substrate 5 substantially external to the recess 25, so that a portion of the barrier layer 102 remains covering the surface of the metal conductor 20 within the recess 25, as illustrated in FIG. 3. The removal of the barrier layer 102 from the surface external to the recess can be performed by techniques such as chemical-mechanical polishing (CMP), or by an etch process, such as a wet etch or a dry etch such as a reactive ion etch (RIE). The corners of the recess after removal of the barrier 102 outside of the recess may vary as long as the surface of the conductor 20 remains hermetically sealed. In the case of removal by CMP, the upper corners of the recess may suffer some damage (not shown), but the depth of the recess 25 must be sufficiently deep to prevent removal of the barrier 102 from the bottom of recess 25 and exposure of the conductor 20. The depth of the recess may be in the range 0.4 to about 4.0 μm, and more preferably from about 0.6-0.8 μm. In the case of a removal by an etch process, a small portion of the barrier layer 102 may extend outside the recess, due to masking of the recess area (not shown).

Next, a second dielectric layer 105 is formed to blanket the surface of the substrate 5, as illustrated in FIG. 4. Typically, the blanket dielectric layer 105 will fill the recess 25. The second dielectric is preferably a spin-on dielectric such as polyimide, BCB (benzocyclobutane, which is non-photosensitive) and the like, and more preferably polyimide, and is preferably photosensitive. A non-photosensitive dielectric may be used, such as oxides and nitrides, which may be deposited by methods such as CVD, PECVD (plasma enhanced chemical vapor deposition) and other methods known in the art. The thickness of the second dielectric layer 105 may range from 4 to 12 μm, preferably about 5 to 7 μm, and most preferably 6 μm. Note that if the conductive interconnect 20 is copper, the first conductive barrier 102 prevents the copper from contaminating the blanket dielectric layer 105.

Next, referring to FIG. 5, a recess 27 is formed in the second, blanket dielectric layer 105, so that at least a portion of the conductive barrier 102 directly overlying the conductor 20 at the bottom of the recess 25. Although the second recess 27 is preferably aligned with the first recess 25, it may be misaligned as long as a portion of the bottom surface of the first conductive barrier 102 over the conductor 20 is exposed, as illustrated in FIG. 5. A blanket dielectric layer may act as a scratch protection layer for the packaged IC. The recess 27 may be formed by patterning methods as known in the art, such as wet or dry (e.g. RIE) etch techniques, and lithographic techniques. Preferrably, the blanket dielectric layer 105 is photosensitive, which may allow patterning using a lithographic process using the same mask that was used to create the initial recess pattern 25 in the starting structure. This would save the cost of manufacturing an additional lithographic mask, and would avoid the formation of an additional masking material that would be required in a conventional etch process. In the case of a spin-on dielectric, after patterning, the material requires curing, typically by thermal processing according to the material used, as known in the art.

Referring now to FIG. 6, a second conductive barrier layer 107 is deposited conformally on the surface of the substrate 5. The second conductive barrier layer 107 should have good adhesion to the second dielectric layer 105 and first barrier layer 102. The conductive barrier 107 should also be self-passivating when exposed to oxygen, i.e., sufficiently reactive so as to form an oxide which acts as an insulator, and will prevent subsequent plating on that surface. Examples of suitable conductive barrier layers 107 are TaN, TiN, and preferably TiW. The second barrier layer 107 may be deposited by a method such as CVD, PVD, and the like, under vacuum. The thickness of the second barrier layer 107 should be in the range 1500 Å to 1600 Å (0.15-0.16 μm), and preferably about 1600 Å.

A third conductive layer 109 is then deposited on the second conductive barrier layer 107, so as to provide copper on the upper surface of the third barrier layer 109. The third conductive barrier layer 109 is preferably deposited under vacuum, to ensure adhesion to the underlying second conductive barrier layer 109 (for example, to prevent oxidation of the surface of second layer 107). The third conductive layer 109 is formed to provide a surface comprising a seed metal for plating, preferably copper. Other seed metals may be used, including Ru, Rd, In, Os and the like. Preferably, the third conductive (seed) layer 109 is graded, starting with a mixture of copper and a metal compatible with the CrCu/Cu, which is graded from CrCu (preferably 50% Cr to 50% Cu by weight) at the interface of with the second barrier 107 (e.g., of TiW or TaN), until the surface of the third (seed) layer 109 is

essentially Cu. Alternatively, third conductive layer 109 may be formed from multiple layers, wherein the layer at the interface with the second barrier layer 107 includes a mixture of Cu and another metal compatible with the second layer 107, and an upper layer essentially consisting of Cu. Preferably, a CrCu graded layer is about 2500 Å to 4000 Å, and the copper seed layer is preferably less than about 5000 Å, more preferably about 4500Å. The invention is not limited to particular thicknesses of the second or third conductive layers 107, 109, which can be changed to accomodate the capabilities of a particular manufacturing facility. The deposition of the second and third layers 107, 109 are preferably done serially, for example, in a vacuum, so as to ensure good adhesion and prevent the formation of a passivation layer on the second barrier 107 at this stage of the process.

The third conductive layer 109, which acts as the seed layer, is then removed from regions outside the recess 27. For example, the recess 27 may be protectively masked using a lithographic process to form a protective resist feature 111, as illustrated in FIG. 8, that is formed using a patterned lithographic mask (not shown). The mask used to pattern the resist feature 111 may be the same mask as used to create the recess 25, except by using a reverse tone resist process. For example, if the recess 25 was formed using a positive resist, then resist feature 111 may be formed from the same mask by using a negative resist. At least a portion of the bottom of the recess 27 must be covered, which will form the conductive path to the conductive feature 20 to allow normal chip operation. The seed layer 109 (e.g. CrCu/Cu) may be removed by an etch process, such as a wet etch, RIE, or preferably, an electroetch process, except where it is protected by the resist feature 111. The electroetch process may be performed, for example, using an aqueous solution including sulfate and glycerin.

Subsequently, the resist 111 is removed by techniques known in the art. Alternatively, if the topography is sufficiently minimized, the seed layer 109 may be removed from the second barrier layer 107 external to the recess, by polishing, e.g. CMP. The resulting structure is illustrated in FIG. 9, in which the seed layer 109 at least covers the bottom surface of the recess 27. Preferably, the seed layer has at least a portion extending along the uppermost surface of the wafer 5 external to the recess 27. This may be done by using the same mask that formed the first recess 25, for example, by using a negative resist, and performing the exposure using an overdose condition, as is well known by those skilled in the art. This provides the advantage that two separate masks will not be required to form patterned recess 25 and patterned recess 27.

Next, a nickel-containing layer 113 is plated on the seed layer 109, as illustrated in FIG. 10. The nickel-containing layer may be essentially nickel, or a nickel alloy, such as NiP or the like. The plating may be performed using an electroplating process or an electroless plating process. Note that, in accordance with the invention, the nickel-containing layer 113 will plate only on the seed layer 109, but not on the second barrier layer 107 which has been passivated by a native oxide. For example, if an electroetch process is performed in the selective removal of the seed layer 109 external to the recess 27, the presence of water in the etch solution provides a source of oxygen for the self-passivation of the second barrier layer 107. The second barrier 107 may also be used as an electrode for subsequent electroplating. For electroplating, the applied potential should be balanced so that the nickel will nucleate on the seed layer 109 and not on the current carrying layer 107. Other factors may be adjusted according to the requirements of the specific tool used, as known in the art, such as current, flow rates and other tool specific parameters. In the case of electroless plating, the second barrier 107 provides a protective barrier preventing ingress of chemicals into the second dielectric layer 105, such as polyimide.

Next, referring now to FIG. 11, a pad layer of noble metal 115 is plated over the nickel-containing layer 113. The pad layer 115 may be a noble metal such as gold, platinum or palladium, more preferably gold. The plating of the noble metal 115 may be performed by an electroplating or electroless plating method. It is preferable that the nickel-containing layer 113 not be allowed to oxidize prior to the plating of the noble metal layer 115, for example, by using a rinse bath between the nickel and gold plating baths. The plating potential should be balanced so that the noble metal 115 will selectively nucleate on the nickel-containing layer 113, but not on the second barrier (e.g. TiW) layer 107. The noble metal pad 115 preferably has a thickness in the range 0.4-0.6 μm, preferably about 0.5 μm thick for a gold pad. The nickel-containing layer 113 must be sufficiently thick so as to prevent intermixing of the noble metal (e.g. gold) and the seed metal (e.g. copper). For example, using a THRU-NIC CL electroplating bath available from Uyemura, a thickness of about 1 μm is preferred.

The second barrier 107 is next removed from areas not covered by the pad 115 (i.e. the field areas) as shown in FIG. 12. The removal may be performed by etching, such as a wet etch or dry etch. Polishing may be used to remove the barrier layer 107 as long as the dielectric layer 105 is not damaged. Preferably, an anisotropic etch, such as RIE is performed. The power for the RIE etch should be as low as possible to remove the barrier

layer 107 from the field areas, such that the pad 115 may be used as a RIE mask such that the noble metal will not sputter. For example, a bias of about 200 watts is sufficient to remove a TiW barrier layer without substantial sputtering of a gold pad. The power used for the RIE will be dependent on the equipment utilized. The structure after removal of the second barrier layer 107 from the field areas is illustrated in FIG. 12.

Subsequently, referring to FIG. 13, a wire 117 may be bonded to the pad 115. The wire 117, which is preferably a noble metal, such as gold, may be bonded to the pad 115 using techniques such as thermosonic bonding, ultrasonic bonding or thermocompression bonding.

One advantage of the present invention is that the size of the pad 115 can be designed to conform more closely with the size of the ball being formed on the pad, thereby reducing the dimensions of the pad compared to conventional pads. For example, referring to FIG. 14A, which illustrates a conventional pad 215 in plan view, such as an aluminum pad, typically a length L1 that is longer than its width W1 to accomodate both a probe mark 219 and a wire bond 217. However, a pad 115 formed in accordance with the present invention, may accomodate both a probe mark (not shown) and a wire bond 117 subsequently formed over the probe mark, so that the length L2 can be substantially reduced compared to the length L1 of conventional pads. For example, if a ball at the end of a wire to be bonded had a diameter of about 45 μm, and the bonding tool has a placement tolerance of ± 2 μm, and an allowance of 1 μm is acceptable, then the pad could be designed to have a width W2 that is equal to its length L2, i.e. having dimensions of 50 μm $\times$ 50 μm. Considering some conventional pads have dimensions of 52 μm $\times$ 145 μm, a pad of dimensions 50 μm $\times$ 50 μm would provid savings of 5040 μm^2 per pad. If the chip has 100 bond pads, the present invention would realize a savings of at least 500,000 μm^2.

The applicants have found that pads formed in accordance with the present invention result in a 30-50% reduction in bonding forces required for wire bond. Such lower forces may permit the pads to be placed over active areas or devices, which would provide a further improvement in chip size.

The present invention also realizes a cost savings in manufacturing. While conventional I/O pads are often manufactured during the final stages of semiconductor processing, the present invention allows the manufacturing of the I/O pads to be performed using current packaging technology, which provides equipment and processing for the deposition of metal over an organic dielectric, such as a CrCu/Cu layers over a spin-on

dielectric such as polyimide. The use of semiconductor equipment and processes is significantly more costly than the use of packaging equipment and processes, due to the higher tolerance requirements during semiconductor manufacturing stages.

While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the following claims.

Industrial Applicability

The structure and method of this invention is useful in manufacturing of integrated circuits and is particularly useful for providing pads for probe testing and wire bond for copper interconnection technology.

Claims

1. A method of manufacturing an input-output structure comprising the steps of:

providing a substrate comprising a dielectric layer having a recess formed therein, wherein said recess has a bottom surface comprising copper;

conformally depositing a first electrically conductive barrier layer on said substrate;

selectively removing said first barrier layer external to said recess so that a portion of said first electrically conductive barrier layer remaining in said recess at least covers said bottom surface;

depositing a second dielectric layer on the surface of said substrate;

forming a second recess in said second dielectric layer so as to expose at least a portion of said first electrically conductive barrier layer covering said bottom surface of said first recess;

conformally depositing a second electrically conductive barrier layer on said substrate having said second recess;

conformally depositing a seed layer on said second electrically conductive barrier layer;

selectively removing said seed layer from the surface of said second barrier layer external to said second recess;

selectively plating a nickel-containing layer on said remaining portion of said seed layer; and

selectively plating a noble metal on said nickel-containing layer.

2. The method of claim 1, wherein said second dielectric layer comprises an organic polymer.

3. The method of claim 2, wherein said organic polymer comprises polyimide.

4. The method of any of claims 1-3 wherein said second electrically conductive barrier layer comprises a material selected from the group consisting of TiW, TiN and TaN.

5. The method of any of claims 1-4 wherein said seed layer comprises a CrCu/Cu layer.

6. The method of any of claims 1-5 wherein said noble metal is selected from the group consisting of gold, platinum and palladium.

7. The method of any of claims 1-6 further comprising, after said step of selectively plating a noble metal, a step of selectively removing exposed portions of said second barrier layer.

8. The method of claim 7 wherein said step of selectively removing exposed portions of said second barrier layer comprises a reactive ion etch at a bias power sufficiently low so that said noble metal does not sputter.

9. The method of any of claims 1-8 further comprising the steps of performing a probe test on said noble metal layer, and bonding a wire to said noble metal layer at substantially the same location of the noble metal layer as the probe test.

10. An input-output structure formed by the method of any of claims 1-9.

FIG. 1

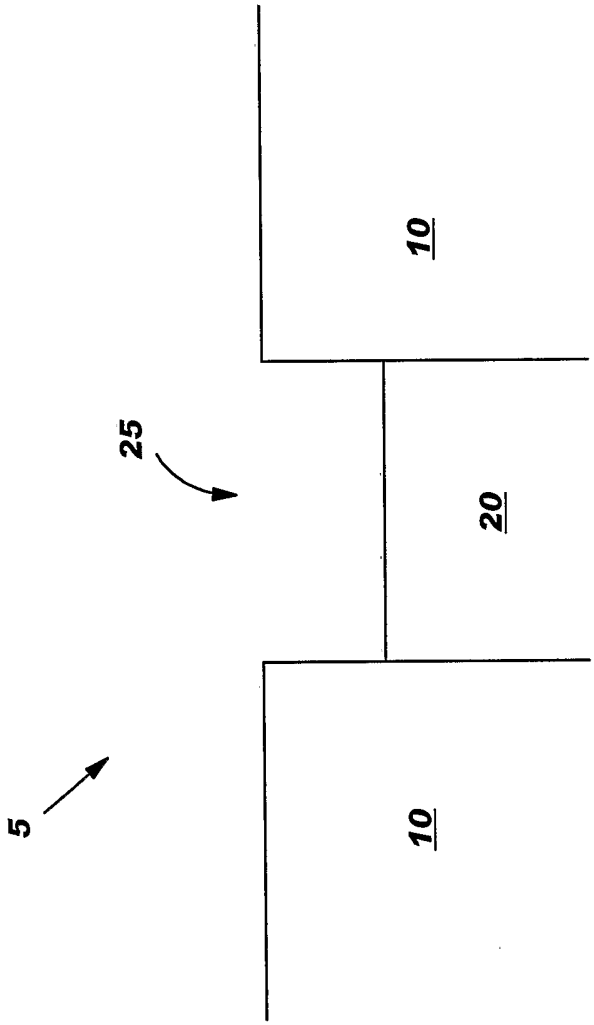


FIG. 2

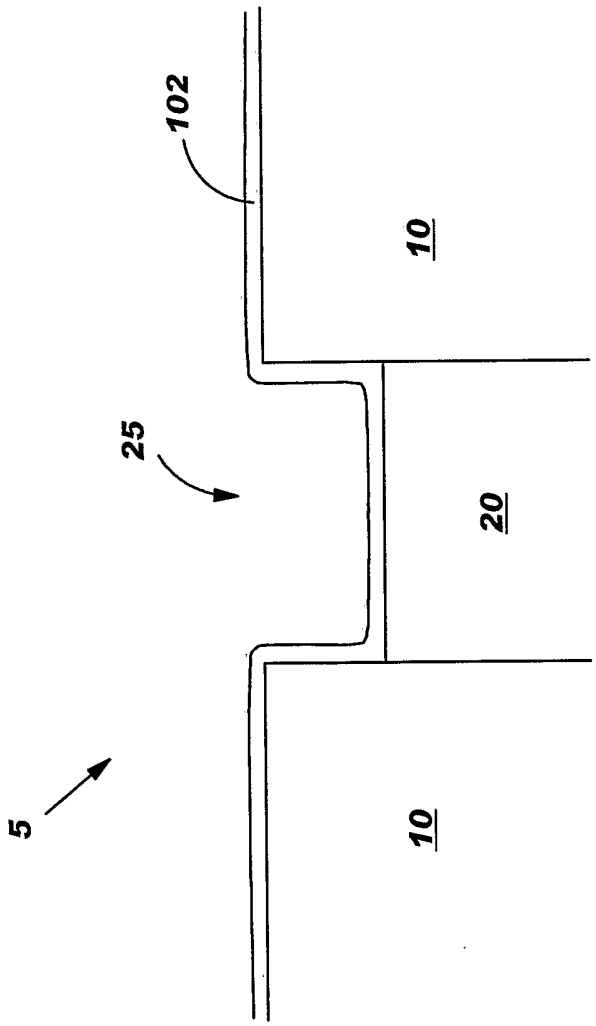


FIG. 3

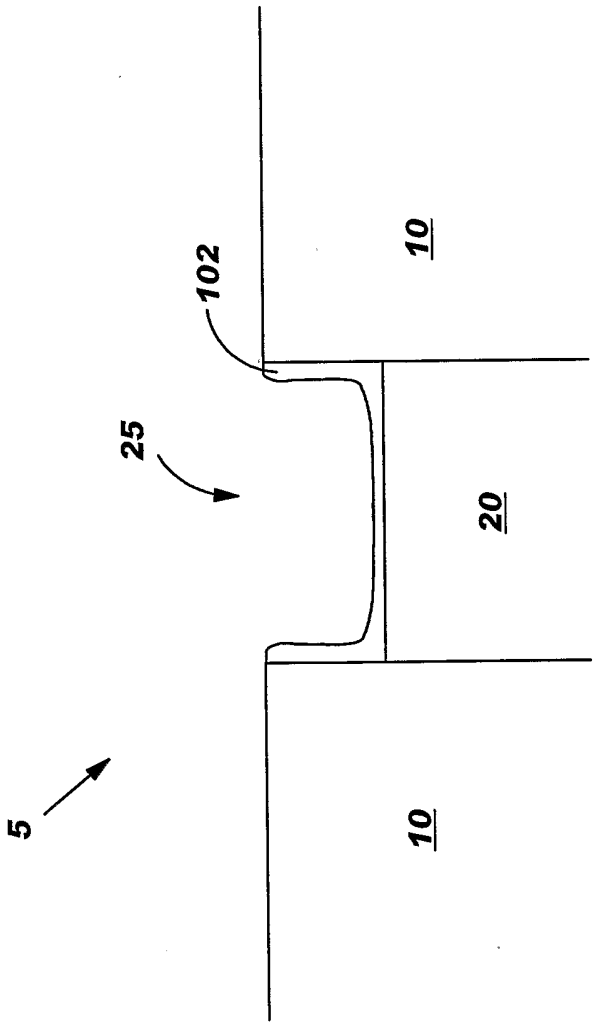


FIG. 4

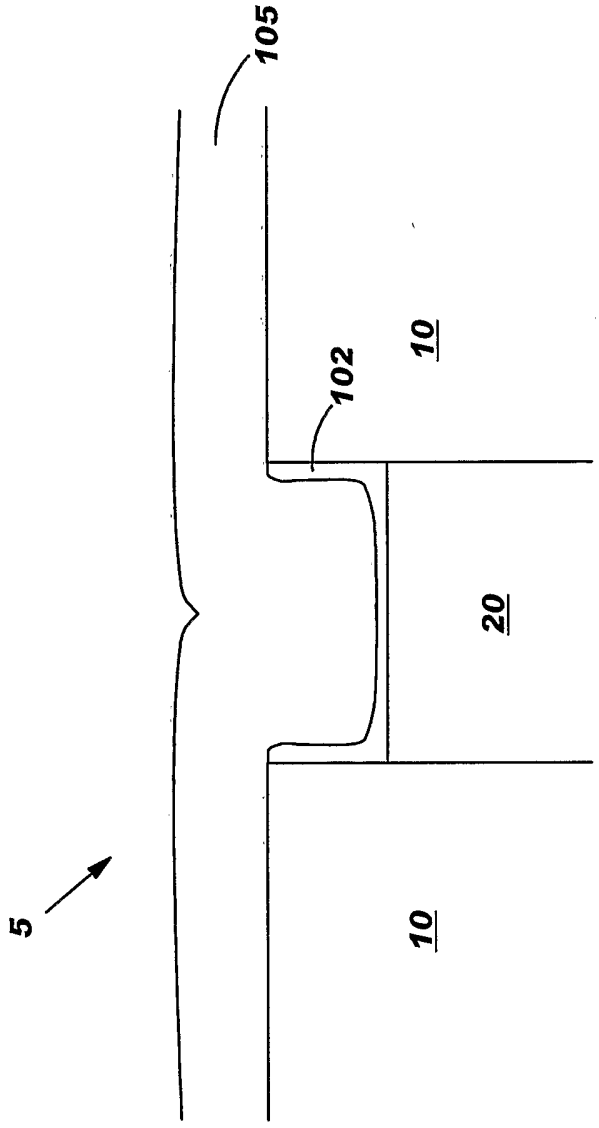


FIG. 5

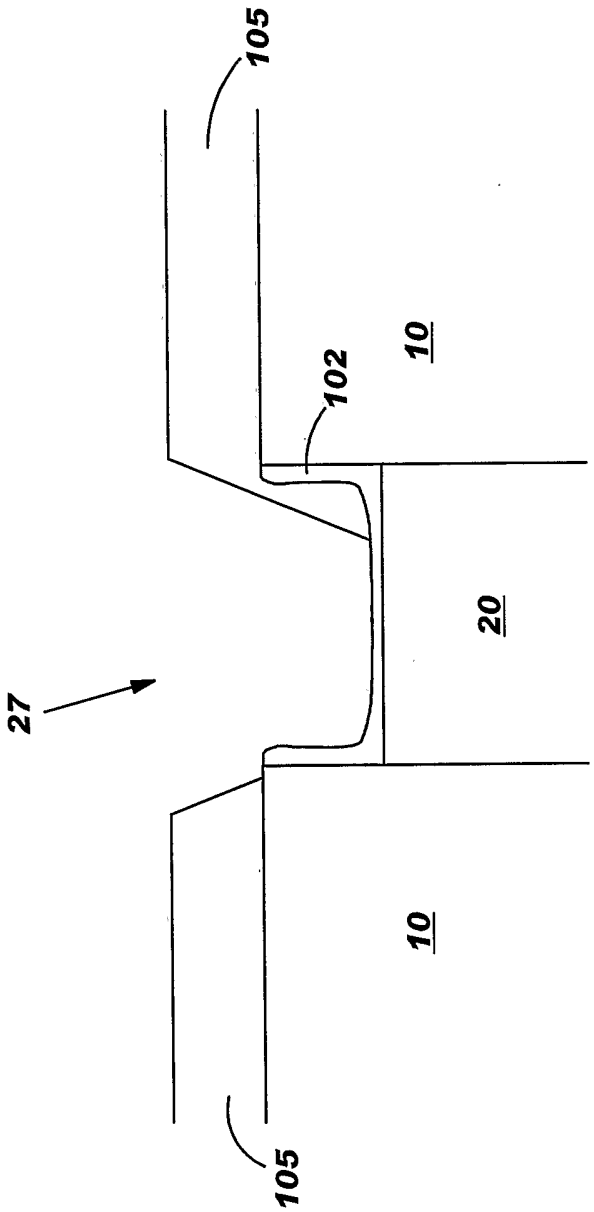


FIG. 6

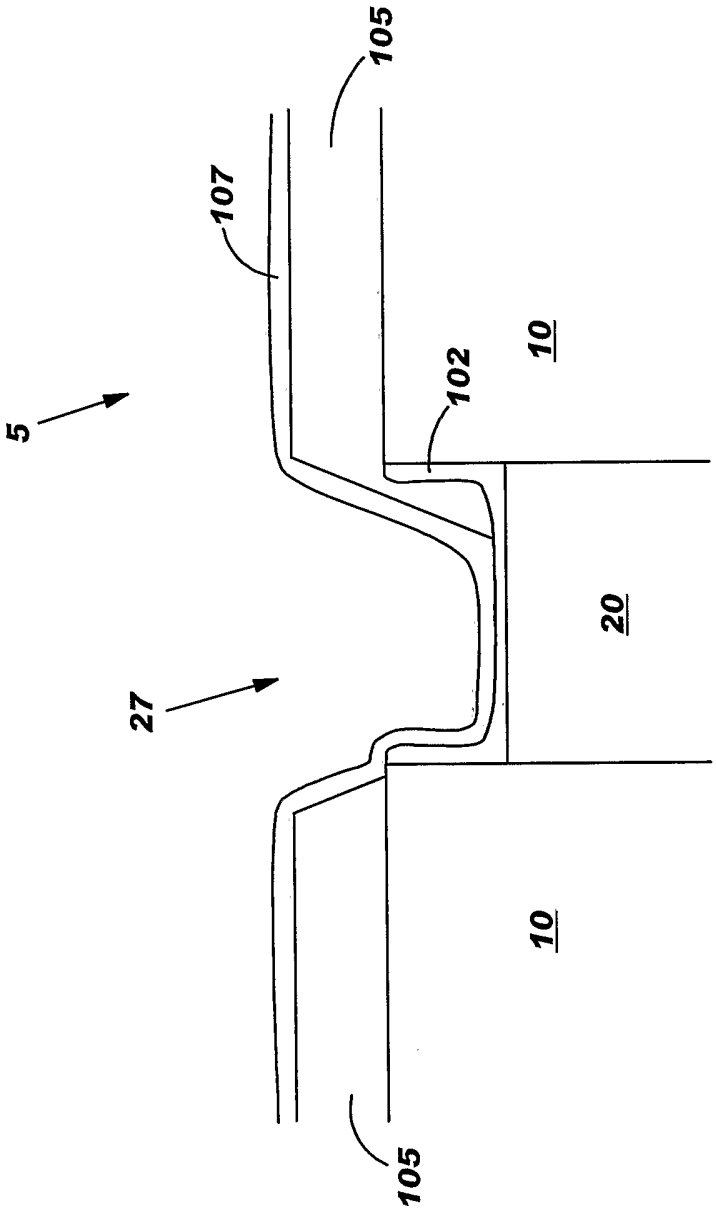


FIG. 7

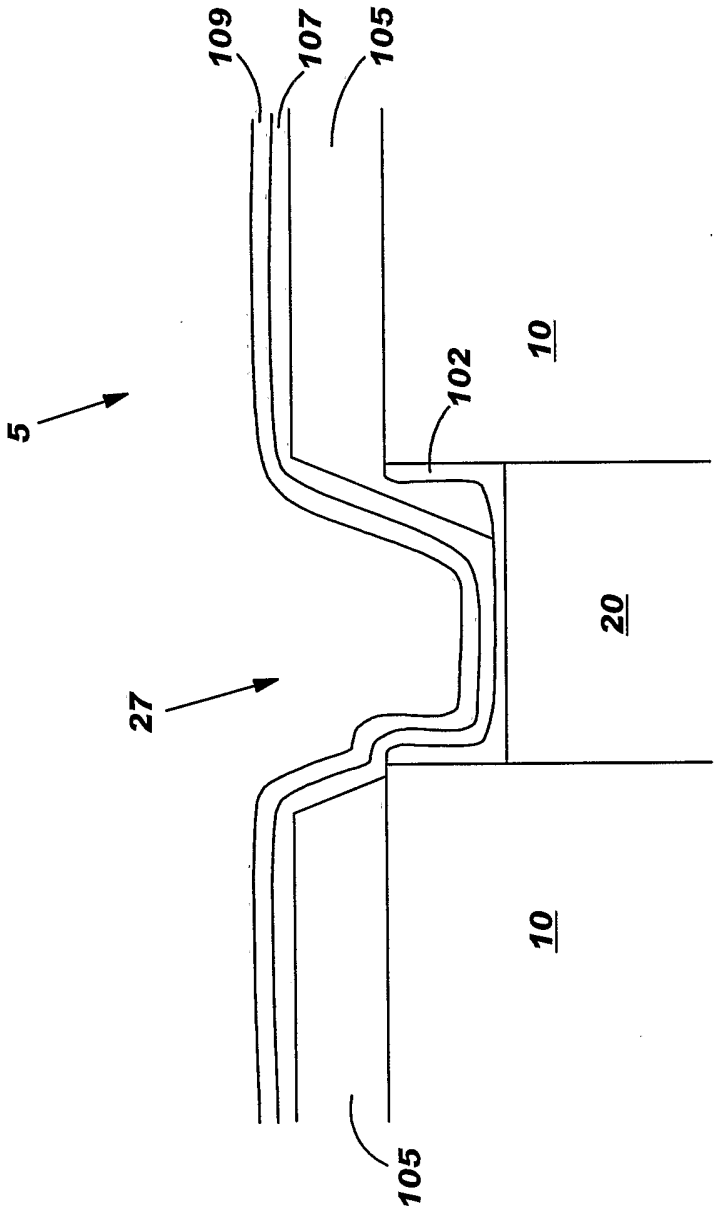


FIG. 8

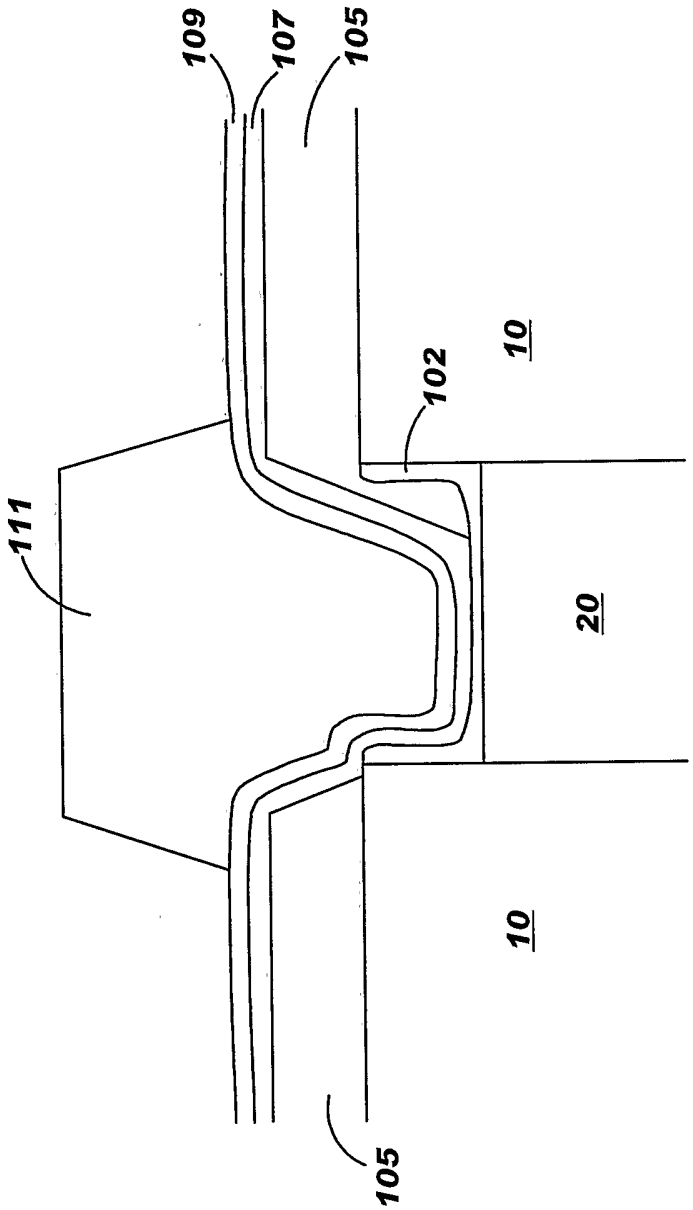


FIG. 9

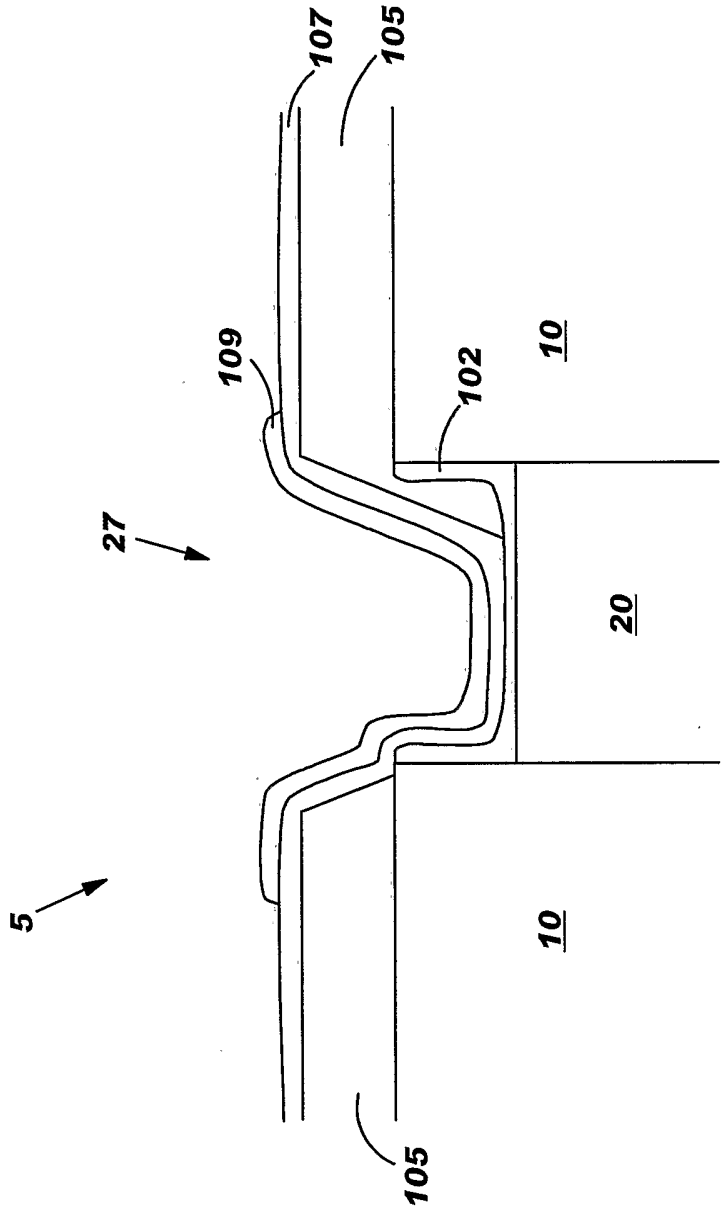


FIG. 10

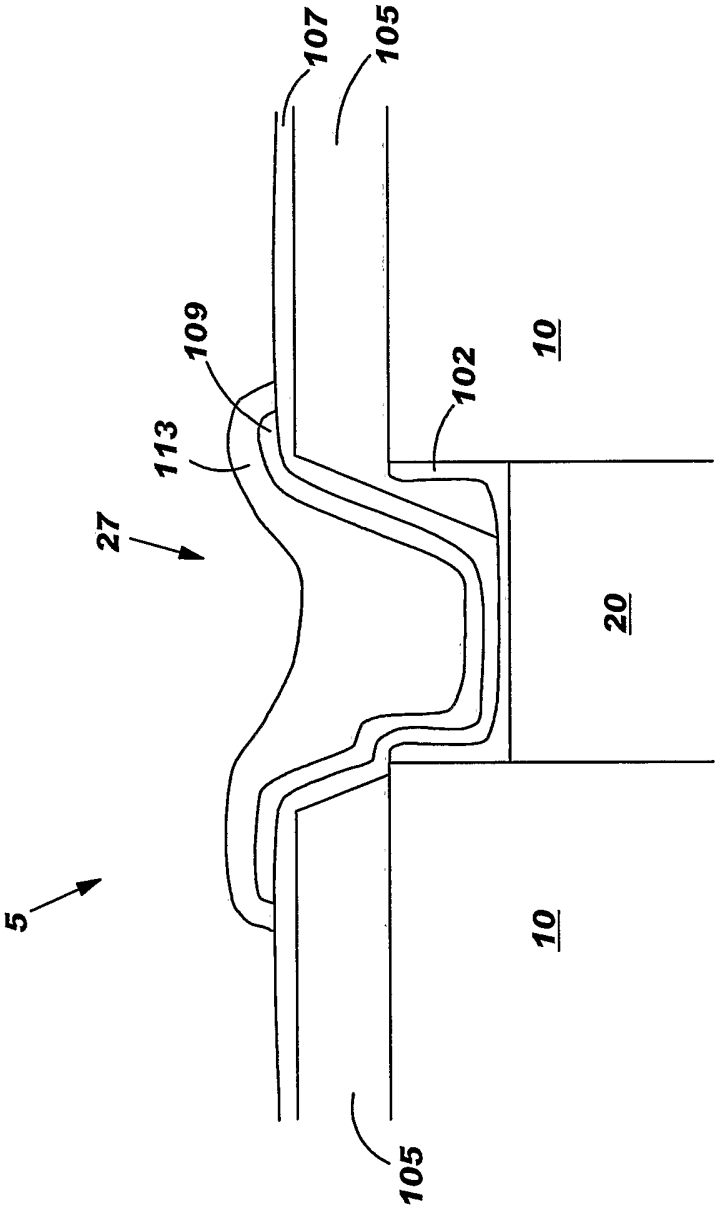


FIG. 11

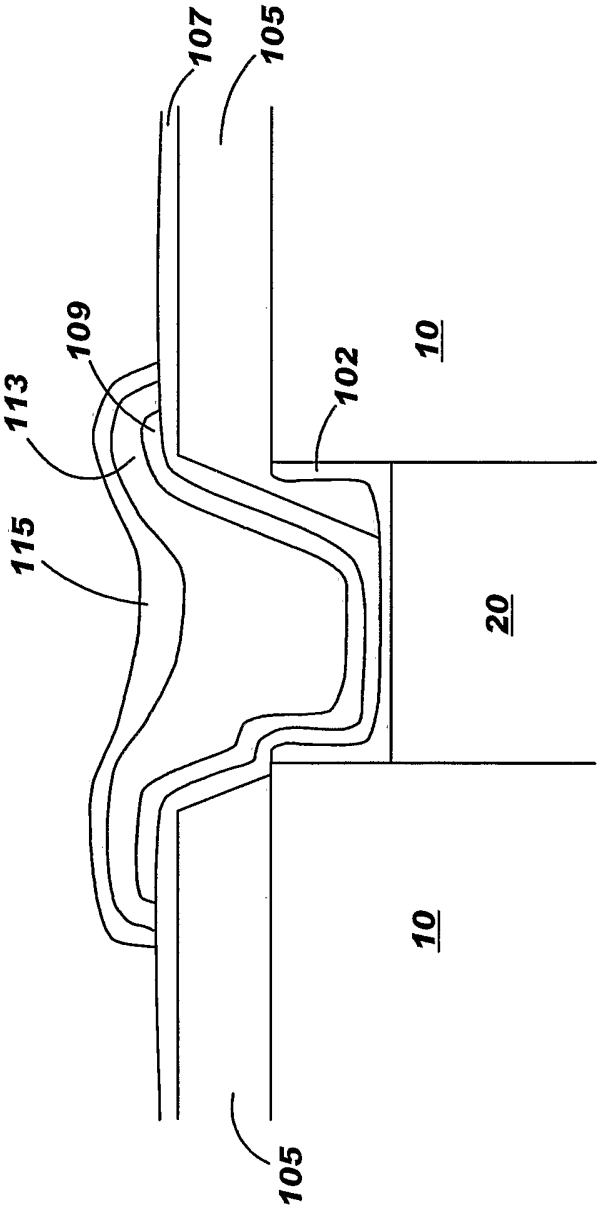


FIG. 12

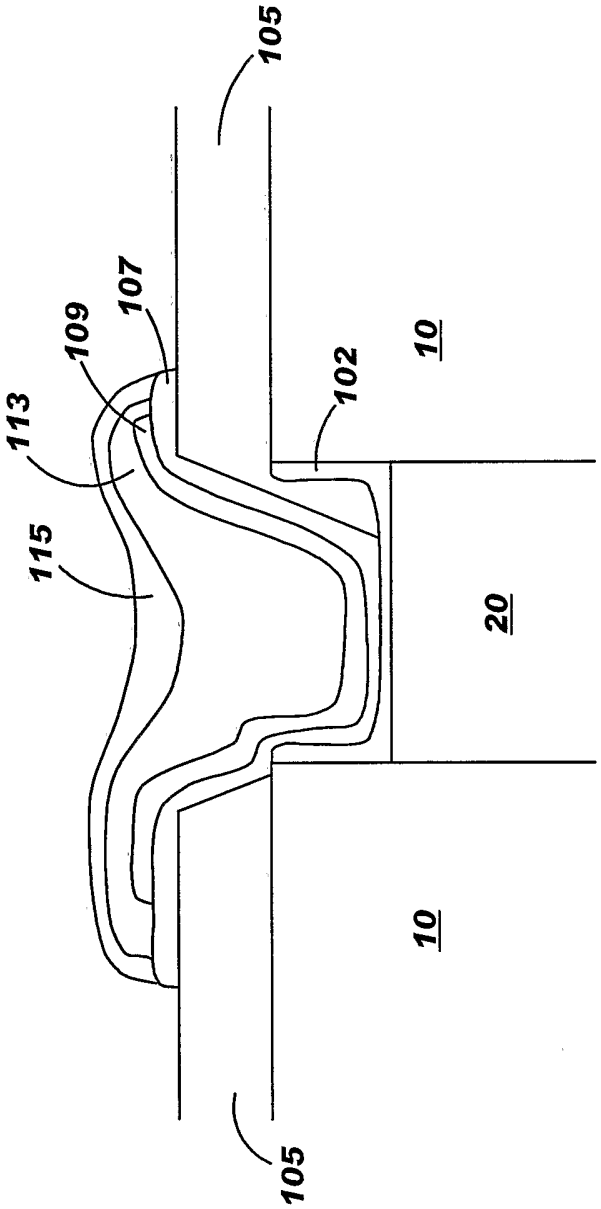


FIG. 13

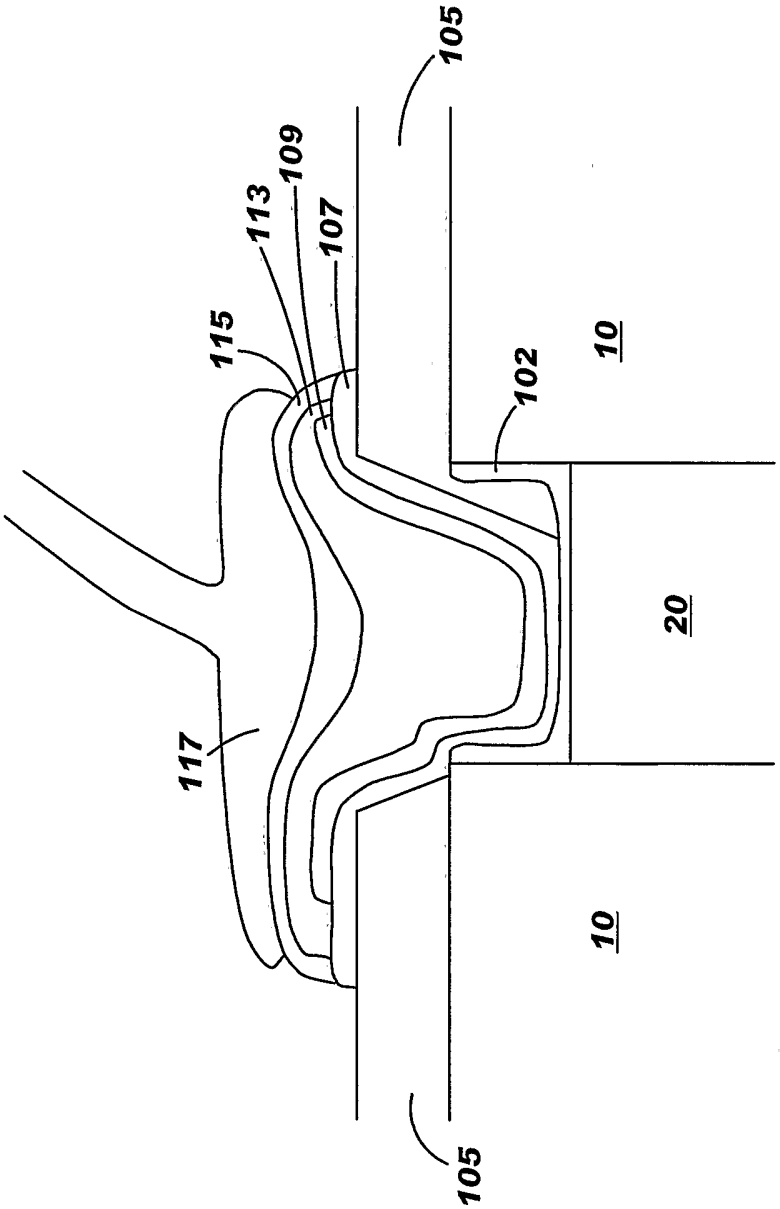


FIG. 14B

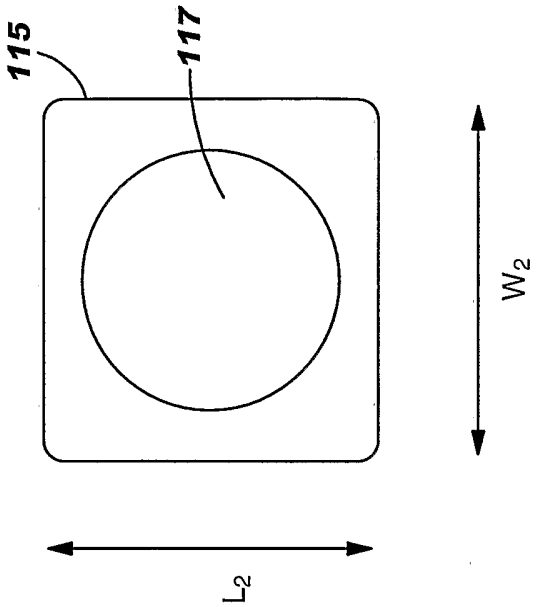
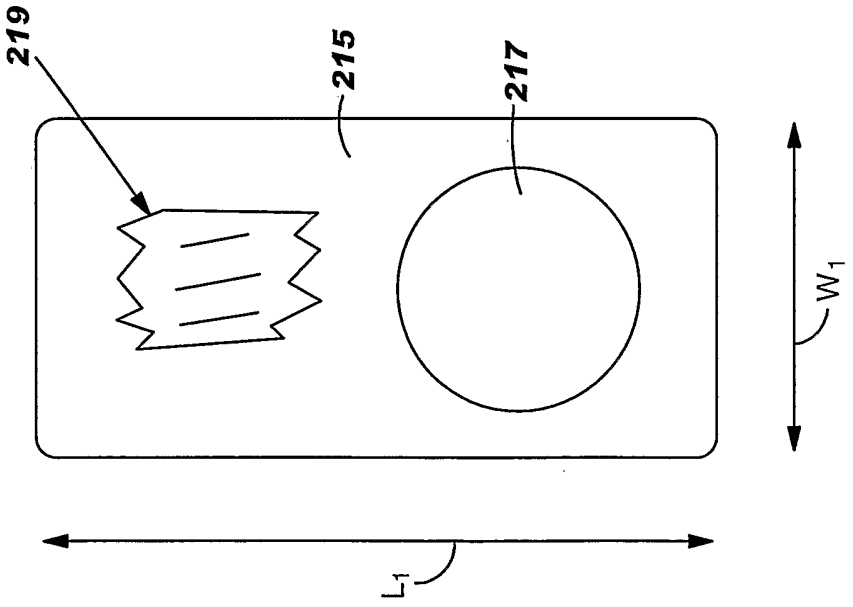


FIG. 14A
Prior Art



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/37162

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/44, 21/48, 21/50, 21/302, 21/461
US CL : 438/106, 612, 614, 617, 685, 687; 257/751, 761, 762, 766, 769, 781, 784

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/106, 612, 614, 617, 685, 687; 257/751, 761, 762, 766, 769, 781, 784

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,534,863 B2 (WALKER et al.) 18 March 2003 (18.03.2003), columns 1-6	1-10
A	US 2001/0033020 A1 (STIERMAN et al.) 25 October 2001 (25.10.2001), pages 1-5	1-10
A	US 2003/0092254 A1 (WALKER et al) 15 May 2003 (15.05.2003), pages 1-4	1-10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

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25 October 2004 (25.10.2004)

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Form PCT/ISA/210 (second sheet) (July 1998)