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(54) **Title**: DUAL SQUELCH DETECTORS AND METHODS FOR LOW POWER STATES

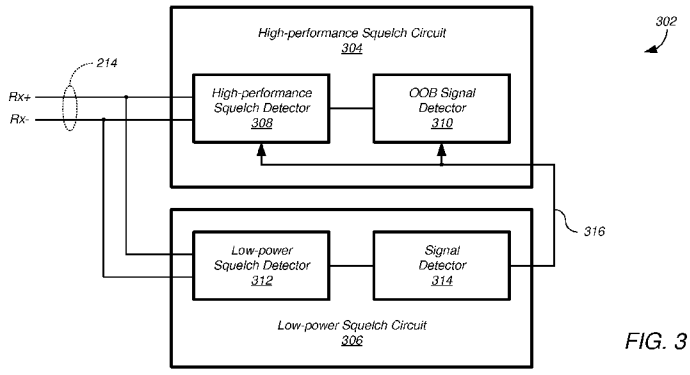

FIG. 3

(57) **Abstract**: Apparatus having corresponding methods comprise: a first squelch circuit configured to detect possible squelch signals in a communication signal; and a second squelch circuit configured to i) operate in a low-power state responsive to the first squelch circuit detecting none of the possible squelch signals in the communication signal, and ii) operate in a high-power state responsive to the first squelch circuit detecting one of the possible squelch signals in the communication signal.

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DUAL SQUELCH DETECTORS AND METHODS FOR LOW POWER STATES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This disclosure claims priority to U.S. Utility Patent Application No. 13/848,817, filed on March 22, 2013, and the benefit of U.S. Provisional Patent Application Serial No. 61/615784, filed on March 26, 2012, entitled "DUAL SQUELCH DETECTOR ARCHITECTURE FOR SATA ATA LOW POWER STATES," the disclosures thereof are incorporated by reference herein in their entirety.

FIELD

[0002] The present disclosure relates generally to the field of digital communication. More particularly, the present disclosure relates to reducing power consumption in communication devices employing squelch detectors.

BACKGROUND

[0003] This background section is provided for the purpose of generally describing the context of the disclosure. Work of the presently named inventor(s), to the extent the work is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0004] The Serial ATA (SATA) interface defines power states that a SATA device or host (both occasionally referred to herein as "SATA devices") can enter to reduce power consumption. Out-of-band (OOB) signals received by a squelch detector are used to communicate during these low-power states. In the lowest-power states, power consumption is limited by the power used by the squelch detector. The SATA specification defines minimum and maximum amplitudes at which to reject and detect the OOB signals, as well as minimum and maximum durations for elements of the OOB signals used to determine OOB signaling

sequences such as COMINIT, COMRESET, and COMWAKE. The squelch detector must consume power to correctly measure these amplitudes and durations, significantly increasing the power consumption of SATA devices in low-power states.

SUMMARY

[0005] In general, in one aspect, an embodiment features an apparatus comprising: a first squelch circuit configured to detect possible squelch signals in a communication signal; and a second squelch circuit configured to i) operate in a low-power state responsive to the first squelch circuit detecting none of the possible squelch signals in the communication signal, and ii) operate in a high-power state responsive to the first squelch circuit detecting one of the possible squelch signals in the communication signal.

[0006] Embodiments of the apparatus can include one or more of the following features. In some embodiments, the second squelch circuit is further configured to: iii) determine an out-of-band (OOB) signaling sequence based on a squelch signal in the communication signal responsive to operating in the high-power state. In some embodiments, the first squelch circuit comprises: a first squelch detector configured to detect one of the possible squelch signals in the communication signal responsive to an amplitude of the one of the possible squelch signals being greater than a threshold amplitude. In some embodiments, the second squelch circuit comprises: a second squelch detector configured to detect the squelch signal in the communication signal responsive to i) the first squelch detector detecting one of the possible squelch signals in the communication signal, ii) an amplitude of the squelch signal being greater than a first threshold amplitude, and iii) the amplitude of the squelch signal being less than a second threshold amplitude, wherein the second threshold amplitude is greater than the first threshold amplitude. In some embodiments, the communication signal is selected from the group consisting of: a serial ATA

(SATA) signal; a PCI Express (PCIe) signal; and a Universal Serial Bus (USB) signal.

[0007] In general, in one aspect, an embodiment features a method comprising: detecting possible squelch signals in a communication signal in a first squelch circuit; operating a second squelch circuit in a low-power state responsive to detecting none of the possible squelch signals in the communication signal in the first squelch circuit; and operating the second squelch circuit in a high-power state responsive to detecting one of the possible squelch signals in the communication signal in the first squelch circuit.

[0008] Embodiments of the method can include one or more of the following features. Some embodiments comprise determining an out-of-band (OOB) signaling sequence based on one of the possible squelch signals responsive to operating in the high-power state. Some embodiments comprise detecting one of the possible squelch signals in the communication signal responsive to an amplitude of the one of the possible squelch signals being greater than a threshold amplitude. Some embodiments comprise detecting a squelch signal in the communication signal responsive to i) detecting one of the possible squelch signals in the communication signal, ii) an amplitude of the squelch signal being greater than a first threshold amplitude, and iii) the amplitude of the squelch signal being less than a second threshold amplitude, wherein the second threshold amplitude is greater than the first threshold amplitude. In some embodiments, the communication signal is selected from the group consisting of: a serial ATA (SATA) signal; a PCI Express (PCIe) signal; and a Universal Serial Bus (USB) signal.

[0009] The details of one or more implementations are set forth in the accompanying drawings and the description below. Other features will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0010] FIG. 1 shows elements of a computing system according to one embodiment.

[0011] FIG. 2 shows detail of a SATA analog front end according to one embodiment.

[0012] FIG. 3 shows detail of a SATA dual squelch detector according to one embodiment.

[0013] FIG. 4 shows a process for the low-power squelch circuit of FIG. 3 according to one embodiment.

[0014] FIG. 5 shows a process for the high-performance squelch circuit of FIG. 3 according to one embodiment.

[0015] FIG. 6 shows detail of a SATA dual squelch detector according to an embodiment where the high-performance squelch circuit enters the high-power state only when an enable signal is asserted.

[0016] The leading digit(s) of each reference numeral used in this specification indicates the number of the drawing in which the reference numeral first appears.

DETAILED DESCRIPTION

[0017] Embodiments of the present disclosure feature dual squelch detectors, and corresponding methods, that significantly lower the power required for squelch detection in low-power states. Although the disclosed embodiments are discussed in terms of Serial ATA (SATA) devices, the techniques disclosed herein apply to other sorts of signals as well, including PCI Express (PCIe) signals, Universal Serial Bus (USB) signals, and the like.

[0018] FIG. 1 shows elements of a computing system 100 according to one embodiment. Although in the described embodiments the elements of the computing system 100 are presented in one arrangement, other embodiments may

feature other arrangements. For example, elements of the computing system 100 can be implemented in hardware, software, or combinations thereof.

[0019] Referring to FIG. 1, the computing system 100 includes a SATA host 102 connected to a SATA device 104 by a cable 106. The SATA host 102 can be implemented, for example, as a personal computer or the like. The SATA device 104 can be implemented, for example, as a hard disk drive or the like. The cable 106 can be implemented, for example, as a flexible printed cable or the like. Both the SATA host 102, and the SATA device 104, include a respective SATA analog front end 108A,B that is connected to the cable 106. Together the SATA analog front ends 108A,B and the cable 106 provide a SATA link.

[0020] FIG. 2 shows detail of a SATA analog front end 202 according to one embodiment. Although in the described embodiments the elements of the SATA analog front end 202 are presented in one arrangement, other embodiments may feature other arrangements. For example, elements of the SATA analog front end 202 can be implemented in hardware, software, or combinations thereof. The SATA analog front end 202 can be used as one or both of the SATA analog front ends 108A,B of FIG. 1.

[0021] Referring to FIG. 2, the SATA analog front end 202 includes a SATA receiver 204, a SATA transmitter 206, and a SATA dual squelch detector 208. The SATA receiver 204, and the SATA transmitter 206, can be implemented according to conventional techniques. The SATA dual squelch detector 208 can be implemented as described below.

[0022] The SATA transmitter 206 receives data (Tx Data), and transmits a differential communication signal 212 on conductors Tx+ and Tx- that represents the data Tx Data over a SATA link. The SATA receiver 204 receives a differential communication signal 214 on conductors Rx+ and Rx- that represents data (Rx Data) over the SATA link, and recovers the data Rx Data from the differential communication signal 214. The SATA dual squelch detector 208 detects squelch signals on the conductors Rx+ and Rx-, and determines out-of-

band (OOB) signaling sequences 216 based on the squelch signals. The OOB signaling sequences 216 can be used by a SATA host 102 or a SATA device 104 to recover from low-power states.

[0023] FIG. 3 shows detail of a SATA dual squelch detector 302 according to one embodiment. Although in the described embodiments the elements of the SATA dual squelch detector 302 are presented in one arrangement, other embodiments may feature other arrangements. For example, elements of the SATA dual squelch detector 302 can be implemented in hardware, software, or combinations thereof. The SATA dual squelch detector 302 can be used as the SATA dual squelch detector 208 of FIG. 2.

[0024] Referring to FIG. 3, the SATA dual squelch detector 302 includes two squelch circuits: a high-performance squelch circuit 304, and a low-power squelch circuit 306. The high-performance squelch circuit 304 is capable of operating in either a high-power state or a low-power state responsive to a control signal 316 provided by the low-power squelch circuit 306. In particular, the high-performance squelch circuit 304 operates in the high-power state responsive to negation of the control signal 316, and operates in the low-power state responsive to assertion of the control signal 316. The high-performance squelch circuit 304 detects squelch signals, and determines out-of-band (OOB) signaling sequences 216 based on the squelch signals, only while operating in the high-power state.

[0025] The high-performance squelch circuit 304 includes a high-performance squelch detector 308 and an out-of band (OOB) signal detector 310. The high-performance squelch detector 308, and the out-of band (OOB) signal detector 310, are each capable of operating in either a high-power state or a low-power state responsive to the control signal 316 provided by the low-power squelch circuit 306.

[0026] In particular, the high-performance squelch detector 308, and the OOB signal detector 310, operate in the high-power state responsive to negation of the

control signal 316, and operate in the low-power state responsive to assertion of the control signal 316.

[0027] The high-performance squelch detector 308 detects squelch signals only while operating in the high-power state. The high-performance squelch detector 308 detects a squelch signal based on the amplitude of the squelch signal and two predetermined amplitude thresholds. In particular, the high-performance squelch detector 308 detects a squelch signal only when the amplitude of the squelch signal falls between the predetermined amplitude thresholds. In one embodiment, the predetermined threshold amplitudes may be 75mV and 200mV. In some embodiments, the high-performance squelch detector 308 detects squelch signals in compliance with all or part of the Serial ATA International Organization: Serial ATA Revision 3.0 specification, the disclosure thereof incorporated by reference herein in its entirety.

[0028] The OOB signal detector 310 determines OOB signaling sequences 216 based on squelch signals only while operating in the high-power state. In particular, the OOB signal detector 310 determines OOB signaling sequences 216 based on minimum and maximum durations for elements of the squelch signal. In some embodiments, the OOB signal detector 310 determines OOB signaling sequences 216 in compliance with all or part of the Serial ATA International Organization: Serial ATA Revision 3.0 specification.

[0029] The low-power squelch circuit 306 controls the power state of the high-performance squelch circuit 304 by asserting and negating the control signal 316. In particular, the low-power squelch circuit 306 negates the control signal 316 responsive to detecting a possible squelch signal, and asserts the control signal 316 otherwise. In this manner, the high-performance squelch circuit 304 is placed in the high-power state only when a possible squelch signal is detected.

[0030] The low-power squelch circuit 306 includes a low-power squelch detector 312 and a signal detector 314. The low-power squelch detector 312 detects a possible squelch signal based on the amplitude of the possible squelch signal and

a predetermined threshold amplitude. In particular, the low-power squelch detector 312 detects a possible squelch signal only when the amplitude of the possible squelch signal is greater than a predetermined threshold amplitude. A signal exceeding the predetermined threshold amplitude may, or may not, be a squelch signal, and so is referred to herein as a "possible squelch signal." In one embodiment, the predetermined threshold amplitude may be 100mV. The signal detector 314 negates the control signal 316 when the low-power squelch detector 312 detects a possible squelch signal in the inbound differential communication signal 214.

[0031] FIG. 4 shows a process 400 for the low-power squelch circuit 306 of FIG. 3 according to one embodiment. Although in the described embodiments the elements of process 400 are presented in one arrangement, other embodiments may feature other arrangements. For example, in various embodiments, some or all of the elements of process 400 can be executed in a different order, concurrently, and the like. Also some elements of process 400 may not be performed, and may not be executed immediately after each other. In addition, some or all of the elements of process 400 can be performed automatically, that is, without human intervention.

[0032] Referring to FIG. 4, at 402, process 400 begins. At 404, the low-power squelch detector 312 monitors the inbound differential communication signal 214 for possible squelch signals. In particular, the low-power squelch detector 312 detects a possible squelch signal when the amplitude of the possible squelch signal is greater than a predetermined threshold amplitude.

[0033] At 406, responsive to the low-power squelch detector 312 detecting no possible squelch signals, at 408 the signal detector 314 asserts, or continues to assert, the control signal 316. But at 406, responsive to the low-power squelch detector 312 detecting a possible squelch signal, at 410 the signal detector 314 negates the control signal 316.

[0034] FIG. 5 shows a process 500 for the high-performance squelch circuit 304 of FIG. 3 according to one embodiment. Although in the described embodiments the elements of process 500 are presented in one arrangement, other embodiments may feature other arrangements. For example, in various embodiments, some or all of the elements of process 500 can be executed in a different order, concurrently, and the like. Also some elements of process 500 may not be performed, and may not be executed immediately after each other. In addition, some or all of the elements of process 500 can be performed automatically, that is, without human intervention.

[0035] Referring to FIG. 5, at 502, process 500 begins. At 504, the high-performance squelch detector 308, and the OOB signal detector 310, monitor the control signal 316. At 506, responsive to detecting the control signal being asserted, at 508, the high-performance squelch detector 308, and the OOB signal detector 310, operate in the low-power state. In the low-power state, the circuits in the high-performance squelch detector 308, and the OOB signal detector 310, can be powered off, except for those circuits required to monitor the control signal 316, and to power on the remaining circuits responsive to detecting the control signal 316 being negated. Then, at 504, the high-performance squelch detector 308, and the OOB signal detector 310, continue to monitor the control signal 316.

[0036] At 506, responsive to detecting the control signal being negated, at 510, the high-performance squelch detector 308, and the OOB signal detector 310, operate in the high-power state. In the high-power state, the circuits in the high-performance squelch detector 308, and the OOB signal detector 310, are powered on and fully functional. Then, at 512, the high-performance squelch detector 308 monitors the inbound differential communication signal 214 for squelch signals. In particular, the high-performance squelch detector 308 detects a squelch signal when the amplitude of the squelch signal is greater than a predetermined minimum threshold amplitude and less than a predetermined maximum threshold amplitude.

[0037] At 514, responsive to the high-performance squelch detector 308 detecting no squelch signal during a predetermined interval, at 508, the high-performance squelch detector 308, and the OOB signal detector 310, operate in the low-power state. Then, at 504, the high-performance squelch detector 308, and the OOB signal detector 310, continue to monitor the control signal 316.

[0038] At 514, responsive to the high-performance squelch detector 308 detecting a squelch signal during the predetermined interval, at 516, the OOB signal detector 310 determines an OOB signaling sequence 216 based on the squelch signal. For example, the OOB signal detector 310 determines a SATA OOB signaling sequence 216 such as COMINIT, COMRESET, and COMWAKE. Then, at 508, the high-performance squelch detector 308, and the OOB signal detector 310, operate in the low-power state. Then, at 504, the high-performance squelch detector 308, and the OOB signal detector 310, continue to monitor the control signal 316.

[0039] In some embodiments, the high-performance squelch circuit 304 enters the high-power state only when an enable signal is asserted. FIG. 6 shows detail of a SATA dual squelch detector 602 according to one such embodiment. Although in the described embodiments the elements of the SATA dual squelch detector 602 are presented in one arrangement, other embodiments may feature other arrangements. For example, elements of the SATA dual squelch detector 602 can be implemented in hardware, software, or combinations thereof. The SATA dual squelch detector 602 can be used as the SATA dual squelch detector 208 of FIG. 2.

[0040] Referring to FIG. 6, the SATA dual squelch detector 602 is similar to the SATA dual squelch detector 302 of FIG. 3, but with the addition of logic 604. Logic 604 negates a control signal 606 only when the control signal 316 is negated, and an enable signal 608 is asserted. The high-performance squelch circuit 304 enters the high-power state only when the control signal 606 is negated. In particular, the high-performance squelch detector 308, and the OOB signal detector 310, enter the high-power state only when the control signal 606

is negated. The enable signal 608 can represent, for example, a link status of the SATA link providing the differential communication signal 214 signal.

[0041] Various embodiments of the present disclosure can be implemented in digital electronic circuitry, or in computer hardware, firmware, software, or in combinations thereof. Embodiments of the present disclosure can be implemented in a computer program product tangibly embodied in a computer-readable storage device for execution by a programmable processor. The described processes can be performed by a programmable processor executing a program of instructions to perform functions by operating on input data and generating output. Embodiments of the present disclosure can be implemented in one or more computer programs that are executable on a programmable system including at least one programmable processor coupled to receive data and instructions from, and to transmit data and instructions to, a data storage system, at least one input device, and at least one output device. Each computer program can be implemented in a high-level procedural or object-oriented programming language, or in assembly or machine language if desired; and in any case, the language can be a compiled or interpreted language. Suitable processors include, by way of example, both general and special purpose microprocessors. Generally, processors receive instructions and data from a read-only memory and/or a random access memory. Generally, a computer includes one or more mass storage devices for storing data files. Such devices include magnetic disks, such as internal hard disks and removable disks, magneto-optical disks; optical disks, and solid-state disks. Storage devices suitable for tangibly embodying computer program instructions and data include all forms of non-volatile memory, including by way of example semiconductor memory devices, such as EPROM, EEPROM, and flash memory devices; magnetic disks such as internal hard disks and removable disks; magneto-optical disks; and CD-ROM disks. Any of the foregoing can be supplemented by, or incorporated in, ASICs (application-specific integrated circuits). As used herein, the term "module" may refer to any of the above implementations.

[0042] A number of implementations have been described. Nevertheless, various modifications may be made without departing from the scope of the disclosure. Accordingly, other implementations are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. An apparatus comprising:

a first squelch circuit configured to detect possible squelch signals in a communication signal; and

a second squelch circuit configured to

i) operate in a low-power state responsive to the first squelch circuit detecting none of the possible squelch signals in the communication signal, and

ii) operate in a high-power state responsive to the first squelch circuit detecting one of the possible squelch signals in the communication signal.

2. The apparatus of claim 1, wherein the second squelch circuit is further configured to:

iii) determine an out-of-band (OOB) signaling sequence based on a squelch signal in the communication signal responsive to operating in the high-power state.

3. The apparatus of claim 2, wherein the first squelch circuit comprises:

a first squelch detector configured to detect one of the possible squelch signals in the communication signal responsive to an amplitude of the one of the possible squelch signals being greater than a threshold amplitude.

4. The apparatus of claim 3, wherein the first squelch circuit further comprises:

a signal detector configured to negate a control signal responsive to the first squelch detector detecting one of the possible squelch signals in the communication signal;

wherein the second squelch circuit is further configured to operate in the high-power state responsive to the control signal being negated.

5. The apparatus of claim 3, wherein the first squelch circuit further comprises:

a signal detector configured to negate a first control signal responsive to the first squelch detector detecting one of the possible squelch signals in the communication signal; and

logic configured to negate a second control signal responsive to

i) the first control signal being negated, and

ii) an enable signal being asserted;

wherein the second squelch circuit is further configured to operate in the high-power state responsive to the second control signal being negated.

6. The apparatus of claim 5, wherein:

the enable signal represents a link status of a link, wherein the link provides the communication signal to the apparatus.

7. The apparatus of claim 2, wherein the second squelch circuit comprises:

a second squelch detector configured to detect the squelch signal in the communication signal responsive to

i) the first squelch detector detecting one of the possible squelch signals in the communication signal,

ii) an amplitude of the squelch signal being greater than a first threshold amplitude, and

iii) the amplitude of the squelch signal being less than a second threshold amplitude, wherein the second threshold amplitude is greater than the first threshold amplitude.

8. The apparatus of claim 7, wherein the second squelch circuit further comprises:

an OOB signal detector configured to determine the OOB signaling sequence based on the squelch signal responsive to the second squelch detector detecting the squelch signal in the communication signal.

9. The apparatus of claim 1, wherein the communication signal is selected from the group consisting of:

a serial ATA (SATA) signal;

a PCI Express (PCIe) signal; and

a Universal Serial Bus (USB) signal.

10. One or more integrated circuits comprising the apparatus of claim 1.

11. An analog front end comprising the apparatus of claim 1.

12. A communications device comprising the analog front end of claim 11.

13. The apparatus of claim 1, wherein the apparatus is compliant with all or part of the Serial ATA International Organization: Serial ATA Revision 3.0 specification.

14. A method comprising:

detecting possible squelch signals in a communication signal in a first squelch circuit;

operating a second squelch circuit in a low-power state responsive to detecting none of the possible squelch signals in the communication signal in the first squelch circuit; and

operating the second squelch circuit in a high-power state responsive to detecting one of the possible squelch signals in the communication signal in the first squelch circuit.

15. The method of claim 14, further comprising:

determining an out-of-band (OOB) signaling sequence based on one of the possible squelch signals responsive to operating in the high-power state.

16. The method of claim 15, further comprising:

detecting one of the possible squelch signals in the communication signal responsive to an amplitude of the one of the possible squelch signals being greater than a threshold amplitude.

17. The method of claim 16, further comprising:

negating a control signal responsive to detecting one of the possible squelch signals in the communication signal; and

operating the second squelch circuit in the high-power state responsive to the control signal being negated.

18. The method of claim 16, further comprising:

negating a first control signal responsive to the first squelch detector detecting one of the possible squelch signals in the communication signal;

negating a second control signal responsive to

i) the first control signal being negated, and

ii) an enable signal being asserted; and

operating the second squelch circuit in the high-power state responsive to the second control signal being negated.

19. The method of claim 18, wherein:

the enable signal represents a link status of a link, wherein the link provides the communication signal.

20. The method of claim 15, further comprising:

detecting a squelch signal in the communication signal responsive to

i) detecting one of the possible squelch signals in the communication signal,

ii) an amplitude of the squelch signal being greater than a first threshold amplitude, and

iii) the amplitude of the squelch signal being less than a second threshold amplitude, wherein the second threshold amplitude is greater than the first threshold amplitude.

21. The method of claim 20, further comprising:

determining the OOB signaling sequence based on the squelch signal responsive to detecting the squelch signal in the communication signal.

22. The method of claim 14, wherein the communication signal is selected from the group consisting of:

a serial ATA (SATA) signal;

a PCI Express (PCIe) signal; and

a Universal Serial Bus (USB) signal.

AMENDED CLAIMS
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1. An apparatus comprising:

a first squelch circuit configured to detect possible squelch signals in a communication signal; and

a second squelch circuit configured to

i) selectively detect the possible squelch signals in the same communication signal,

ii) operate in a low-power state responsive to the first squelch circuit detecting none of the possible squelch signals in the communication signal, and

iii) operate in a high-power state responsive to the first squelch circuit detecting one of the possible squelch signals in the communication signal.

2. The apparatus of claim 1, wherein the second squelch circuit is further configured to:

iv) determine an out-of-band (OOB) signaling sequence based on a squelch signal in the communication signal responsive to operating in the high-power state.

3. The apparatus of claim 2, wherein the first squelch circuit comprises:

a first squelch detector configured to detect one of the possible squelch signals in the communication signal responsive to an amplitude of the one of the possible squelch signals being greater than a threshold amplitude.

4. The apparatus of claim 3, wherein the first squelch circuit further comprises:

a signal detector configured to negate a control signal responsive to the first squelch detector detecting one of the possible squelch signals in the communication signal,

wherein the second squelch circuit is further configured to operate in the high-power state responsive to the control signal being negated.

5. The apparatus of claim 3, wherein the first squelch circuit further comprises:

a signal detector configured to negate a first control signal responsive to the first squelch detector detecting one of the possible squelch signals in the communication signal; and

logic configured to negate a second control signal responsive to

i) the first control signal being negated, and

ii) an enable signal being asserted,

wherein the second squelch circuit is further configured to operate in the high-power state responsive to the second control signal being negated.

6. The apparatus of claim 5, wherein:

the enable signal represents a link status of a link, and

the link provides the communication signal to the apparatus.

7. The apparatus of claim 2, wherein the second squelch circuit comprises:

a second squelch detector configured to detect the squelch signal in the communication signal responsive to

i) the first squelch circuit detecting one of the possible squelch signals in the communication signal,

ii) an amplitude of the squelch signal being greater than a first threshold amplitude, and

iii) the amplitude of the squelch signal being less than a second threshold amplitude, wherein the second threshold amplitude is greater than the first threshold amplitude.

8. The apparatus of claim 7, wherein the second squelch circuit further comprises:

an OOB signal detector configured to determine the OOB signaling sequence based on the squelch signal responsive to the second squelch detector detecting the squelch signal in the communication signal.

9. The apparatus of claim 1, wherein the communication signal is selected from the group consisting of:

a serial ATA (SATA) signal;

a PCI Express (PCIe) signal; and

a Universal Serial Bus (USB) signal.

10. One or more integrated circuits comprising the apparatus of claim 1.

11. An analog front end comprising the apparatus of claim 1.

12. A communications device comprising the analog front end of claim 11.

13. The apparatus of claim 1, wherein the apparatus is otherwise compliant with the Serial ATA International Organization: Serial ATA Revision 3.0 specification.

14. A method comprising:

detecting possible squelch signals in a communication signal using a first squelch circuit;

selectively detecting the possible squelch signals using the same communication signal in a second squelch circuit;

operating the second squelch circuit in a low-power state responsive to detecting none of the possible squelch signals in the communication signal in the first squelch circuit; and

operating the second squelch circuit in a high-power state responsive to detecting one of the possible squelch signals in the communication signal in the first squelch circuit.

15. The method of claim 14, further comprising:

determining an out-of-band (OOB) signaling sequence based on one of the possible squelch signals responsive to operating in the high-power state.

16. The method of claim 15, further comprising:

detecting one of the possible squelch signals in the communication signal responsive to an amplitude of the one of the possible squelch signals being greater than a threshold amplitude.

17. The method of claim 16, further comprising:

negating a control signal responsive to detecting one of the possible squelch signals in the communication signal; and

operating the second squelch circuit in the high-power state responsive to the control signal being negated.

18. The method of claim 16, further comprising:

negating a first control signal responsive to detecting one of the possible squelch signals in the communication signal;

negating a second control signal responsive to

i) the first control signal being negated, and

ii) an enable signal being asserted; and

operating the second squelch circuit in the high-power state responsive to the second control signal being negated.

19. The method of claim 18, wherein:

the enable signal represents a link status of a link, wherein the link provides the communication signal.

20. The method of claim 15, further comprising:

detecting a squelch signal in the communication signal responsive to

i) detecting one of the possible squelch signals in the communication signal,

ii) an amplitude of the squelch signal being greater than a first threshold amplitude, and

iii) the amplitude of the squelch signal being less than a second threshold amplitude, wherein the second threshold amplitude is greater than the first threshold amplitude.

21. The method of claim 20, further comprising:

determining the OOB signaling sequence based on the squelch signal responsive to detecting the squelch signal in the communication signal.

22. The method of claim 14, wherein the communication signal is selected from the group consisting of:

a serial ATA (SATA) signal;

a PCI Express (PCIe) signal; and

a Universal Serial Bus (USB) signal.

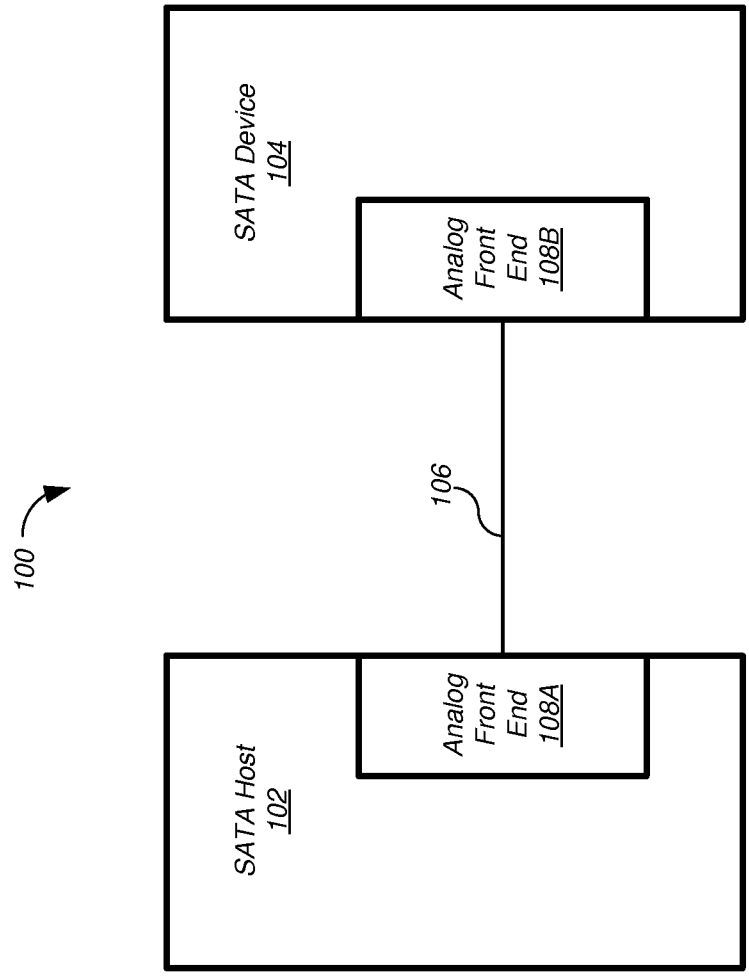
100
SATA Host
102
Analog
Front
End
108A
106
SATA Device
104
Analog
Front
End
108B

FIG. 1

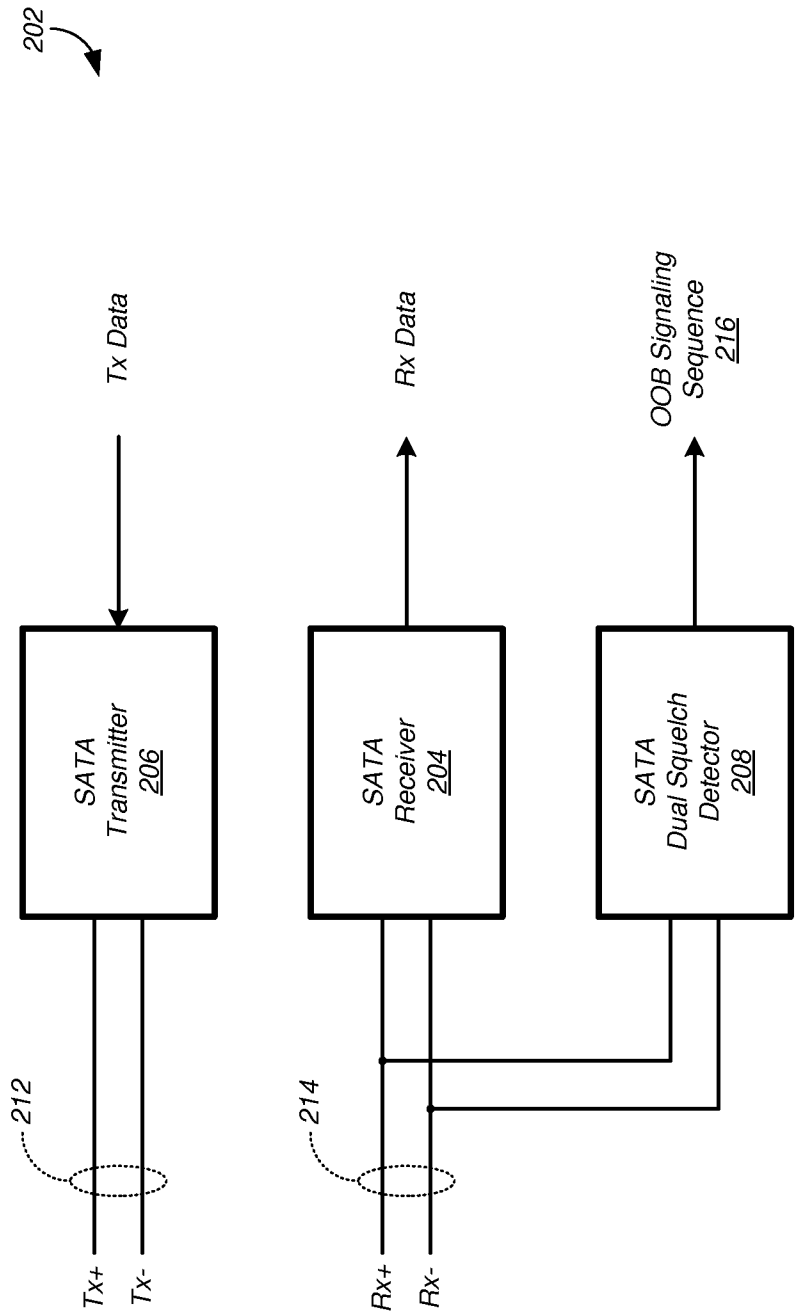
202
Tx Data
Rx Data
OOB Signaling Sequence 216
SATA Transmitter 206
SATA Receiver 204
SATA Dual Squelch Detector 208
212
214
Tx+
Tx-
Rx+
Rx-

FIG. 2

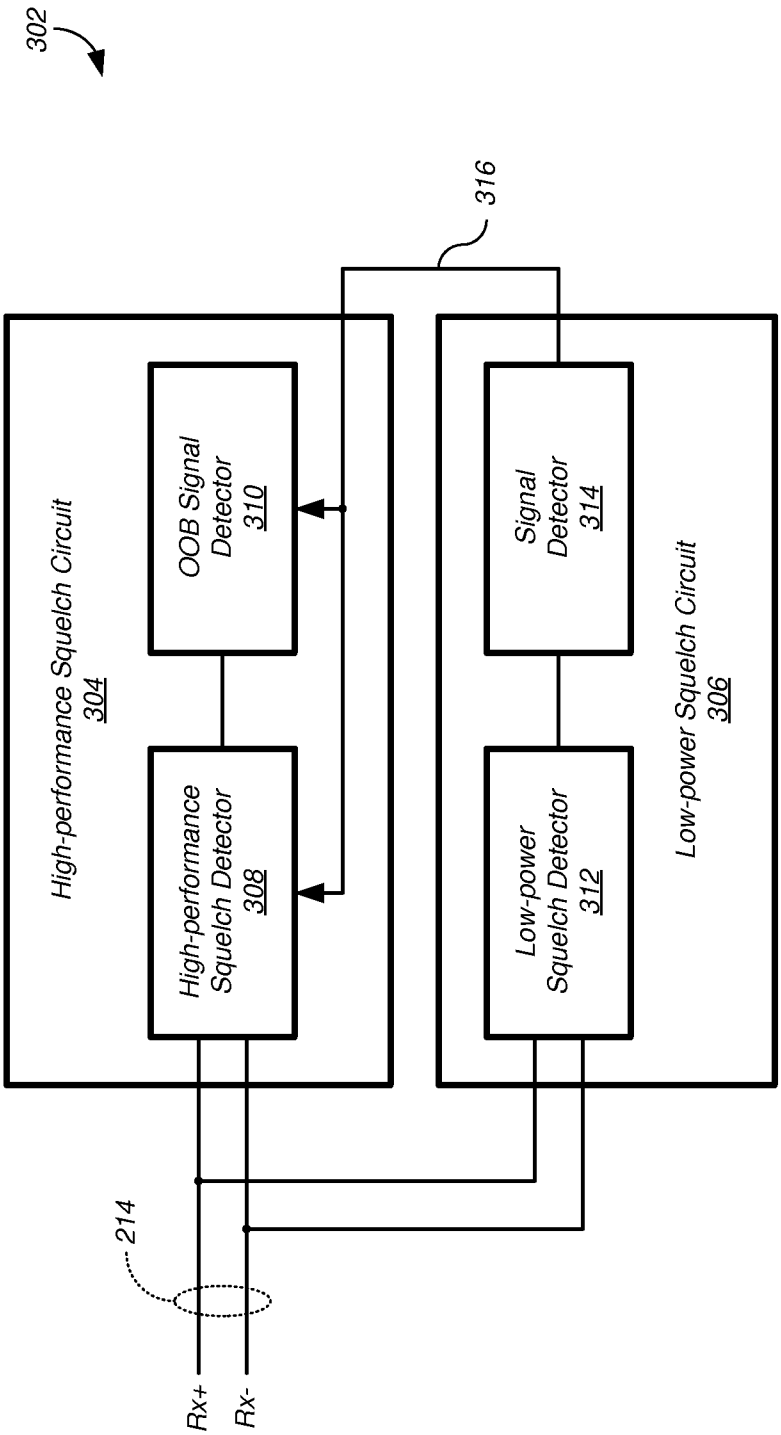
302
316
High-performance Squelch Circuit
304
OOB Signal Detector
310
High-performance Squelch Detector
308
Low-power Squelch Circuit
306
Signal Detector
314
Low-power Squelch Detector
312
214
Rx+
Rx-

FIG. 3

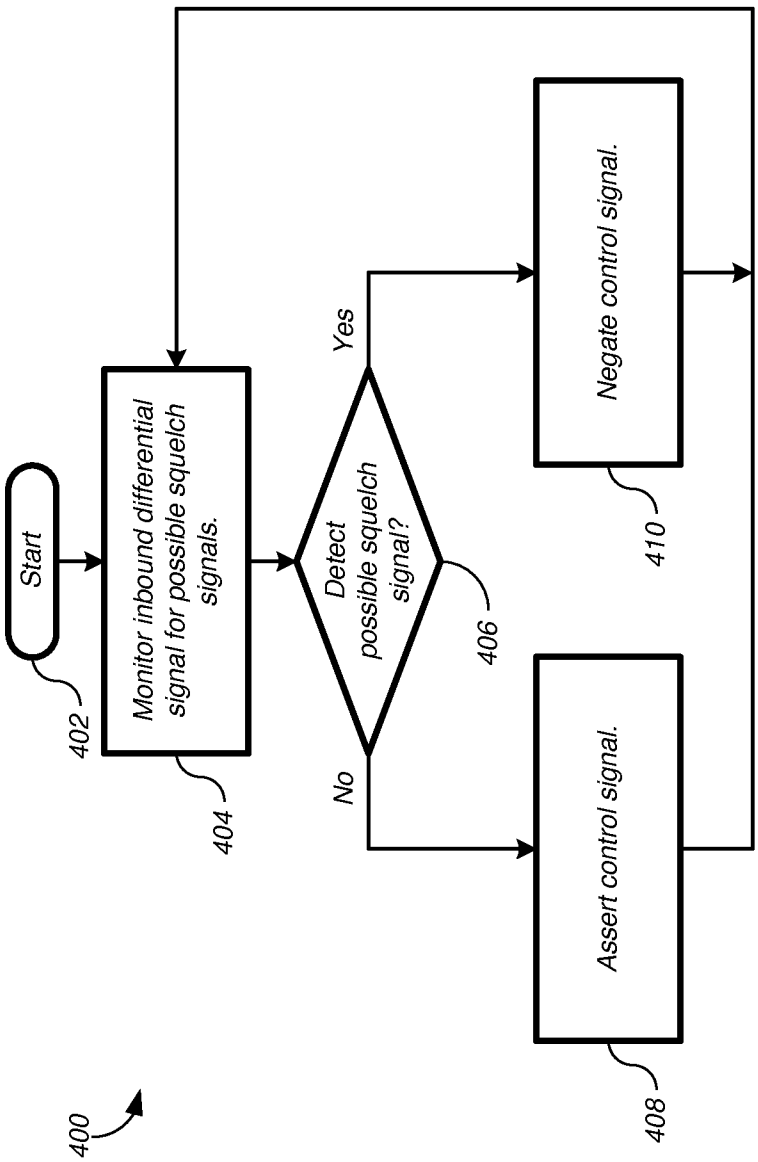
Start
Monitor inbound differential signal for possible squelch signals.
Detect possible squelch signal?
Yes
No
Negate control signal.
Assert control signal.
402
404
406
408
410
400

FIG. 4

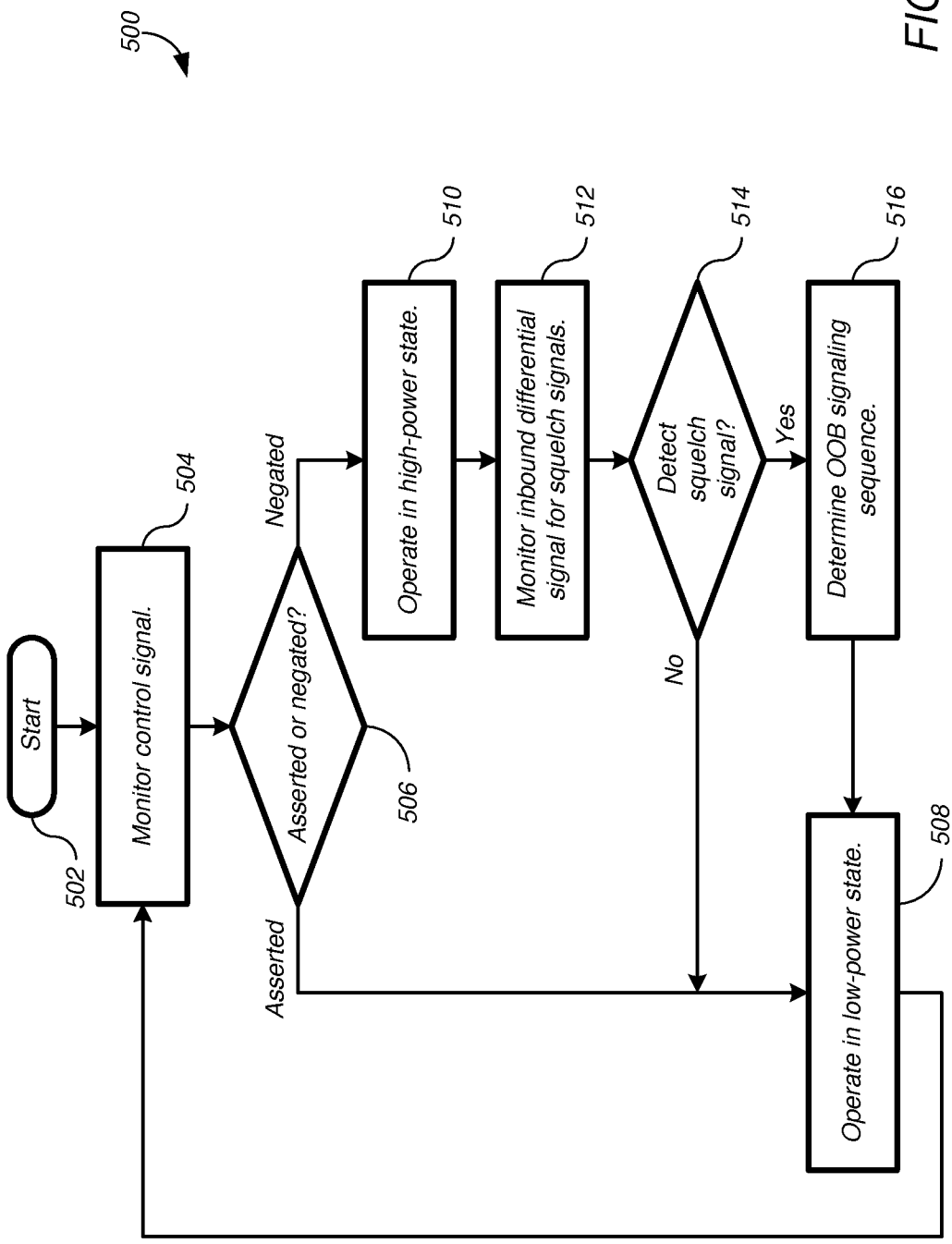
500
Start
502
Monitor control signal.
504
Asserted or negated?
506
Asserted
Negated
Operate in high-power state.
510
Monitor inbound differential signal for squelch signals.
512
Detect squelch signal?
514
Yes
No
Determine OOB signaling sequence.
516
Operate in low-power state.
508

FIG. 5

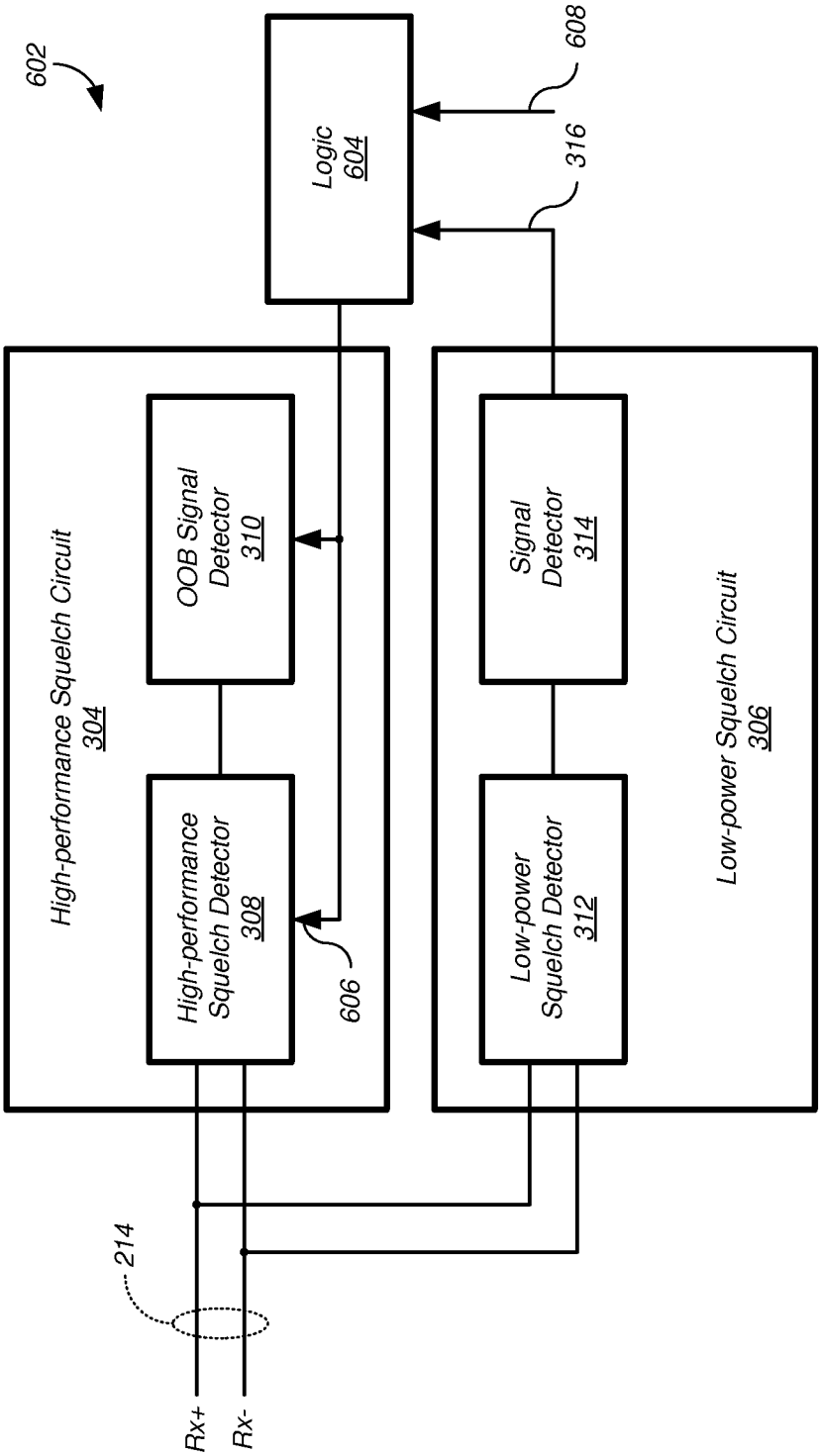
602
Logic
604
608
316
High-performance Squelch Circuit
304
OOB Signal
Detector
310
High-performance
Squelch Detector
308
606
Signal
Detector
314
Low-power
Squelch Detector
312
Low-power Squelch Circuit
306
214
Rx+
Rx-

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/033711

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F1/32
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2010/081406 A1 (TAN SIN [US] ET AL) 1 April 2010 (2010-04-01) paragraph [0008] - paragraph [0012]	1,14 2-13, 15-22
X,P	DE 10 2011 089875 A1 (SAMSUNG ELECTRONICS CO LTD [KR]) 26 July 2012 (2012-07-26) paragraph [0055]	1-22
Y	US 2009/083587 A1 (NG JIEN-HAU [MY] ET AL) 26 March 2009 (2009-03-26) the whole document	2-13, 15-22
A	US 2005/054311 A1 (KOMATSU DANICHI [JP] ET AL) 10 March 2005 (2005-03-10) the whole document	1-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 June 2013	28/06/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ghidini, Mario

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/033711

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		DE 102011089875 A1	26-07-2012
		JP 2012155711 A	16-08-2012
		KR 20120086542 A	03-08-2012
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		US 2012280719 A1	08-11-2012
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