

[54] **ELECTRONIC COMBINATION LOCK SYSTEM**

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[57]

ABSTRACT

A combination lock system of the electronic type for doors and other applications includes digit selector switches at each door location or station and a central comparator utilizing NAND gates, separate comparator units being provided for each digit. A multiple digit code is selected by simple switch means such as multiple contact thumb wheel switches and the code may be changed quickly at any time with no modification or rewiring of the circuits. The system includes a timer for resetting the entire system if the code is not entered within a preselected time and a control for resetting the system in the event that more than the number of digits in the code are entered. An alarm system is provided to indicate the selector station at which more than a predetermined excess number of digits are entered, thus indicating a possible attempt to break the code at that station. In addition the selection of a digit at any station disables all other stations and actuates indicators at all stations showing that the system is in use. A plurality of such combination systems each having its respective central comparator may be controlled by a single digit code selector or determinator so that the same code must be entered for all stations but so that the signal entry, indicator, resetting and alarm functions of each system are independent of those of the other systems.

18 Claims, 6 Drawing Figures

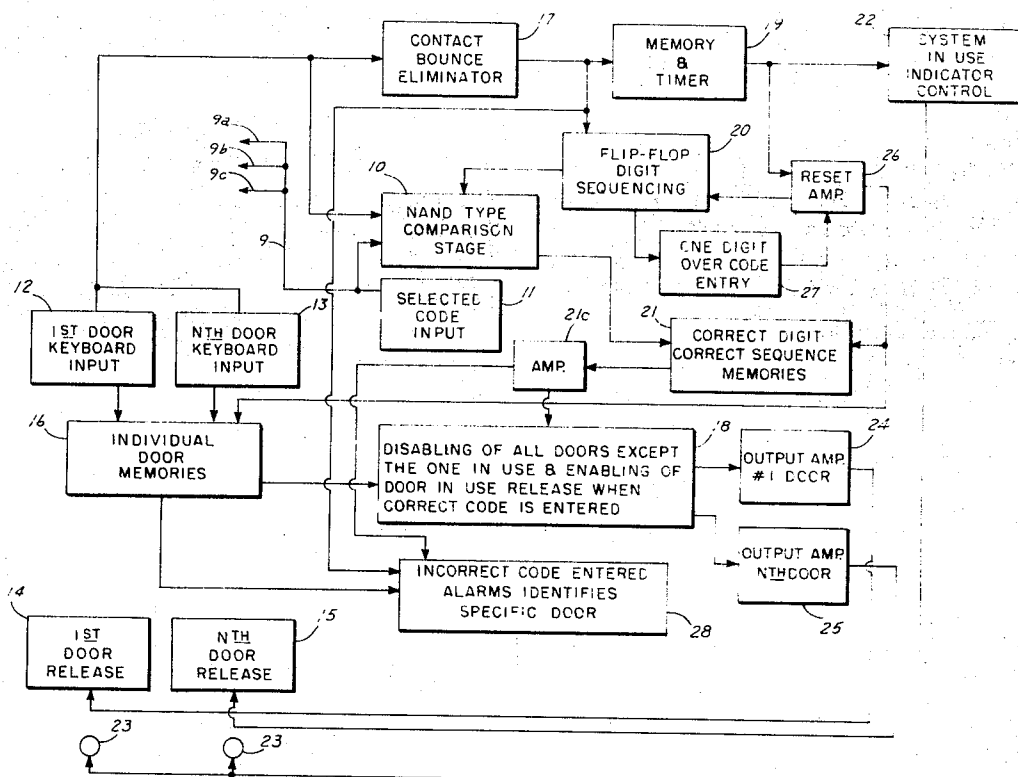
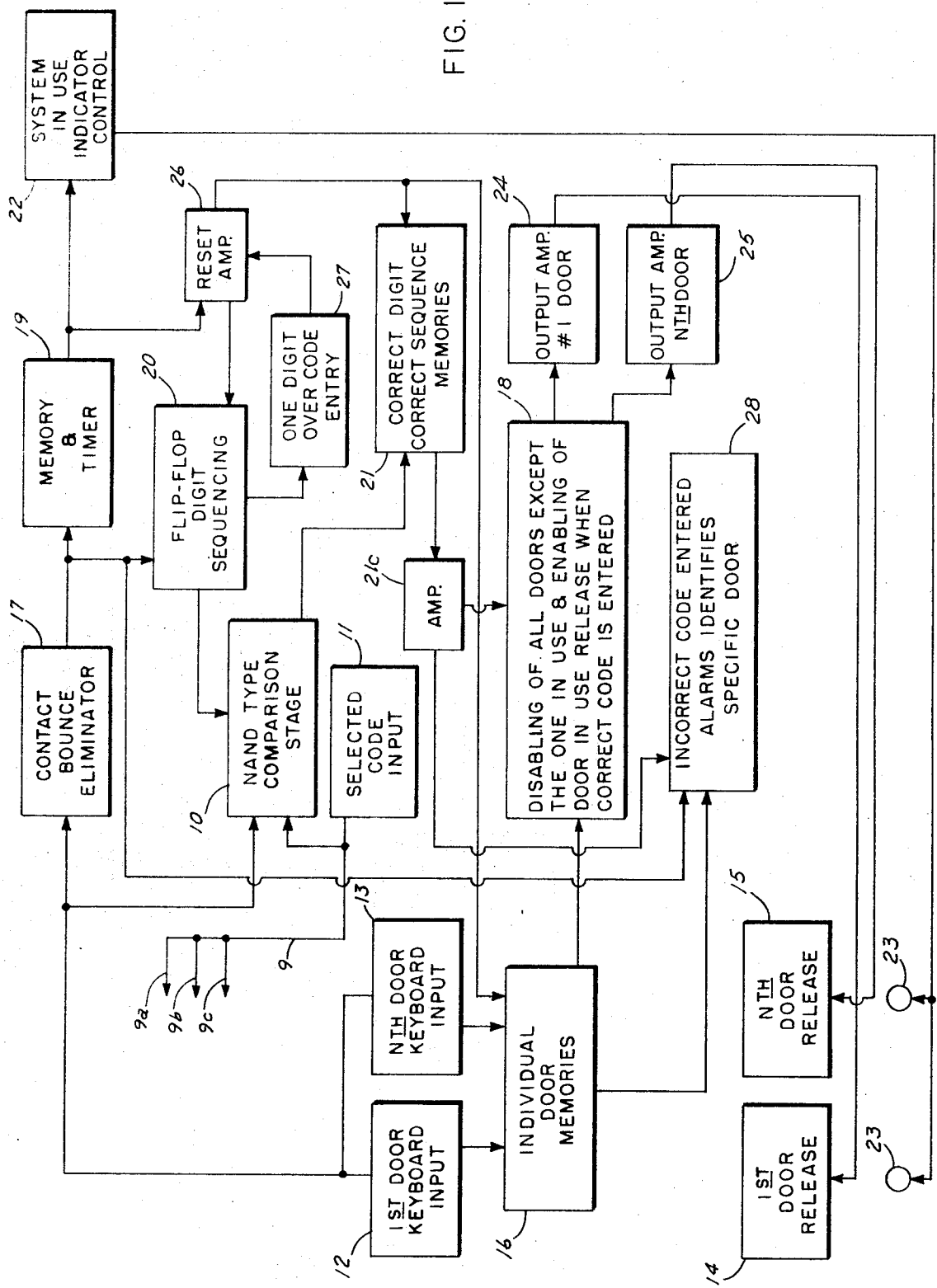
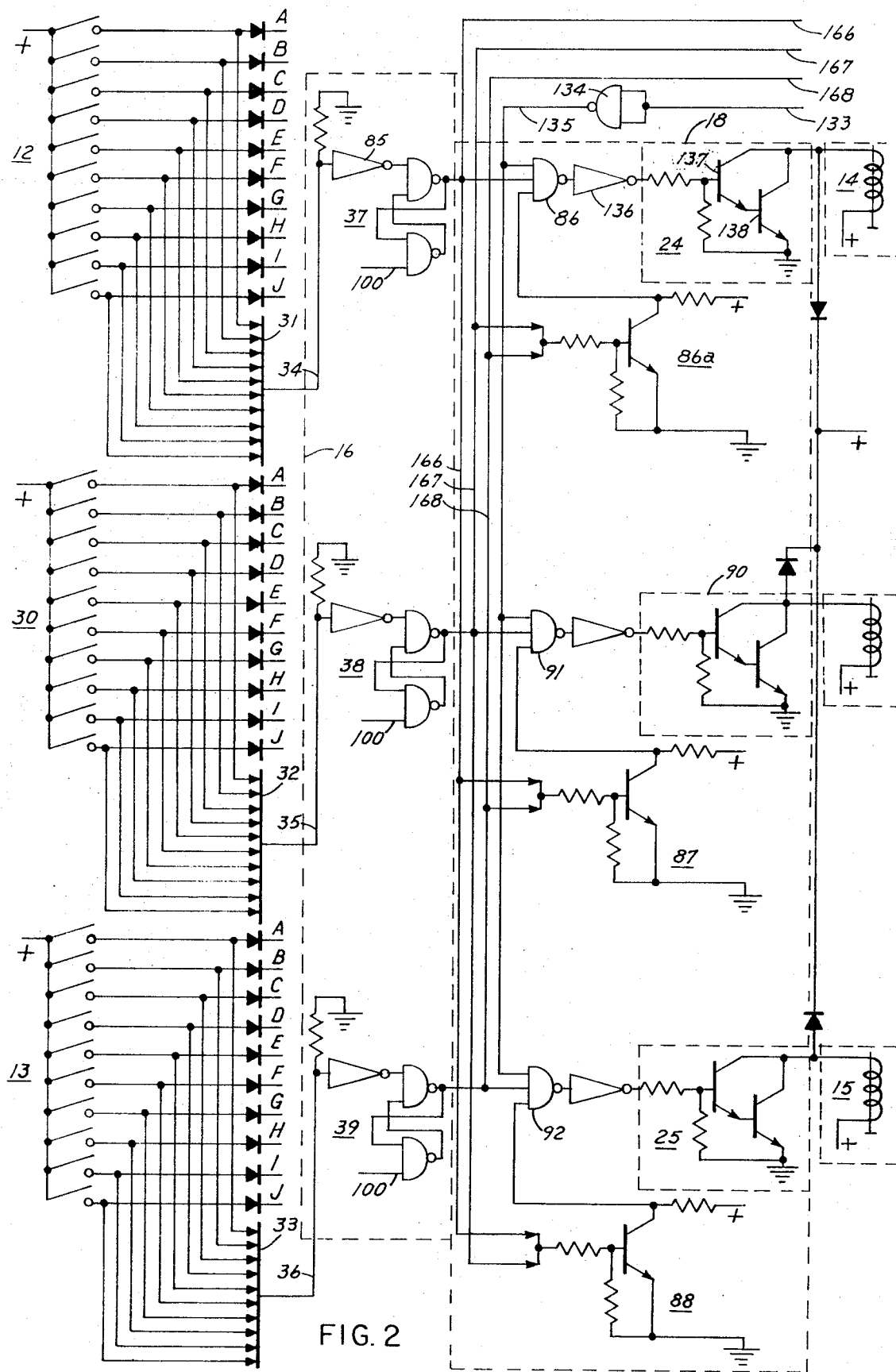
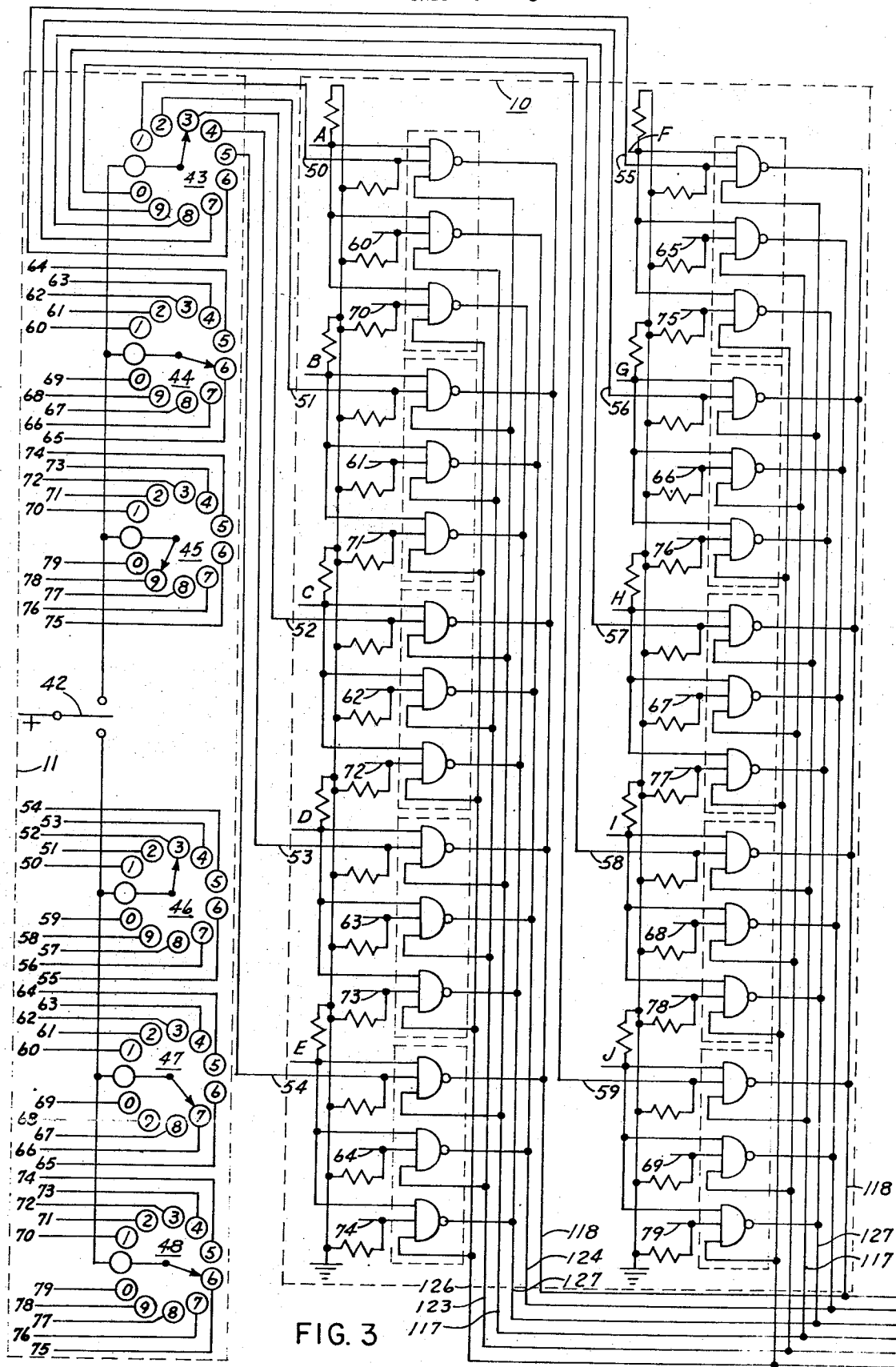
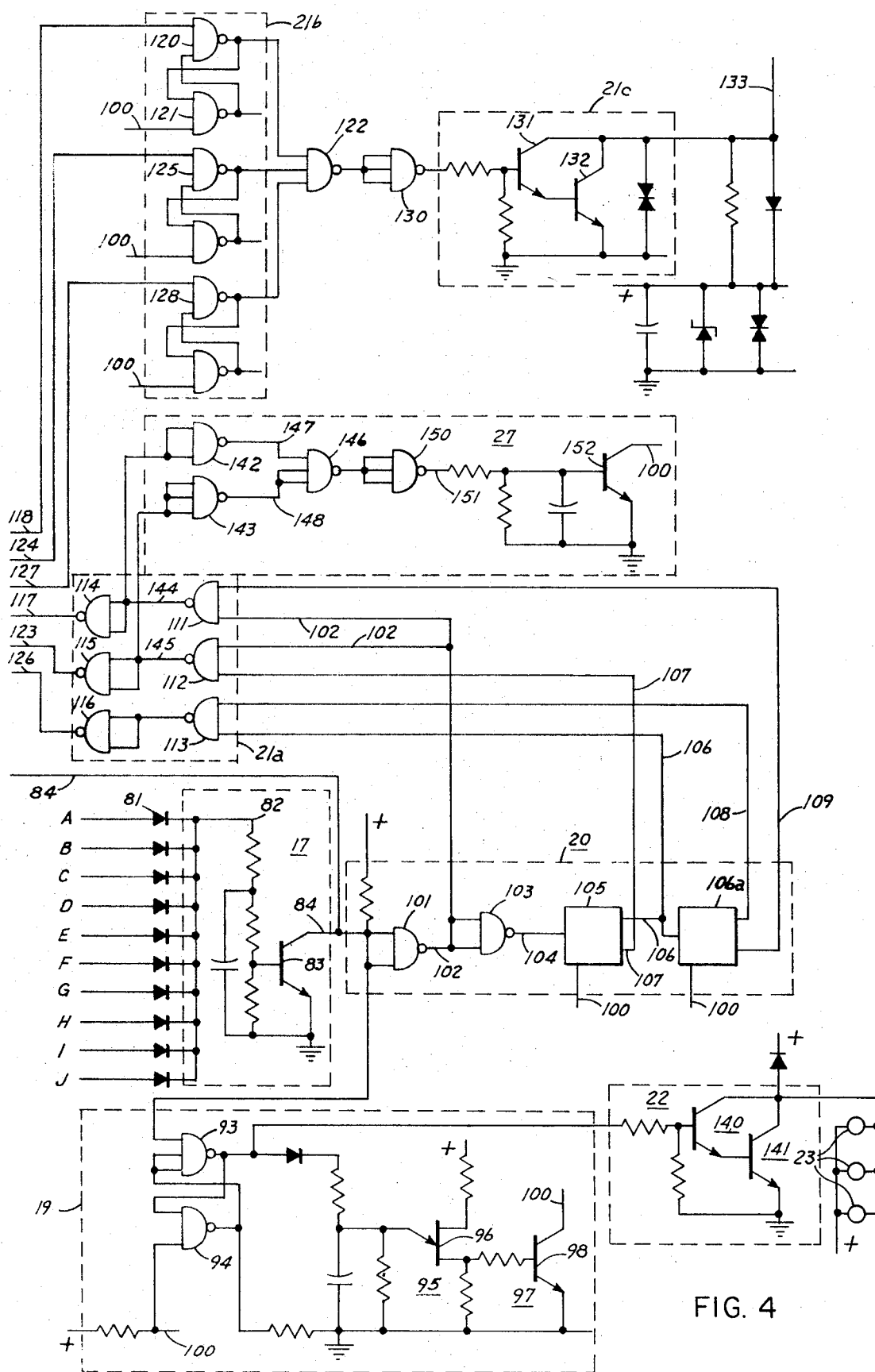


FIG. 1









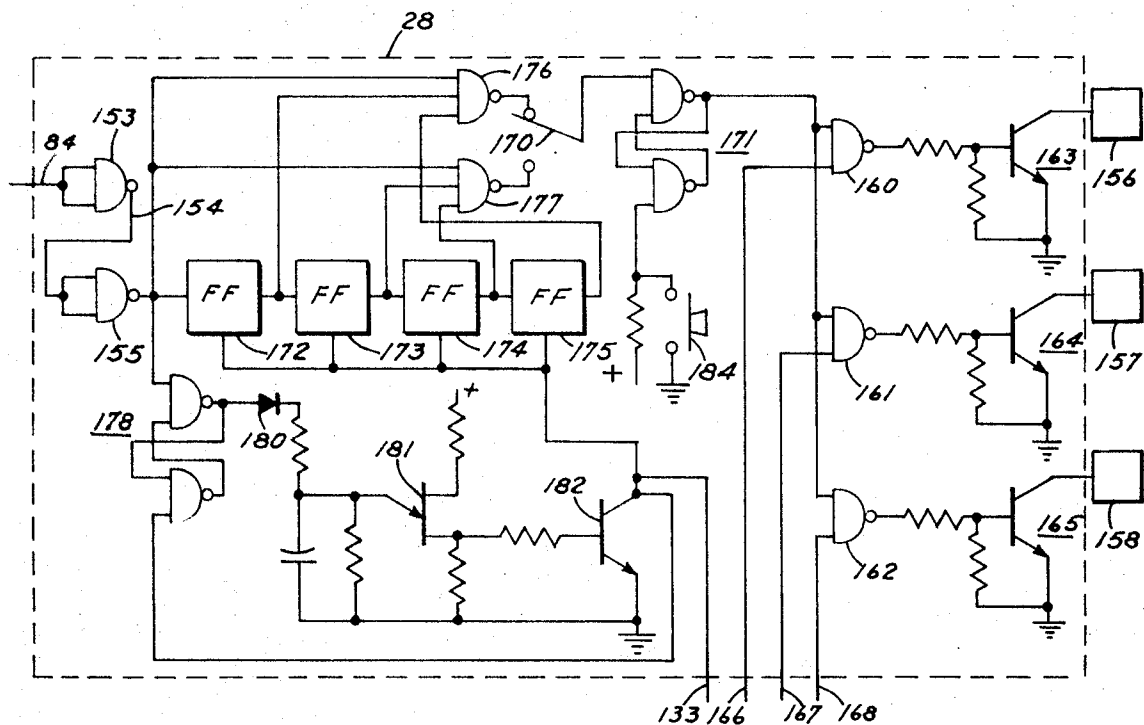


FIG. 5

TERM. OF LINE	RESET	1ST DOWN	1ST UP	2ND DOWN	2ND UP	3RD DOWN	3RD UP	4TH DOWN	4TH UP	5TH DOWN
84	1	0	1	0	1	0	1	0	1	0
102	0	1	0	1	0	1	0	1	0	1
104	1	0	1	0	1	0	1	0	1	0
106	0	1	1	0	0	1	1	0	0	1
107	1	0	0	1	1	0	0	1	1	0
108	0	0	0	1	1	1	1	0	0	0
109	1	1	1	0	0	0	0	1	1	1
117	0	1	0	0	0	0	0	1	0	1
123	0	0	0	1	0	0	0	1	0	0
126	0	0	0	0	0	1	1	0	0	0
144	1	0	1	1	1	1	1	0	1	0
145	1	1	1	0	1	1	1	0	1	1
147	0	1	0	0	0	0	0	1	0	1
148	0	0	0	1	0	0	0	1	0	0
151	0	0	0	0	0	0	0	1	0	0

FIG. 6

ELECTRONIC COMBINATION LOCK SYSTEM

This invention relates to combination locks of the electronic type and particularly to an improved electronic system whereby a plurality of code entry selectors may be provided one at each of a plurality of doors or other stations and wherein a single central unit controls the entire multiple lock system.

Various combination lock systems have been devised with a view to preventing unauthorized entry into buildings and other areas and these have included electronic systems for detecting the entry of a predetermined digital code and for releasing a door latch or other lock upon the entry of the correct code. The systems heretofore known have provided various features including the disabling or resetting of the system upon the entry of an incorrect code or upon failure to enter the correct code within a predetermined time. The systems provided heretofore, although satisfactory for many purposes, have not been entirely satisfactory for all applications or have involved complicated or costly systems. Further, it is desirable to provide a simplified system including a minimum number of components and also to provide a system suitable for monitoring a large number of locks such as those provided for the many entrance doors and internal doors of a large building. Accordingly, it is an object of the present invention to provide a combination lock system of the electronic type including an improved arrangement for assuring positive identification of the correct code when entered and immediate release of the lock.

It is another object of this invention to provide a combination lock system of the electronic type for controlling a plurality of locks including an improved arrangement for employing a single central station control for all locks.

It is another object of this invention to provide a combination lock system of the electronic type for controlling a plurality of locks including an improved arrangement for resetting of the system upon an incorrect code entry and for providing an alarm indication in the event that continuous incorrect entries are made within a predetermined number of entries.

It is a further object of this invention to provide a combination lock system of the electronic type including an improved arrangement whereby an alarm is provided to indicate a predetermined number of extended entries regardless of resetting of the system.

It is a further object of this invention to provide a combination lock system of the electronic type for effecting a release of any one of a plurality of locks upon entry of the correct code and wherein the entry of the code at any one of a plurality of lock stations disables all other stations.

It is a further object of this invention to provide a combination lock system of the electronic type including an improved arrangement whereby a single set of code determination switches can be used to set the door code on a number of independent central station controls.

It is a still further object of this invention to provide a combination lock system of the electronic type for controlling locks at a plurality of stations including an improved arrangement for assuring operation and release of a selected lock and preventing interference from other stations.

Briefly, in carrying out the objects of this invention in one embodiment thereof, a plural lock station con-

trol system is provided which includes separate code selectors, one at each station, and a single central comparator which is connected to compare the code input from a station with a selected code preset on multiple contact switches, one selector for each digit of the plural digit code and one contact in each selector for each selectable digit. A memory control activated upon selection of the first digit at any station is arranged to lock out all other door releases. A bank of correct digit enabling controls is provided to determine the sequence of comparison effected by the comparator and a correct entered digit memory control bank is provided, one memory for each digit of the code, and which upon triggering of all the memory controls of the bank initiates a signal to release the lock at the station from which the code entry has been made. Additional controls are provided one to reset the system in the event a predetermined time elapses after selection of the first digit of the code, another to provide a "system-in-use" indication at all station upon the selection of a digit at any station, and a third control to provide an alarm indication at the central control in the event that more than the predetermined digits are selected at any station regardless of the resetting of the system by the other controls.

The features of novelty which characterize this invention are pointed out with particularity in the claims annexed to and forming a part of this specification. The invention itself, however, both as to its organization and its manner of operation, together with further objects and advantages thereof, will best be understood upon reference to the following description taken in connection with the accompanying drawings in which:

FIG. 1 is a block diagram illustrating a combination lock system embodying the invention;

FIGS. 2, 3, 4 and 5 taken together constitute a schematic diagram of the system of FIG. 1; and

FIG. 6 is a table illustrating characteristics of the system during use.

Referring now to the drawings, the combination lock control system illustrated in FIG. 1 is arranged to control individual locks which, by way of example, may be located at a plurality of doors in a building. The system comprises a comparator 10 connected to a code selecting and setting input 11 which provides for the selection of the code entry necessary to effect the release of any of the locks and also may include a switchover control whereby, for example, one code may be employed during the daytime and another one at night. The code from the input 11 is compared with the code entered at any one of a plurality of doors or stations, indicated at 12 for the first door and at 13 for the Nth door, the total number of doors between the numerals 12 and 13 depending upon the number of locks to be controlled. The numerals 12 and 13 represent door stations and include door latches having electrical release mechanisms and a code selection input such as a plurality of push-button switches one for each digit from which the code is to be selected. Release latches are indicated at 14 for the door station 12 and at 15 for the door station 13.

When a digit is selected at one of the door stations, for example the first door station 12, triggering signals are supplied to an individual door memory unit 16 and to a switch contact bounce eliminator 17 and respectively thence to a disabling control 18 and to a memory 19 and to a digit sequencing control 20. The control 18

prevents release of all other doors and of the selected door until the correct code has been entered. If the digit entered in the comparator from the selected door is correct for the first digit of the code as determined by the sequencing control 20 the comparator transmits a correct digit signal to a memory 21 where this information is stored. When the first digit is entered at the memory 19 a "system-in-use" indicator control 22 is activated to energize "in use" indicators 23, one at each station, thereby informing persons wishing to enter at other doors that the system is being used and that they must wait before they can gain entry. When the second digit is entered, if it is correct, this information is also stored in the memory 21, and assuming a three-digit code is employed, then when the third correct digit is entered within the time determined by the timer 19 an output signal is supplied to an amplifier 21c and through the control 18; this signal is carried to a respective release signal amplifier, one for each door, these release amplifiers being indicated at 24 and 25 for the first and Nth doors, respectively. The output of each amplifier is supplied to the respective door release after entry of the correct code and the selected door lock is released.

If the code is not entered within the required time, the timer 19 energizes a reset amplifier 26 and restores the entire system to its starting condition.

In the event that an incorrect code is entered the system will be reset at the end of a time period determined by the timer 19; and should the incorrect entry comprise one more digit than the correct code, a control 27 will be triggered to actuate the reset amplifier 26 and reset the system before the expiration of the time set by the timer 19.

In the event that a predetermined excess number of digit entries are made regardless of the resetting of the system an alarm circuit 28 will operate to energize an alarm indicator at the central location indicating the alarm condition and the door at which the excess digit entries have been made. This advises a supervisor of the system that an unauthorized entry is possibly being attempted at the door.

From the foregoing it will be apparent that the system can be used at any time when the "system-in-use" indicators are not energized and that prompt entry of the correct code will result in releasing the lock at the selected door or station. All of the control equipment is located at the central station and only a single comparator is employed regardless of the number of stations at which the plural digit code may be entered. Thus a large number of locks may be controlled with single central apparatus and complication and duplication of equipment is avoided.

In large buildings having a great number of doors it may be found impractical to require persons at all doors to wait while the "system-in-use" lights are on. The present system makes it possible to employ the same code determining or selecting unit for a plurality of similar systems each having its own central control including its respective comparator. Thus, a large number of locks may be controlled by the same selected code and the total number of doors divided into selected groups each including one or more locks and each operated from an independent comparator system so that "system-in-use" lights will be energized only at the stations of the respective system or systems where code inputs have been initiated. When several central

control systems are installed in this manner, entry can be gained at a plurality of doors simultaneously provided each of the doors is connected to a different one of the central controls. At the same time the code selection is determined and controlled at a single location for all of the systems. By way of illustration, the provision of additional central systems has been indicated in FIG. 1 by a cable or lead 9 having a plurality of branched illustrated by way of example by three branches 9a, 9b and 9c. Each of these branches is connected to an independent NAND comparison stage like the stage 10. The same predetermined code may thus be set for a plurality of control systems without affecting the independent operation of each of the systems.

The schematic diagram comprising FIGS. 2 through 5 illustrates the solid state electronic components and their correct arrangements for a combination lock system for three doors or stations and employing a three-digit code. The components illustrated in the block diagram FIG. 1 have been indicated by dotted lines bearing the same numerals except that the correct digit sequencing control 21 of FIG. 1 has been indicated as comprising a digit enabling circuit 21a and a memory circuit 21b.

The code entry keyboard for the first door is indicated at 12, for the second door at 30, and for the third or Nth door at 13. Each of the keyboards, as shown in FIG. 2, includes ten switches each connected on one side to the high side of the power supply; these switches represent the digits 1 through 9 and 0, respectively, from top to bottom of each keyboard. Each of the keyboards is connected through diodes, one in each line leading from each switch to output terminal A, B, C, D, E, F, G, H, I, and J for the digits 1 through 9 and 0, respectively. The output terminals from the switches are also connected through respective diodes to common connections 31, 32 and 33, respectively. The connections 31, 32 and 33 are connected through lines 34, 35 and 36, respectively, to memory circuits or memories 37, 38 and 39, respectively. Each of the memories includes a pair of NAND elements, the output of each element being connected to one of the inputs of the other, and the other input of the first element being connected to the respective line 34, 35 or 36, and the other input of the other element being connected to the reset circuit of the system.

All signal levels are referenced to the low side of the power supply which serves as a common or zero potential connection. For convenience the common connection has been indicated by the ground symbol throughout the circuit.

The comparator 10 shown in FIG. 3 comprises 10 comparator elements, one for each digit and 0. Each comparator element is identical and comprises three input NAND elements or gates, one for each digit of the three-digit code. The top inputs of the three gates of each element are connected together and to a respective one of the output lines A through J of all of the keyboards 12, 30 and 13, as indicated by the corresponding letters applied to the terminals in the comparator 10. The code to be used is entered through the selected code input 11, illustrated as comprising two sets of three rotary switches each switch having ten switch positions, one for each of the digits 1 through 9 and 0. Only one set of three code switches is used at a time and a switch 42 is provided to select the set of switches to be used. One set may, for example, be for the day-

time code and the other for the nighttime code, the code being changed merely by moving the switch from one position to the other to connect the selected set of switches to the high side of the supply lines. The first set of switches comprises the switch 43 for the first digit of the code, switch 44 for the second digit of the code, and switch 45 for the third digit of the code. Similarly, the second set of switches comprises a switch 46 for the first digit of the code, a switch 47 for the second digit of the code, and a switch 48 for the third digit of the code. On each switch the digits have been indicated by circled numerals. In the switch as indicated, the set of switches on the top end of the code selector has been set for the code 3-6-9, and the set of switches on the bottom end has been set for the code 3-7-6. The contacts of the switches 43 and 46 are connected by lines 50 through 59 to respective center input terminals of the top NAND gate of the group of three NAND gates for each respective digit. In a similar manner, the contacts of switches 44 and 47 are connected to the center input terminal of the middle NAND gate of each set of three gates, these connections being indicated by the numerals 60 through 69, inclusive. The contacts of switches 45 and 48 for the third digit of the code are similarly connected to the center input terminal of the bottom NAND gate of each respective set of gates, these connections being indicated at 70 through 79, inclusive.

The closing of any switch in the keyboards 12, 30 and 13 connects the lines A to J inclusive, through a row of diodes 81, shown in FIG. 4, to a common input line 82 of the contact bounce eliminator 17. The eliminator comprises a resistance-capacitance circuit connected to the base of a transistor 83, the emitter of which is connected to the common circuit or ground and the collector to the input of the flip-flop digit sequencing control 20 and also through a line 84 to the input of the alarm circuit 28. Thus, each time an entry signal is supplied to any of the lines A through J, a low signal appears at the inputs of the circuits 20 and 28, the collector circuit of the transistor 83 returning to its high condition after termination of each high input pulse.

The switches of keyboards 12, 30 and 13 of FIG. 2 are biased to their open positions and may, for example, be pushbutton switches similar to those employed for telephone number selection. The keyboard switches are, however, required to be electrically or mechanically interlocked with each other in a manner insuring that only one switch can be closed at a time at any one station. When a switch in any of the keyboards is closed, the high signal appears on its respective line 34, 35 or 36. For example, if digit switch 3 is closed in keyboard 12 the high signal appears at the input of the memory circuit 37. The signal is inverted by an inverter 85 and the normally high input of the upper input terminal of the top NAND gate goes low; the other input already being high, the normally low output of the upper NAND gate becomes high and this high signal retained by the memory is impressed on the center input of a NAND gate 86 of the door disabling and release control 18. This high signal is also impressed on the input of transistors 87 and 88 of the release circuit 90 for the second door, and 25 for the third door. The collector circuits of the transistors 87 and 88 then go low, thereby changing from high to low the lowest input circuits of each of the NAND gates 91 and 92 and thereby preventing triggering of the release circuits for

the respective two door locks. Thus, the entry of a signal from the keyboard 12 prevents the activation of the lock releases of the other two doors. In a similar manner, each of the outputs of the memories 38 and 39 are impressed on a respective center terminal of the NAND gates 91 and 92, and at the same time on the transistor inputs for the other two door release controls. Thus, the control 18 disables all door releases except the one selected by the first digit input. If now a signal is entered at any other door keyboard the memory 38 or 39 for that door release will go high and the high signal be impressed on the transistor for the first door, indicated at 86a; this locks out the release for the first door and then no door release can be actuated. This condition is maintained until the system is reset.

When any one of the keyboard switches is closed a signal is entered on the respective one of the lines A through J of the input to the contact bounce eliminator 17, through the set of diodes 81, as indicated heretofore. This signal is also impressed on the line 84 as stated above and on the memory 19 and on the digit sequencing control 20. This triggers a memory comprising a pair of NAND elements 93 and 94 which in turn trigger a timing circuit 95 including a unijunction transistor 96 and an amplifier 97 including a transistor 98. A reset (low) signal is produced at the collector of the transistor 98 after a predetermined time period, the reset signal being entered on a reset line 100 which is connected to the reset terminals of the various functional components of the circuit, as indicated by the numeral 100 at the reset terminal of each of these components. Thus, if the correct code has not been entered at one of the doors or stations within the predetermined set time the entire system is reset.

The signal from the collector of the transistor 83 is also applied to the terminals of a NAND gate 101 of the digit sequencing control 20. This is a "low" signal and the output of the gate at 102 is high and is impressed on both terminals of a NAND gate 103 so that the normal high condition of its output goes low at 104. This low signal is applied to a flip-flop 105 having two outputs 106 and 107 which go high and low, respectively. The output 106 is impressed on a second flip-flop 106a and its two outputs 108 and 109 remain low and high, respectively. The outputs of the sequencing control 20, comprising lines 102, 106, 107, 108 and 109, are connected to input terminals of three NAND gates 111, 112 and 113 of a correct digit enabling unit 21a, the line 102 being connected to the lower input of the gate 111 and the upper input of the gate 112, line 106 to the lower input terminal of gate 113, and the line 107 to the lower input terminal of the gate 112; the lines 108 and 109 are connected to the upper input terminals of the gates 113 and 111, respectively.

For convenience, FIG. 6 has been provided which is a table indicating the high and low conditions of various points on the circuit, the digits 1 and 0 being used in accordance with common practice. The condition at reset is indicated in the first column, and thereafter the conditions depending upon whether high or low signals are impressed on the indicated components, these conditions changing depending upon the number of high and low signals impressed and the nature of the response of each circuit component when triggered.

When the first digit signal is entered on any one of the lines A to J, inclusive, after the system has been reset, the line 84 goes low, the terminal lines 102, 106

and 109 go high, while the lines 107 and 108 are low. Thus, the NAND element 111 is the only one of the three input gates 111, 112 and 113 at which the input signals are both high. The normally high output of the gate 111 therefore goes low, thereby making both the input terminals of a NAND gate 114 high. NAND gates 115 and 116 connected to the outputs of gates 112 and 113, respectively, remain low since the normally high outputs of the gates 112 and 113 remain high. The output of gate 114 is connected through a line 117 and a cross or branch of the line 117 to the lowermost input terminals of the uppermost NAND gates of each of the 10 comparator elements of the comparator 10. In the illustrated position of the code selector switch 43, the middle terminal of the NAND gate for the digit 3 is high since the line 52 is connected through the switch 43 to the high side of the line. If now the digit 3 is selected at any of the doors, the top input terminal of the uppermost gate of the third comparator element will be high, and thereby all three input terminals of this element will be high and the output of this gate will change from high to low, thereby placing a low signal on the common output line 118; the line 118 is connected to the upper of the two terminals of a NAND gate 120 of the uppermost of three memories, one for each digit, in the memory component 21b. NAND gate 120 is cross-connected with a second NAND gate 121 forming the top memory element of the component 21b. The output of gate 120 is normally low, and when the gate is triggered by a low signal the output becomes high and this high output is then maintained on a NAND element 122 at the output of the component 21b.

If in the example above any digit other than 3 is selected at the door there will be no change in the outputs of any of the top gates of the comparator unit 10.

If now the digit 6 is selected at station 12 the uppermost input terminals of the three gates of the comparator element for the sixth digit will be changed to high and when the input entry is made at the bounce eliminator 17 the output line 84 which has returned to high, as indicated in the third column of FIG. 6, will shift to low, the output line 102 to high, 104 and 106 to low, 107 and 108 to high, and 109 to low. Under this condition high inputs will be applied to the lower input of the gate 111 and the upper input of the gate 112, a low signal to the lower input terminal of the gate 113, high signals to the lower terminal of the gate 112 and the upper terminal of the gate 113, and a low signal to the upper terminal of the gate 111. Under these conditions, the center gate 112 of the digit enabling component 21a will be triggered and a low signal applied to the gate 115, thereby changing the output of the gate 115 to high and applying this signal to a line 123, thereby rendering high all the lowest input terminals of the center gates of the comparator elements. The correct digit having been selected, the output of the center gate of the sixth comparator element will change from high to low and this signal will be applied through a line 124 to the top NAND element 125 of the middle memory of the component 21b. The output of this memory will then change to high thereby holding the middle input of the gate 122 high.

By selecting 9 as the third digit at the keyboard 12, the high signal would be applied again to the line 82 of the bounce eliminator 17 and the terminal 84 will again change from high to low bringing up the conditions indicated in the sixth column of FIG. 6, line 102 then

being high, 104 low, 106 high, 107 low, 108 high, and 109 low. Under these conditions, lines 106 and 108 being high, the gate 113 will be triggered and its low signal applied to the gate 116, thereby changing the output from normally low to high, the high signal being applied through a line 126 to the lowermost input terminal of the bottom NAND element in each of the comparator elements. The lines 107 and 109 being low, the output of the gates 111 and 112 will be high and the normally low signal will be present at the outputs of both the NAND elements 114 and 115.

It is thus apparent that the circuit 21a provides sequential digit enabling for the first, second and third digits.

Since the comparator element for the digit 9 has been selected at the switch 45 all terminals of the bottom NAND element of the comparator element for the digit 9 will be high and the output will change from high to low upon the keyboard entry of the digit 9. This low signal will be applied through a line 127 to the top input terminal of a NAND gate 128 of the lowermost memory of the component 21b, thereby triggering this memory and applying a high signal to the bottom input terminal of the NAND element 122. All of the inputs of the element 122 now being high, the output shifts to low and all the terminals of a NAND element 130 are low and the output is high and is applied to the output, a transistor 131 having its emitter connected to the base of a transistor 132, the collector of which is connected to the collector of the transistor 131; a low signal is thereby applied to a line 133 and input terminals of a gate 134 change from high to low, thereby applying a high signal through a line 135 to the top terminals of the three gates 86, 91 and 92 of the disabling and release control component 18. The other two input terminals of the gate 86, also being high, the output of the gate is shifted to low and is applied to the base of the transistor 137 through an inverter 136. This signal is amplified through transistors 137 and 138 and applied to the door release 14 to release the latch of the first door or station.

Any signal other than the correct code as selected on the dial switch 43, 44 and 45 will fail to actuate the release at the station 12.

Because the release control circuits of all doors except the one in use are disabled when the first signal is applied to the memories 37, 38 and 39, the indicator signal is provided at each of the stations 12, 13 and 30 to apprise persons who might seek to unlock the doors of these stations that the system is in use so that any effort to enter the code during such use will not be effective. For this purpose, the system in use control 22 is connected to the output of the NAND element 93 so that it is triggered whenever a signal is received from the bounce eliminator 17. This signal is then amplified through transistors 140 and 141 and applied to indicators shown as signal lights 23, one of which is provided at each of the stations 12, 13 and 30. These signals are removed whenever the system is reset.

It is further desirable to reset the system in the event that an attempt is made to enter more than the number of digits in the code within the time determined by the timer 19. For this purpose the circuit control component 27 is provided. This control includes two input NAND elements 142 and 143, having their inputs connected to the output of the gate 111, indicated at 144, and the output of the gate 112, indicated at 145. The

outputs of the NAND elements 142 and 143 are connected to the inputs of a NAND element 146, the output of the element 142 indicated at 147 being connected to the upper input terminal, and the output of gate 143 indicated at 148 being connected to the middle and lowermost terminals. The sequence of signals at the terminals of lines 117, 123, 126, 144, 145, 147 and 148 are all indicated on the Chart FIG. 6. The combinations of these signals are such that the input terminals of the NAND element 146 are either or both low until the fourth down or low signal on the line 84 when both lines 147 and 148 are high, whereupon the output of the element 146 goes low and a NAND element 150 having all its input terminals connected to the output of the element 146 goes high at its output 151. This condition represents the entry of a fourth digit regardless of the station at which it is entered and the signal is amplified through a transistor 152 and applied to the reset circuit 100 of the reset system.

Thus, although the locks will be released upon insertion of the correct code, an incorrect entry will not release any lock and the entry of more than the correct number of digits in the preset time will produce a reset signal and reset the entire system.

It is desirable in the event that an attempt is made to break the code by inserting digits continuously at any of the stations, a signal will be provided to notify the operator at the central station that either there is mischief or an unauthorized attempt to gain entry at one of the stations. For this purpose, the alarm component 18 is provided which, as shown, includes a NAND element or gate 153 having both its terminals connected to the line 84. Thus, each time the line 84 changes from low to high a low signal appears at the output 154 of the gate 153 and the input terminals of a NAND gate 155 change alternately from low to high.

As shown in FIG. 5, the alarm system 28 is arranged to activate any one of the alarms or indicators 156, 157 and 158 for the doors or lock stations 12, 30 and 13, respectively. Each of the alarms is actuated by triggering of a respective gate 160, 161 and 162 which upon triggering energizes a respective amplifier 163, 164 and 165. The gates 160, 161 and 162 are prepared for triggering by connection to lines 166, 167 and 168 connected respectively to the outputs of individual door or station lock memories 37, 38 and 39. The gates 160, 161 or 162 are triggered by operation of a system for triggering the gates at either of two selected numbers of incorrect digit entries. The selection is made by operation of a manual switch 170 which in its upper position as shown will trigger a memory 171 when say nine digits have been entered incorrectly and the other of which will when the switch is in its lower position trigger the memory when say six digits have been entered incorrectly. The detection of the number of digits entered is effected by triggering of a series of four flip-flops 172, 173, 174 and 175. The flip-flops are triggered when the signal from the gate 155 changes from high to low. The outputs of the flip-flops 172 and 175 are connected to input terminals of a NAND gate 176 and the outputs of the flip-flops 173 and 174 are connected to two of the inputs of a NAND gate 177, these being the gates for the ninth and sixth incorrect digit entries, respectively. The flip-flop circuit is further controlled by a memory 178 connected through a diode 180 to a resistance-capacitance timing circuit employing a unijunction transistor 181 and an output transis-

tor 182, the collector of which is connected to all reset terminals of the flip-flops 172 through 175. The collector of transistor 182 is also connected to the line 133 so that it receives a low signal each time a correct code is entered at one of the lock stations. The entry of the correct code resets the flip-flops.

When any one of the alarm gates 160, 161 or 162 has been prepared for triggering by a signal from its respective one of the memory circuits 37, 38 and 39, and when the required number of incorrect signals are entered, the output of memory 171 will go high and the one of the gates 160, 161 or 162, which have been prepared for triggering, will be triggered thereby by producing an alarm at the respective station 156, 157 or 158.

The alarm system may be reset by closing a normally open manually operated switch 184 to reset the memory 171.

The control system as illustrated in the diagram, FIGS. 2, 3, 4 and 5, assures operation of a lock at one of the stations 12, 13 or 30 only in the event that a correct code is entered within a predetermined time interval. The expiration of the time interval or the insertion of an incorrect code or a code having an excess number of digits will reset the system. Furthermore, in the event that an attempt is being made to break the code at any station wherein a number of digits in excess of a predetermined number is entered, the alarm system providing a station identifying alarm at the central control point will be activated.

Two or more codes may be provided for use at selected hours, for example, this being done by providing a plurality of sets of selector switches such as 43, 44, 45 and 46, 47, 48, the particular one of the codes being selected by operation of the switch 42.

The use of the central control system is under control of the station at which the first digit is selected, all other stations being apprised that entry of the code should not be attempted at any such other station until termination of the "system-in-use" indication. If, while the "system-in-use" indicators are one, a digit is entered at a station other than the first entering station all releases including the first entering station release will be locked out. The correct code must be inserted within the predetermined period of time or the system will be reset.

When a plurality of independent central control systems are to be employed, the connections indicated by the numerals 9a, 9b and 9c in FIG. 1 are effected by connecting additional leads between the contact points of the switches 43 through 48 of FIG. 3 to the NAND gates of respective comparators like the comparator 10. Additional leads or connections for this purpose have not been illustrated in FIG. 3 in order to avoid further complication of the illustrated circuitry. The manner in which such connections are to be made will, however, be obvious from the connection shown in FIG. 3.

We claim:

1. A combination lock system of the electronic type for selectively releasing locks at a plurality of stations and utilizing a plural digit code said system comprising: an electrically releasable lock at each station, a digit selector switch assembly at each station, a code setting unit comprising a plurality of selector switches one for each digit of the code, a comparator,

means connecting said switch assemblies and said comparator,

means connecting said code selector switches and said comparator,

enabling means for preparing said comparator to compare the selected code digit and the digit selected at said switch assemblies in predetermined order,

a plurality of lock release signal generators,

a plurality of memory devices one associated with each of said lock release signal generators, each of said memory devices being connected with the respective one of said switch assemblies for triggering regardless of the digit selected,

means responsive to the first digit signal from said digit selector switch for preventing the actuation of all door release signal generators other than the first selected signal generator, and

means dependent upon the entry of the correct code for triggering the selected signal generator to release its respective lock.

2. A combination lock system of the electronic type for doors and the like and utilizing a plural digit code, said system comprising:

a digit comparator including a plurality of comparing units one for each digit,

a plurality of locks each at a respective lock station, digit selectors one at each station and each including a respective selector switch for each digit,

means connecting the switches at all of said lock stations to corresponding respective digit units of said comparator,

code selecting means one for each digit of a plural digit code for preparing selected ones of the units of said comparator for operation,

a plurality of pairs of memory means and lock release means one pair for each of said stations, said memory means being connected to be triggered by the operation of one of said switches at the respective station,

means for connecting all of the switches of each of said stations to a respective one of said memory means,

means for preventing the operation of the remaining ones of said memory means upon triggering of any one of said memory means,

enabling means associated with said comparator for preparing the selected units of said comparator in sequential order whereby only one of said comparator units may be triggered at one time,

means dependent upon the selection of a predetermined plurality of digits in a predetermined order for producing an output signal, and

means for applying said output signal to respective ones of said lock release means whereby the respective lock is released.

3. A combination lock system of the electronic type for doors and the like as set forth in claim 2 wherein each of said code selecting means includes a single pole multiple position switch, each position being connected to a respective one of said comparing units.

4. A combination lock system of the electronic type for doors and the like as set forth in claim 2, including timing means energized upon closing of any switch at any of said stations for resetting said system after a predetermined interval of time.

5. A combination lock system of the electronic type for doors and the like as set forth in claim 2, including alarm means including digit counting means for energizing an alarm upon the selection of a predetermined number of incorrect digits at one of said stations.

6. A combination lock system of the electronic type for doors and the like as set forth in claim 2, including means connected with said digit enabling means for resetting said system upon the selection of one digit more than the number of digits in the plural digit code.

7. A combination lock system of the electronic type for doors and the like as set forth in claim 5, including means connected with said digit enabling means for resetting said system upon the selection of one digit more than the number of digits in the plural digit code, said alarm means producing an alarm upon the selection of a predetermined plurality of incorrect digits within a predetermined time regardless of the resetting of said system.

8. A combination lock system of the electronic type for doors and the like as set forth in claim 2, including indicating means at each of said stations; means responsive to the actuation of any one of said digit selectors at any of said stations for actuating all of said indicators to indicate initiation of use of the system.

9. A combination lock system of the electronic type for doors and the like utilizing a plural digit code and comprising:

comparator circuit means including a separate circuit unit for each digit,

a plurality of digit selecting means one for each digit of a plural digit code and each including a plurality of digit selecting elements, each respective digit selecting element of each respective selecting means being connected to the corresponding one of said units of said comparator circuit means, each of said circuit units including a plurality of similar circuit components one for each digit of the code and connected to a respective one of said selecting elements,

a digit selector means associated with the lock to be controlled for entering a plural digit code in said comparator circuit,

a plurality of enabling means one for each digit of the plural digit code and each connected to said comparator circuit means for preparing the respective circuit component of each of said units of said comparator means for signal generation,

means responsive to successive correct signals from said code selecting means for preparing the respective ones of said enabling means in the order of the predetermined code sequence of digits to be selected, only one of said enabling means being prepared at any one time,

memory means including a plurality of memory units and dependent upon the input of a digit signal corresponding to the selected digit of said comparator means for activating a respective one of said memory units upon selection of each successive correct digit,

means responsive to the selection of the digits of the selected plural digit code in sequence for producing a release signal, and

means for applying the release signal produced by said last mentioned means for releasing said lock.

10. A combination lock system of the electronic type comprising:

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a plurality of lock stations each including an electrically releasable lock and a digit selecting device, a code selector comprising a respective digit selecting device one for each digit of a plural digit code, central comparator means connected to the digit selecting devices of all said stations and to said digit selecting devices of said code selector means for comparing the digits entered at any of said stations with the code entered on said code selector means, means responsive to the entry of a digit at any one of said stations for preventing the entry of digits from any other station from effecting release of any lock, and

means dependent upon the entry of a plurality of digits at any station which are the same and in the same sequence as the digits selected by said code selecting means for actuating the release of the lock at such station.

11. A combination lock system of the electronic type as set forth in claim 10 including timing means activated upon the entry of any digit at any of said stations for resetting said system in the event the correct code is not entered before the expiration of a predetermined period of time.

12. A combination lock system of the electronic type as set forth in claim 10 including means for resetting said system upon the entry of a number of digits in excess of the number in said code.

13. A combination lock system of the electronic type as set forth in claim 11 including means for resetting said system upon the entry before the expiration of said time period of more digits than the number of digits in said code.

14. A combination lock system of the electronic type as set forth in claim 10 including a plurality of indicator means one at each of said stations, and means dependent upon the selection of any digit at any of said stations for actuating all of said indicator means to indicate at all stations that the system is in use.

15. A combination lock system of the electronic type as set forth in claim 10 including means including a plurality of alarms one for each station and responsive to the entry of more than a predetermined excess number of digits at any one of said stations and regardless of the resetting of said system for actuating the respective one of said alarms.

16. A combination lock system of the electronic type as set forth in claim 13 including means including a plu-

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ality of alarms one for each station and responsive to the entry of more than a predetermined excess number of digits at any one of said stations and regardless of the resetting of said system for actuating the respective one of said alarms.

17. A combination lock system of the electronic type comprising:

a multiplicity of lock stations each including an electrically releasable lock and a digit selecting device, said lock stations being divided into a plurality of separate different groups each including one or more of said stations,

a respective independent central comparator and control means connected to the respective digit selecting devices of all stations of each of said groups, a code selector means comprising a plurality of digit selecting devices, one for each digit of a plural digit code,

means connecting said code selector means to all of said central comparator means whereby each of said comparator means compares the digits entered at any of its respective stations with the code determined by said code selector means,

means responsive to the entry of a digit at any one of said stations of each respective one of said groups for preventing the entry of digits from any other station in the same group from effecting release of any lock in said group, and

means dependent upon the entry of a plurality of digits at any station in a respective group which are the same and in the same sequence as the digits selected by said code selecting means for actuating the release of the lock at such station.

18. A combination lock system of the electronic type as set forth in claim 17 including a "system-in-use" indicator at each station of said groups having a plurality of stations, and wherein each of said independent central comparator and control means of such groups includes means for energizing said "system-in-use" indicators at all other stations of the respective group upon entry of an input signal at any one of the stations of such groups, whereby the entry of a signal at any station in a respective group provides a "system-in-use" indication for all other stations of such group without affecting the "system-in-use" control of any other group.

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