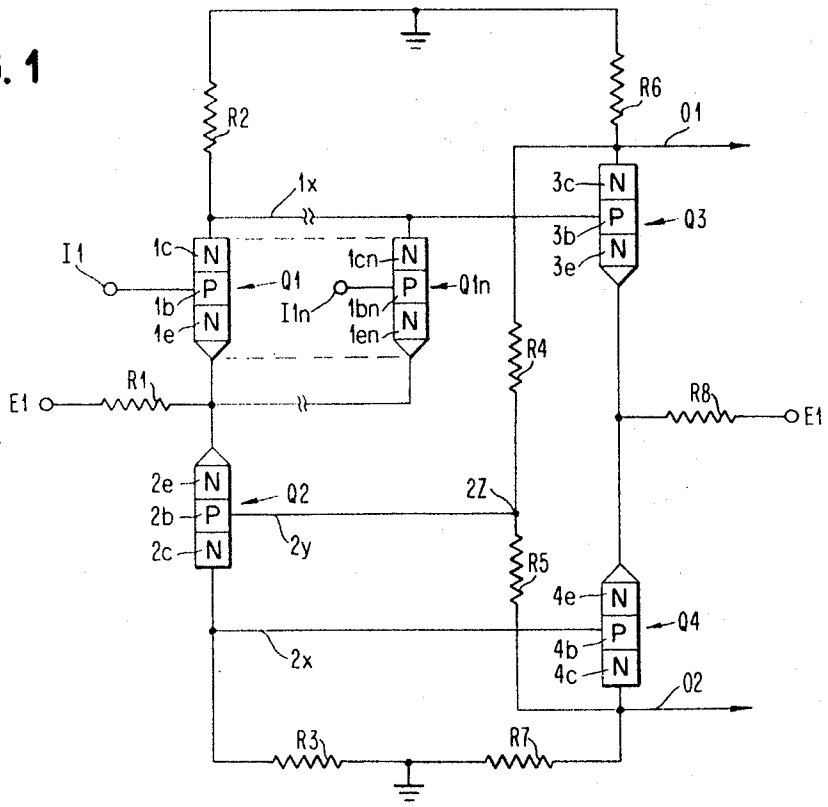
July 29, 1969 L. WEISS 3,458,719

THRESHOLD LOGIC SWITCH WITH A FEED-BACK CURRENT PATH

Filed Oct. 14, 1965 10 Sheets-Sheet 1

FIG. 1



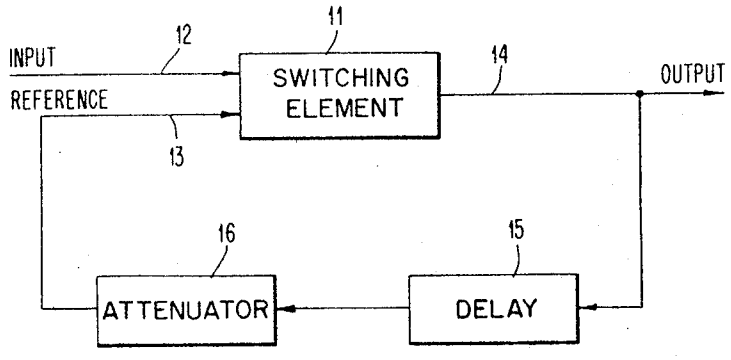




FIG. 2

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BY Martin G. Reiff
ATTORNEY

THRESHOLD LOGIC SWITCH WITH A FEED-BACK CURRENT PATH

Filed Oct. 14, 1965 10 Sheets-Sheet 2

FIG.3

PRIOR ART

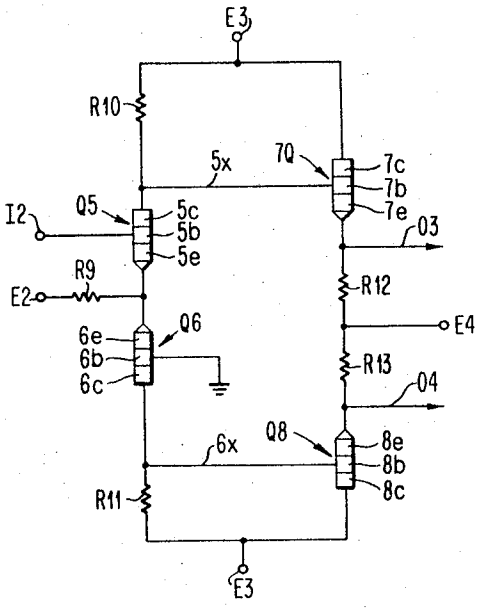



FIG.4

PRIOR ART MODIFIED

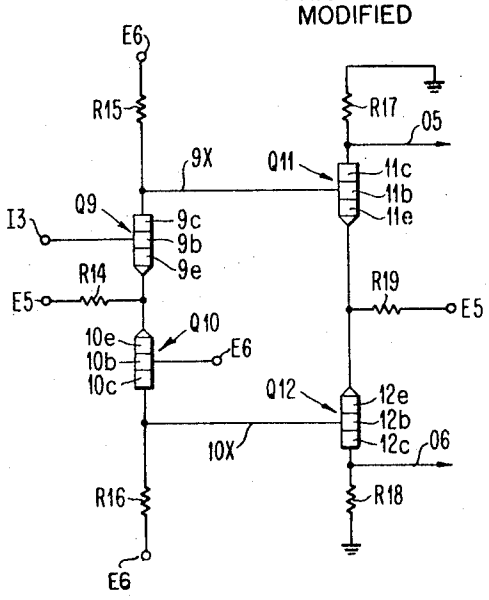



FIG.5

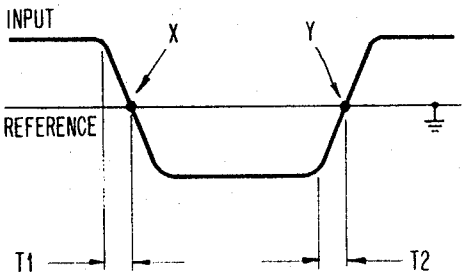
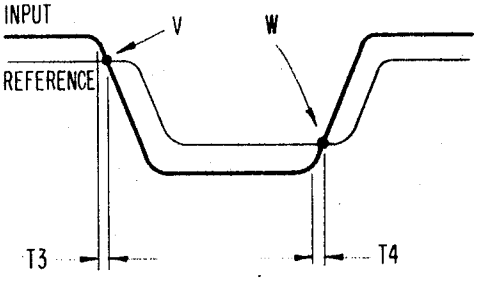



FIG.6



THRESHOLD LOGIC SWITCH WITH A FEED-BACK CURRENT PATH

Filed Oct. 14, 1965 10 Sheets-Sheet 3

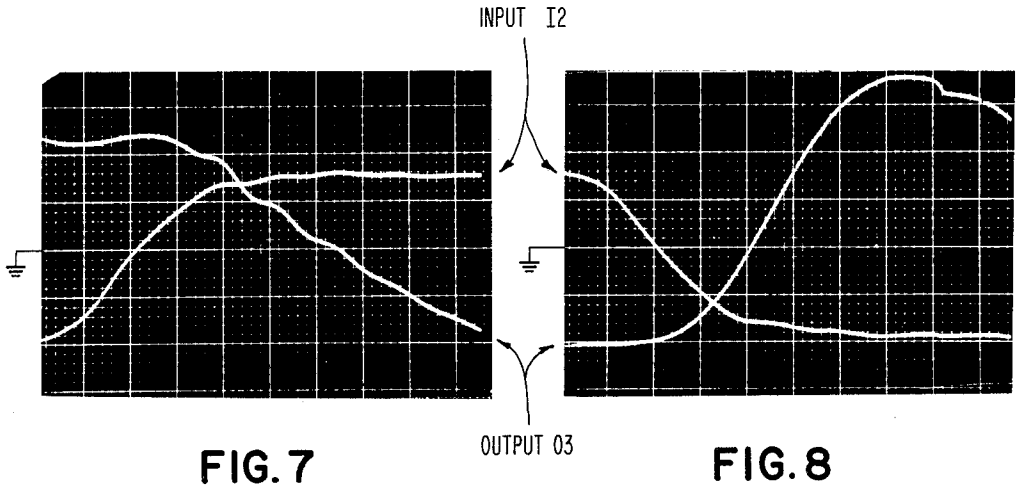



FIG. 7

FIG. 8

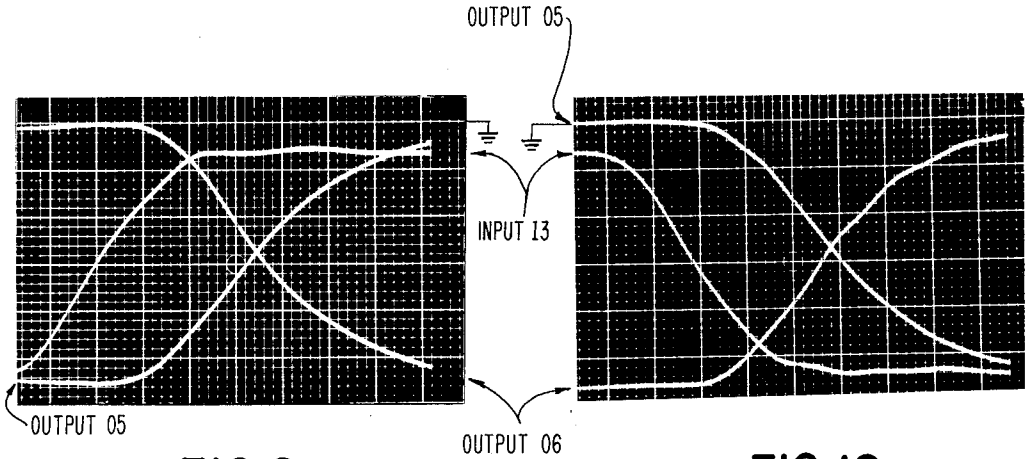



FIG. 9

FIG. 10

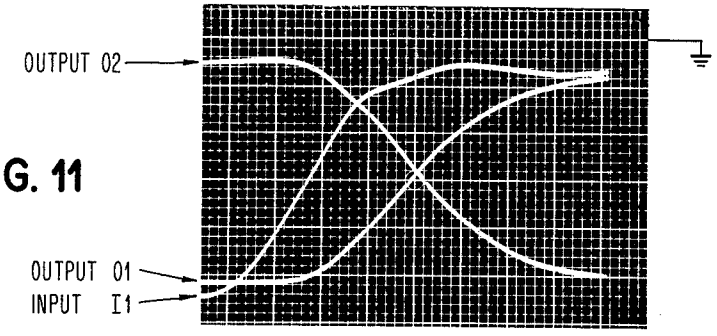



FIG. 11

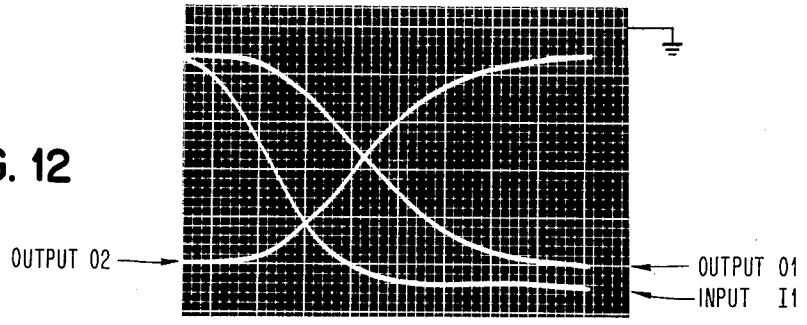



FIG. 12

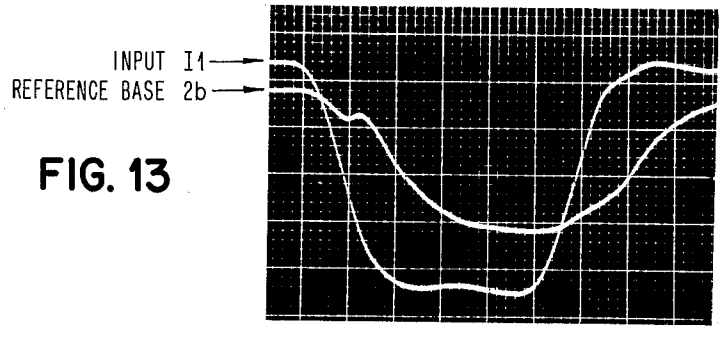



FIG. 13

THRESHOLD LOGIC SWITCH WITH A FEED-BACK CURRENT PATH

Filed Oct. 14, 1965 10 Sheets-Sheet 5

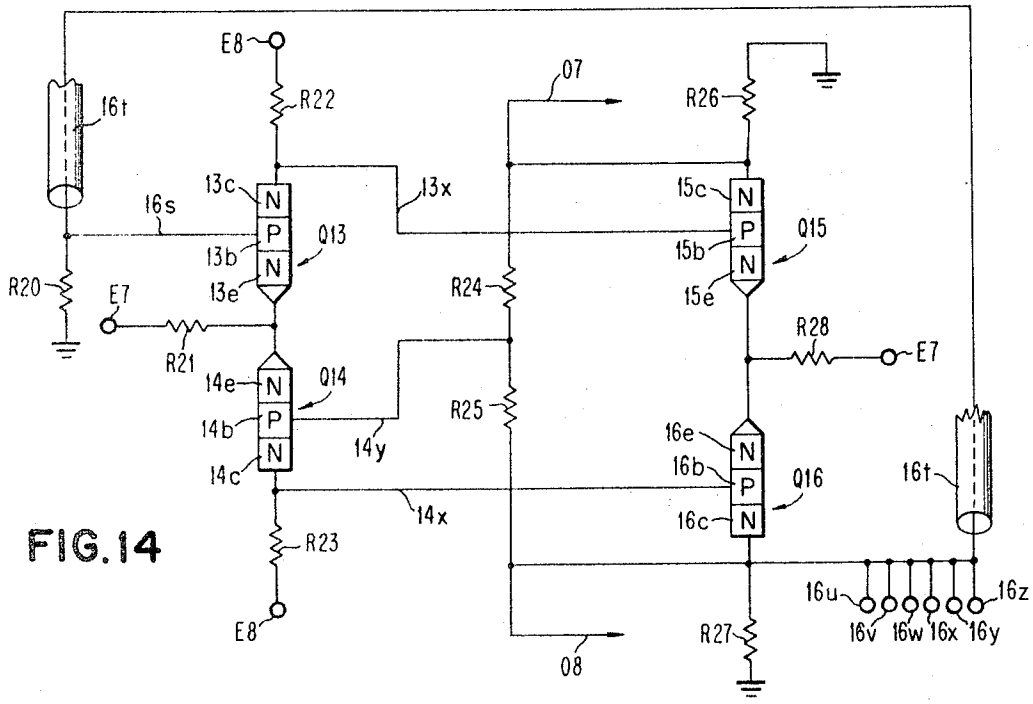



FIG. 14

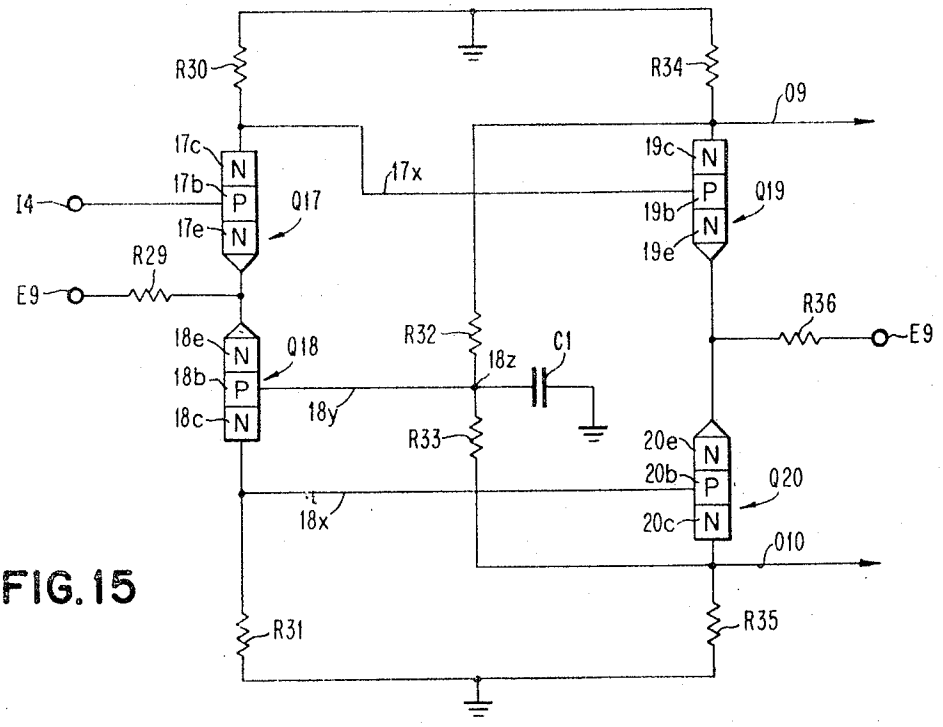
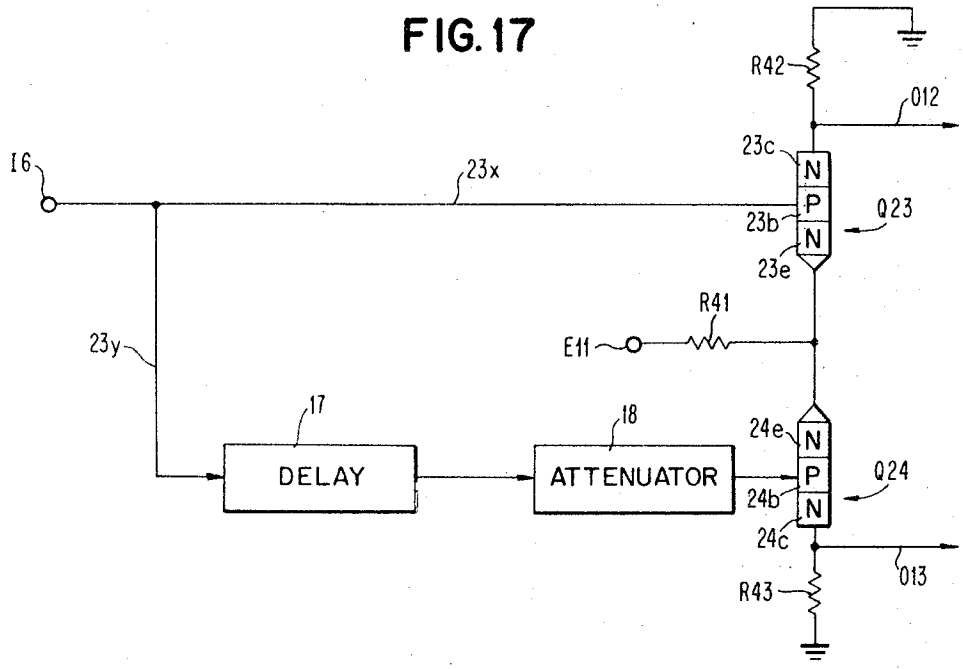



FIG. 15

FIG. 17


I6
23x
23y
R42
O12
23c
N
P
N
23b
23e
Q23
R41
E11
17
DELAY
18
ATTENUATOR
24e
24b
24c
Q24
O13
R43

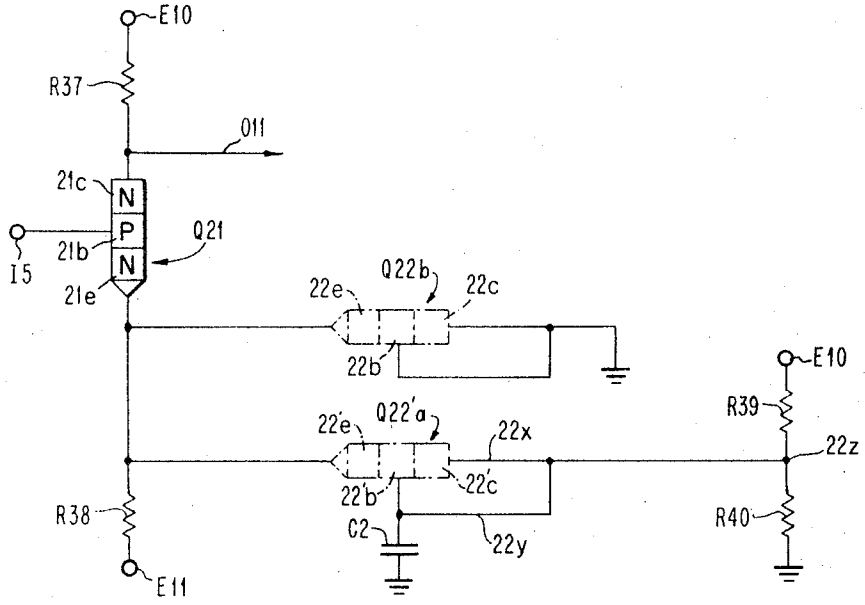

E10
R37
O11
21c
21b
21e
Q21
I5
22e
Q22b
22c
22b
E10
R39
22z
22'e
Q22'a
22x
22'b
22'c
C2
22y
R38
R40
E11

FIG. 16

THRESHOLD LOGIC SWITCH WITH A FEED-BACK CURRENT PATH

Filed Oct. 14, 1965 10 Sheets-Sheet 7

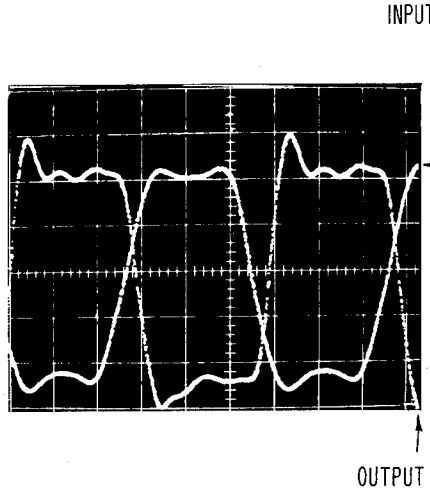



FIG. 18

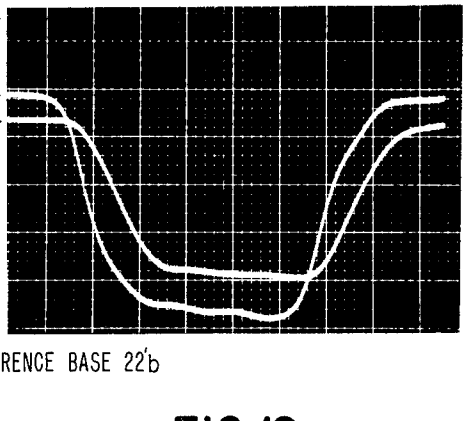



FIG. 19

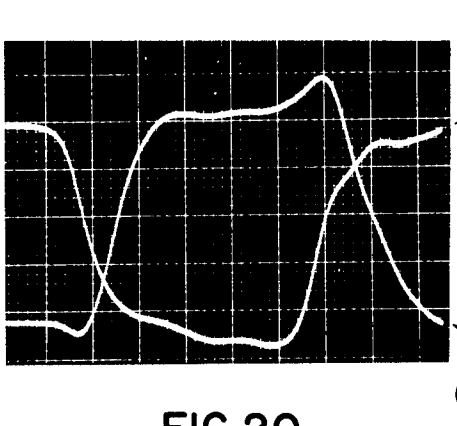



FIG. 20

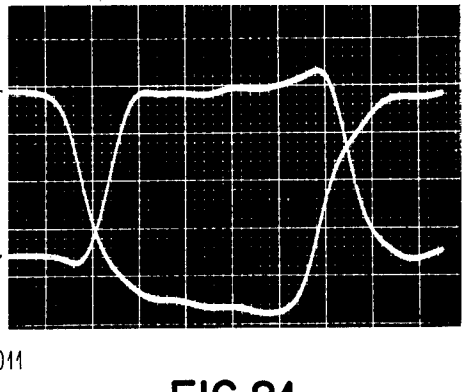


FIG. 21

THRESHOLD LOGIC SWITCH WITH A FEED-BACK CURRENT PATH

Filed Oct. 14, 1965 10 Sheets-Sheet 8

FIG. 22

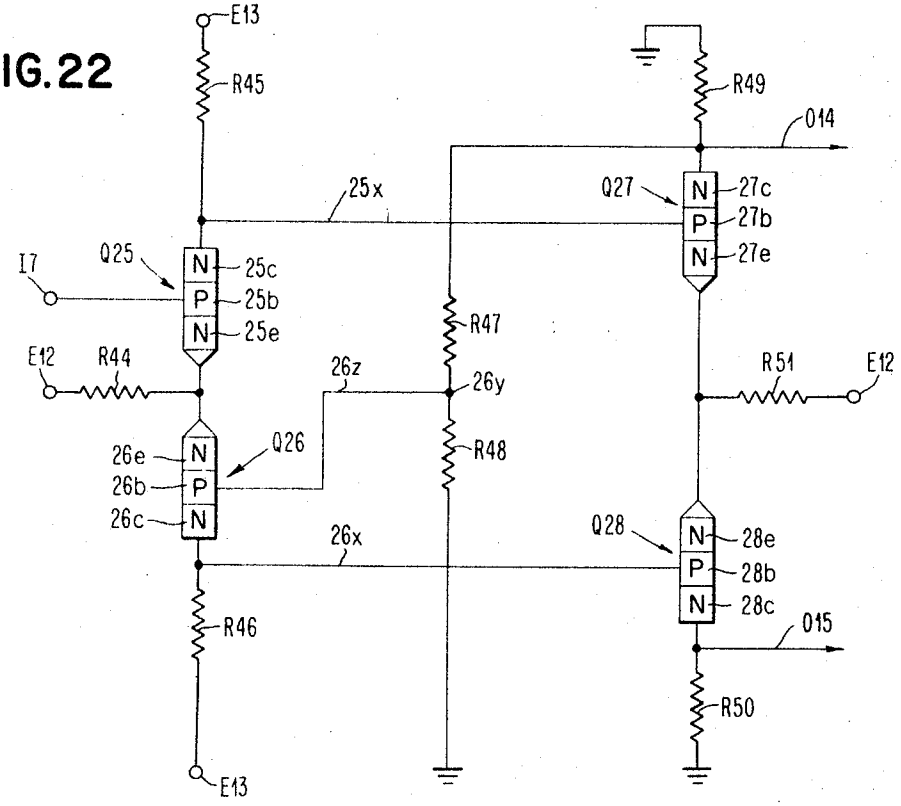
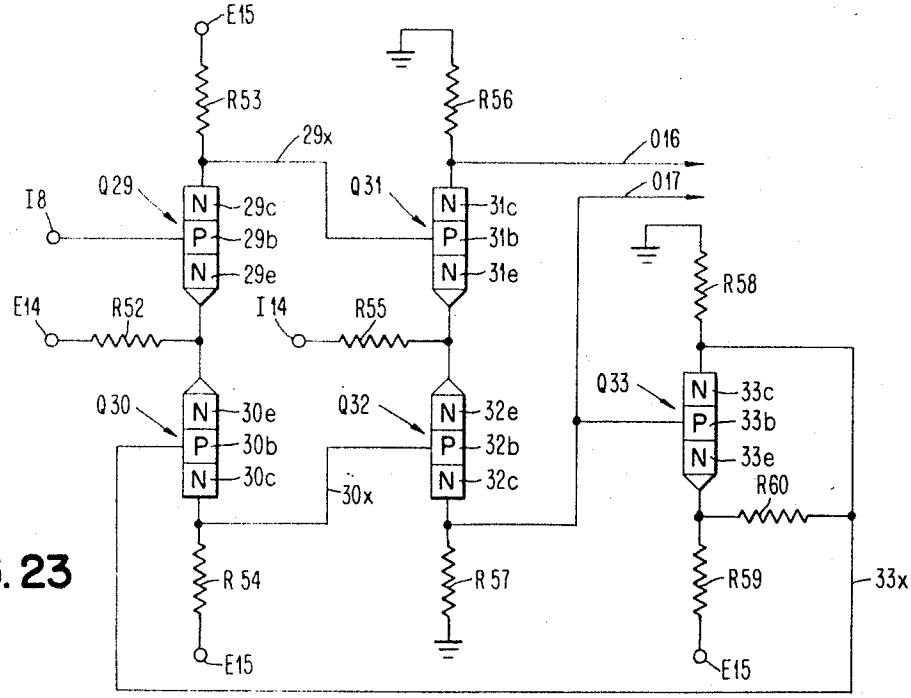



FIG. 23



THRESHOLD LOGIC SWITCH WITH A FEED-BACK CURRENT PATH

Filed Oct. 14, 1965 10 Sheets-Sheet 9

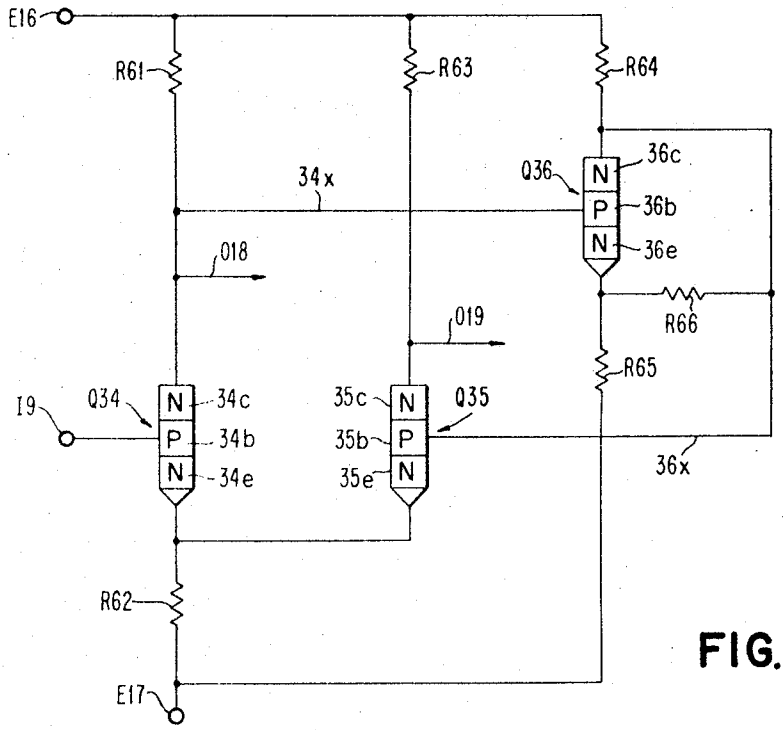



FIG. 24

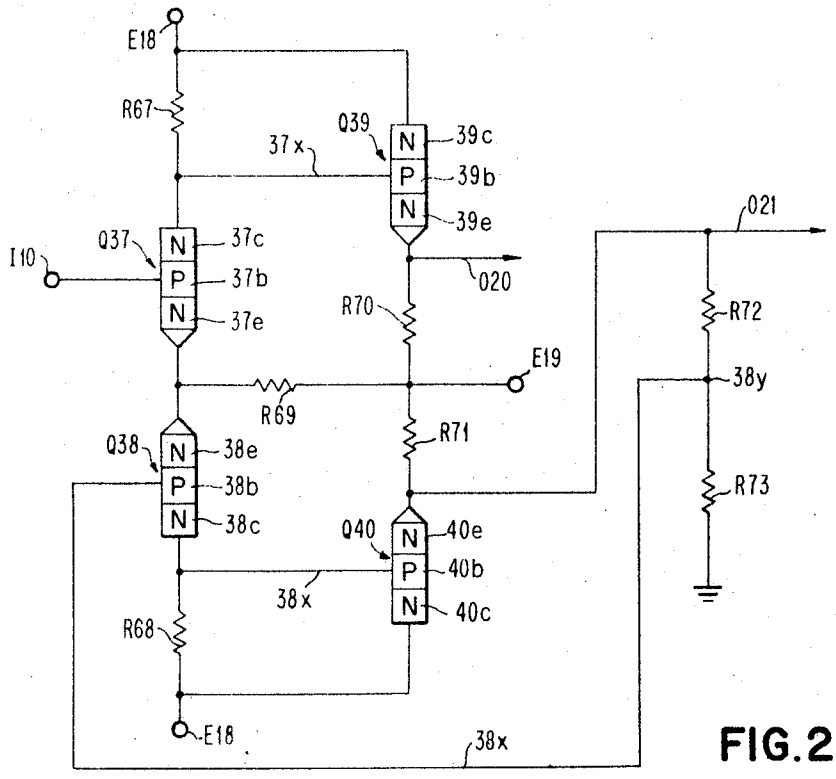



FIG. 25

THRESHOLD LOGIC SWITCH WITH A FEED-BACK CURRENT PATH

Filed Oct. 14, 1965 10 Sheets-Sheet 10

FIG.26

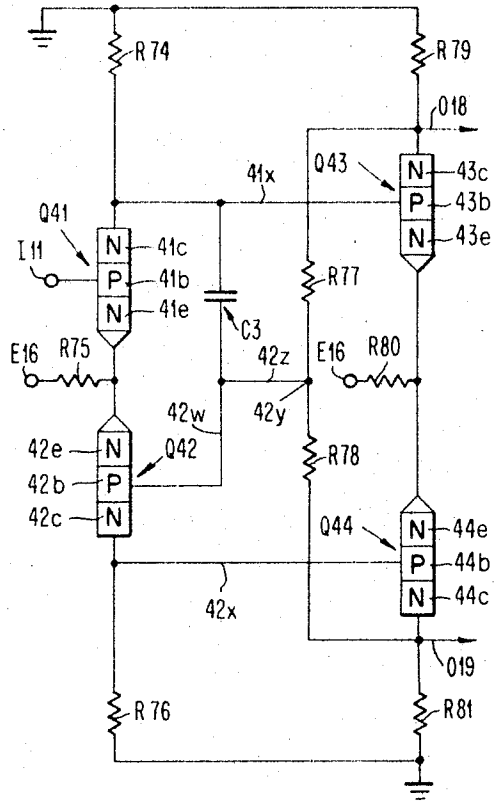
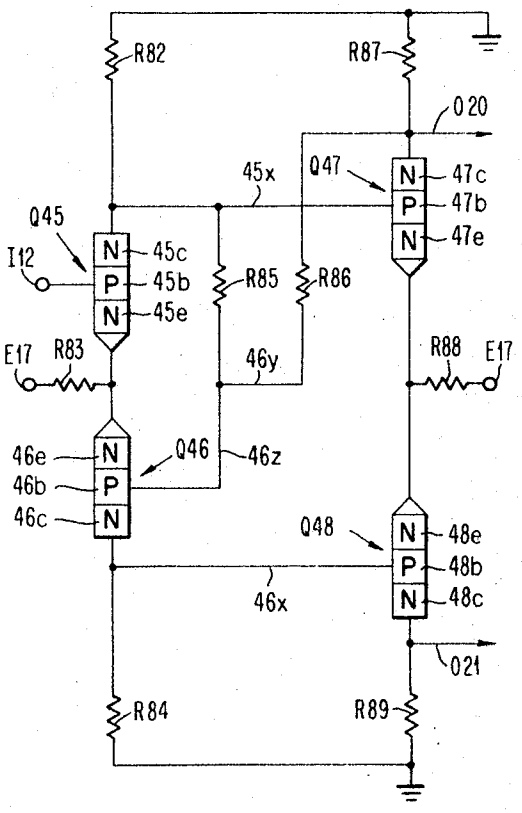



FIG.27



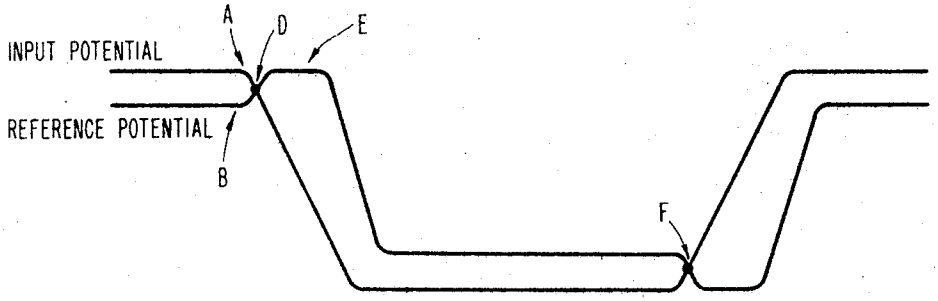




FIG.28

United States Patent Office 3,458,719
Patented July 29, 1969



3,458,719

# THRESHOLD LOGIC SWITCH WITH A FEEDBACK CURRENT PATH

Leonard Weiss, Poughkeepsie, N.Y., assignor to International Business Machines Corporation, Armonk, N.Y., a corporation of New York

Filed Oct. 14, 1965, Ser. No. 495,943
Int. Cl. H03k 19/08
U.S. Cl. 307—203 22 Claims

## ABSTRACT OF THE DISCLOSURE

An improved integrated circuit current switch having a time-dependent negative feed-back path for decreasing the switching time. The feed-back signal changes the level of the reference voltage applied to the current switch thereby decreasing the required level change in the potential of the input signal for the current switch to change its state.

This invention relates to switching circuits for performing logic functions in digital computers and for other applications where binary switches are required.

The overall performance capability of digital computers and other systems employing switching circuits is largely dependent upon the switching speed of the individual circuits, particularly in view of the enormous number of switching operations which must be performed in any given time period or for any particular computation or data process. Therefore, the art has devoted itself to the development of circuits having the highest possible switching speed.

The so-called "current switch" disclosed in United States Patent No. 2,964,652 to H. S. Yourke, issued Dec. 13, 1960 and assigned to the assignee of the present application, has come to be well known as significantly superior to other switching circuits with respect to both speed and stability.[1,2] Experimental comparison has shown the current switch to be about ten times as fast as its fastest rivals, the diode-logic and modified resistor-transistor-logic circuits.[3] The current switch is probably used more extensively than any other digital circuit.

Because of its importance and extensive use, since its initial publication [4] the current switch has been the subject of intensive studies by many workers in attempts to improve its speed and other characteristics. The usual approach has been based upon sound reasoning. Since the current switch changes from one state to the other when the input potential traverses the fixed reference potential, it was believed by those skilled in the art that the time for his traversal to occur could be reduced by employing positive feedback to vary a non-fixed reference potential in a direction opposite to that of the input potential swing during the switching operation, that is, toward the input poential until the traverse and away from the input potential thereafter. Because the two potentials would "meet" sooner as a result of the positive feedback, the circuit would switch faster, or so it was reasoned. Furthermore it was expected that the resulting increased overdrive fould further accelerate the switching speed.

All such known attempts failed, with the possible sole exception of a novel load-line displacing technique disclosed in copending application Ser. No. 495,826, entitled "Feedback Current Switch With Load-Line Displacing Network," filed of even date herewith by T.S. Jen and assigned to the assignee of the present application. The prior positive feedback arrangements resulted in a substantial loss in switching speed rather than the improvement to be expected. Nevertheless the reasoning behind the positive feedback concept was seemingly irrefutable and many of those skilled in the art still adhered to and pursued this approach at the time of the present invention.

See references in Column No. 16.



Others skilled in the art, in view of the many futile efforts to devise circuit modifications which would improve the speed of the current switch, became resigned to the belief that the conventional version of the current switch, is the ultimate form of this circuit in the sense that no substantial increase in speed is obtainable by modifying its circuitry and that only with the advent of new faster transistors or other active components would any significant speed improvement be possible.

The present invention has achieved a substantial increase in speed by an approach directly contrary to both the prevailing positive feedback and ultimate circuit philosophies:

It has been discovered that by applying negative feedback to urge the reference potential in the same direction as the input potential swing the switching speed of a current switch is so substantially improved that for the first time it is possible to obain a propagation delay of less than one nanosecond.

Although analysis would indicate that negative feedback should cause the input potential and reference potential to traverse or meet each other at a later time so as to retard the switching action, this adverse effect is obviated in the present invention by delaying the feedback until after the switching action is well under way. The feedback then becomes effective in the quiescent condition between switching to maintain the reference potential within a small predetermined incremental range about the input potential so that the circuit is effectively on the threshold of switching. Hence when the input potential changes in response to the next input signal, it quickly traverses the closely adjacent reference potential to provide a faster switching speed. The reference potential remains at its original quiescent level for a predetermined time after traversal by the input potential so as to provide a large overdrive which further improves the switching speed.

It is therefore a primary object of the present invention to provide in a switching circuit actuated by traversal of input and reference potentials a novel network for maintaining the quiescent value of the reference potential within a small predetermined incremental range about the input potential so that the two potentials will traverse each other quickly and thereby provide a substantially faster switching action.

A further object is to maintain the reference potential within said predetermined range by varying the reference potential in time-delayed phase with respect to the input potential.

Another object is to provide a preferred embodiment of the invention wherein said time-delayed in-phase variation of the reference potential is obtained by a novel negative feedback network extending from the in-phase output of the circuit to the reference node of the latter.

Still another object is closely related to the negative feedback aspect of the present invention. That is, circuits embodying the negative feedback are more economical in that they do not require tight component specifications and hence may utilize relatively less expensive transistors or other active devices, passive elements and power supplies. For a given set of component tolerances the negative feedback reduces the range of variation of the signal swing amplitudes at the outputs of the circuit.

A further object achieved by the negative feedback is to provide greater stability of the circuit at high frequencies. That is, any tendency to oscillation or transient ringing is substantially reduced.

Another object is to provide a novel current switch which requires only one power supply, as opposed to prior current switch circuits, which generally require at least two power supplies.

A further object, again achieved by virtue of the negative feedback, is to provide a switching circuit having greater stability with respect to quiescent direct current levels. Any tendency of a direct current level to vary due to an input level variation or to a component parameter deviation is counteracted by the negative feedback.

Another object is to provide a novel switching circuit wherein the switching speed is less adversely affected by heavy loads on the outputs. In the preferred embodiment of the invention this advantage is particularly evident when loading the in-phase output. This loading increases the time delay of the reference potential with respect to the input potential swing and thereby increases the overdrive. The increased overdrive improves the switching speed so as to counteract the retarding effect of the heavy load.

Still another object is to eliminate the reference base lead inductance that is inherent in the conventional current switch when embodied in the form of a monolithic integrated circuit. This elimination of base lead inductance further improves the high frequency stability.

Another object is to provide a current switch having a higher input impedance and lower input capacitance so as to result in less loading of the preceding circuit. This is achieved in the preferred embodiment of the present invention because the reference base is no longer grounded but is in effect connected to the relatively high impedance of the feedback network which impedance is reflected through both transistors to the input base so as to increase the impedance looking into the latter.

A further object is to provide a novel switching circuit wherein the rise time of the output is less dependent on the rise time of the input signal. If the rise time of the input signal is sufficiently slow it is even possible to provide a negative propagation delay. That is, the output signal will reach its midpoint before the input signal reaches its midpoint.

It will thus be seen that the present invention varies the reference potential in approximate phase with the input potential but slightly time-delayed with respect thereto. Although in the preferred embodiments of the invention this variation of the reference potential is achieved by a negative feedback network extending from the in-phase output, similar results can be achieved by deriving the reference potential in other ways. For example, the reference potential may be derived from the input with a delay line or other means to provide the required delay with respect to the input signal.

Although the subject invention is disclosed for purposes of illustration as embodied in a transistor current switch, it is readily embodied in any other form of switching circuit which is switched in response to the traversal of input and reference potentials, and irrespective of whether such other form of circuit utilizes transistors or any other type of active component.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention as illustrated in the accompanying drawings wherein:

FIG. 1 is a circuit diagram showing a preferred embodiment of the invention;

FIG. 2 is a schematic diagram of a switching circuit illustrating the basic principle of those embodiments of the invention which are of the feedback type;

FIG. 3 shows a conventional emitter follower current switch in accordance with the prior art;

FIG. 4 shows a modification of the prior art wherein in the emitter follower stage is replaced by a differential amplifier;

FIG. 5 is an idealized plot of the input and reference potentials during the switching operation of the current switch circuits of FIGS. 3 and 4;



FIG. 6 is an idealized plot of the input and reference potentials during the switching operation of the present invention as embodied in FIG. 1;

FIGS. 7 and 8 are oscilloscope photographs of the input and out-of-phase output potentials during respectively the turn-on and turn-off switching operations of the emitter follower current switch circuit of FIG. 3;

FIGS. 9 and 10 are oscilloscope photographs of the input and output potentials during respectively the turn-on and turn-off switching operations of the differential amplifier current switch circuit of FIG. 4;

FIGS. 11 and 12 are oscilloscope photographs showing the input and output potentials during respectively the turn-on and turn-off switching operations of the current switch in accordance with the present invention as shown in FIG. 1;

FIG. 13 shows the input and reference potentials of the current switch embodiment of FIG. 1 for both the turn-on and turn-off switching operations;

FIG. 14 is a circuit diagram showing the current switch embodiment of FIG. 1 arranged in a closed-loop test whereby the circuit drives itself;

FIG. 15 shows a modification of the current switch embodiment of FIG. 1 wherein a capacitor is added to the reference base to increase the delay of the reference potential;

FIG. 16 is a circuit diagram showing a comparison test of a single current switch stage both with and without a feedback network in accordance with the present invention;

FIG. 17 shows a modified form of the invention wherein the reference potential is derived from the input instead of the output;

FIG. 18 is an oscilloscope photograph showing the input and out-of-phase output potentials of the closed-loop test circuit shown in FIG. 14;

FIG. 19 is an oscilloscope photograph of the input and reference potentials of the comparison test circuit of FIG. 16 with the feedback network connected therein;

FIG. 20 is an oscilloscope photograph showing the input and output potentials of the comparison test circuit of FIG. 16 with the feedback network omitted;

FIG. 21 is an oscilloscope photograph similar to FIG. 20 but showing the input and output potentials of the comparison test circuit of FIG. 16 with the feedback network connected therein in accordance with the present invention;

FIG. 22 shows a modified form of the invention similar to FIG. 1 but having the lower end of the feedback network connected to ground instead of to the out-of-phase output;

FIG. 23 shows another modified form of the invention similar to FIG. 1 but having an active feedback network comprising an additional transistor to reset the magnitude of the reference potential and to provide additional delay in the feedback loop;

FIG. 24 shows still another modified form of the invention comprising a single current switch stage and an active feedback network similar to the network of FIG. 23;

FIG. 25 shows another modified form of the invention comprising an emitter follower second stage and a passive feedback network extending therefrom to provide the reference potential; and

FIGS. 26 to 28 show the circuitry and idealized input and output potential traces of two further modifications each having a positive feedback network in addition to the negative feedback network of the previous embodiments.

Referring now to the drawings in more detail, a better understanding of the subject invention may be had by first studying the mode of operation of a conventional emitter follower type of current switch as disclosed in

FIG. 3. In this figure transistors Q5, Q6 constitute the current switch stage and transistors Q7, Q8 constitute the emitter follower stage. The latter provides a relatively high load impedance for the current switch stage Q5, Q6 so as to prevent the latter from being excessivley loaded by succeeding circuits (not shown).

Input terminal 12 is connected to the base 5*b* of transistor Q5 having its collector 5*c* connected through collector load resistor R10 to a positive power supply E3. The emitter 5*e* of transistor Q5 and the emitter 6*e* of transistor Q6 are connected at a common node to a constant current source comprising a resistor R9 and a negative power supply E2. Resistor R9 is of sufficiently high impedance so as to pass a relatively constant current which is switched through either transistor Q5 or Q6 in a manner to be described. The base 6*b* of transistor Q6 is connected to a fixed reference potential which for purposes of illustration is shown in FIG. 3 as at ground level. The collector 6*c* of transistor Q6 is connected through collector load resistor R11 to the power supply E3.

The collector 5*c* of transistor Q5 is direct-coupled by lead 5*x* to the base 7*b* of transistor Q7, and the collector 6*c* of transistor Q6 is similarly direct-coupled by lead 6*x* to the base 8 of transistor Q8. The respective collectors 7*c*, 8*c* of transistors Q7, Q8 are directly connected to power supply E3. The emitters 7*e*, 8*e* of transistors Q7, Q8 are connected through respective resistors R12, R13 to a negative power supply E4. The two outputs O3, O4 of the circuit are taken from the emitters 7*e*, 8*e*.

Referring now to FIG. 5, the mode of operation of the prior art circuit of FIG. 3 will be described. The potential of the signal at the input 12 is designated by the label "INPUT" in FIG. 5, and the potential at the reference base 6*b* is shown at a constant ground level designated "REFERENCE." Assuming that the potential at the input 12 is initially at the "up" level, it will be seen that the base-to-emitter potential of transistor Q5 is greater than that of transistor Q6. Hence the current flows through transistor Q5 while transistor Q6 is either cut off or has substantially less current flow therethrough. The potential at the collector 5*c* of transistor Q5 is therefore at a "down" level where as the potential at the collector 6*c* of transistor Q6 is at a relatively "up" level. This difference of collector potential when applied to the respective bases 7*b*, 8*b* of transistors Q7, Q8 biases transistor Q7 to the "off" state and transistor Q8 to the "on" state. Hence initially the emitter 7*e* and output lead O3 are at a "down" level whereas the other emitter 8*e* and output lead O4 are at the "up" level.

Now let it be assumed that the input potential at input 12 swings downwardly as shown in FIG. 5. As long as the input potential at base 5*b* remains above the reference potential at base 6*b* the conditions of the quiescent state described above remain substantially unchanged. However, after the input potential traverses the reference potential at the point marked X the base-to-emitter voltage of transistor Q6 becomes greater than that of transistor Q5 since the emitters 5*e*, 6*e* of both transistors are tied together and are at the same potential. Assuming that these transistors have matching characteristics, the current formerly flowing through transistor Q5 then switches to flow through transistor Q6 instead.

It will thus be seen in FIG. 5 that there is a substantial time delay T1 from the instant when the input signal commences to swing downwardly until the input potential traverses the reference potential at the point X. The circuit cannot undergo the switching action until the after this time delay.

After the switching operation the initial polarities are reversed. Since transistor Q5 is now "off," its collector 5*c* as well as the emitter 7*e* of transistor Q7 and output lead O3 are at the "up" level, whereas transistor Q6 is "on" so that its collector 6*c* as well as the emitter 8*e* of transistor Q8 and output lead O4 are at a "down" level. This state will be maintained until the input potential at input terminal 12 moves upwardly to again traverse the reference potential as indicated at the point Y in FIG. 5 at which time the fixed current switches from transistor Q6 back to transistor Q5. It will thus be seen that the turn-on switching operation of transistor Q5 does not occur until after the time delay T2 from the instant when the input potential starts to rise to the instant when the input potential again traverses the reference potential at point Y.

The basic approach by which the subject invention achieves a faster switching speed is shown schematically in FIG. 6. The plot of the input signal potential in the latter figure is substantially identical to that in FIG. 5. However, it will be noted in FIG. 6 that the reference potential is now no longer fixed at ground level but instead varies in time-delayed phase with the input potential so as to remain within a predetermined incremental range about the latter.

More specifically, when the input potential is at its "up" level the reference potential is also at its "up" level which is below but closely adjacent to that of the input potential. When the latter swings downwardly, the reference potential is maintained at its "up" level for a time-delay period until after the input potential has traversed the reference potential at the point V. At this instant the circuit of the subject invention commences its switching action. Because of the relatively close proximity of the reference potential to the input potential at their respective "up" levels, it will be seen that the time period T3 for this traversal to occur is relatively small as compared with the time period T1 for the traversal to occur in the prior art circuit of FIG. 3 as shown in FIG. 5.

After the input potential attains its "down" level the reference potential will reach its "down" level which is higher than but closely adjacent to that of the input potential. Hence when the latter swings upwardly it quickly traverses the reference potential at the point W after a relatively small time period T4 which is substantially less than the time period T2 for the corresponding traversal to occur in the prior art circuit of FIG. 3 as shown in FIG. 5.

After the switching action the circuit of the present invention then assumes its initial quiescent state with the input potential at its "up" level and the reference potential also at its "up" level which is below but closely adjacent to the "up" level of the input potential. It will thus be seen that by maintaining the input and reference potentials at relatively close levels the time for the potential traversal to occur is substantially reduced thereby accelerating the commencement of the switch action, and substantially improving the switching speed of the circuit.

The preferred manner in which this may be achieved is shown in FIG. 1 which discloses one of the many embodiments which the invention may take in practice. In this figure the first stage comprising transistors Q1 to Q1*n* inclusive and Q2 constitutes a current switch. In order to provide the OR and NOR logic functions a plurality of transistors are connected in parallel with transistor Q1 as shown by only the single transistor Q1*n* for simplicity in illustration. Collectors 1*c*, 1*cn*, 2*c* of transistors Q1, Q1*n*, Q2 are connected through respective collector load resistors R2 and R3 to ground.

The emitters 1*e*, 1*en*, 2*e* of transistors Q1, Q1*n*, Q2 are connected at a common node to a constant current source comprising a resistor R1 and a negative power supply E1. The input terminals I1, I1*n* are connected to the respective bases 1*b*, 1*bn* of transistors Q1, Q1*n* whereas the base 2*b* of transistor Q2 has applied thereto the time-delayed in-phase reference potential described above with respect to FIG. 6 and derived from the output in a manner to be described below.

The second stage comprising transistors Q3, Q4 functions as a differential amplifier. Power supply E1 and resistor R8 constitute a source of constant current which

is switched to either transistor Q3 or transistor Q4 in response to the polarity of the difference between the signal at base 3*b* and that at base 4*b*.

The collectors 3*c*, 4*c* of transistors Q3, Q4 are connected to ground through respective collector load resistors R6, R7. The respective emitters 3*e*, 4*e* of transistors Q3, Q4 are connected at a common node to resistor R8. The base 3*b* of transistor Q3 is direct-coupled by lead 1*x* to the collector 1*c* of transistor Q1, and the base 4*b* of transistor Q4 is similarly direct-coupled by lead 2*x* to the collector 2*c* of transistor Q2.

This differential amplifier stage Q3, Q4 serves a similar function to that of the emitter follower stage Q7, Q8 of FIG. 3 in that it provides a high impedance load on the first stage to permit higher fan-out power of the circuit while maintaining unity gain. The stage Q3, Q4 has the further advantage of providing greater noise tolerance in that noise of a magnitude less than that required to reach the switching threshold will not be transmitted to the outputs O1, O2.

The varying time-delayed in-phase reference potential for application to the base 2*b* of transistor Q2 is derived in the following manner. A direct-current negative feedback network comprising a pair of resistors R4, R5 is provided. One end of resistor R4 is connected to collector 3*c* of transistor Q3 at the in-phase output O1 and one end of the other resistor R5 is connected to collector 4*c* of transistor Q4 at the out-of-phase output O2. The opposite ends of resistors R4, R5 are mutually connected at a common node 2*z* which is in turn direct-coupled by lead 2*y* to the reference base 2*b* of transistor Q2 so as to apply thereto the reference potential.

The magnitude of resistor R4 is substantially less than that of resistor R5 so that the reference potential swing is approximately in phase with the swing of output O1 which is, except for a time delay, in phase with the input signal at input terminal I1. The relative magnitudes of resistors R4, R5 are further selected so as to act as a voltage dividing attenuator to attenuate the amplitude of the reference potential swing at base 2*b* to a predetermined fraction of the amplitude of the output potential swing at ouput O1. Since the component parameters of the circuit are selected so that the circuit as a whole has unity gain, the amplitude swing at output O1 is substantially equal to that at input terminal I1 and hence the amplitude of the reference potential swing will be a predetermined fraction of the amplitude of the input potential swing. Therefore, as shown in FIG. 6, when the input potential is at its "up" level the reference potential will also be at its "up" level but below the input level. On the other hand, when the input potential is at its "down" level, the reference potential will also be at its "down" level but at a somewhat higher level than that of the input potential.

Proper operation of the circuit of FIG. 1 requires that there be a time delay of reference potential swing with respect to that of the input potential swing as shown in FIG. 6. That is, the reference potential should be maintained at its quiescent level until after the input potential has traversed the reference potential to commence the switching action. Furthermore, it is preferable that the reference potential remain at the quiescent level for a time period after the instant of traverse in order to provide a large overdrive which further improves the switching speed.

This time delay of the reference potential may be provided either in the forward transmission path as in the embodiment of FIG. 1, or in the feedback network as embodied in other modified forms of the invention to be described below. Furthermore, the time delay may be obtained as the inherent delay in the transistors or other active devices, or may be provided by a delay line or other component expressly designed for that purpose. Of course, the delay may also be provided by various combinations of these factors; that is, partially in the forward transmission path and partially in the feedback network, and/or partially in the inherent transistor structure and partially in a separate delay line. In the preferred embodiment of FIG. 1 the delay arises primarily in the forward transmission path from the input I1 to the outputs O1, O2 and is due to the delays caused by the junction capacitances and diffusion phenomena inherent in the structure of the several transistors.

Although the reference potential variation shown in FIG. 6 may be obtained by means other than direct-current negative feedback, as will be explained in connection with a modified form of the invention where the reference potential is derived from the input, the feedback approach is highly advantageous in that it automatically corrects any undesired variations due to component tolerances, input level deviations, temperature-induced variations, and power supply tolerances. For example, if the quiescent input potential level should change due to some variation in a preceding circuit, the negative feedback network will cause the quiescent reference potential level to change in the same direction and by almost the same amount so as to maintain substantially the same potential difference between the two levels. Hence the circuit will neither switch inadvertently due to an unintentional traverse of the two potentials, nor will its switching action be slowed down due to an excessive difference in the two levels. In a similar manner other variations will be corrected by the negative feedback so the circuit may be embodied in economical form with inexpensive components and power supplies while maintaining reliability of operation and high switching speed.

Referring to FIG. 2, there is shown schematically a switching circuit illustrating the basic inventive concept utilizing negative feedback to derive the reference potential. A switching element **11** is actuated to switch from one of its binary states to the other in response to traversal of the respective potentials at the signal input **12** and the reference input **13**. Extending from output **14** is a feedback network comprising a delay **15** and an attenuator **16** in series between output **14** and reference input **13**. Delay **15** may instead be embodied in the structure of switching element **11** or may be placed in the forward transmission path between switching element **11** and output **14**.

It will thus be seen that although for purposes of illustration the invention is disclosed in various specific current switch embodiments, the inventive concept is sufficiently broad to encompass any form of switching element which is actuated in response to the traversal of input and reference potentials.

The improvement in switching speed provided by the present invention over the prior art may be demonstrated by an experimental setup wherein four transistors are mounted on a module which is then plugged into either of two positions on a printed-circuit board so as to obtain either the conventional emitter follower type current switch in accordance with the prior art as shown in FIG. 3 or the circuit of FIG. 1 embodying the present invention, whereby both circuits may be tested and compared using the identical set of four transistors.

FIGS. 7 and 8 show the input and output traces obtained with the circuit of FIG. 3, and FIGS. 11 and 12 show the input and output traces obtained with the circuit of FIG. 1. In these photographs of oscilloscope traces, the horizontal scale is one nanosecond per centimeter and the vertical scale is 200 millivolts per centimeter. The ground reference is shown by the horizontal line identified by the ground symbol.

The generally employed figure of merit for switching speed is the propagation delay which is the time period from the instant of time when the input signal reaches its midpoint between its two quiescent levels and the instant of time when the output signal reaches its midpoint. It will be seen in FIG. 7 that in the prior art circuit the propagation delay during the rise of the input potential is about 4.2 nanoseconds whereas in FIG. 11 the propagation delay of the in-phase output O1 is 2.2 nanoseconds

and the out-of-phase output O2 has a propagation delay of 2.4 nanoseconds. In FIG. 8 during the fall of the input potential at **12** the propagation delay of output O3 is 2.0 nanoseconds for the prior art circuit whereas, as shown in FIG. 12, the propagation delay is 2.2 nanoseconds for the in-phase output O1 and 1.8 nanoseconds for the out-of-phase output O2 for the present invention of FIG. 1. FIG. 13 shows the traces of the input and reference potentials for the circuit of FIG. 1.

The component values utilized in the physical realization of the circuit of FIG. 1 which provided the oscilloscope traces of FIGS. 11 and 12 were as follows:

CIRCUIT OF FIG. 1

| | | |
|---|---|---|
| R1 | ohms | 340 |
| R2 | do | 32 |
| R3 | do | 36 |
| R4 | do | 50 |
| R5 | do | 340 |
| R6 | do | 42 |
| R7 | do | 42 |
| R8 | do | 150 |
| E1 | volts | 3.0 |

The component values utilized in the physical realization of the prior art circuit of FIG. 3 and which provided the oscilloscope traces of FIGS. 7 and 8 were as follows:

CIRCUIT OF FIG. 3

| | | |
|---|---|---|
| R9 | ohms | 320 |
| R10 | do | 120 |
| R11 | do | 18 |
| R12 | do | 500 |
| R13 | do | 500 |
| E2 | volts | 3.0 |
| E3 | do | 3.0 |
| E4 | do | 3.0 |

The differences in the component values of the physical realizations of the circuits of FIGS. 1 and 3 were required in order to obtain approximately equal signal levels with the two circuits. To demonstrate that the improvement in switching speed resulted from the present invention rather than from the difference in component values in the physical realizations of FIGS. 1 and 3 or because of the emitter follower of the latter as compared with the differential amplifier final stage of the former, another comparison test was made whereby the circuit of FIG. 4 was compared with that of FIG. 1.

FIG. 4 shows a modification of the prior art current switch of FIG. 3 in that the second stage constitutes a differential amplifier similar to the second stage of FIG. 1 rather than an emitter follower. More specifically, the first stage constitutes a current switch comprising transistors Q9, Q10 having their collectors **9***c*, **10***c* connected to power supply E6 through respective load resistors R15, R16. The emitters **9***e*, **10***e* of transistors Q9, Q10 are connected to a source of constant current comprising a resistor R14 and a power supply E5. The base **9***b* of transistor Q9 is direct-coupled to the input **13** and the base **10***b* of transistor Q10 is connected to a fixed reference potential which may be the same power supply E6.

The differential amplifier stage comprises a pair of transistors Q11, Q12 comprising collectors **11***c*, **12***c* connected to ground through the respective load resistors R17, R18; emitters **11***e*, **12***e* connected to a source of constant current comprising power supply E5 and resistor R19; and bases **11***b*, **12***b* direct-coupled by leads **9***x*, **10***x* to the respective collectors **9***c*, **10***c* of transistors Q9, Q10. The in-phase output O5 is taken from the collector **11***c* of transistor Q11 and the out-of-phase output O6 is taken from collector **12***c* of transistor Q12. It will thus be seen that the circuit of FIG. 4 is identical to that of FIG. 1 except that the reference base **10***b* is provided with a fixed reference potential by the power supply E6 instead of with the time-delayed in-phase reference potential provided at the base **2***b* by the feedback network in FIG. 1.

The input and output traces of the circuit of FIG. 4 are shown in the oscilloscope photographs of FIGS. 9 and 10. The horizontal scale is one nanosecond per centimeter and the vertical scale is 100 millivolts per centimeter. Referring first to FIG. 9, it will be seen that the propagation delay for the in-phase output during the rise of the input potential is about 3.2 nanoseconds and that for the out-of-phase output is about 3.6 nanoseconds. In FIG. 10 it will be seen that during the fall of the input potential the in-phase output has a propagation delay of 3.1 nanoseconds whereas that for the out-of-phase output is 2.7 nanoseconds. It will thus be seen that the present invention achieves a substantially faster switching speed solely by virtue of the time-delayed in-phase reference potential.

The component values for the physical realization of the circuit of FIG. 4 employed in the tests giving the oscilloscope traces shown in FIGS. 9 and 10 were as follows:

CIRCUIT OF FIG. 4

| | | |
|---|---|---|
| R14 | ohms | 340 |
| R15 | do | 32 |
| R16 | do | 36 |
| R17 | do | 42 |
| R18 | do | 42 |
| R19 | do | 130 |
| E5 | volts | 3.0 |
| E6 | mv | 300 |

It will be noted that in the tests providing the oscilloscope traces shown in FIGS. 7 to 12 inclusive the outputs of all output traces shown were loaded with approximately 50 picofarads to simulate a realistic load. The transistors employed in these tests were identical for all three circuits and were IBM Type S–101 having the following specifications:

IBM Type S–101 transistor

| | | |
|---|---|---|
| Transit time Te ($V_{bc}=O$, $I_e=20$ ma.) | ps | 150 |
| Junction capacitance, collector to base $C_{cb}(V_{bc}=O)$ | pf | 1.8 |
| Junction capacitance, collector to base $C_{cb}(V_{bc}=600$ mv.) | pf | 4.0 |
| Junction capacitance, emitter to base $C_{te}(V_{be}=o)$ | pf | 0.9 |
| Internal base resistance $\gamma_b(I_e=0.5$ ma.) | ohms | 90 |
| Internal collector resistance $\gamma_c$ | do | 120 |
| Avalanche breakdown voltage from collector to base with emitter open circuited $BV_{cbo}(I_c=1\mu a.)$ | volts | 25 |
| Avalanche breakdown voltage from emitted to base with collector open circuited $BV_{ebo}(I_e=1\mu a.)$ | do | 5 |
| Beta B ($I_e=15$ ma.) | | 30 |
| Base to collector voltage $V_{bc}(I_e=15$ ma., $I_c=14$ ma.) | mv | 700 |

The experimental tests described above were made with transistors of moderate speed. Substantially faster switching times may be achieved with the circuit of FIG. 1 by utilizing faster transitors. FIG. 14 shows such a circuit connected so as to perform the usual closed-loop test whereby the output is connected to the input so that the circuit drives itself.

Referring to FIG. 14 in more detail, transistors Q13 and Q14 constitute a current switch and are provided with collectors **13***c*, **14***c* connected to power supply E8 through respective load resistors R22, R23. The emitters **13***e*, **14***e* of transistors Q13, Q14 are connected at a common node to a constant current source comprising a power supply E7 and a resistor R21. Transistors Q15 and Q16 constitute the second current switch which performs the function of a differential amplifier. The collectors **15***c*, **16***c* are connected to ground through respective load resistors R26, R27. The bases **15***b*, **16***b* of transistors Q15, Q16 are direct-coupled to the respective collectors **13***c*,

14c of transistors Q13, Q14 through leads 13x, 14x. The emitters 15e, 16e of transistors Q15, Q16 are connected at a common node to a constant current source comprising a power supply E7 and resistor R28.

The in-phase output O7 at the collector 15c of transistor Q15 is unloaded. However, the out-of-phase output O8 at the collector 16c of transistor Q16 is provided with six connections 16u to 16z inclusive to the respective bases of six transistors (not shown) constituting an active load on the out-of-phase output O8. Also connected to the latter is a transmission line 16t having its other end terminated in a load R20 and connected by lead 16s to the base 13b of transistor Q13.

The circuit of FIG. 14 is further provided with the same feedback network described above with respect to the modification of FIG. 1 and comprising a resistor R24 extending from the collector of transistor Q15 and a resistor R25 extending from the collector of transistor Q16 and joined to a common node which is in turn connected by lead 14y to the base 14b of transistor Q14.

The potential traces at input 16s and output O8 of the closed-loop test of FIG. 14 are shown in FIG. 18. During the input potential rise the propagation delay was 0.5 nanosecond, and during the input potential fall the propagation delay was 0.9 nanosecond. It will thus be seen that by using relatively fast transistors the subject invention achieves a propagation delay in the subnanosecond range. The transistors employed for the close-loop test of FIG. 14 were IBM Type Y and had the following specifications:

IBM Type Y transistor

| | |
|---|---|
| Transit time TE ($V_{bc}=O$, $I_e=20$ ma.) ps | 70 |
| Junction capacitance, collector to base $C_{cb}$ ($V_{bc}=O$) pf | 0.7 |
| Junction capacitance, collector to base $C_{cb}$ ($V_{bc}=600$ mv.) pf | 2.6 |
| Junction capacitance, emitter to base $C_{ce}$ ($V_{bc}=O$) pf | 0.5 |
| Internal base resistance $\gamma_b$ ($I_e=0.5$ ma.) ohms | 25 |
| Internal collector resistance $\gamma_c$ do | 9 |
| Avalanche breakdown voltage from collector to base with emitter open circuited $BV_{cbo}$ ($I_c=1\mu a.$) volts | 12 |
| Avalanche breakdown voltage from emitter to base with collector open circuits $BV_{ebo}$ ($I_e=1\mu a.$) volts | 3 |
| Beta B ($I_e=15$ ma.) | 30 |
| Base to collector voltage $V_{bc}$ ($I_e=15$ ma., $I_c=14$ ma.) mv | 75 |

Referring now to FIG. 15, there is shown a modified form of the invention wherein, in addition to the delay inherent in the forward transmission path as provided by the transistors, the reference potential is further delayed by the addition of a capacitor in the feedback network. It will be seen in FIG. 6 that as the reference potential is maintained at its quiescent level after transversal by the input potential, the overdrive continually increases as the input potential continues to move in a direction away from the reference potential. The longer the reference potential is maintained at its quiescent level after the instant of traversal, the greater will be the overdrive. The latter in turn provides a faster switching action.

Referring to FIG. 15 in more detail, transistors Q17 and Q18 constitute the first stage current switch and are provided with collector load resistors R30, R31 extending from collectors 17c, 18c to ground. The emitters 17e, 18e of transistors Q17, Q18 are connected to a common node which is in turn connected through register R29 to a power supply E9 so as to provide a source of constant current. The input I4 of the circuit is connected to the base of transistor Q17.

The second stage operates as a differential amplifier and comprises transistors Q19, Q20 having respective collector load resistors R34, R35 connected from collectors 19c, 20c to ground. The emitters 19e, 20e of transistors Q19, Q20 are connected to one end of resistor R36 having its opposite end connected to power supply E9 so as to provide a source of constant current. The collector 17c of transistor Q17 is direct-coupled by lead 17x to the base 19b of transistor Q19 and the collector 18c of transistor Q18 is similarly direct-coupled by lead 18x to the base 20b of transistor Q20.

The feedback network comprises resistors R32, R33 each having an end connected respectively to the outputs O9, O10 and another end joined to a common node 18z and connected to lead 18y to the base 18b of transistor Q18.

As thus described, the circuit of FIG. 15 is identical to that of FIG. 1. However, in FIG. 15 an additional delay of the reference potential swing is provided by a capacitor C1 connected between the common node 18z of feedback resistors R32, R33 and ground. It will be seen that after the potentials at the oututs O9, O10 commence to swing, the potential at node 18z, instead of varying instantaneously therewith, will be delayed to the extent required by the charging or discharging of capacitor C1. Hence, the reference potential at the base of transistor Q18 tends to maintain its quiescent level after traversal by the input potential so as to provide a larger overdrive to improve the switching speed of the circuit.

Referring now to FIG. 16, there is shown a circuit diagram of a comparison test which demonstrates that the present invention does not depend for its improved switching speed upon the existence of the second differential amplifier stage as at Q3, Q4 in FIG. 1. By providing that one of the transistors may be manually inserted into either of two sockets, the circuit of FIG. 16 enables the identical transistor specimens to be arranged in either a conventional current switch having a fixed reference potential in accordance with the prior art, or as a current switch stage wherein the reference potential is derived by a negative feedback network in accordance with the present invention.

Referring to FIG. 16 in more detail, transistor Q21 has its collector 21c connected through load resistor R37 to a power supply E10. Its base 21b is connected to input I5 and its emitter 21e is connected to a constant current source comprising power supply E11 and resistor R38. The output O11 is taken at the collector 21c.

A second transistor is connected in the position shown in dash-dot lines at Q22 when inserted into one of the two sockets (not shown) and is in the position shown at Q22' when inserted into the other of the sockets. In both positions the emitter 22e of the second transistor is connected to the junction of emitter 21e of transistor Q21 and resistor R38. In the position at Q22 both the collector 22c and base 22b of the second transistor are grounded as shown, thereby providing a conventional current switch stage. However, when the second transistor is in the position at Q22', its collector 22c and base 22b are connected by leads 22x and 22y to the node 22z of a feedback network comprising resistors R39 and R40 connected in series between a power supply E10 and ground. A further delay in the reference potential swing is provided by a capacitor C2 extending from the base 22b of the second transistor to ground.

FIG. 20 shows the input and out-of-phase output traces for the conventional circuit with the second transistor at the position Q22. The propagation delays were 1.0 nanosecond and 0.8 nanosecond for rising and falling input potentials respectively. FIG. 21 shows propagation delays of 0.5 nanosecond and 0.6 nanosecond for rising and falling input potentials with the second transistor at the position Q22'. FIG. 19 shows the input and reference potential swings for the latter position.

The component valves employed in the physical realization of FIG. 16 which provided the results shown in FIGS. 19 to 21 inclusive were as follows:

CIRCUIT OF FIG. 16

| | |
|---|---|
| R37 | 58 ohms. |
| R38 | 270 ohms. |
| R39 | 66.5 ohms. |
| R40 | 604 ohms. |
| E10 | +250 mv. |
| E11 | —3.0 volts. |
| C2 | 5 picofarads. |
| Q21, Q22 | IBM Type "S–101." |

Referring now to FIG. 17, there is shown a modified form of the invention wherein the varying time-delayed in-phase reference potential is derived from the input rather than from the output as in the previously described modifications. A pair of transistors Q23 and Q24 are arranged as a current switch with their respective emitters 23*e*, 24*e* connected through resistor R41 to a power supply E11. The collectors 23*c*, 24*c* are connected to ground through respective load resistors R42, R43. Out-of-phase and in-phase outputs O12, O13 are taken from collectors 23*c*, 24*c* respectively. The input node 16 is connected by lead 23*x* to the base 23*b* of transistor Q23.

As thus far described the circuit is conventional. However, the reference potential at the base 24*b* of transistor Q24, instead of being at a fixed level as in the prior art, or being derived from the output as in the above described modifications of the present invention, is instead derived from the input 16 by a network comprising lead 23*y* extending from said input to a delay 17, the output of which is fed to an attenuator 18 which is in turn connected to said reference base 24*b*. It will be seen that attenuator 18 will maintain the reference potential swing at base 24*b* at a predetermined proportion of the input potential swing. Furthermore, delay 17, which may be realized as a delay line or by other suitable means, will maintain the reference potential at its quiescent level until after traversal by the input potential. The circuit of FIG. 17 will thus provide the input and reference potential traces shown in idealized form in FIG. 6 so as to operate in a manner somewhat similar to that of the previously described modifications employing feedback from the output.

Referring now to FIG. 22, there is shown a modified form of the invention wherein the feedback for the reference potential is derived from only the in-phase output rather than from both outputs as in the modification of FIG. 1. Transistors $Q^{25}$, $Q^{26}$ constitute a current switch having their respective collectors 25*c*, 26*c* connected by load resistors R45, R46 to a power supply E13. The emitters 25*e*, 26*e* are connected to a constant current source comprising power supply E12 and resistor R44. The base 25*b* of transistor Q25 is connected to the input node I7.

Transistors Q27, Q28 constitute a differential amplifier. The collectors 27*c*, 28*c* of transistors Q27, Q28 are connected through load resistors R49, R50 to ground. The bases 27*b*, 28*b* of transistors Q27, Q28 are connected by respective leads 25*x*, 26*x* to the collector 25*c*, 26*c* of transistors Q25, Q26. The in-phase output O14 is taken from the collector 27*c* of transistor Q27 and the out-of-phase output O15 is taken from the collector 28*c* of transistor Q28. The emitters 27*e*, 28*e* of transistors Q27, Q28 are connected to a constant current supply comprising resistor R51 and power supply E12.

The feedback network comprises resistors R47 and R48 each having one end connected at the node 26*y*. The latter is direct-coupled by lead 26*z* to the base 26*b* of transistor Q26. The other end of resistor R47 is connected to the in-phase output O14. As thus far described the embodiment of FIG. 22 is identical to that of FIG. 1. In the latter figure the other end of the resistor corresponding to resistor R48 is connected to the out-of-phase output. However, in the modification of FIG. 22 the other end of resistor R48 is connected to ground as shown. The reference potential is therefore derived solely from the in-phase output.



It will be noted that in the modifications of the invention discussed thus far the feedback network is passive. However, in FIG. 23 there is shown a modified form wherein the feedback network is active in that it comprises a transistor which provides both level setting and an additional delay for the reference potential swing. More specifically, transistors Q29, Q30 constitute a current switch and have their collector 29*c*, 30*c* connected through load resistors R53, R54 to a power supply E15 and their emitters 29*e*, 30*e* connected to a constant current source comprising power supply E14 and resistor R52. The base 29*b* of transistor Q29 is direct-coupled to the input node 18.

Transistors Q31, Q32 constitute a differential amplifier and have their respective collectors 31*c*, 32*c* connected to ground through load resistors R56, R57, their bases 31*b*, 32*b* direct-coupled by leads 29*x*, 30*x* to collectors 29*c*, 30*c* of transistors Q29, Q30, and their emitters 31*e*, 32*e* connected to a constant current source comprising a power supply E14 and resistor R55. The outputs O16, O17 are taken respectively from collectors 31*c*, 32*c* of transistors Q13, Q32.

The feedback network is taken from the out-of-phase output O17 and comprises a transistor Q33 having its base 33*b* direct-coupled to said output O17, its collector 33*c* connected through load resistor R58 to ground, and its emitter 33*e* connected through resistor R59 to power supply E15. A resistor R60 is connected between collector 33*c* and emitter 33*e* to provide flexibility in design whereby the upper and lower limits of the reference potential swing may be adjusted to the desired magnitudes. The feedback signal is derived from the collector 33*c* and is applied through lead 33*x* to the base 30*b* of transistor Q30 so as to provide the latter with a time-delayed in-phase reference potential as shown in FIG. 6.

The active feedback network of FIG. 23 may also be utilized in a current switch circuit having only a single stage as shown in FIG. 24 wherein transistors Q34, Q35 constitute the current switch and are provided with collectors 34*c*, 35*c* connected to power supply E16 through load resistors R61, R63 and emitters 34*e*, 35*e* connected to a constant current source comprising power supply E17 and resistor R62. The base 34*b* of transistor Q34 is connected to the input node I9. Theout-of-phase output O18 is taken from the collector 34*c* of transistor Q34 and the in-phase output O19 is taken from the collector 35*c* of transistor Q35.

The feedback network comprises transistor Q36 having its collector 36*c* connected through load resistor R64 to power supply E16, its base 36*b* direct-coupled by lead 34*x* to collector 34*c* of transistor Q34, and its emitter 36*e* connected to power supply E17 through resistor R65. Resistor R66 extends between collector 36*c* and emitter 36*e* to provide flexibility in design as noted above with respect to resistor R60. Transistor Q36 serves to invert the out-of-phase signal at output O18, further delay said signal, and set the signal to the proper level. The resulting time-delayed in-phase signal is then applied as the reference potential by lead 36*x* to the base 35*b* of transistor Q35 so as to obtain the mode of operation illustrated in FIG. 6.

FIG. 25 shows another modification wherein the invention is embodied in the current switch of the emitter follower type. The current switch function is provided by the first stage comprising transistors Q37 and Q38 having collectors 37*c*, 38*c* connected through load resistors R67, R68 to power supply E18 and emitters 37*e*, 38*e* connected to a constant current source comprising resistor R69 and power supply E19. The base 37*b* of transister Q37 is connected to the input I10.

The second stage functions as an emitter follower and comprises transistors Q39, Q40 having collectors 39*c*, 40*c* connected to power supply E18, bases 39*b*, 40*b* direct-coupled by leads 37*x*, 38*x* to the respective collectors 37*c*, 38*c* of transistors Q37, Q38, and emitters 39*e*, 40*e* con-

nected through respective emitter resistors R70, R71 to power supply E19. The out-of-phase output O20 is taken from emitter 39*e* and the in-phase output O21 is taken from emitter 40*e*.

The reference potential is derived from the in-phase output O21 by a feedback network comprising resistors R72 and R73 each having one end joined at the node 38*y*. The opposite end of resistor R72 is connected to the in-phase output O21 and the opposite end of resistor R73 is grounded as shown. A lead 38*z* extends from node 38*y* to the base 38*b* of transistor Q38 so as to apply thereto the time-delayed-in-phase reference potential related to the input potential in the manner disclosed in FIG. 6.

FIG. 26 shows still another modified form of the invention embodying the negative feedback network of FIG. 1 in combination with a positive feedback network to further increase the switching speed. In this figure the first stage is a current switch comprising transistors Q41 and Q42 having respective collectors 41*c*, 42*c* connected to ground through load resistors R74, R76 and emitters 41*e*, 42*e* connected to a constant current supply comprising resistor R75 and power supply E16. The base 41*b* of transistor Q41 is connected to the input I11.

The second stage functions as a differential amplifier and comprises transistors Q43, Q44 having collectors 43*c*, 44*c* connected to ground through load resistor R79, R81 and emitters 43*e*, 44*e* connected to a constant current source comprising resistor R80 and power supply E16. The in-phase output O18 is taken from collector 42*c* and the out-of-phase output O19 is taken from collector 44*c*.

The negative feedback network comprises a pair of resistors R77, R78 each having one end connected to a node 42*y*. The opposite end of resistor R77 is connected to the in-phase output O18 and the opposite end of resistor R78 is connected to the out-of-phase output O19. Node 42*y* is connected through leads 42*z* and 42*w* to the base 42*b* of transistor Q42 so as to apply thereto the time-delayed in-phase reference potential.

As thus far described the circuit of FIG. 26 is identical to that of FIG. 1. The positive feedback network added to the circuit of FIG. 26 is illustrated in the form of a capacitor C3 having one end connected to collector 41*c* of transistor Q41 through lead 41*x* and the other end connected to base 42*b* of transistor Q42 through lead 42*w*. The effect of capacitor C3 may be best understood by reference to FIG. 28 showing idealized traces of the input and reference potentials during the switching operation. It will be seen that the reference potential, instead of remaining at its quiescent level until after traversal by the input potential as shown in FIG. 6 in connection with the circuit modification of FIG. 1, is urged by the positive feedback effect of capacitor C3 in a direction opposite to the direction of swing of the input potential so as to cause a mutual traverse.

More specifically, almost immediately after the input potential starts to move downwardly at the point A the reference potential starts to move upwardly at the point B until the two potentials traverse at D. The reference potential continues to move upwardly to a maximum level at E while the input potential continues to move downwardly towards its lowermost level. A similar relationship between the two potentials exists when the circuit is switched in the opposite direction to cause a traverse at the point F.

This mode of operation increases the switching speed because of two effects. First, the traverse point D occurs sooner in time because the reference potential moves upwardly to meet the input potential instead of merely at the quiescent level as shown in FIG. 6. Second, the increased swing of the reference potential, such as indicated at E, causes a greater difference between the input and reference potentials so as to provide a large overdrive which further increases the switching speed.

In manufacturing monolithic integrated circuits, the use of capacitors is relatively expensive. For these applications the circuit of FIG. 27 may be particularly advantageous in that is provides both negative and positive feedback networks similar to FIG. 26 but without requiring a capacitor. More specifically, the first stage of FIG. 27 functions as a current switch and comprises transistors Q45, Q46 having collectors 45*c*, 46*c* connected to ground through load resistors R82, R84, and emitters 45*e*, 46*e* connected to a constant current source comprising resistor R83 and power supply E17. Base 45*b* of transistor Q45 is connected to input node I12.

The second stage constituting the differential amplifier comprises a pair of transistors Q47, Q48 having collectors 47*c*, 48*c* connected to ground through load resistors R87, R89 and emitters 47*e*, 48*e* connected to a constant current source comprising resistor R88 and power supply E17. The base 47*b* of transistor Q47 is direct-coupled by lead 45*x* to the collector 45*c* of transistor Q45, and the base 48*b* of transistor Q48 is similarly direct-coupled by lead 46*x* to the collector 46*c* of transistor Q46. The in-phase output O20 is taken from the collector 47*c* of transistor Q47 and the out-of-phase output O21 is taken from the collector 48*c* of transistor Q48.

The negative feedback network comprises a resistor R86 having one end connected to the in-phase output O20 and the other end connected to the reference base 46*b* of transistor Q46 through leads 46*y* and 46*z*. The positive feedback network comprises a resistor R85 having one end connected to collector 45*c* of transistor Q45 through lead 45*x* and its other end connected to reference base 46*b* of transistor Q46 through lead 46*z*. The traces of the input potential and reference potential of the circuit modification of FIG. 27 will thereby be approximately similar to the idealized curves shown in FIG. 28. The circuit of FIG. 27 will thus provide a faster switching operation for the reasons and in the manner discussed above with respect to the circuit of FIG. 26.

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While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

I claim:

1. A switching circuit comprising
an input node,
an active element switchable in response to the potential of the input node traversing a reference potential, and
a direct-current negative feedback network to maintain the quiescent value of the reference potential within a predetermined incremental range about the quiescent potential of the input node.

2. A logic circuit comprising
an input node,
an active element switchable in response to the potential of the input node traversing a reference potential,
a network to maintain the quiescent value of the reference within a predetermined range about the quiescent potential of the input node, and

means to delay the effect of said network until after said input node potential traverses said reference potential.

3. A switching circuit comprising
an input node for receiving an input signal having a predetermined amplitude,
a switch actuable in response to the potential of the input node traversing a reference potential, and
a network to vary the reference potential with an amplitude less than that of the input signal and approximately in phase therewith but with a time delay with respect thereto.

4. A logic switching circuit comprising
a reference node,
an input node,
an active element switchable from one state to another in response to the potential of the input node traversing the potential of the reference node, and
a feedback network to vary the potential of said reference node in time-delayed phase with any variation of the potential of the input node.

5. A logic switching circuit comprising
a reference node,
an input node,
an active binary element switchable from one state to another in response to the potential of the input node traversing the potential of the reference node,
an output network for connecting said binary element to a load, and
a feedback network extending from said output network to said reference node to vary the potential of the latter in time-delayed phase with any variation of the potential of the input node.

6. A logic switching circuit comprising
a reference node,
an input node,
an active binary element switchable from one state to another in response to the potential of the input node traversing the potential of the reference node,
an output network for connecting said binary element to a load,
a feedback network extending from said output network to said reference node to maintain said element on the threshold of switching, and
said active element including means for delaying the effect of said feedback network until said input node potential traverses said reference node potential.

7. A logic switching circuit comprising
a reference node,
an input node,
an active binary element switchable from one state to another in time-delayed response to the potential of the input node traversing the potential of the reference node,
an output network for connecting said binary element to a load,
an attenuator for attenuating the signal at said output network, and
a feedback network extending from said attenuator to said reference node to apply thereto said attenuated signal.

8. A logic circuit comprising
a reference node,
an input node,
an active binary element switchable from one state to another in response to the potential of the input node traversing the potential of the reference node, and
a feedback network extending from said binary element to said reference node to maintain the quiescent potential of the latter at a predetermined increment from the quiescent potential of the input node in both states of said binary element.

9. A logic circuit comprising
an input node,
a current switch actuable in response to the potential of the input node traversing a reference potential, and
a network to maintain the quiescent value of the reference potential within a predetermined increment of the quiescent potential of the input node.

10. A logic switching circuit comprising
a reference node,
an input node,
a current switch actuable from one state to another in response to the potential of the input node traversing the potential of the reference node,
an output network for connecting said binary element to a load,
a negative feedback network extending from said output network to said reference node to vary the potential of the latter, and
means for delaying the effect of said feedback network until after said input node potential has traversed said reference node potential.

11. A logic switching circuit comprising
a reference node,
an input node,
a current switch actuable from one state to another in response to the potential of the input node traversing the potential of the reference node,
an output network for connecting said switch to a load,
an attenuator for attenuating the signal at said output network,
a direct-current negative feedback network extending from said attenuator to said reference node to apply thereto said attenuated output signal.

12. A logic switching circuit comprising
a reference node,
an input node,
a current switch actuable from one state to another in response to the potential of the input node traversing the potential of the reference node,
an output network for connecting said switch to a load,
means for delaying the signal at said output network,
an attenuator for attenuating the signal at said output network, and
a feedback network extending from said attenuator to said reference node to apply thereto said attenuated delayed signal.

13. A logic switching circuit comprising
a reference node,
an input node,
a current switch actuable to switch a constant current from one path to another in response to the potential of the input node traversing the potential of the reference node,
an output network for connecting said switch to a load,
means for delaying the signal at said output network with respect to the signal at said input node,
an attenuator for attenuating the signal at said output network, and
a feedback network extending from said attenuator to said reference node to apply thereto said delayed attenuated signal.

14. In a transistor switching circuit having a source of constant current, a source of reference potential, a plurality of asymmetric impedance current paths connected in the forward direction between said current source and said reference potential, at all times at least one of which is carrying said constant current and at least one of which is the path from emitter to collector of a transistor, and an input node, the improvement comprising
a network to maintain the quiescent condition of said circuit on the threshold of switching.

15. A logic switching circuit comprising:
a reference node,
an input node,
an active element switchable into one of two stable states in response to the potential of the input node traversing the potential of the reference node,

an output network having an in-phase output node and an out-of-phase output node, said network being responsive to said active element, for providing two outputs,

a first attenuator connected between the in-phase output node and the reference node,

a second attenuator having a value of resistance greater than that of the first attenuator, connected between the out-of-phase output node and the reference node, and

capacitive means connected to said reference node, thereby aplying a delayed attenuated signal to said reference node.

**16.** A logic switching circuit comprising:

a reference node,

an input node,

an active element switchable into one of two stable states in response to the potential of the input node traversing the potential of the reference node,

an output network having an in-phase output node and an out-of-phase output node, said network being responsive to said active element, for providing two outputs,

a first attenuator connected between the in-phase output node and the reference node, and

a second attenuator having a value of resistance greater than that of the first attenuator, connected between the out-of-phase output node and the reference node,

thereby applying a delayed attenuated signal to said reference node.

**17.** In a transistor switching circuit having a source of constant current, a source of reference potential, a plurality of assymetric impedance current paths connected in the forward direction between said current source and said reference potential, at all times at least one of which is carrying said constant current and at least one of which is the path from emitter to collector of a transistor, an input node, said constant current being switchable from one path to another in response to the potential of the input node traversing the reference potential, and an output network for connecting said circuit to a load, the improvement comprising

a direct-current negative feedback network extending from said output network to said reference potential to maintain the quiescent value of the latter at a predetermined increment from the quiescent potential of the input node.

**18.** In a transistor switching circuit having a source of constant current, a source of reference potential, a plurality of asymmetric impedance current paths connected in the forward direction between said current source and said reference potential, at all times at least one of which is carrying said constant current and at least one of which is the path from emitter to collector of a transistor, an input node, said constant current being switchable from one path to another in response to the potential of the input node traversing the reference potential, and an output network for connecting said circuit to a load, the improvement comprising

a negative feedback network extending from said output network to said reference potential source to vary the potential of the latter in time-delayed phase with any variation of the potential of the input node, and

means for delaying the effect of said feedback network until after said input node potential has traversed said reference potential.

**19.** In a transistor switching circuit having a common point, a source of constant current, means connecting said source of constant current to said common point, a reference potential, a plurality of asymmetric impedance current paths connected in the forward direction between said common point and said reference potential at least one of said paths being from emitter to collector of a transistor, means operable to cause said constant current to flow at all times through at least one of said paths, and



sensing means associated with at least one of said paths, an input node, said constant current being switchable from one path to another in response to the potential of the input node traversing the reference potential, and an output network for connecting said circuit to a load, the improvement comprising

an attenuator for attenuating the signal at said output network, and a feedback network extending from said attenuator to provide said reference potential in the form of said attenuated signal.

**20.** In a transistor switching circuit having a common point, a source of constant current, means connecting said source of constant current to said common point, a reference potential, a plurality of asymmetric impedance current paths connected in the forward direction between said common point and said reference potential, at least one of said paths being from emitter to collector of a transistor, means operable to cause said constant current to flow at all times through at least one of said paths, and sensing means associated with at least one of said paths, an input node, said constant current being switchable from one path to another in response to the potential of the input node traversing the reference potential and an output network for connecting said circuit to a load, the improvement comprising

means for delaying the signal at said output network with respect to the signal at said input node,

an attenuator for attenuating the signal at said output network, and

a feedback network extending from said attenuator to provide said reference potential in the form of said delayed attenuated signal.

**21.** A logic switching circuit comprising:

a reference node,

an input node,

an active element switchable into one of two stable states in response to the potential of the input node traversing the potential of the reference node,

an output network having an in-phase output node and an out-of-phase output node, said output network being responsive to said active element, for providing two outputs, and

a feedback network connected between the in-phase output node and the reference node for providing said reference node with a reference potential.

**22.** A switching circuit comprising

an input node,

an active element switchable in response to the potential of the input node traversing a reference potential,

a direct-current negative feedback network to maintain the quiescent value of the reference potential within a predetermined incremental range about the quiescent potential of the input node, and

a network to urge the reference potential in a direction opposite to the swing of the input potential during the switching of said active element.


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