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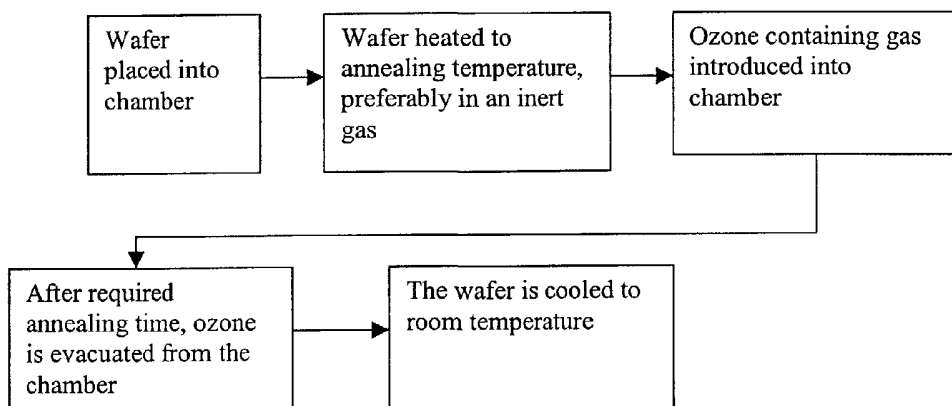
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ning of each regular issue of the PCT Gazette.

(54) Title: LOW TEMPERATURE OZONE ANNEAL OF GATE AND CAPACITOR DIELECTRICS



(57) Abstract: A method of thermal annealing of semiconductor devices is provided. In one aspect the present invention, gate and/or capacitor dielectric layer(s) on a semiconductor substrate are annealed characterized in that the dielectric layer(s) is exposed to an ozone-containing atmosphere for a period of time in the range of about 0.1 second to 5 minutes and at a temperature in the range of about 20°C to 500°C.

WO 2004/010468 A3

INTERNATIONAL SEARCH REPORT

International application No.

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A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/8242, 21/44

US CL : 438/240, 265, 381, 396, 648, 683, 770, 772

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/240, 265, 381, 396, 648, 683, 770, 772

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPAT EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,E	US 2003/0207528 A1 (LI) 06 November 2003 (06.11.2003), see abstract; figure 1; paragraphs 25-32.	1-20
Y,P	US 6,482,686 B1 (TAKEMURA) 19 November 2002 (19.11.2002), column 3, lines 37-35; column 6, lines 13-25, 60-66; column 9, lines 1-6.	1-20
X	US 6,165,834 A (AGARWAL et al) 26 December 2000 (26.12.2000), abstract; column 3, lines 55-65; column 4, lines 4-26; column 5, lines 15-22.	1-5, 7-11
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Y		13-20



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