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Eisenberg et al.

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[54] **DISPLAY PANEL RESET AND SAFETY TIMING CIRCUIT**

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[73] Assignee: **Burroughs Corporation,** Detroit, Mich.

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[63] Continuation-in-part of Ser. No. 47,650, June 19, 1970, abandoned.

[52] **U.S. Cl.** ..... **315/169 TV,** 315/169 R

[51] **Int. Cl.** **H05b 37/00**

[58] **Field of Search** ..... 315/169 TV, 169 R

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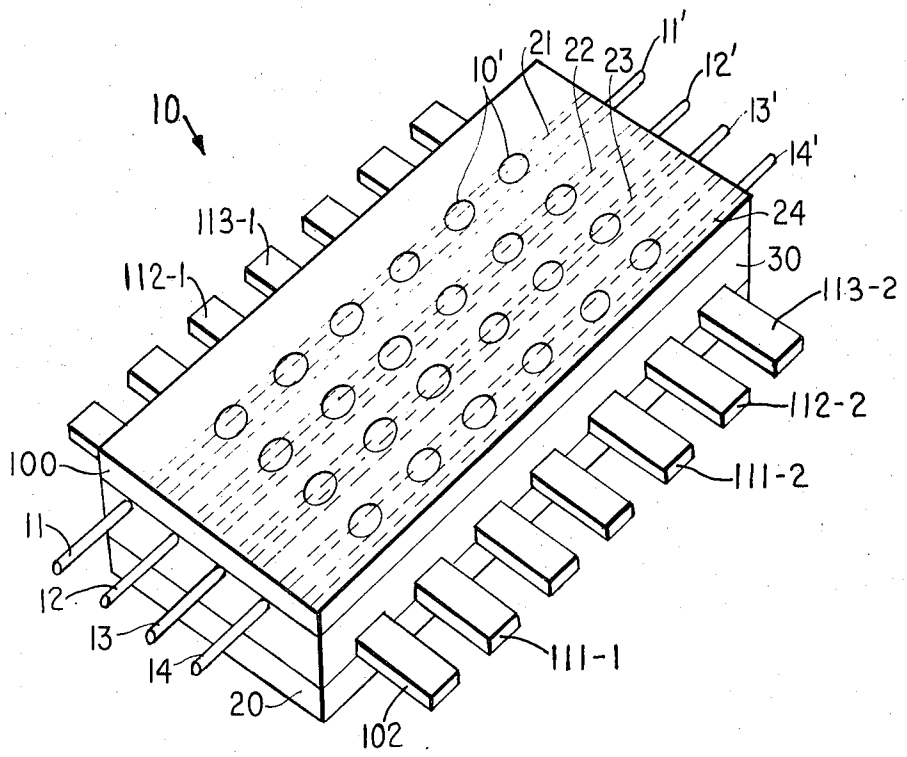
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[57] **ABSTRACT**

Information display apparatus including a multiple element display panel having an anode electrode and a cathode electrode intersecting at each display element, a plurality of drivers for selectively energizing one set of the electrodes in a pattern corresponding to the information to be displayed, and reset and timing circuitry for sequentially energizing the other set of electrodes with decreased risk of damaging the display elements, while increasing the reset energy applied to the panel and insuring activation or firing of only the selected display elements.

7 Claims, 3 Drawing Figures



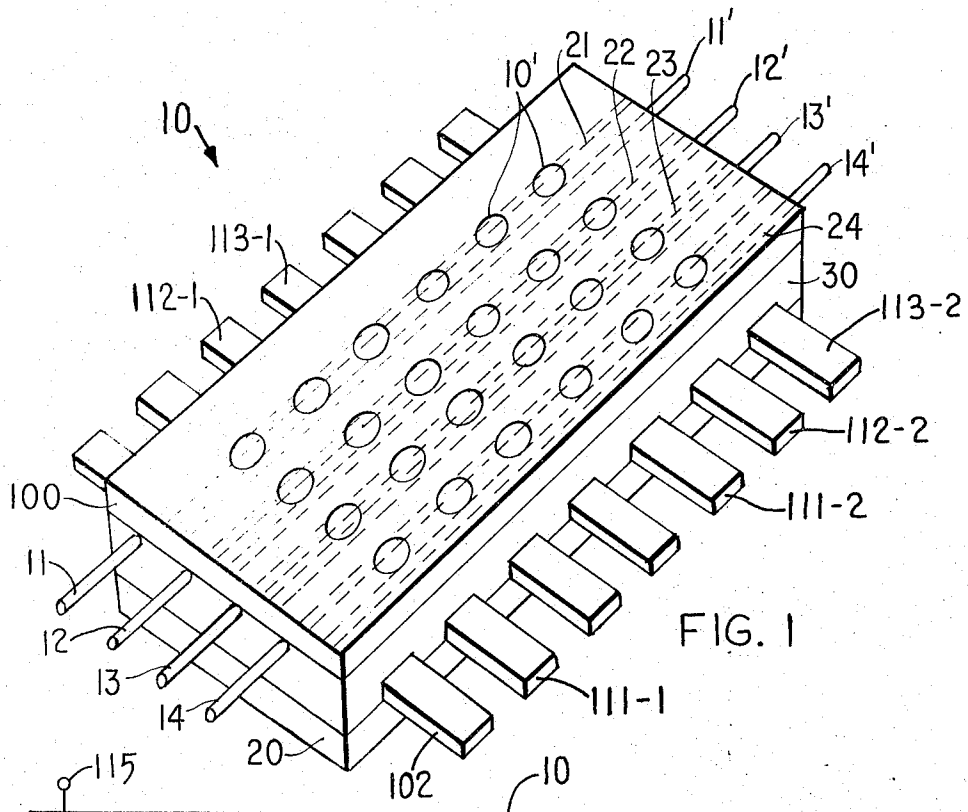


FIG. 1

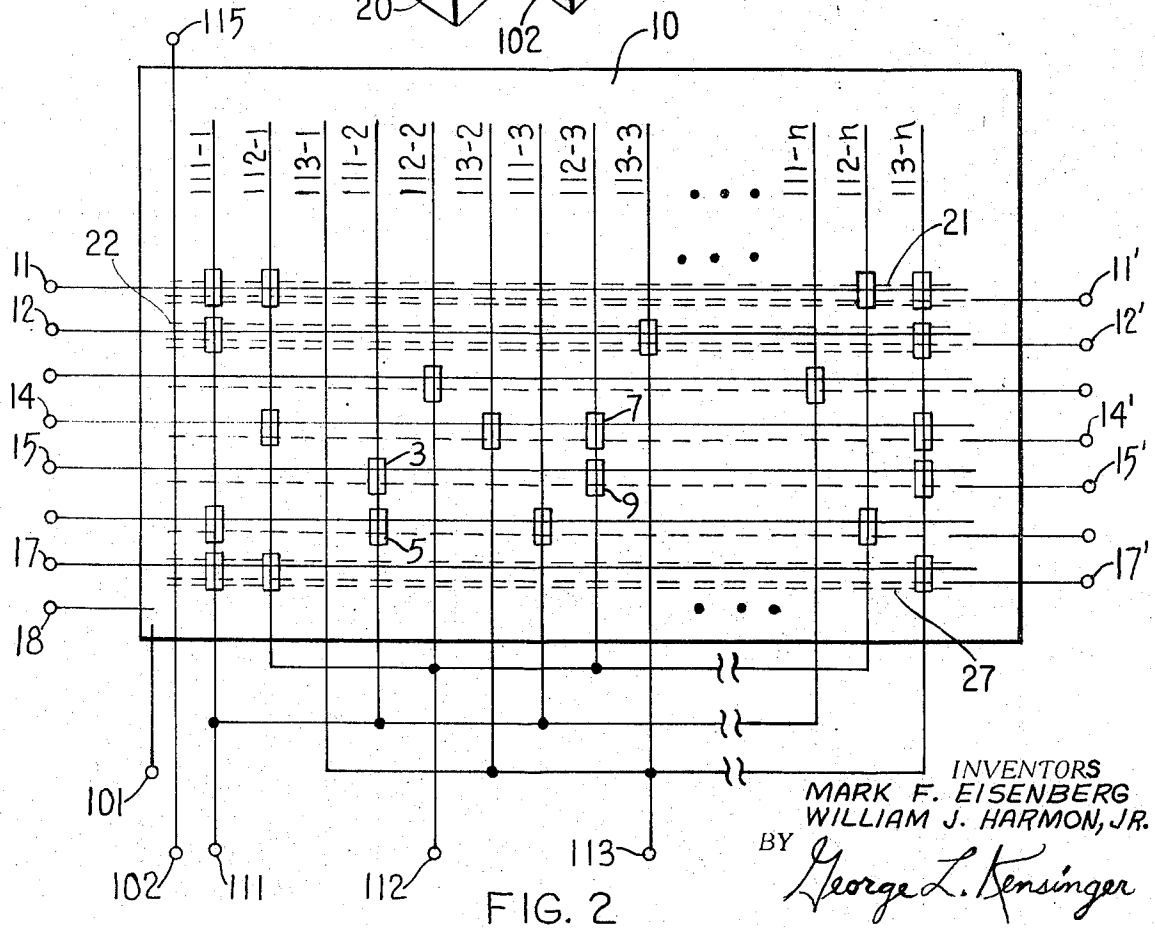
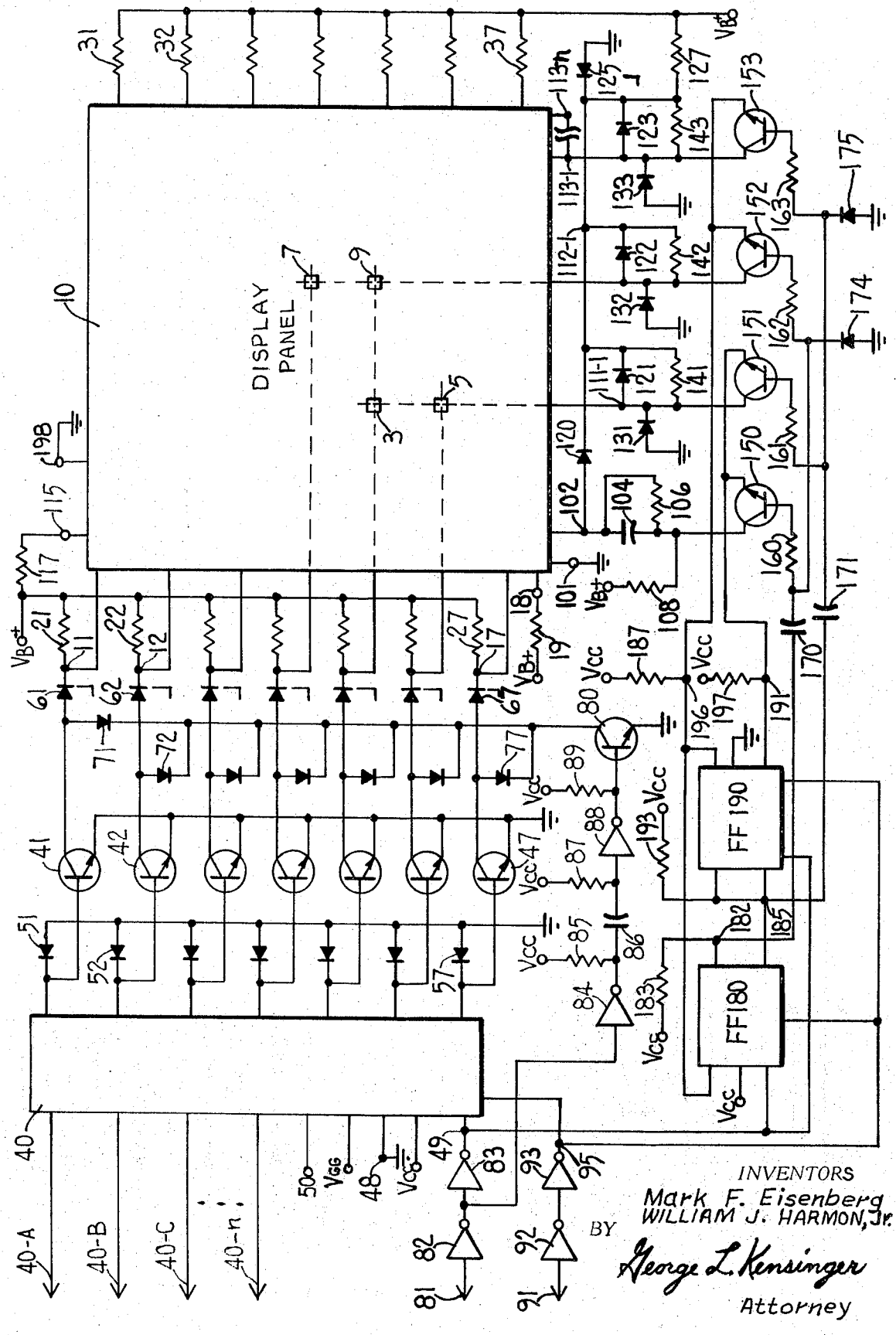


FIG. 2

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DISPLAY PANEL
FF 190
FF180
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DISPLAY PANEL RESET AND SAFETY TIMING CIRCUIT

This patent application is a continuation-in-part of application Ser. No. 47,650, filed June 19, 1970, now abandoned.

This invention relates to display systems incorporating display panels having a large number of elements or cells arrayed in rows and columns and energizable selectively to display a character or mssage or other form of information. More particularly, the subject invention relates to apparatus for safely sequencing the operation of such a panel and for positively resetting the panel when necessary.

Generally, such devices include at least two electrodes, an anode and a cathode, for each element or cell and a separate driver circuit for each cathode and anode, or for each row of cathodes or each column of anodes. Certain improved display panels, however, are themselves structured for facilitating the energization of the cells and thus simplifying the required external drive circuitry. Examples of such improved devices are disclosed in Ogle, et al., patent application Ser. No. 828,793, filed May 28, 1969, now abandoned in favor of U.S. patent application Ser. No. 850,984, filed Aug. 18, 1969, and in J. A. Ogle patent application Ser. No. 855,448, also filed Aug. 18, 1969, both of which are incorporated herein by reference.

In some of these display systems a small number of drivers successively energize one set of the panel electrodes by being sequentially activated from a counter or from a multiple phase clock circuit. The cathodes, for example, may be driven in different groups by the several sequentially cycled drivers. If the clock or counter circuit happens to stop due to failure or otherwise, one of these drivers may be held on and one of the associated cathodes, together with associated display elements, would remain energized. If the elements are glow discharge cells, they could thus become overheated and blackened.

Such display panels also may include a column of reset calls positioned just ahead of the first column of display cells. At the beginning of each scanning cycle of operation, the reset cells are turned on to facilitate the subsequent activation of selected cells in the first column of display cells. It has been discovered that the column of reset cells does not turn on as readily as do the other cells as a consequence of preferential glow transfer between adjacent columns of them. Since the reset cells are positioned ahead of, or upstream from the other cells, no such preferential glow transfer aids the firing or activation of the reset coils themselves.

Another difficulty which has occurred in gas-filled glow discharge display devices is that previously activated cells may fire by accident if ionization in a subsequent selected cell does not build up earlier in time to fire itself. This is especially a problem in display panels having communicating slots or grooves between cells and in those having common driving apparatus for different columns of display cells.

Any of these difficulties may be encountered in any multiple element display device, whether or not incorporating glow discharge elements or cells.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a fail-safe timing or sequencing circuit for multiple element display devices.

Another object of the invention is to increase the energy available in a display system for resetting the display devices for more positively resetting the device.

A further object of this invention is to delay activation of each column of display cells in display panels momentarily, to insure pre-ionization and correct firing of the selected cells.

A further object of the invention is to prevent overheating of display elements due to clock circuit failure and to momentarily blank each column of elements as it is about to be activated to assure proper energization of the selected elements.

In accordance with these objects there is provided a reset and safety timing circuit for display devices having multiple display elements and two sets of control conductors including a plurality of first drivers for driving the first set of control conductors in a pattern corresponding to the information to be displayed, a plurality of second drivers for sequencing the second set of conductors, and timing apparatus for momentarily blanking the first set of drivers for each column of information to be displayed, sequentially controlling the second set of drivers in a failsafe manner, and for applying an increased amount of reset energy for assuring proper resetting of the display device.

Other features and advantages of the present invention will be apparent from consideration of the following detailed description of the preferred embodiments together with the accompanying drawings in which:

FIG. **1** is a perspective view of a representative display panel with which the subject invention may be utilized;

FIG. **2** is a schematic representation of such a panel with attendant electrodes and representative array of display cells; and,

FIG. **3** is an electrical schematic circuit diagram of the display panel reset and safety timing apparatus of applicants' invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The system described and claimed herein is intended primarily for operating and scanning the cells in a display panel having a matrix array of similar light-producing cells. It is particularly useful in operating the panels described and claimed in the U.S. patent application Ser. No. 850,984 of Ogle and Holz, filed Aug. 18, 1969, as continuation-in-part of Ser. No. 828,793, and in the U.S. patent application Ser. No. 855,448 of J. A. Ogle, filed concurrently therewith. To properly illustrate the invention, such a panel is shown and described herein as panel **10.** The panel may have substantially any desired size and shape, and it may include substantially any number of gas cells or the equivalent. The panel also contains any suitable ionizable gas such as neon argon, xenon, etc., singly or in combination, and a vapor of a metal such as mercury to minimize cathode sputtering.

Different numbers of cells are shown in the various figures for illustrating the panel itself and for use in describing the operating system of the invention. For example, the panel structure shown in FIG. **1** has six col-

umns of four cells each. And in FIG. 2, a greater number of cells is indicated in a schematic representation of the panel and of the addressing or scanning system associated with it.

Referring to FIG. 1, a representative display panel 10 having a plurality of display cells 10' includes an insulating housing of glass, ceramic, or the like, formed of parallel insulating layers 20, 30 and 100 sandwiched together. A row of electrodes 11, 12, . . . 14 is disposed in the top layer 100 thereof and electrodes 11', 12' . . . 14' are disposed in the bottom layer 20, preferably being wires used as display control anodes and scanning anodes, respectively, in the operation of the device. A gas communication slot or channel 21, 22, . . . 24 is provided in the panel along each of the scan control anodes 11', 12' . . . 14', either in insulating layer 20 or in insulating layer 30, or between them.

The cathode electrodes 111-1, 112-1, 113-1, . . . 113-2 are preferably flat strips, each having a series of holes or apertures for a column of display cells 10'. The cathodes are oriented vertically, parallel to each other, and at an angle, preferably 90°, to the anode electrodes 11', 12', . . . 14'. Each crossing of a cathode and a scan anode defines a scanning cell. A cathode aperture is located at each such crossing for the corresponding display cell 10'. Each cathode 111-1 . . . 113-2 thus lies along a column of cells, and each anode lies along a row of the cells. In addition, each column of cathode apertures is associated with a column of cells and each row of cathode apertures, defined by adjacent cathodes, lies along a row of the cells. Thus, each scanning cell includes a portion of a scan control anode 11', 12', . . . 14', the associated portion of a cathode 111-1 . . . 113-2 above it, and the volume of gas between these electrode portions. The scanning cells are identified by the anode and cathode which cross them and are connected in rows by the gas communication paths 21–24 situated along scan anodes 11'–14'.

In one form of the invention, the panel 10 is completed by a cover or viewing plate of glass or the like and a reset cathode 102. In the completed panel 10, the plates and the various electrodes are hermetically secured together by a seal formed along their adjacent edges by any suitable material such as glass frit, for example, Pyroceram, or the like. Reset cathode 102 may have a separate group of gas cells associated with it, if desired. The gas used in panel 10 is introduced in any suitable manner, for example, by means of a ball jar or by means of tubulation (not shown), secured to the bottom plate.

To execute a scanning operation in panel 10, the cells are actuated beginning with the first column of cells and proceeding from column to column to the last column of cells in the device, after which a signal is generated to fire the cells. associated with reset cathode 102 to initiate another scanning cycle. The arrangement shown in FIG. 2 is used to perform this scanning operation. The system of the invention utilizes cell-scanning principles described in application Ser. No. 850,984, the panel having its cathode electrodes connected in th ee groups, which may be described as phases. The panel shown in FIG. 2 has its cathodes 111, 112, 113 connected in such groups or phases. The first cathode electrode 111-1 associated with the first column of display cells at the left-hand edge of the panel is designated a phase 1 cathode and every third cathode 111-2, 111-3, . . . 111-*n* is connected in this group. The other cathodes 112 and 113 are connected in the other groups as shown, including the last cathodes 112-*n* and 113-*n*.

A plurality of display cells are illustrated, including representative cells 3 and 5 associated with cathode 111-2 and cells 7 and 9 associated with cathode 112-3. Any number of cells may be included in the array, of course, including cells in association with reset cathode 102, if desired. In addition, the panel includes scan control anodes 11', 12', . . . 17' situated in gas communication slots or channels 21–27, and display control anodes 11, 12, . . . 17, which are operated independently.

The slots or channels 21–27 provided along scan anodes 11'–17' allow gaseous communication to occur between adjacent columns of scan cells. As a consequence, when an electrical discharge occurs in one column of cells and ionizes the gas in them, it serves to prime the two adjacent columns for ionization and discharge. For example, when a column of scan cells along cathode 112-1 is glowing, it primes the preceding and succeeding columns along cathodes 111-1 and 113-1. Scan control pulses are applied to terminals 111-113 sequentially and, therefore, when the next pulse is applied to terminal 113, it will produce a glow discharge only in column 113-1 which was primed by the previously glowing column 112-1. It is this selective gaseous priming along slots or channels 21–27 which results in preferential glow transfer from column to column and allows the cells of a panel to be scanned with as few as three driving sources connected to terminals 111-113.

Referring now to FIG. 3 in detail, there is illustrated a block diagram of a display system including a display panel 10 having a plurality of display anode electrodes 11, 12, . . . 17 connected through resistors 21, 22, . . . 27 to a potential terminal V_B and a plurality of scan anodes also coupled to potential terminal V_B through resistors 31, 32, . . . 37. Display control cathodes 111-1, 112-1 and 113-1 are associated with the first three display columns and are, therefore, at one end of the panel. The panel also includes reset cathode 102 and a plurality of display control cathodes 111-1 . . . 111-*n*, 112-1 . . . 112-*n*, 113-1 . . . 113-*n*.

The display device 10 includes a large number of display elements or cells, representative ones of which are designated 3, 5, 7 and 9. There are also provided keep-alive anodes 18 and 115 coupled to potential terminal V_B by resistors 19 and 117, respectively, and keep-alive cathodes 101 and 198, respectively, which are grounded.

The anode electrodes 11, 12 . . . 17 of the panel are driven in a pattern representative of the information to be displayed from a character generator apparatus 40 having input terminals 40-A through 40-*n* for receiving the information signals, bias terminals V_{GG} and V_{CC} and reference terminal 48 which is grounded. The character generator 40 may include both decoding apparatus and encoding apparatus and includes a read-only memory (ROM) which may utilize integrated circuit or other semiconductive information storage means or magnetic information storage means.

The information signals applied to terminals 40-A through 40-*n* of the character generator may be encoded in binary or binary coded decimal (BCD) or a different such terminal may be provided for each infor-

mation symbol, character or numeral to be displayed.

In the illustrated embodiment of the invention character generator **40** has seven outputs which are applied to the base electrodes of NPN transistors **41, 42** through **47** and to the cathodes of base protection diodes **51, 52 . . . 57,** the anodes of which are grounded. The emitters of driving transistors **41, 42 . . . 47** are also grounded and the collector output terminals are coupled to the anode electrodes **11, 12 . . . 17** of the display device **10** through Zener diodes **61, 62 . . . 67.** The collectors of the anode drivers are also connected to the anodes of diodes **71, 72 . . . 77,** the cathodes of which are all connected to the collector electrode of blanking control transistor **30.**

In response to information signals received on its input terminals, character generator **40** provides a pattern of sequential, parallel information signals to the anode drivers for sequentially driving the anode electrodes of the display panel. There may be, for example, four sets of signals for each character or symbol if a 4 × 7 matrix is employed or five sets if a 5 × 7 matrix is employed. The display elements are activated upon the coincident energization of selected ones of the anodes and one of the display control cathodes, which are scanned sequentially.

The character generator **40** is sequenced in synchronism with the display control cathode by a clocking circuit having an input terminal **81** coupled to control terminal **49** by buffers **82** and **83.** The character generator in turn is reset in synchronism with the reset control cathode under control of a circuit having an input terminal **91** coupled to generator reset terminal **95** by buffers **92** and **93.**

The output of buffer **82** of the clock circuit is also applied to a blanking control circuit including amplifier **84** coupled to the input of amplifier **88** by the Pi-connected resistor-capacitor (RC) timing control circuit including resistors **85** and **87** and capacitor **86.** The output of amplifier **88** is connected to the base of blanking control transistor **80,** which is also biased through resistor **89** to reference potential terminal V_{CC}.

As each column of information signals is clocked out of character generator **40** to the display anode drivers **41, 42 . . . 47,** blanking control transistor **80** is momentarily operated by the timing control circuit to delay the application of the energization signals to the display anodes **11, 12 . . . 17.** This allows time for the selected display cells to become initially ionized at the beginning of each clock period so that only the selected elements actually turn on or fire, and the previously glowing cells do not re-ignite. Alternatively, blanking may be achieved by applying a control signal to terminal **50** of the character generator (ROM) if such is available. At the end of the blanking interval the display anode drivers **41, 42 . . . 47** operate for the display of the desired information.

The display control cathodes **111-1** through **113-n** are driven by three saturated drivers including NPN transistors **151, 152** and **153** having base electrode resistors **161** through **163,** respectively. There is also provided a reset driver including NPN transistor **150** having base resistor **160,** the collector of which is coupled to reset electrode **102** by the parallel RC network including capacitor **104** and resistor **106.** The collector resistor of transistor **150** is coupled to potential terminal V_B by resistor **108.**

The cathode electrodes including reset cathode **102** and the display control cathodes are coupled to a point of reference potential, established by grounded Zener diode **125** and resistor **127** connected to potential terminal V_B, through the parallel combinations of diodes **121** and resistor **141,** diode **122** and resistor **142** and diode **123** and resistor **143,** respectively. The display control cathodes are also clamped to ground by diodes **131, 132** and **133.**

The cathode drivers are controlled by a counter circuit including flip flops **180** and **190** which in turn are pulsed by the output of buffer amplifier **83** of the clock circuit and the output of buffer amplifier **93** of the reset control circuit. The flip flops are interconnected as a module **2** counter which normally applies a cycle of three pulses or counts for controlling the display control cathode drivers. The counter flip flops are referenced to ground and to potential terminal V_{CC} directly and the outputs are coupled to potential terminal V_{CC} through resistors **183** and **187** and resistors **193** and **197,** respectively.

One output of counter flip flop **180,** designated **182,** is applied to the base circuits of cathode driver transistors **150** and **152** through capacitor **170,** coupled to ground by reverse-biased diode **174.** Another output terminal **185** of the counter is applied through capacitor **171** to the base circuits of cathode driver transistors **151** and **153,** which are coupled to ground by reverse-biased diode **175.** Alternatively, diodes **174** and **175** could be replaced by resistors, although with less satisfactory results. Counter output terminal **191** is connected to the emitter electrodes of cathode driver transistors **150** and **151** and counter output terminal **196** is connected to the emitter electrodes of cathode drivers **152** and **153.**

In operation, the receipt of a reset signal on terminal **91** will reset both the character generator **40** and the counter flip flops, which will in turn actuate reset driver **150** for pulsing reset cathode **102** of the display panel. Since the reset cells of the panel associated with reset cathode **102** are not readily fired or actuated, applicants have provided an energy storage circuit in the output circuit of the reset cathode driver. This storage circuit is comprised of capacitor **104** and resistors **106** and **108.**

One load of capacitor **104** and one load of resistor **106,** at cathode **102,** are connected to the reference potential established by Zener diode **125,** through forward biased **120.** The opposite side of capacitor **104** and resistor **106** is coupled to V_B through resistor **108** and allows capacitor **104** to charge to a voltage determined by the ratio of resistor **106** to resistor **108.** The junction of resistor **106,** resistor **108** and capacitor **104** is connected to the collector of the reset driver transistor **150.** During the reset conditions this point is brought to ground potential forcing cathode **102** to some negative potential equal to the charge across the capacitor **104.** The above-mentioned action establishes a voltage between the reset cathode and the scan anodes of V_{B+}plus the negative potential. As ionization is a function of time and voltage the greater the magnitude of over voltage applied the shorter the time required for ionization, thus the stored charge enables shorter ionization times on the reset elements.

In the ordinary circumstances, Zener diode **125** is a 110 volt reference and, therefore, the remaining control cathodes are only driven between the approximately 110 volts and ground. This lesser potential on the other cathodes is adequate as they are each primed or preconditioned by the operation of the preceding column of elements. The reset cells, however, are much harder to drive since they are the first column in the panel and the glow or discharge must be transferred from the last column driven by cathode **113-*n*** back to the reset cathode **102** near the opposite edge of the panel.

The counter including flip-flops **180** and **190** is cycled or stepped by pulses from the clock circuit and can stop at any count in its cycle if the clock should stop or a circuit interruption occurs. This could hold one of the display cathode drivers **151, 152** or **153** in the "On" condition which could overheat and blacken some of the associated display cells, possibly even rendering them unsuitable for further use. Applicant's capacitive coupling circuit including capacitors **170** and **171,** resistors **160** through **163** and diodes **174** and **175,** however, eliminates this risk of display cell damage or destruction. If the counter or either of its flip-flops should hang up in either state, the capacitor **170** or **171** would charge up through a corresponding circuit path and act to disable the associated cathode driver **150** through **153** which had been activated. The timing or sequencing circuit is therefore both fail-safe in operation and provides insurance through momentary blanking that only the selected display elements are actuated in the display of information provided to the system.

Zener diodes **61, 62, . . . 67** are coupled to the display anode driver outputs instead of other type gating elements to prevent the display anodes from going too far more negative than the scan anodes, the keep-alive anodes **18** and **115,** the keep-alive cathodes **101** and **198** or the panel display control cathodes **111-1 . . . 113-*n***. In the preferred embodiment, Zener diodes **61, 62, . . . 67** are approximately **120** volt units, while Zener diode **125** is a **110** volt unit to protect against firing between the display anodes and the cathodes. Resistors **19** and **117** bias the keep-alive circuits with just sufficient current to keep them ionized. The keep-alive allows some gas to diffuse to the reset column to aid in resetting the panel.

Base protection diodes **51, 52, . . . 57** for the display anode drivers can be eliminated, under certain conditions, depending upon the characteristics of the random access memory (ROM) chosen for character generator **40** and of the driver transistors **41, 42, . . . 47.** Approximate typical values for voltages and circuit parameters are:

$V_{BB}+$	+250 Volts
V_{CC}	+ 5 Volts
V_{GG}	−12 Volts
R_{19}, R_{117}	1 Meg-Ohm
$R_{21} - R_{27}$	50 K Ohms
$R_{31} - R_{37}$	160 K - 200 K Ohms
R_{85}	1 K Ohms
R_{87}	5.6 K Ohms
R_{89}	2 K Ohms
R_{106}	100 K Ohms
R_{108}	200 K Ohms
R_{127}	50 K Ohms
$R_{141} - R_{143}$	100 K Ohms
$R_{160} - R_{163}$	2 K Ohms
$R_{193} - R_{197}$	2 K Ohms
C86	0.02 Micro-farads
C104	0.02 Micro-farads
C170, C171	0.33 - 0.47 Micro-farads

Details of the construction and operation of a typical display device for incorporation into the present system are disclosed in a publication by Burroughs Corporation entitled "Self-Scan Panel Display" designated Bulletin 1161 and 10M/11-69 (1969), and in an article entitled "Dot Matrix Display Features Inherent Scanning Ability" published in the Mar. 2, 1970 issue of "Electronics" magazine by W. J. Harmon, Jr. at pp. 120–125 of Volume 43, Number 5, both of which are incorporated herein by reference for the disclosures they provide. Reference is also made to an article entitled "Strobing Makes Longer LED Alphanumeric Displays Possible" by H. Borden and R. Kniss at pp. 126–130 of the same issue of "Electronics" for its disclosure.

Although the preferred embodiment of the invention has been described in detail, it should be understood that the present disclosure has been made by way of example only. Many modifications and variations of the invention are possible in light of the above teachings. It is, therefore, to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically disclosed.

What is claimed is:

1. A display system including a gas-filled display panel comprising

an array of first scanning cells disposed in rows and columns and including a scan anode electrode aligned with each row of scanning cells and a cathode electrode aligned with each column of scanning cells,

an array of display cells, each aligned with one of said scanning cells and adapted to receive glow transfer therefrom,

a display anode aligned with each row of said display cells and operating with said cathode electrodes,

a power supply coupled to said scan anodes for applying operating potential thereto,

said scanning cathode electrodes being connected in groups with at least every other cathode being in a group,

a separate cathode driver coupled to each of said groups of cathode electrodes for applying operating potential to each group of cathode electrodes separately,

drive means coupled to said cathode drivers and adapted to turn on each cathode driver separately in turn whereby the cathode electrodes are energized separately and in turn whereby each column of scanning cells is energized separately and in turn,

a character generator coupled to said display anodes and adapted to apply information signals thereto as each column of scanning cells is caused to glow whereby selected display cells in each associated column of display cells are caused to glow, and

means coupled to each of said cathode drivers for disabling said cathode drivers if said drive means becomes inoperative while one of said cathode drivers is applying operating potential to a group of cathodes.

2. The system defined in claim **1** wherein said drive means comprises a series of flip-flops having outputs coupled to said cathode drivers to operate each such cathode driver separately.

3. The system defined in claim **2** and including a capacitor connected in each said output to a cathode

driver, each said capacitor becoming charged and turning off its associated cathode driver if said series of flip-flops becomes inoperative.

4. The system defined in claim **1** wherein said display panel includes a column of reset cells adjacent to the first column of scanning cells, said column of scanning cells having a reset cathode electrode aligned therewith and connected to a reset cathode driver circuit, said reset cathode driver circuit including circuit means for applying higher operating potentials to said reset cathode than are applied to the other cathodes by their drivers.

5. The system defined in claim **1** and including blanking circuit means coupled to the output of said character generator for delaying the application of data signals to said display anodes.

6. The system defined in claim **4** wherein each of said cathode drivers includes a cathode drive transistor and said reset cathode driver includes a reset transistor,

said cathode drive transistors having their base electrodes connected to said drive means and their collector electrodes each connected to a group of cathode electrodes,

said reset transistor having its base connected to said drive means and its collector connected to said reset cathode.

7. The system defined in claim **6** wherein the collector of said reset transistor is connected to said reset cathode through a parallel resistor-capacitor circuit, the collectors of the other transistors being connected directly to their groups of cathode electrodes.

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