Abstract: A power supply can be operated in a low power mode by adjusting the pulses provided to a power supply switch until a pulse resulting in a reduced amount of power that exceeds a minimum power threshold required by a load coupled to the power supply switch is identified. For each successive switching cycle, a pulse causing a lower power to be provided to the load is produced. When a pulse is produced that causes a power to be provided to the load that does not exceed the minimum power threshold required by the load, a subsequent pulse is produced that causes a greater power to be provided to the load than the previous pulse. If the greater power exceeds the minimum power threshold, the subsequent pulse is stored and similar pulses are provided for the remainder of the low power mode.
MOSFET DRIVER WITH REDUCED POWER CONSUMPTION

INVENTORS
Andrey B. Malinin

RELATED APPLICATIONS
[0001] The application claims priority to United States Provisional Application No. 61,990,038, filed May 7, 2014, the contents of which are hereby incorporated in their entirety.

BACKGROUND
[0002] The present invention relates generally to power supply driver circuits, and more specifically, to a switching power supply driver circuit with reduced power consumption.
[0003] Switching power supplies utilize a transistor, such as a MOSFET, and a driving circuit configured to switch the transistor on and off. Power is provided to a load coupled to a switching power supply by controlling the switching of the transistor at a primary side of the power supply. The resulting power pulses provide power to a secondary side of the power supply, which in turn provides power to the load. To reduce power during standby modes, the frequency of power pulses provided by the power supply can be reduced, though doing so can cause the power provided to a load to sag as the load current increases. Alternatively, the capacitance of a secondary side capacitor can be increased, though doing so increases power supply costs.

BRIEF DESCRIPTION OF DRAWINGS
[0004] The teachings of the embodiments of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings.
[0005] Fig. 1 is a circuit diagram illustrating an AC to DC flyback switching power supply, according to one embodiment.
[0006] Fig. 2a is a graph illustrating the output current provided to a load when the output capacitance of a switch is fully discharged, according to one embodiment.
[0007] Figs. 2b and 2c are graphs illustrating the output current provided to a load when the output capacitance of a switch is only partially discharged, according to one embodiment.
[0008] Fig. 3 is a flow chart illustrating a process for reducing the energy per pulse provided by a power converter in a low power mode, according to one embodiment.
[0009] The features and advantages described in the specification are not all inclusive and, in particular, many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification, and claims. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and may not have been selected to delineate or circumscribe the inventive subject matter.

DETAILED DESCRIPTION OF EMBODIMENTS

[0010] The Figures (Fig.) and the following description relate to the preferred embodiments of the present invention by way of illustration only. It should be noted that from the following discussion, alternative embodiments of the structures and methods disclosed herein will be readily recognized as viable alternatives that may be employed without departing from the principles of the present invention.

[0011] Reference will now be made in detail to several embodiments of the present invention(s), examples of which are illustrated in the accompanying figures. It is noted that wherever practicable similar or like reference numbers may be used in the figures and may indicate similar or like functionality. The figures depict embodiments of the present invention for purposes of illustration only. One skilled in the art will readily recognize from the following description that alternative embodiments of the structures and methods illustrated herein may be employed without departing from the principles of the invention described herein.

[0012] Fig. 1 is a circuit diagram illustrating an AC to DC flyback switching power supply, according to one embodiment. The switching power converter 100 of Fig. 1 is a primary-side fly-back switching power converter configured to provide power to a load 121 via a Vdd node 132 and a GND node 134. The load 121 can be any electronic device configured to receive power from the switching power converter 100, for example an LED. The switching power converter 100 includes, among other components, a transformer T1 having a primary winding Np, a secondary winding Ns, and an auxiliary winding Na, a switch 104 (e.g., a MOSFET transistor), a controller 102, an output rectifier diode D1, resistors R1, R2, R3, and output filter capacitor CI. It should be noted that although a flyback switching power converter is illustrated in the embodiment of Fig. 1, the principles described herein apply equally to other power converters.

[0013] An input voltage \( (V_{in}) \) 108, typically a rectified AC voltage, is provided to the power converter 100. The controller 102 controls the on state and the off state of switch 104
using switch control signal 106. When the switch 104 is turned on, the switch is configured as a closed switch, allowing current to flow through the switch. When the switch 104 is turned off, the switch is configured as an open switch, preventing current from flowing through the switch. The switch control signal 106 may control the switching of the switch 104 using, for example, pulse width modulation (PWM) or pulse frequency modulation (PFM).

[0014] When the switch 104 is turned on, energy is stored in the primary side windings Np of the transformer T1. The voltage across the secondary winding Ns is negative and the diode D1 is reverse biased, blocking transfer of energy to electronic device 121. In this state, energy is supplied to the load 121 via the capacitor CI. When the switch 104 is turned off, the energy stored in the primary winding Np of the transformer T1 is released to the secondary winding Ns of the transformer T1. In this state, the diode D1 becomes forward biased, enabling a transfer of the energy stored in the transformer T1 to the load 121 and re-charging the capacitor CI.

[0015] The resistors R1 and R2 form a voltage divider coupled in series with the auxiliary winding Na of the transformer T1, producing the sense voltage \( V_{SEN} \) 112, which can be used to estimate the output voltage \( V_{OUT} \) 110. The resistor R3 is coupled in series with the switch 104 to produce a voltage \( I_{SEN} \) 114 which can be used in conjunction with \( V_{SEN} \) to estimate the output current \( I_{OUT} \) 116 through the load 121.

[0016] In normal operation, the controller 102 monitors \( V_{SEN} \) 112 and/or \( I_{SEN} \) 114 and controls switching of the switch 104 to maintain a regulated output. For example, in a constant voltage mode (CVM), the controller 102 controls switching of the switch 104 to maintain \( V_{OUT} \) 110 substantially near a desired regulation voltage \( V_{REF} \) (for example, within an allowable error range). In a constant current mode (CCM), controller 102 controls switching of the switch 104 to maintain \( I_{OUT} \) 116 substantially near a desired regulation current \( I_{REF} \) (for example, within an allowable error range). In alternative embodiments, controller 102 may perform only voltage regulation (without enabling a current regulation mode) and may therefore omit the current sense \( I_{SEN} \) feedback signal.

[0017] In some embodiments, the controller 102 generates the switch control signal 106 based on the received values of the voltage feedback signal \( V_{SEN} \) and the current feedback signal \( I_{SEN} \). As noted above, the switch control signal 106 controls the on/off states of the switch 104. In general, the controller 102 can implement any number of control schemes suitable for switch-mode power converters 100, such as pulse-width-modulation (PWM),
pulse-frequency-modulation (PFM), or any other suitable control scheme or combination thereof. In one embodiment, the controller 102 outputs a control signal that causes the ON time (or duty cycle) of the switch 104 to increase, during a certain switching cycle in order to increase power delivery to the load during that switching cycle, or to decrease in order to decrease power delivery to the load during that switching cycle.

[0018] The primary side auxiliary winding Na of the transformer T1 allows for a low voltage $V_{S_{EN} S_{E}}$ 112 to be generated because the voltage can be scaled down based on the turn ratio of the secondary winding Ns and the auxiliary winding Na. However, in an alternative embodiment, auxiliary winding Na may be omitted, and $V_{S_{EN} S_{E}}$ may instead be detected by directly monitoring the voltage across primary winding Np.

[0019] The controller 102 can be configured to operate in a low power mode. Low power modes can be implemented, for instance, in response to a determination that a load requires a low amount of power for operation, in response to a determination that the amount of power that a load requires will not change in an upcoming period of time, or in response to a determination that the load itself will not change in an upcoming period of time. The controller 102 can select to operate in the low power mode, or can configured itself to operate in a low power in response to an external input received by the controller 102.

[0020] In the low power mode, the energy per pulse provided by the primary side of the power converter 100 is reduced. The primary contributors to the amount of energy per pulse provided by power converter 100 are:

1. The energy dissipated in the switch when turning the switch on in a switching cycle due to parasitic capacitance of the switch
2. The energy delivered to the load 121

[0021] As used herein, "low power mode" can refer to regulation of the energy delivered to a load coupled to a switching power supply by adjusting the energy or charge delivered to a gate node of a switching power supply MOSFET. In contrast, "normal power mode" can refer to the regulation of the energy delivered to a load coupled to the switch power supply by adjusting the "on" time of the MOSFET (in a pulse width modulation mode) or by adjusting the time between pulses provided to the MOSFET with a fixed "on" time (in a pulse frequency modulation mode).

[0022] Reducing switch on time will not reduce the energy dissipated in the switch, which is dependent only on the drain voltage across the switch. Reducing switch on time will also not reduce the energy delivered to the load 121, which is dependent on the current.
provided to the load, which increases even after the switch is configured to the off state. Accordingly, in order to reduce the energy per pulse provided by the power converter 100, the controller 102 can discharge the output capacitance of the switch 104 only partially (as opposed to fully discharging the output capacitance of the switch). By only partially discharging the output capacitance of the switch 104, the amount of energy dissipated when turning on the switch decreases, and the output power provided to the load 121 decreases. However, the output capacitance of the switch 104 must be discharged enough to provide a required minimum amount of power to the load 121.

[0023] As used herein, "partially discharging the output capacitance of the switch" refers to the discharging of the output capacitance of the switch 104 by an amount greater than a first threshold and less than a second threshold, the first threshold associated with a corresponding output energy greater than an energy threshold required by a load, and the second threshold associated with a corresponding output energy associated with operation in a normal power mode. Accordingly, when operating in a low power mode, low power switch control signals 106 (or "gate pulses") are provided by the controller 102 to the switch 104 such that each low power switch control signal 106 only partially discharges the output capacitance of the switch. In some embodiments, the low power switch control signals 106 include an amplitude and duration based on a pre-determined or stored low power switch control signal. In other embodiments, the low power switch control signals 106 are determined based on an iterative process, for instance during a training mode or when transitioning from a normal power mode to a low power mode, by varying the amplitude and duration of provided switch control signals until a satisfactory low power control signal is determined as described below.

[0024] Accordingly, the controller 102 can be configured to implement an algorithm to reduce the energy per pulse provided by the power converter 100 while still providing a threshold amount of power required by the load 121 while the power converter is operated in a low power mode. In such embodiments, the controller 102 iteratively reduces the amount by which the output capacitance of the switch 104 is discharged in successive switching cycles when the power converter 100 enters the low power mode until an optimal energy per pulse is determined. The threshold amount of power required by the load 121 can be pre-determined and stored at the controller 102, can be determined during operation by the controller based on a property of the load (for instance, based on the amount of light emitted by an LED load), or can be received at the controller from an external source during
operation. It should be noted that although reference is made herein to a comparison between an output power provided to the load and a minimum threshold power required by the load, other embodiments can determined and compare an output current or voltage provided to the load to a minimum threshold current or voltage, respectively, required by the load.

When the power converter 100 enters the low power mode, the output capacitance of the switch 104 is fully discharged. After discharging the output capacitance of the switch 104, the controller determines if the output power provided to the load 121 exceeds a required minimum power. If the output power does exceed a required minimum, the output capacitance of the switch 104 is discharged less in the next switching cycle. If, for any given switching cycle, the output power does not exceed the required minimum, a second pulse is immediately provided in the same switching cycle by increasing the amount that the output capacitance of the switch 104 is discharged. If the second pulse results in the output power provided to the load 121 exceeding the required minimum, then the second pulse is stored, and the output capacitance of the switch 104 is discharged at the level that produced the second pulse for all switching cycles for the remainder of operation in low power mode. If the second pulse does not result in the output power provided to the load 121 exceeding the required minimum, then the power converter 100 exits low power mode.

Fig. 2a is a graph illustrating the output current provided to a load when the output capacitance of a switch is fully discharged, according to one embodiment. In the embodiment of Fig. 2a, the controller 102 provides a pulse signal to the gate of the switch 104 (the switch control signal 106, or Vg, of Fig. 1). The magnitude of the pulse of Vg causes the output capacitance of the switch 104 (the drain voltage Vd of Fig. 1) to fully drain, and the output current (lout of Fig. 1) to rise to a first magnitude.

Figs. 2b and 2c are graphs illustrating the output current provided to a load when the output capacitance of a switch is only partially discharged, according to one embodiment. In the embodiment of Fig. 2b, the controller 102 provides a pulse signal Vg that is lower in magnitude than the pulse signal Vg of Fig. 2a, causing the output capacitance of the switch 104 to be partially discharged, and the output current lout to rise to a second magnitude less than the first magnitude of Fig. 2a. In the embodiment of Fig. 2c, the controller 102 provides a pulse signal Vg that is lower in magnitude than the pulse signal Vg of Fig. 2b, causing the output capacitance of the switch 104 to be discharged less than in the embodiment of Fig. 2b, and the output current lout to rise to a third magnitude less than the second magnitude of Fig. 2b.
The embodiments of Figs. 2a-2c can represent an implementation of an algorithm by the controller 102 to reduce the energy per pulse provided by the power converter 100 as described herein. In the event that the power converter 100 enters a low power mode, the controller 102 provides a pulse that fully discharges the output capacitance of the switch 104 in a first switching cycle. In this example, the first switching cycle is illustrated by Fig. 2a. If the output power (represented by lout of Fig. 2a) provided to the load 121 exceeds a minimum power required by the load, then the controller 102 proceeds to a second switching cycle.

In the second switching cycle, the controller provides a pulse that discharges the output capacitance of the switch 104 less than in the first switching cycle. In this example, the second switching cycle is illustrated by Fig. 2b. If the output power provided to the load 121 exceeds the minimum power threshold, then the controller 102 proceeds to a third switching cycle. In the third switching cycle, the controller provides a pulse that discharges the output capacitance of the switch 104 less than in the second switching cycle. In this example, the third switching cycle is illustrated by Fig. 3b. If, during any switching cycle, the output of power provided to the load 121 does not exceed a required minimum power threshold, a second pulse is provided in the same switching cycle that discharges the more than the first pulse of the switching cycle. If the second pulse results in an output power provided to the load that exceeds the minimum power threshold, then the second pulse is saved (for instance at the controller 121 in a non-transitory computer-readable storage medium), and the same pulse is provided for all switching cycles for the remainder of operation in the low power mode. For example, if the power provided in the third cycle illustrated in Fig. 2c (the output current lout multiplied by the voltage provided to the load) does not exceed the required minimum threshold, the controller can discharge the output capacitance of the switch 104 more than in the embodiment of Fig. 2c (for instance, the output capacitance of the switch can be discharged by an amount equal to or less than in the second switching cycle illustrated in Fig. 2b but greater than in the third switching cycle illustrated in Fig. 2c).

To vary the amount that the output capacitance of the switch 104 is discharged, the controller 102 can vary the magnitude of the signal Vg provided to the gate node of the switch. In the embodiment of Fig 1, the controller 121 can determine the amount of output power provided to the load 121 based on the signals VSEN or ISENS, 114. In other embodiments, the power converter 100 can include a power sensor component or circuit.
coupled to the auxiliary winding Na of the transformer T1. In such embodiments, the power sensor component or circuit can be configured to determine an amount of power provided to the load 121, and to provide an indication of the determined amount of power to the controller 102. In some embodiments, the controller 102 can compare the power provided to the load 121 to a minimum threshold required by the load as described herein. Alternatively, a power sensor component or circuit coupled to the auxiliary winding Na of the transformer T1 can determine an amount of power provided to the load 121, can compare the determined amount of power to a minimum threshold required by the load, and can provide an indication of the determination to the controller 102. In response, the controller 102 can control the switching of the switch 104 based on the received indication of the determination of whether the output power exceeds the required minimum threshold as described herein.

[0031] Upon identifying a pulse that, when provided by the controller 102 to the switch 104, results in a reduced amount of power being provided to the load 121 while exceeding the minimum power required by the load (also referred to as an "optimized pulse" hereinafter), the controller can provide the identified pulse to the switch for the remainder of the low power mode. During operation in the low power mode, the amount of power provided to the load can be continually monitored, for instance during each switching cycle. If, during a switching cycle, the monitored amount of output power falls below the minimum required threshold, a second pulse can be immediately generated within the switching cycle, either at the same power or at an increased power (such that the second pulse discharges the output capacitance of the switch 104 more than the first pulse). If the second pulse does not cause power provided to the load to exceed the minimum threshold, the power converter 100 can exit the low power mode (and, for example, resume normal operation).

[0032] It should be noted that in addition to identifying an optimized gate pulse for a MOSFET switch for operation in a low power mode by successively reducing the amount of energy provided to a load coupled to a power converter, an optimized pulse can be identified by successively increasing an amount of energy provided to the load. For instance, upon entering a low power mode or a training mode, a first pulse can be provided to a MOSFET gate. The first pulse can be associated with a first output energy provided to a load that is below a threshold energy required by the load. In response to determining that the first output energy is less than the required threshold output energy, a second pulse can be provided to the MOSFET gate, the second pulse associated with a second output energy greater than the first output energy. In response to determining that the second output energy is below the
required threshold output energy, a third pulse associated with a third output energy greater
than the second output energy can be provided to the MOSFET gate. This process is iterated
until a pulse associated with an output energy greater than the threshold output energy (the
"optimized pulse") is identified. As noted above, optimized pulses can be stored for
subsequent use in controller a MOSFET switch when operating in a low power mode.

[0033] Fig. 3 is a flow chart illustrating a process for reducing the energy per pulse
provided by a power converter in a low power mode, according to one embodiment. A power
supply, such as a flyback switching power supply, enters 300 a low power mode, for instance
in response to a determination that a load coupled to the supply will remain constant for an
upcoming period of time. A driver pulse is generated 302 at a maximum power (a
predetermined power guaranteed to provide a suitable amount of output power to a load). For
example, a controller generates a gate signal for a MOSFET switch of a flyback switching
power supply such that the output capacitance from the drain node of the switch to the source
node of the switch is completely drained.

[0034] In the next switching cycle, a driver pulse is generated 304 at a power lower than
the previous pulse (in this case, the maximum power). The amount of power provided to the
load coupled to the power supply in response to the driver pulse is determined, and is
compared 306 to a pre-determined minimum power threshold required by the load. In
response to a determination 308 that the determined amount of power exceeds the threshold,
a driver pulse is generated in the next switching cycle at a lower power than the previous
pulse. The cycle is repeated until the power provided to the load in response to a generated
driver pulse does not exceed the minimum threshold required by the load.

[0035] In response to a determination 308 that the determined amount of power does not
exceed the minimum threshold, a second pulse is immediately generated 310 within the same
switching cycle at a higher power than the previous pulse within the switching cycle. The
power provided to the load resulting from the second pulse is compared 312 to the minimum
threshold. In response to a determination 314 that the power provided to the load by the
second pulse exceeds the threshold, the second pulse is stored 316 for use for the remainder
of the low power mode. In response to a determination 314 that the power provided to the
load by the second pulse does not exceed the threshold, the power supply exists 318 the low
power mode.

[0036] Upon reading this disclosure, those of skill in the art will appreciate still
additional alternative embodiments through the disclosed principles herein. Thus, while
particular embodiments and applications have been illustrated and described, it is to be understood that the disclosed embodiments are not limited to the precise construction and components disclosed herein. Various modifications, changes and variations, which will be apparent to those skilled in the art, may be made in the arrangement, operation and details of the method and apparatus disclosed herein without departing from the spirit and scope described herein.
What is claimed is:

1. A method for operating a flyback switching power converter coupled to a load, the power converter comprising a MOSFET switch and a controller coupled to the MOSFET switch, comprising:
   - configuring the power converter to operate in a low power mode;
   - generating, by the controller, a first driver pulse, an amplitude of the first driver pulse configured to partially discharge an output capacitance of the MOSFET switch; and
   - generating, by the controller, a second driver pulse, an amplitude of the second driver pulse based on a feedback control signal representative of a voltage provided to the load.

2. The method of claim 1, wherein the amplitude of the first driver pulse and the amplitude of the second driver pulse exceed a pre-defined value.

3. The method of claim 2, wherein the pre-defined value is determined in advance by adjusting the amplitude of driver pulses provided to the MOSFET switch until an optimized driver pulse associated with a pre-defined threshold voltage provided to the load is determined, the pre-defined value representative of the amplitude of the optimized driver pulse.

4. The method of claim 3, wherein the optimized driver pulse is determined by:
   - generating a third driver pulse configured to discharge the output capacitance of the MOSFET switch by a first amount and to provide a first amount of output power to the load coupled to the power converter, the first amount of output power exceeding a minimum power threshold required by the load; and
   - generating a fourth driver pulse configured to discharge the output capacitance of the MOSFET switch by a second amount less than the first amount and to provide a second amount of output power to the load, the second amount of output power less than the first amount of output power;
   - wherein the optimized driver pulse comprises the third driver pulse in response to a determination that the second amount of output power does not exceed the minimum power threshold.
5. The method of claim 3, wherein the optimized driver pulse is determined by:
   generating a third driver pulse configured to discharge the output capacitance of the
   MOSFET switch by a first amount and to provide a first amount of output
   power to the load coupled to the power converter; and
   responsive to a determination that the first amount of output power does not exceed a
   minimum power threshold required by the load, generating a fourth driver
   pulse configured to discharge the output capacitance of the MOSFET switch
   by a second amount greater than the first amount and to provide a second
   amount of output power to the load, the second amount of output power
   greater than the first amount of output power;
   wherein the optimized driver pulse comprises the fourth driver pulse in response to a
   determination that the second amount of output power exceeds the minimum
   power threshold.

6. The method of claim 1, wherein the MOSFET switch is configured to operate at a fixed
   on-time while receiving driver pulses of adjusted drive power when the power converter is
   configured in the low power mode.

7. A flyback switching power converter circuit, comprising:
   a MOSFET switch;
   a transformer coupled to the MOSFET switch and to a load; and
   a controller coupled to a gate node of the MOSFET switch, the controller configured
   to, when operating in a low power mode:
   generate a first driver pulse, an amplitude of the first driver pulse configured
   to partially discharge an output capacitance of the MOSFET switch;
   and
   generate a second driver pulse, an amplitude of the second driver pulse based
   on a feedback control signal representative of a voltage provided to the
   load.

8. The power converter circuit of claim 7, wherein the amplitude of the first driver pulse and
   the amplitude of the second driver pulse exceed a pre-defined value.

9. The power converter circuit of claim 8, wherein the pre-defined value is determined in
   advance by adjusting the amplitude of driver pulses provided to the MOSFET switch until an
optimized driver pulse associated with a pre-defined threshold voltage provided to the load is determined, the pre-defined value representative of the amplitude of the optimized driver pulse.

10. The power converter circuit of claim 9, wherein the optimized driver pulse is determined by:

   generating a third driver pulse configured to discharge the output capacitance of the MOSFET switch by a first amount and to provide a first amount of output power to the load, the first amount of output power exceeding a minimum power threshold required by the load; and

   generating a fourth driver pulse configured to discharge the output capacitance of the MOSFET switch by a second amount less than the first amount and to provide a second amount of output power to the load, the second amount of output power less than the first amount of output power;

   wherein the optimized driver pulse comprises the third driver pulse in response to a determination that the second amount of output power does not exceed the minimum power threshold.

11. The power converter circuit of claim 9, wherein the optimized driver pulse is determined by:

   generating a third driver pulse configured to discharge the output capacitance of the MOSFET switch by a first amount and to provide a first amount of output power to the load coupled to the power converter; and

   responsive to a determination that the first amount of output power does not exceed a minimum power threshold required by the load, generating a fourth driver pulse configured to discharge the output capacitance of the MOSFET switch by a second amount greater than the first amount and to provide a second amount of output power to the load, the second amount of output power greater than the first amount of output power;

   wherein the optimized driver pulse comprises the fourth driver pulse in response to a determination that the second amount of output power exceeds the minimum power threshold.
12. The power converter circuit of claim 7, wherein the MOSFET switch is configured to operate at a fixed on-time while receiving driver pulses of adjusted drive power when the converter is configured to operate in the low power mode.

13. A method for operating a flyback switching power converter, comprising:
   configuring the power converter to operate in a low power mode;
   generating a first driver pulse configured to discharge an output capacitance of a switch of the power converter by a first amount and to provide a first amount of output power to a load coupled to the power converter, the first amount of output power exceeding a minimum power threshold required by the load;
   generating a second driver pulse configured to discharge the output capacitance of the switch by a second amount less than the first amount and to provide a second amount of output power to the load, the second amount of output power less than the first amount of output power;
   responsive to a determination that the second amount of output power does not exceed the minimum power threshold, generating a third driver pulse configured to discharge the output capacitance of the switch by a third amount greater than the second amount and to provide a third amount of output power to the load, the third amount of output power greater than the second amount of output power;
   responsive to a determination that the third amount of output power exceeds the minimum power threshold, storing the third driver pulse for use during the remainder of the low power mode; and
   responsive to a determination that the third amount of output power does not exceed the minimum power threshold, configuring the power converter to stop operation in the low power mode.

14. The method of claim 13, wherein the switch comprises a MOSFET switch, and wherein the first driver pulse, the second driver pulse, and the third driver pulse are generated by a controller coupled to the gate node of the MOSFET switch.

15. The method of claim 14, wherein each driver pulse configures the MOSFET switch to operate as a closed switch.
16. The method of claim 15, wherein a primary winding of a transformer is coupled to the MOSFET switch, and wherein current flowing through the primary winding when the MOSFET switch is configured to operate as a closed switch causes current to flow through a secondary winding of the transformer coupled to the load.

17. The method of claim 16, wherein an auxiliary winding of the transformer is coupled to the controller, and wherein the controller is configured to determine amounts of output power provided to the load in response to a current flowing through auxiliary winding of the transformer.

18. The method of claim 13, further comprising:

after storing the third driver pulse, for each switching cycle in which the power converter is configured to operate in the low power mode:

- generating a first driver pulse for the switching cycle based on the stored third driver pulse;
- determining a first amount of power for the switching cycle provided to the load in response to the generated first driver pulse for the switching cycle;

in response to a determination that the determined first amount of power for the switching cycle does not exceed the minimum power threshold, generating a second driver pulse for the switching cycle within the same switching cycle;

- determining a second amount of power for the switch cycle provided to the load in response to the generated second driver pulse for the switching cycle; and

in response to a determination that the determined second amount of power for the switching cycle does not exceed the minimum power threshold, configuring the power converter to stop operation in the low power mode.

19. The method of claim 18, wherein the second driver pulse for the switching cycle discharges the output capacitance of the switch by the same amount as the first driver pulse for the switching cycle.
20. The method of claim 18, wherein the second driver pulse for the switching cycle discharges the output capacitance of the switch by a greater amount than the first driver pulse for the switching cycle.

21. The method of claim 20, further comprising:
   in response to a determination that the determined second amount of power for the switching cycle exceeds the minimum power threshold, generating a driver pulse for each subsequent switching cycle in which the power converter is configured to operate in the low power mode based on the generated second driver pulse for the switching cycle.

22. A power supply circuit, comprising:
   a switch;
   a transformer coupled to the switch and to a load;
   a controller coupled to the switch, the controller configured to, in a training mode:
      generate a pulse;
      determine an amount of power provided to the load in response to each generated pulse;
      in response to the determined amount of power not exceeding a minimum power threshold required by the load, generate a second pulse causing a greater amount of power to be provided to the load; and
      in response to the greater amount of power exceeding the minimum power threshold, storing the second pulse, the controller configured to generate pulses in subsequent switching cycles based on the stored second pulse.

23. The power supply circuit of claim 22, further comprising a power detection circuit coupled to the controller and configured to provide, to the controller, an indication of output power provided to the load in response to a generated pulse.

24. The power supply circuit of claim 23, wherein the power detection circuit is coupled to an auxiliary winding of the transformer.

25. A power supply circuit, comprising:
   a switch;
   a transformer coupled to the switch and to a load;
a controller coupled to the switch, the controller configured to, in a training mode:
  generate a first pulse;
  determine an amount of power provided to the load in response to each
  generated pulse;
  in response to the determined amount of power exceeding a minimum power
  threshold required by the load, generate a second pulse causing a lesser
  amount of power to be provided to the load; and
  in response to the lesser amount of power not exceeding the minimum power
  threshold, storing the first pulse, the controller configured to generate
  pulses in subsequent switching cycles based on the stored first pulse.

26. The power supply circuit of claim 25, further comprising a power detection circuit
  coupled to the controller and configured to provide, to the controller, an indication of output
  power provided to the load in response to a generated pulse.

27. The power supply circuit of claim 26, wherein the power detection circuit is coupled to an
  auxiliary winding of the transformer.
Enter low power mode 

Generate driver pulse at maximum power 

In next switching cycle, generate driver pulse at lower power than previous pulse 

Compare resulting power provided to load to pre-determined threshold 

Threshold exceeded? 

Yes 

No 

Immediately generate second driver pulse at higher power than previous pulse 

Compare resulting power provided to load to pre-determined threshold 

Threshold exceeded? 

Yes 

Store second pulse for use in remainder of low power mode 

No 

Exit low power mode 

FIG. 3
**INTERNATIONAL SEARCH REPORT**

**Classifications of Subject Matter**

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<th>IPC(8)</th>
<th>CPC</th>
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According to International Patent Classification (IPC) or to both national classification and IPC

**Fields Searched**

Minimum documentation searched (classification system followed by classification symbol)


Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSeer (US, EP, WO, JP, DE, GB, CN, FR, KR, ES, AU, IN, CA, INPADOC Data); ProQuest (Derwent, INSPEC, NTIS, PASCAL, Current Contents Search, Dissertation Abstracts Online, Inside Conferences); EBSCO Discovery Service; Google Scholar; KEYWORDS: MOSFET, metal oxide semiconductor FET, flyback", "switch", "converter", "driver"*, "pulse", "buck", "boost", "power", "load", "gate", "drive"

**Documents Considered to be Relevant**

| Category | Citation of document, with indication, where appropriate, of the relevant passages Relevant to claim No. |
|----------|-------------------------------------------------------------------------------------------------|----------------------------------|
| A        | US 2010/0157636 A1 (LI, Y et al.) June 24, 2010; abstract; figures 1 and 2B; paragraph [0121] | 1, 7, and 13                     |
| A        | US 8,049,481 B2 (LI, Y et al.) November 1, 2011; entire document | 1-21                            |

Further documents are listed in the continuation of Box C. See patent family annex.

**Date of the actual completion of the international search**

31 August 2015 (31.08.2015)

**Date of mailing of the international search report**

17 Sep 2015

**Name and mailing address of the ISA/**

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-8300

**Authorized officer**

Shane Thomas
PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)
This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. □ Claims Nos.: because they relate to subject matter not required to be searched by this Authority, namely:

2. □ Claims Nos.: because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. □ Claims Nos.: because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

This International Searching Authority found multiple inventions in this international application, as follows:

See Extra Sheet.

1. □ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. □ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. □ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

   1-21

4. □ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

   The additional search fees were accompanied by the applicant’s protest and, where applicable, the payment of a protest fee.

   The additional search fees were accompanied by the applicant’s protest but the applicable protest fee was not paid within the time limit specified in the invitation.

   No protest accompanied the payment of additional search fees.

Form PCT/ISA/2 10 (continuation of first sheet (2)) (January 2015)
This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-12 are directed towards a method for operating a flyback switching power converter using a MOSFET switch.

Group II: Claims 13-21 are directed towards a method for operating a flyback switching power converter utilizing first, second, and third driver pulses, minimum power thresholds, and stopping the operation of the power converter.

Group III: Claims 22-27 are directed towards a power supply circuit, a switch, a transformer coupled to the switch and to a load, a training mode, determining an amount of power provided to the load in response to each generated pulse, storing a pulse, and generating pulses in subsequent switching cycles based on the stored pulse.

Group I has at least a MOSFET switch with a gate node, an amplitude of the first driver pulse configured to partially discharge an output capacitance of the MOSFET switch, an amplitude of the second driver pulse based on a feedback control signal representative of a voltage provided to the load, which Groups II & III do not have. Group II has at least discharging an output capacitance of a switch of the power converter by a first amount, the first amount of output power exceeding a minimum power threshold required by the load, a second driver pulse configured to discharge the output capacitance of the switch by a second amount less than the first amount and to provide a second amount of output power to the load, the second amount of output power less than the first amount of output power, responsive to a determination that the second amount of output power does not exceed the minimum power threshold, generating a third driver pulse configured to discharge the output capacitance of the switch by a third amount greater than the second amount and to provide a third amount of output power to the load, the third amount of output power greater than the second amount of output power; responsive to a determination that the third amount of output power exceeds the minimum power threshold, storing the third driver pulse for use during the remainder of the low power mode; and responsive to a determination that the third amount of output power does not exceed the minimum power threshold, configuring the power converter to stop operation in the low power mode, which Groups I & II do not have. Group III has at least a training mode, determining an amount of power provided to the load in response to each generated pulse, storing a pulse, and generating pulses in subsequent switching cycles based on the stored pulse, which Groups I & II do not have.

The common technical features of Groups III are at least a flyback switching power converter, a load which receives power, a switch coupled to a controller, transformer coupled to the switch and to a load, a low power mode, a first pulse, a second pulse, an output capacitance of the switch. These common technical features are previously disclosed by US 8,049,481 B2 to Li, Y et al. (hereinafter "Li"). Li discloses a flyback switching power converter (a flyback switching power converter 100; abstract, figure 2A), a load which receives power (a load at node 109 which receives power; figure 2A, column 5, lines 57-65), a switch coupled to a controller (BJT power switch Q1 is coupled to controller IC 102; figure 2A, column 5, lines 37-57), transformer coupled to the switch and to a load (transformer T1-A coupled to switch Q1 and load at 109, figure 2A, column 5, lines 24-57), a low power mode (a second PFM mode which corresponds to a lower power; column 8, lines 18-32), a first pulse (a first pulse from a first PWM; column 8, lines 18-32), a second pulse (a second pulse from a second PWM; column 8, lines 18-32), an output capacitance of the switch (an output capacitance will exist for the BJT power switch Q1 between terminals, such as a collector-base capacitance; figure 2A).

Since the common technical features are previously disclosed by Li, these common features are not special and so Groups I and II lack unity.