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(continued on next page)

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(56) Documents Cited:
JP 110003955 A **US 6232659 B1**
US 4495546 A

(58) Field of Search:
INT CL **G11C, H05K**
Other: **EPODOC, WPI**

(54) Abstract Title**: Circuit module for memory expansion**

(57) A circuit module comprises a rigid, preferably thermally conductive, substrate 14, a flexible circuit 12 wrapped around an edge of the substrate, a plurality of chip scale packages (CSPs) attached to the flexible circuit and expansion board contacts 20 formed on the flexible circuit adjacent to the edge. The CSPs may be standard memory modules and are connected to the contacts 20 by means of conductive traces in the flexible circuit 16. The contacts 20 are arranged so that the circuit module may be plugged at its edge into a standard circuit board expansion slot in e.g. a computer. The substrate may assist in heat dissipation from the attached CSPs.

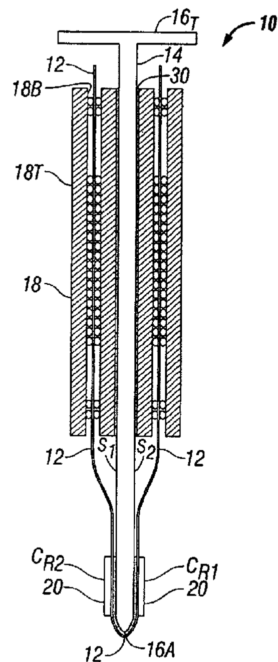

FIG. 3

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GB 2453064 A continuation

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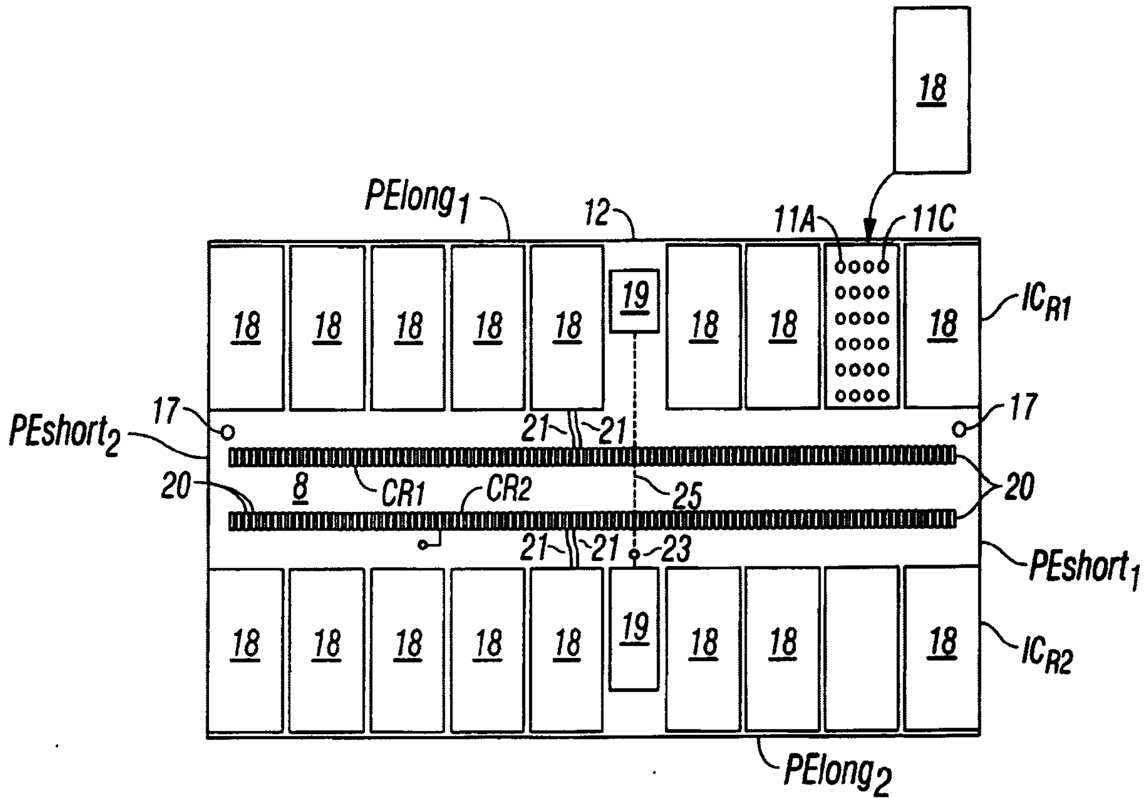


FIG. 1

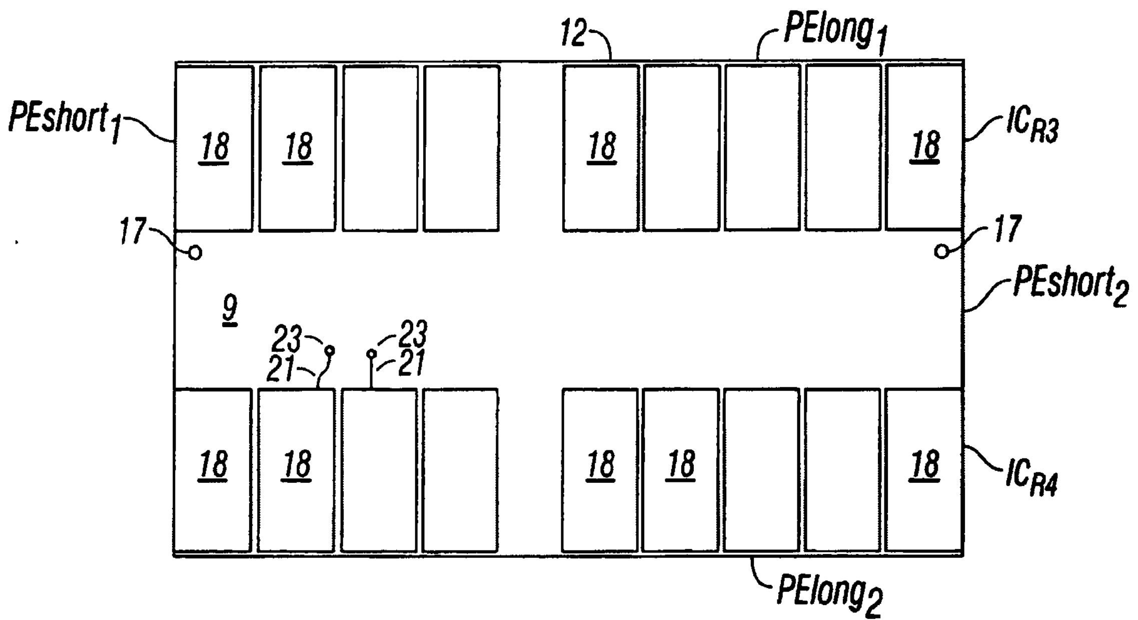


FIG. 2

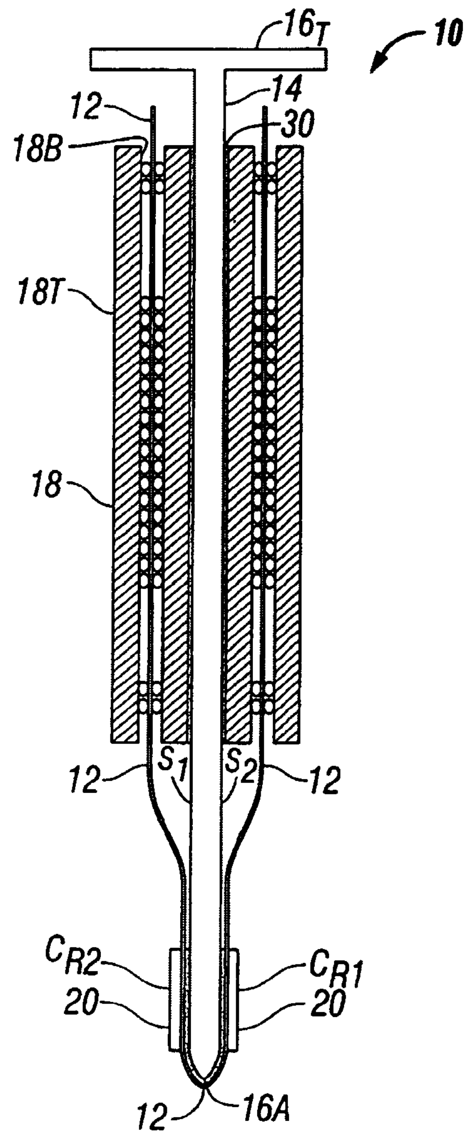
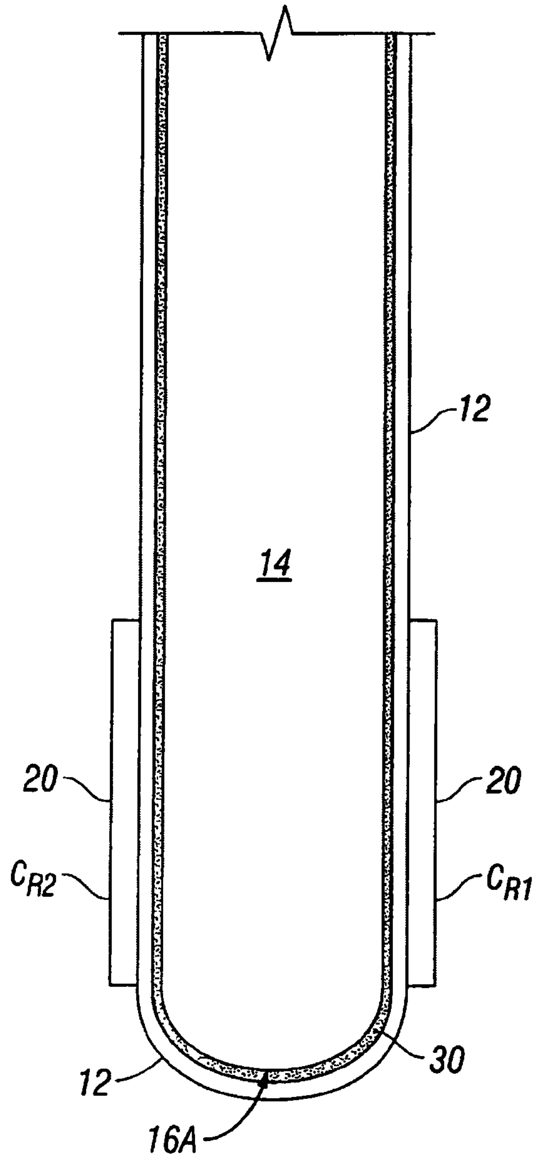


FIG._3



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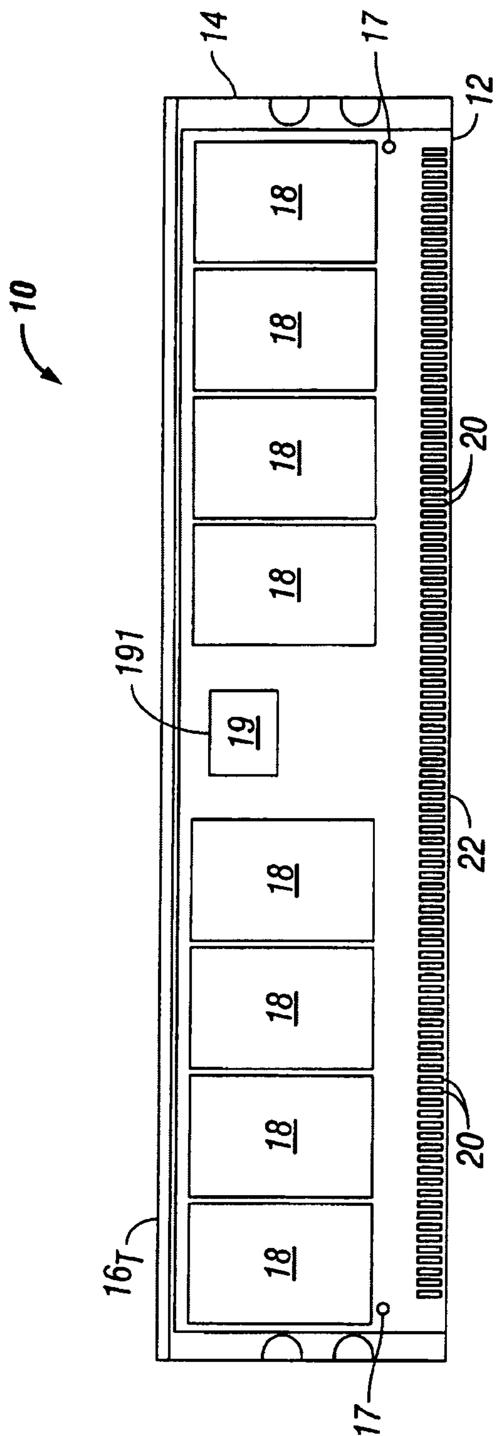
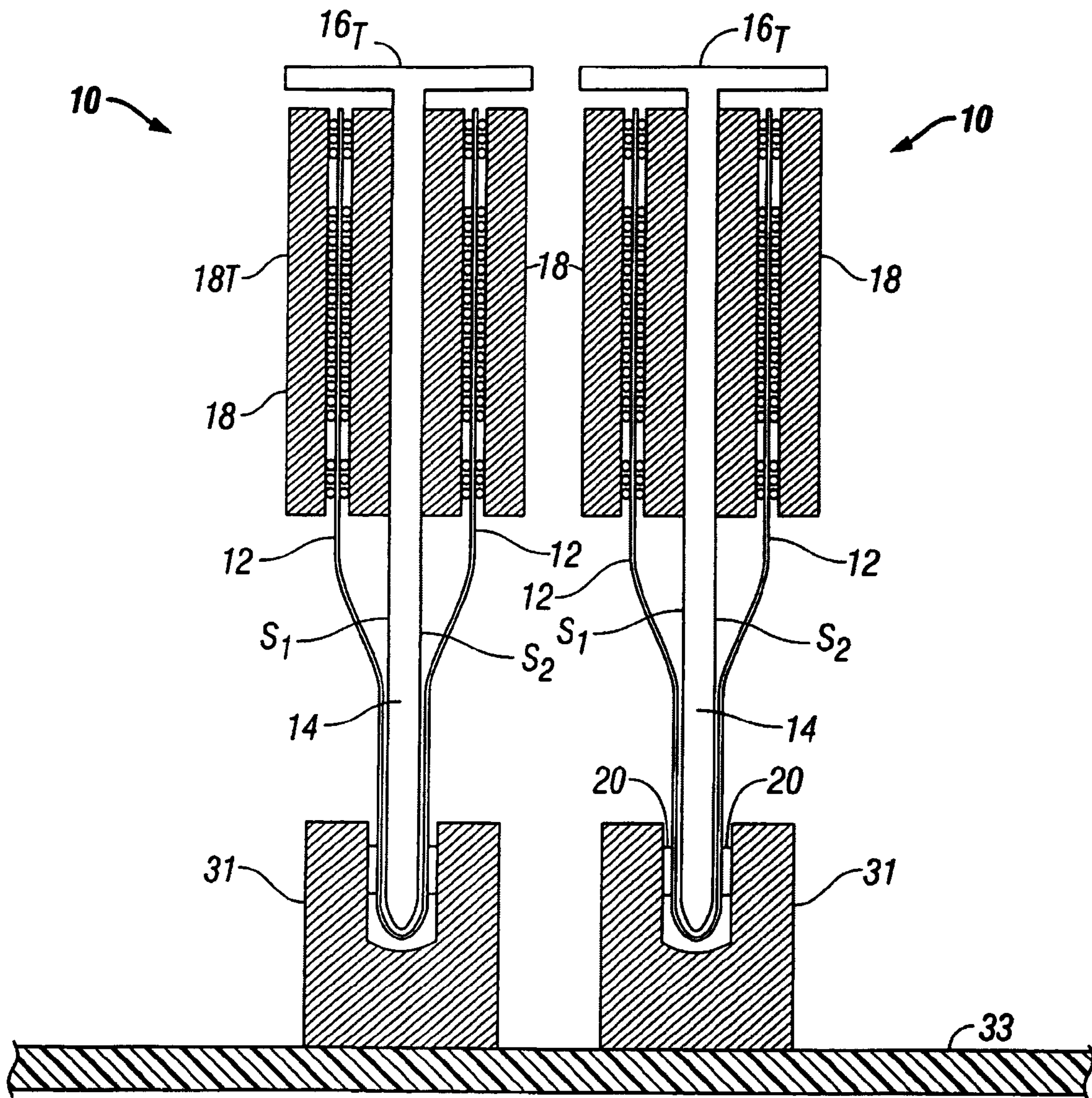


FIG. 5



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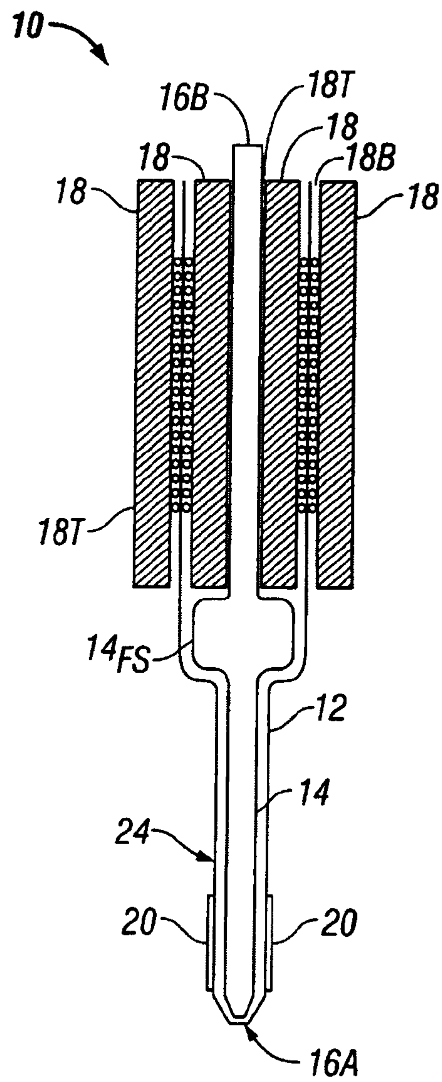


FIG. 7

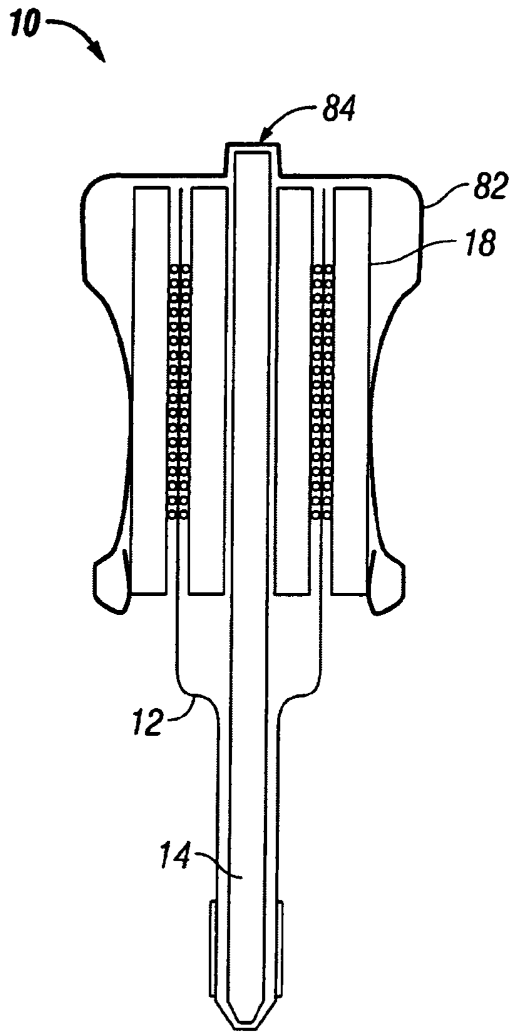


FIG. 8

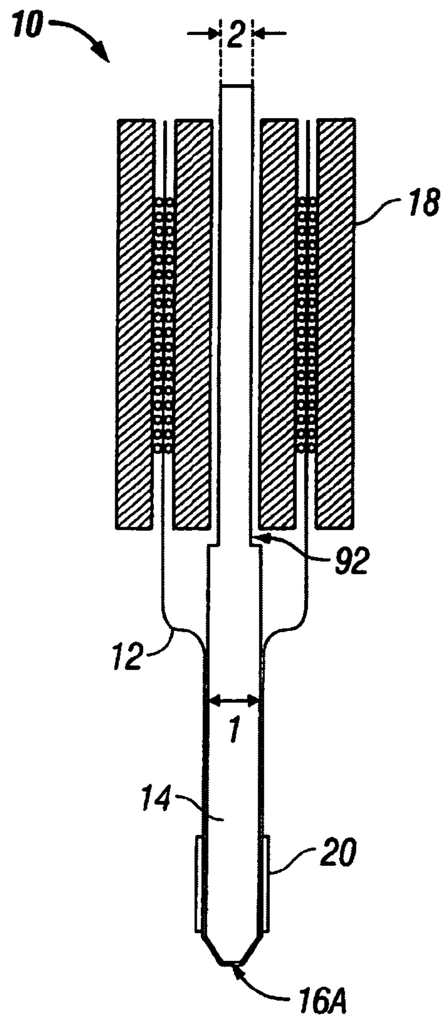
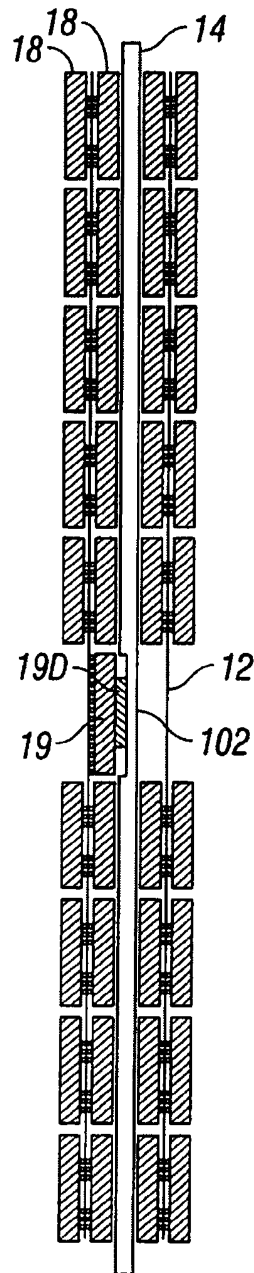


FIG. 9



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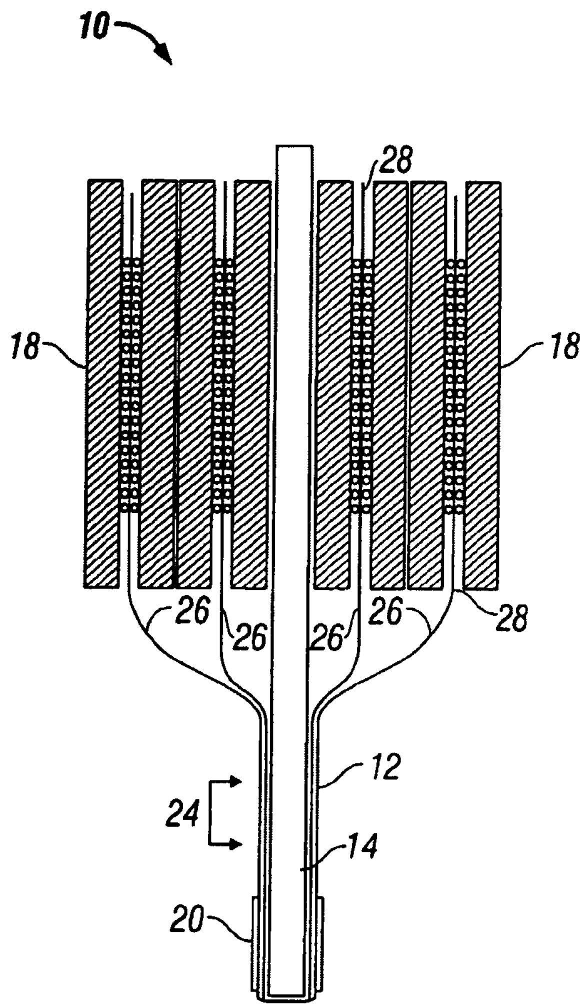

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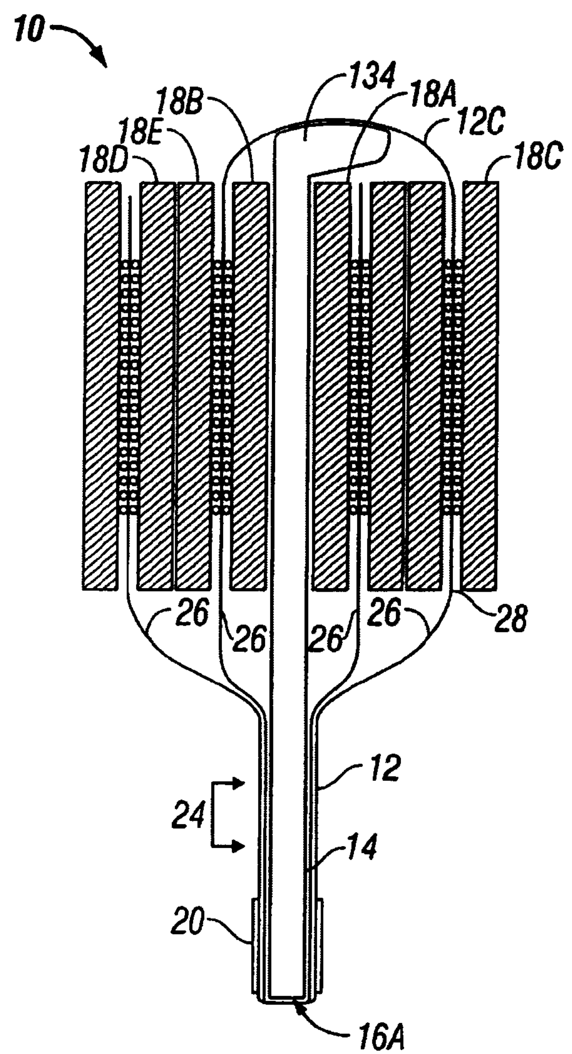


FIG. 12

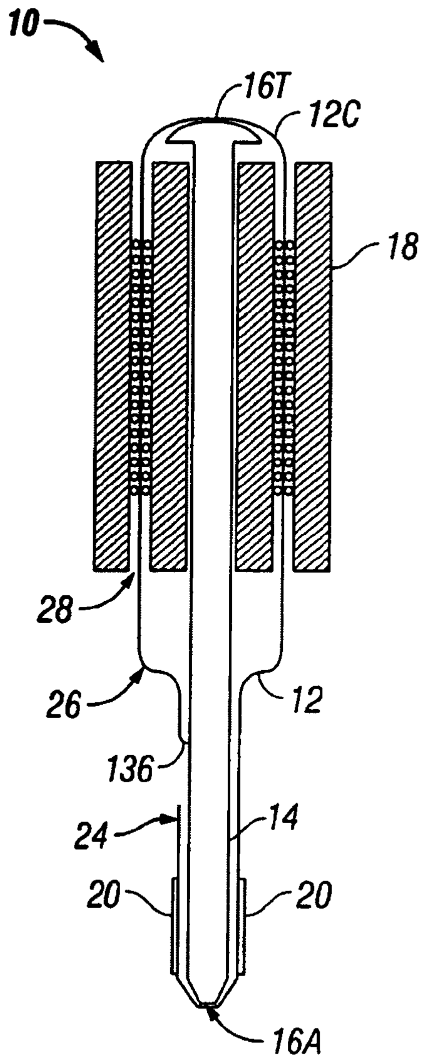


FIG._13

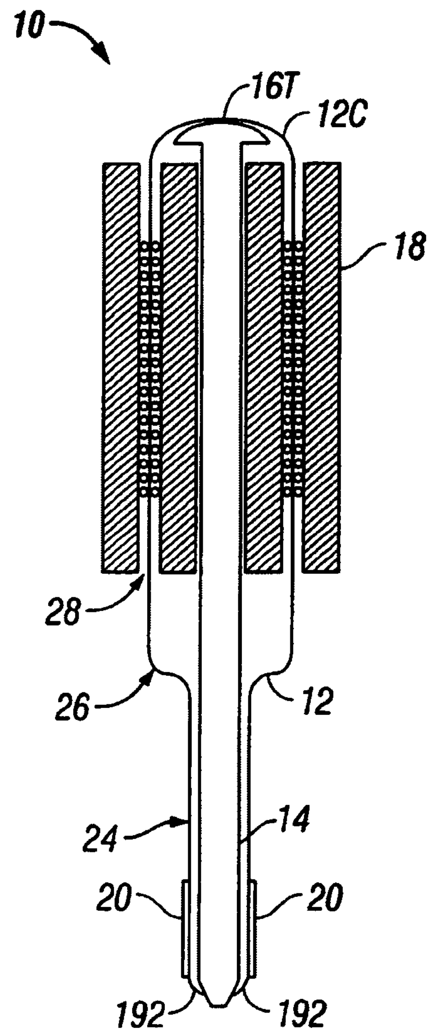


FIG. 14

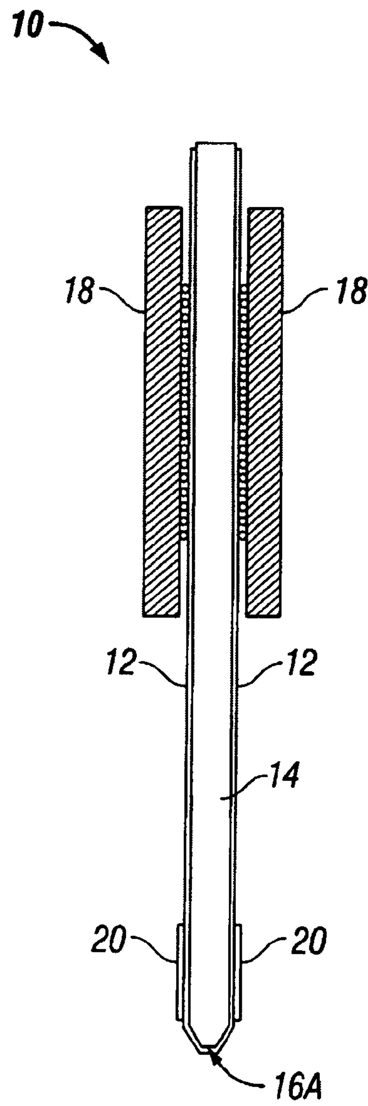


FIG. 15

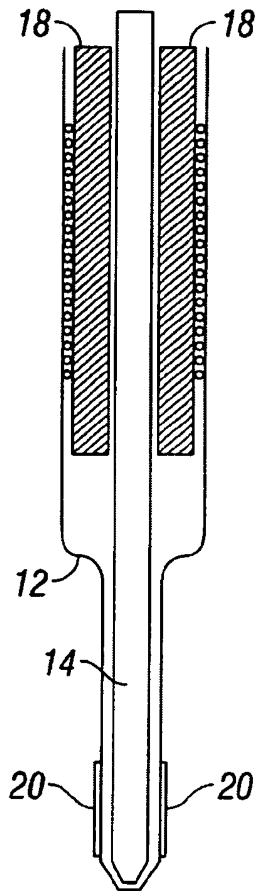


FIG._16

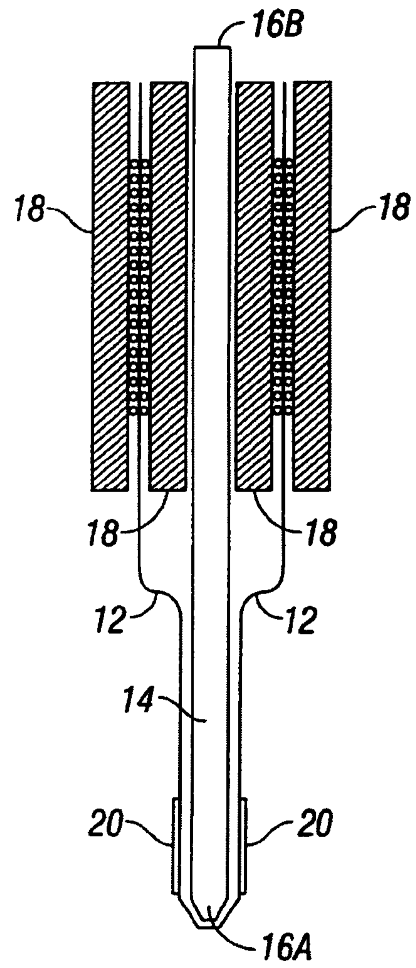


FIG._17

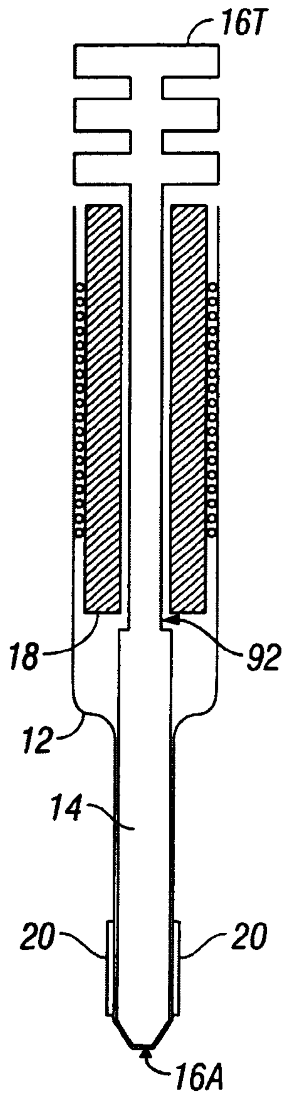


FIG. 18

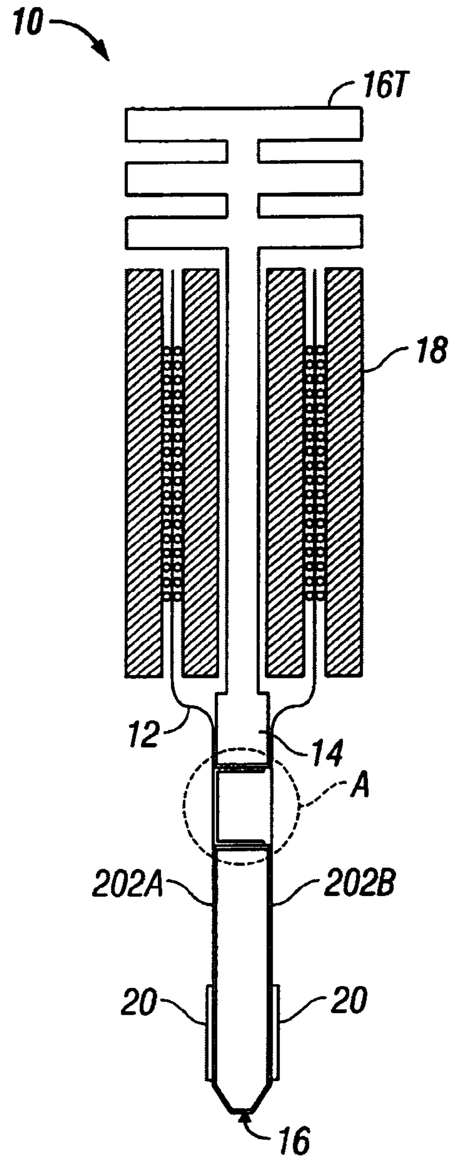


FIG. 19

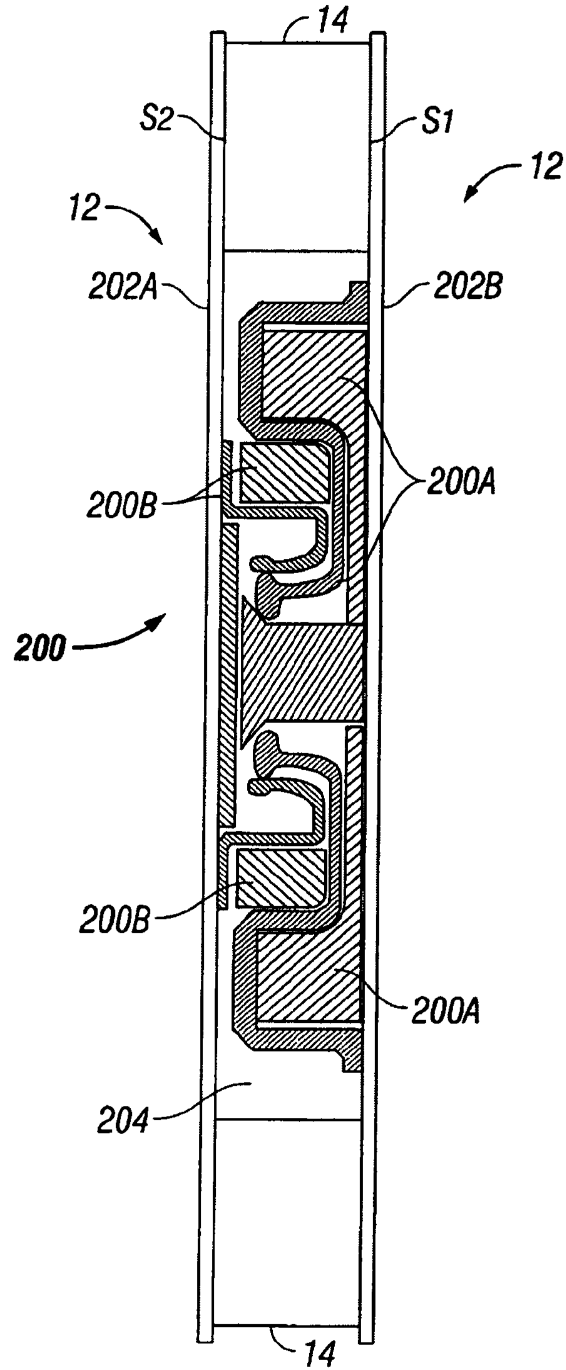
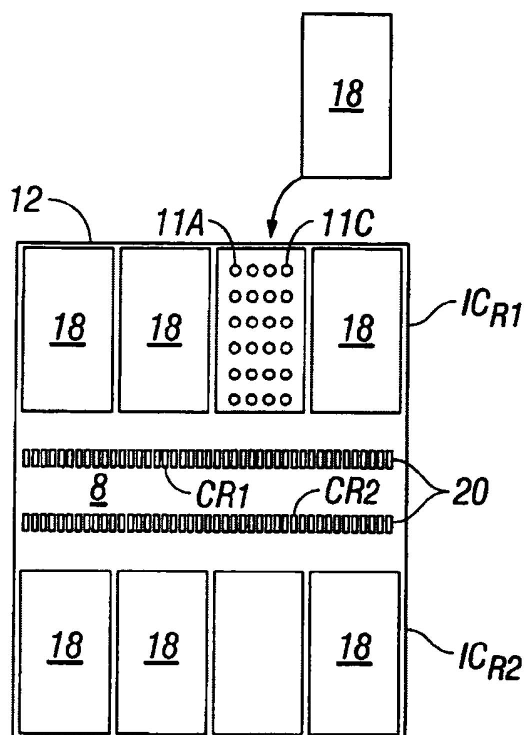


FIG._20



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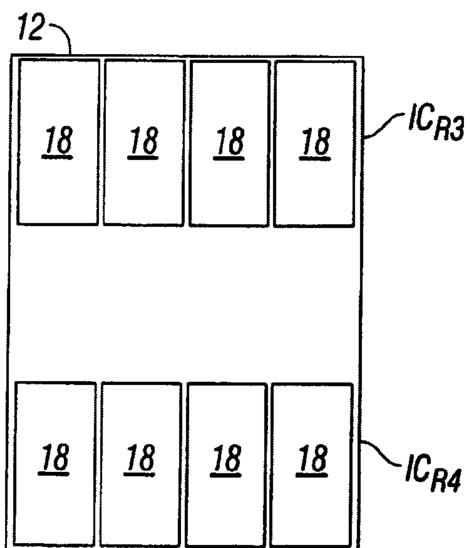

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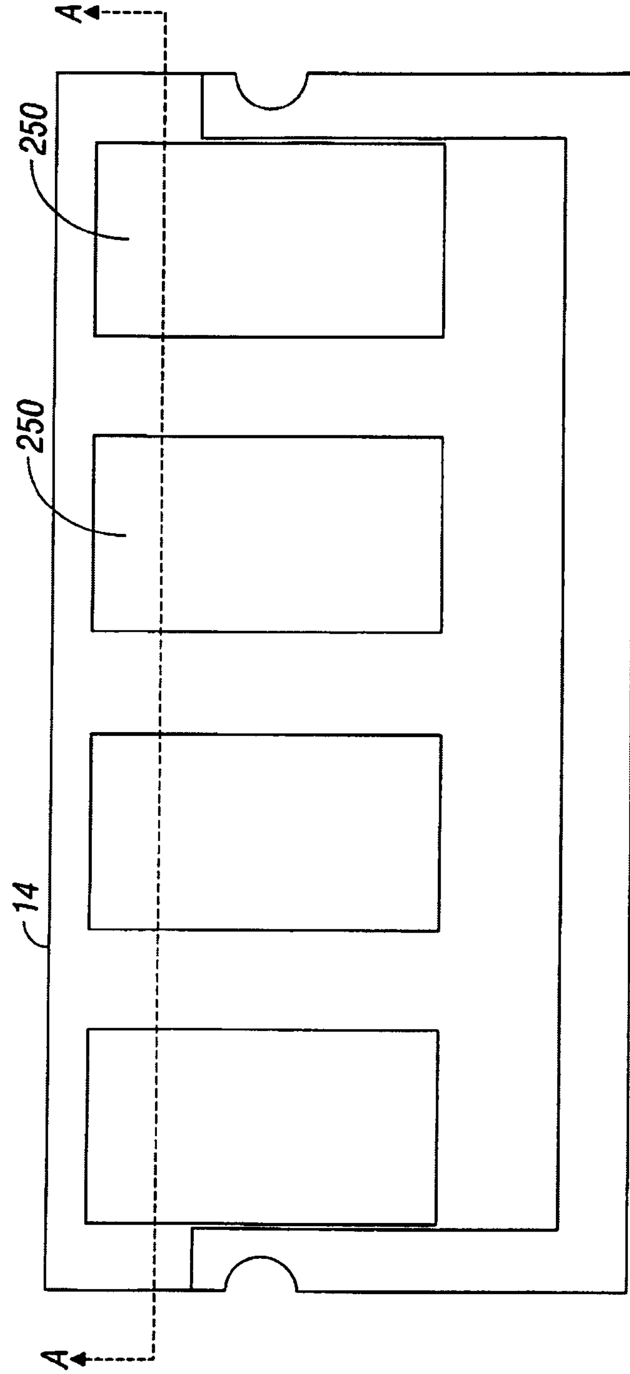

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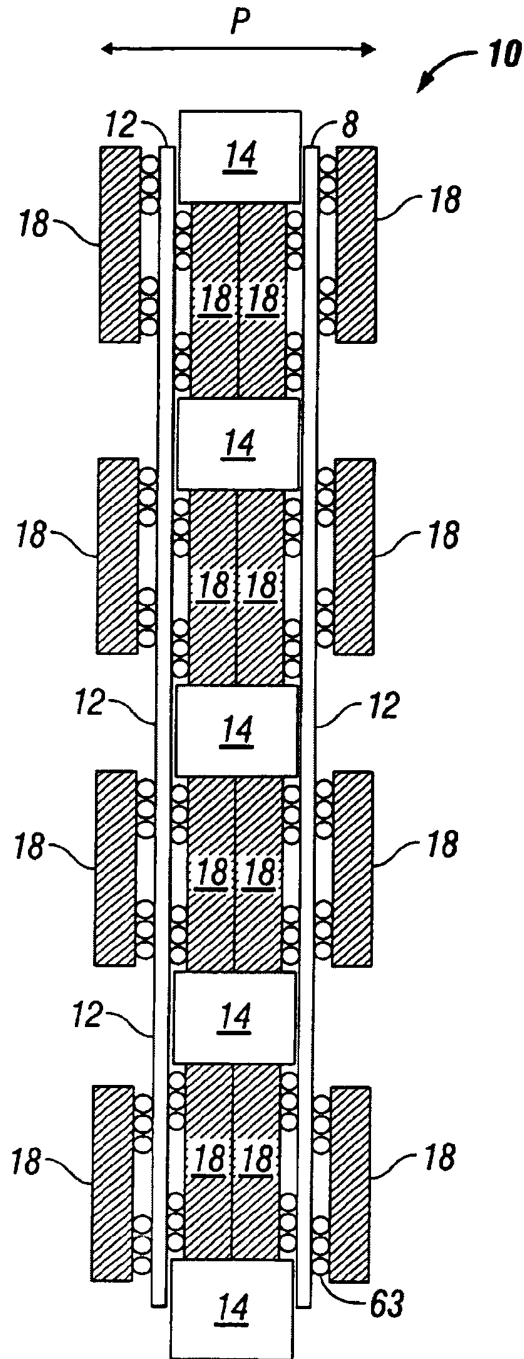
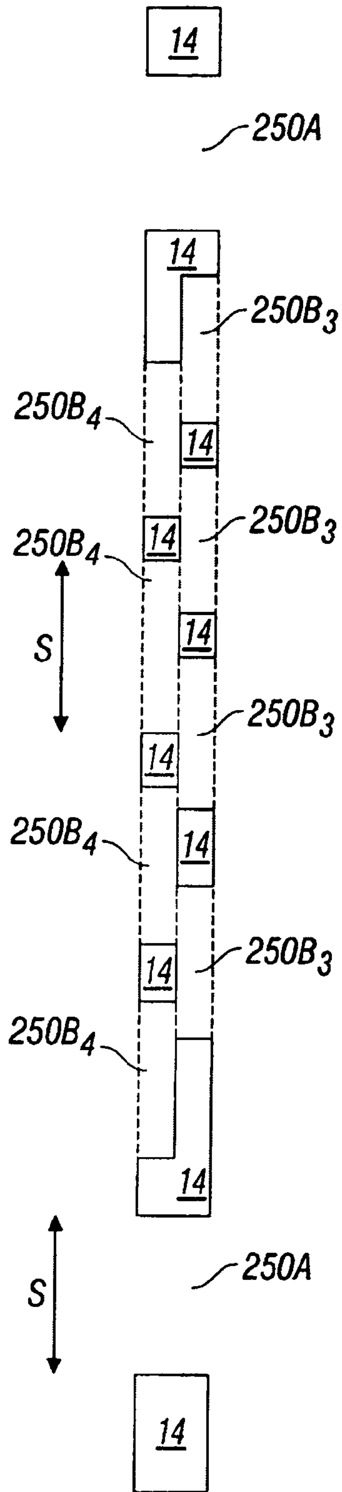


FIG. 24

FIG. 25



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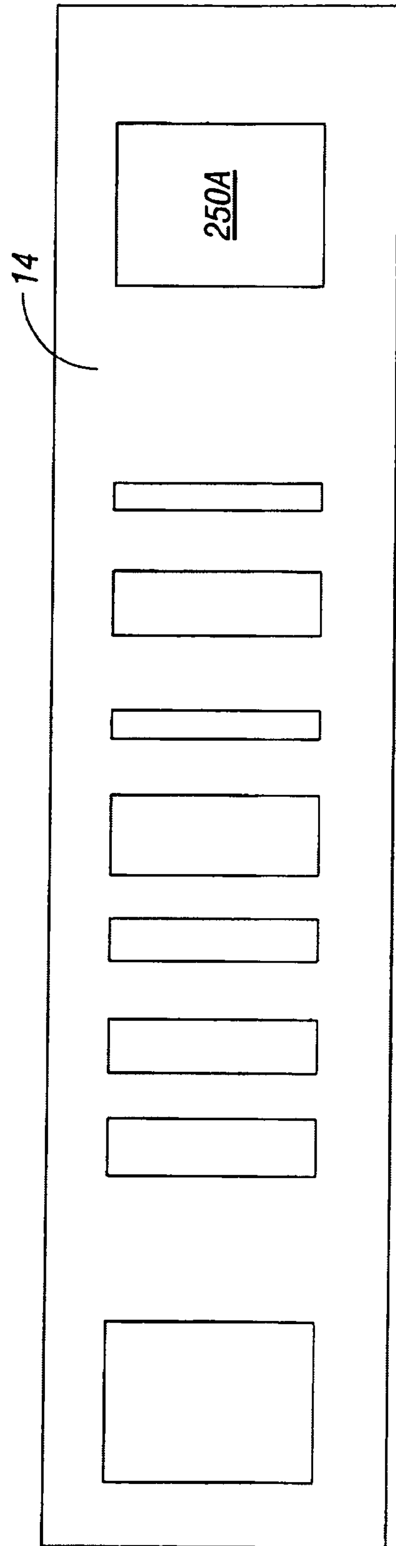

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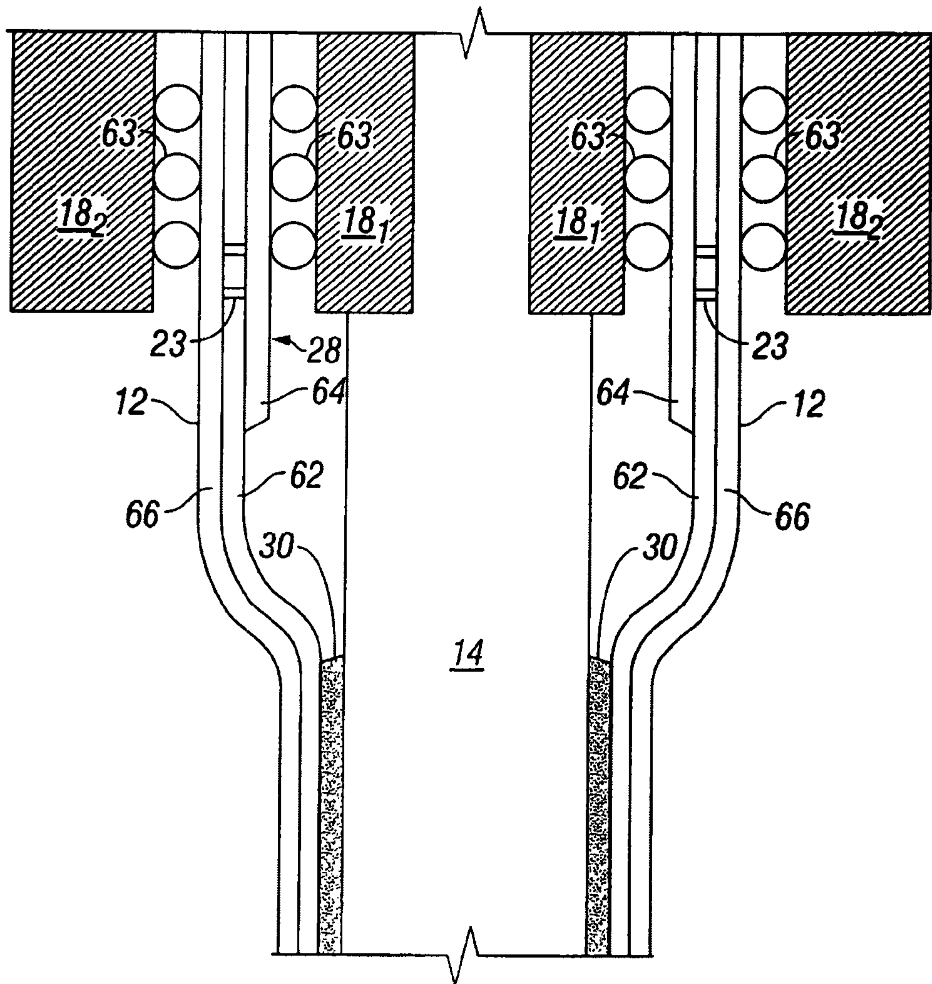

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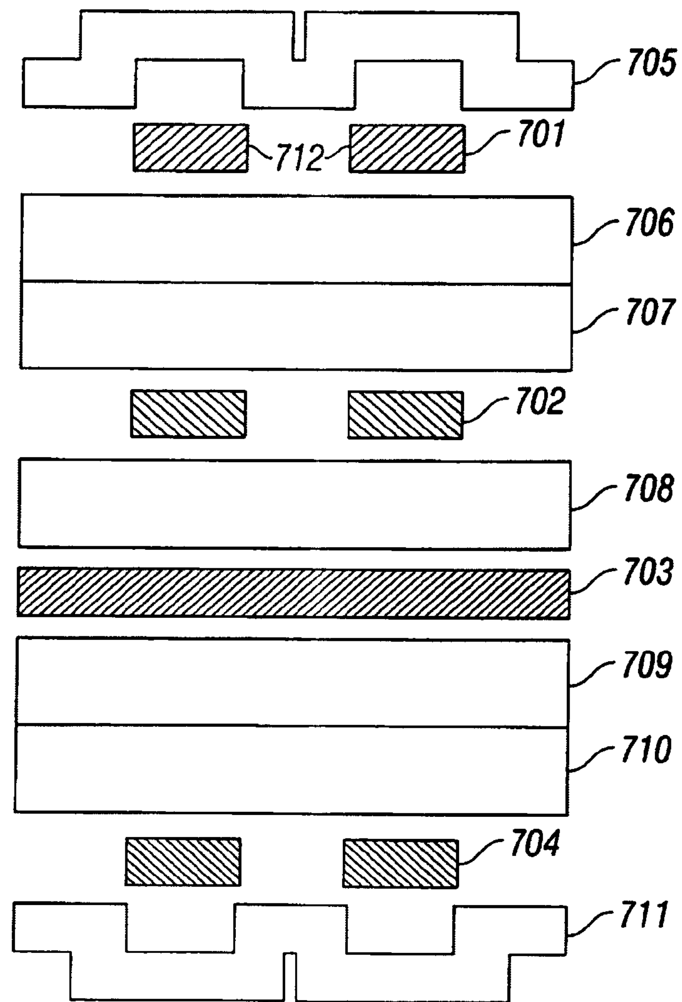

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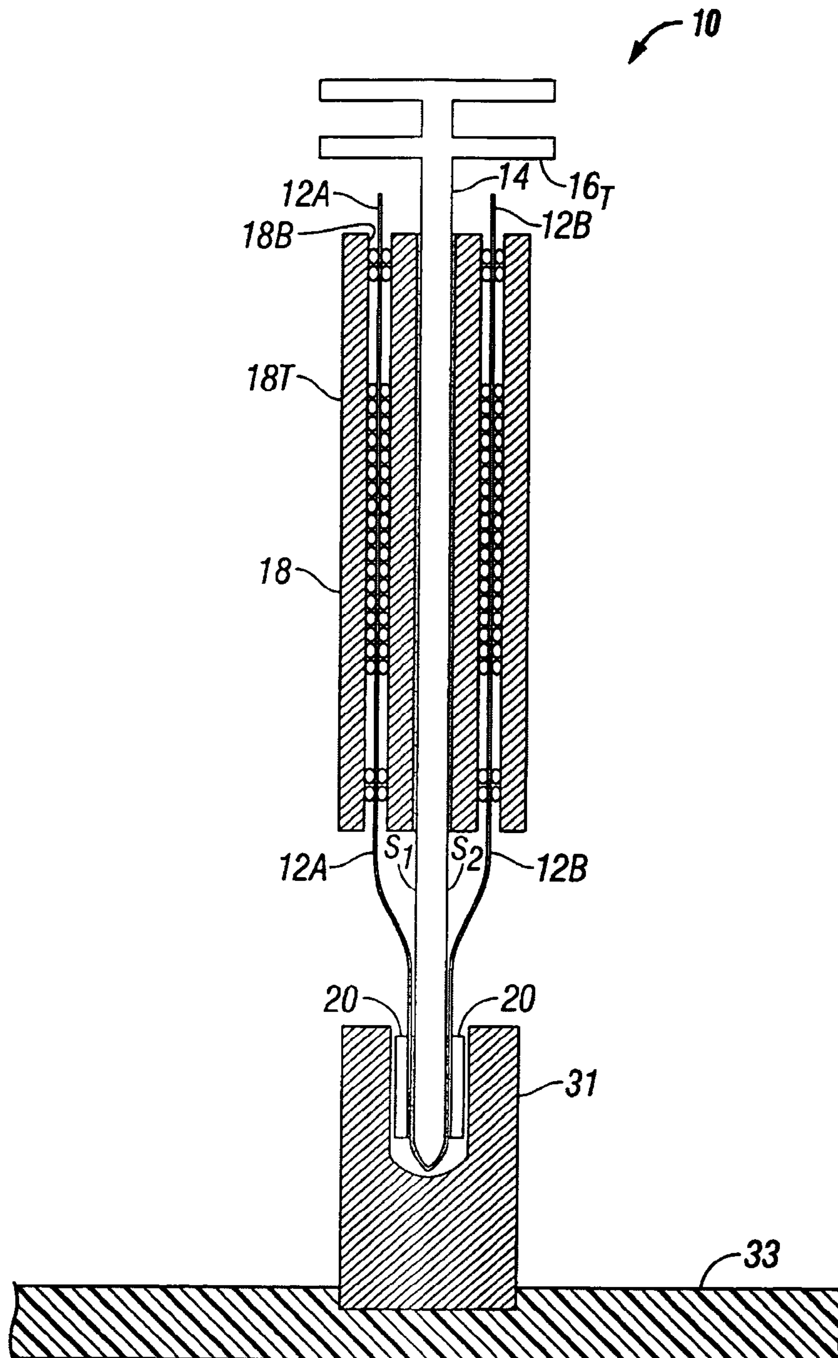


FIG._30

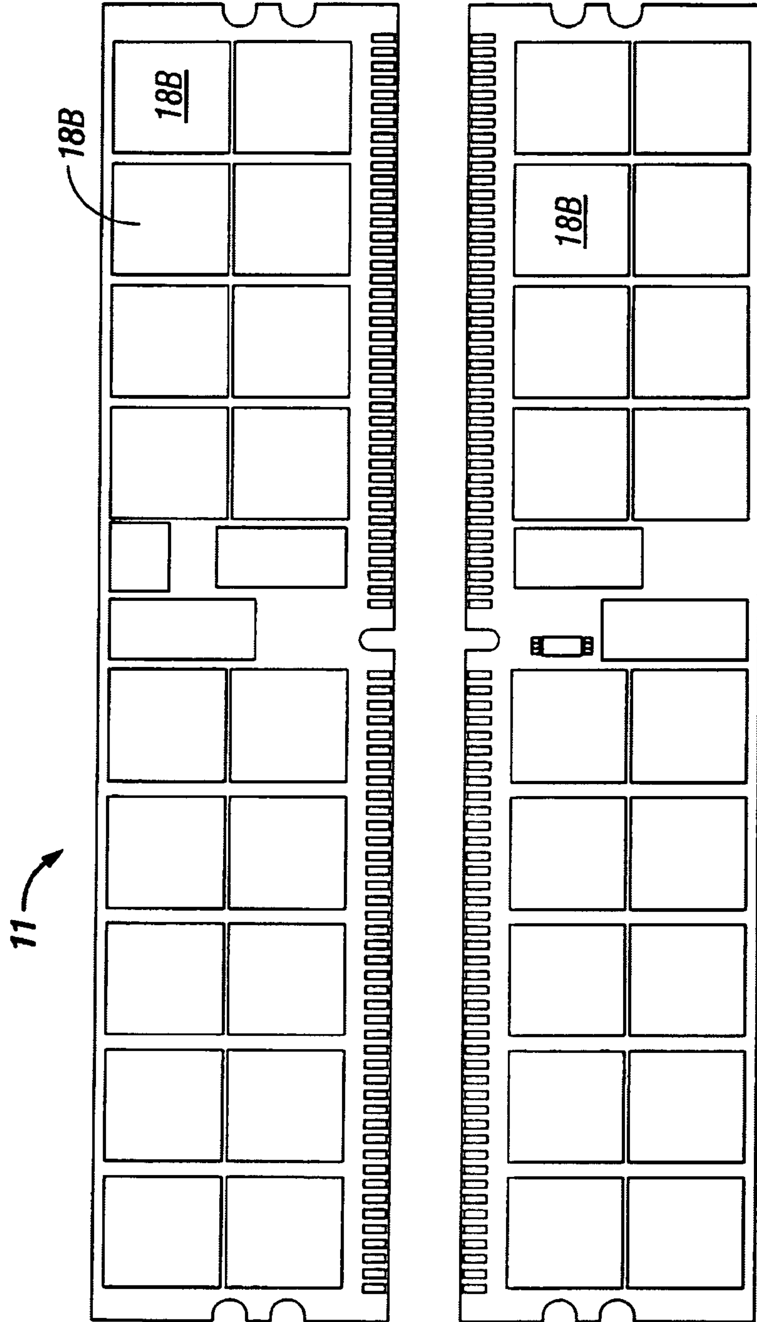
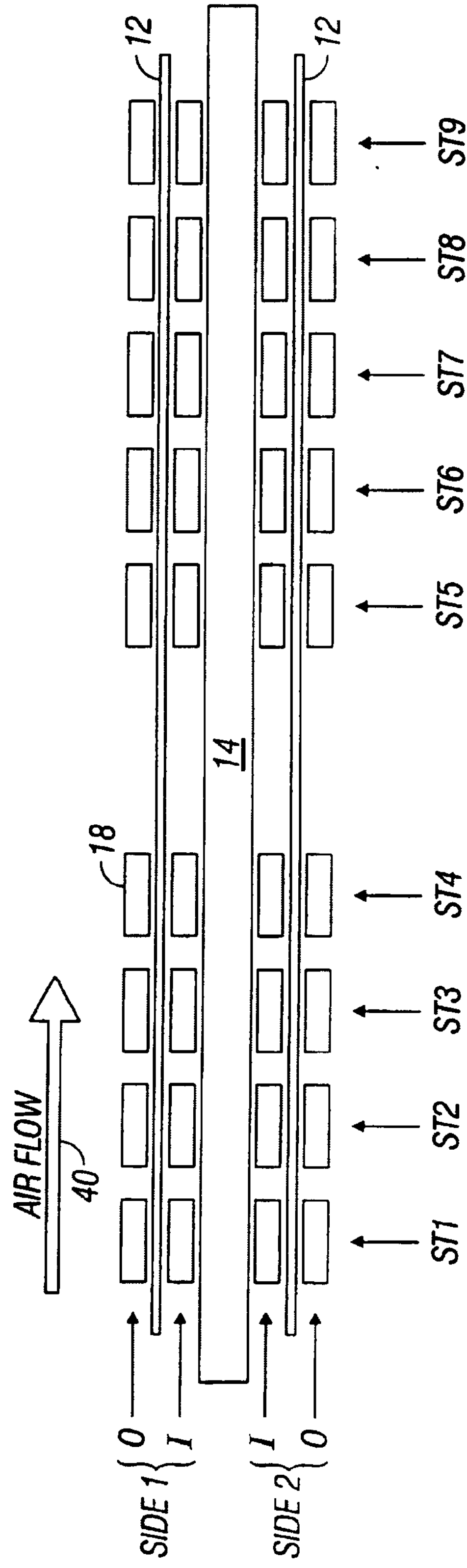


FIG. 31
(Prior Art)



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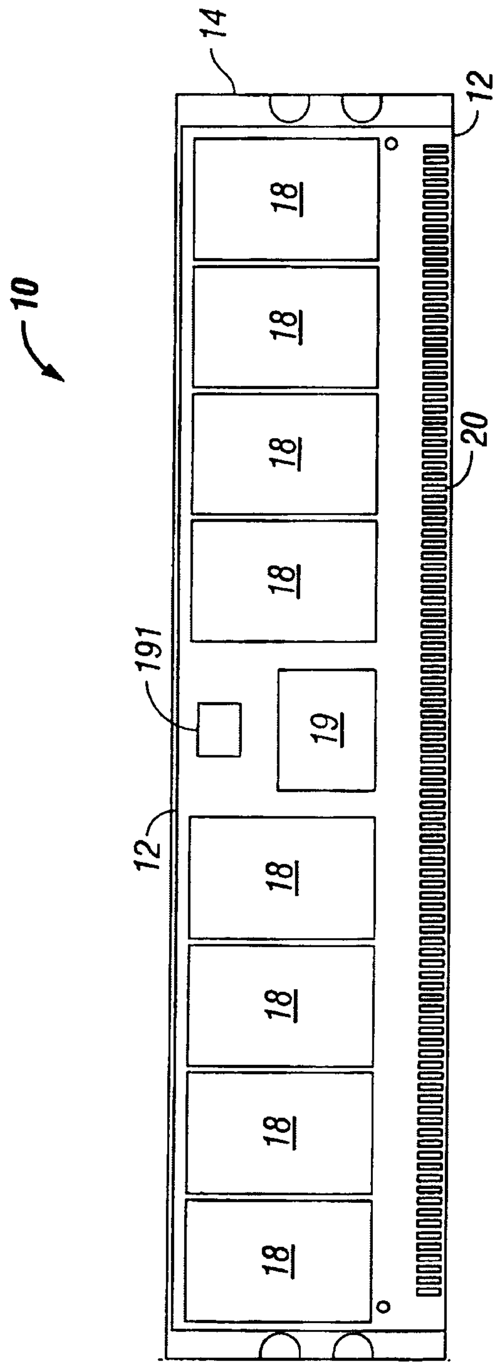

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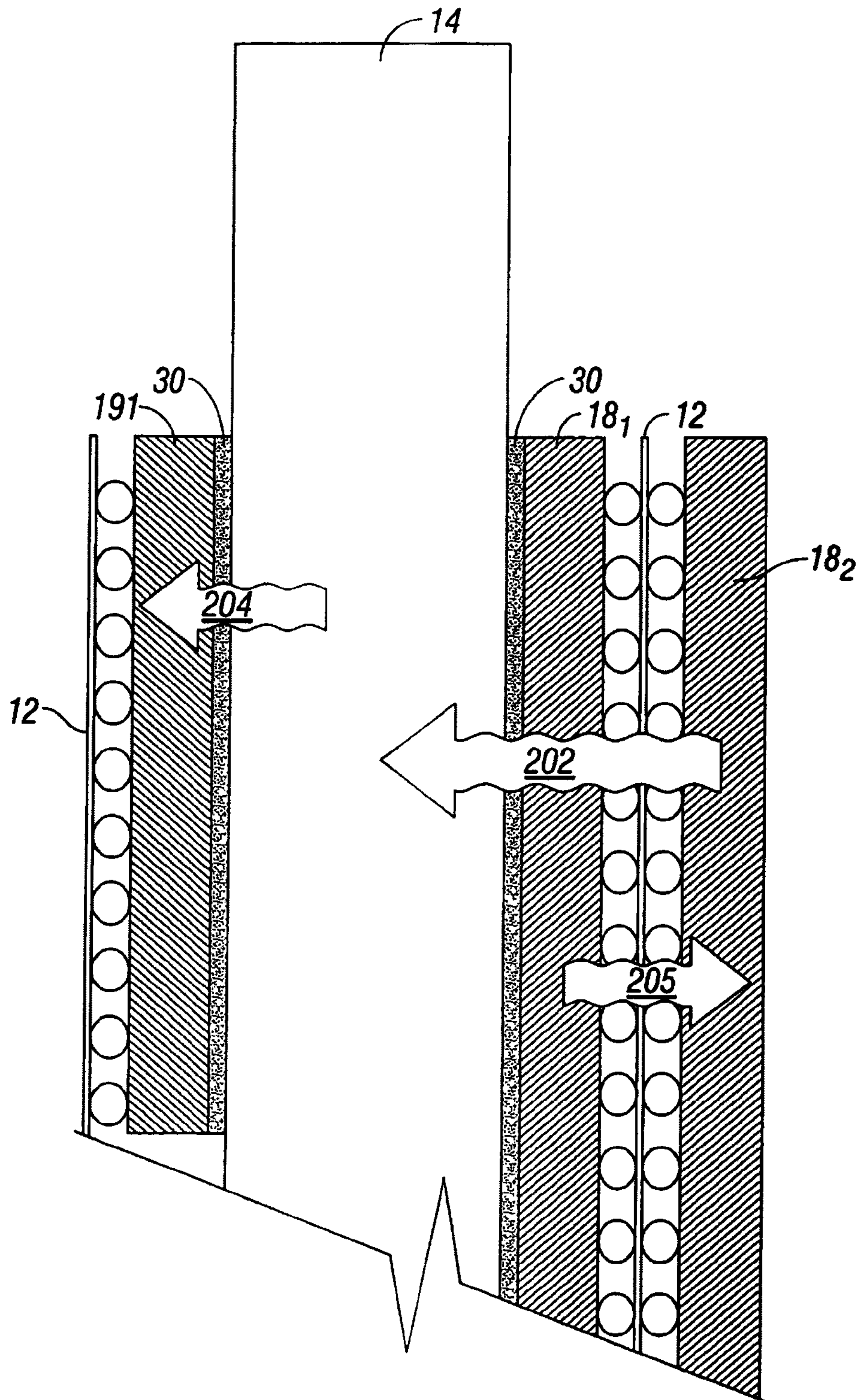


FIG. 34

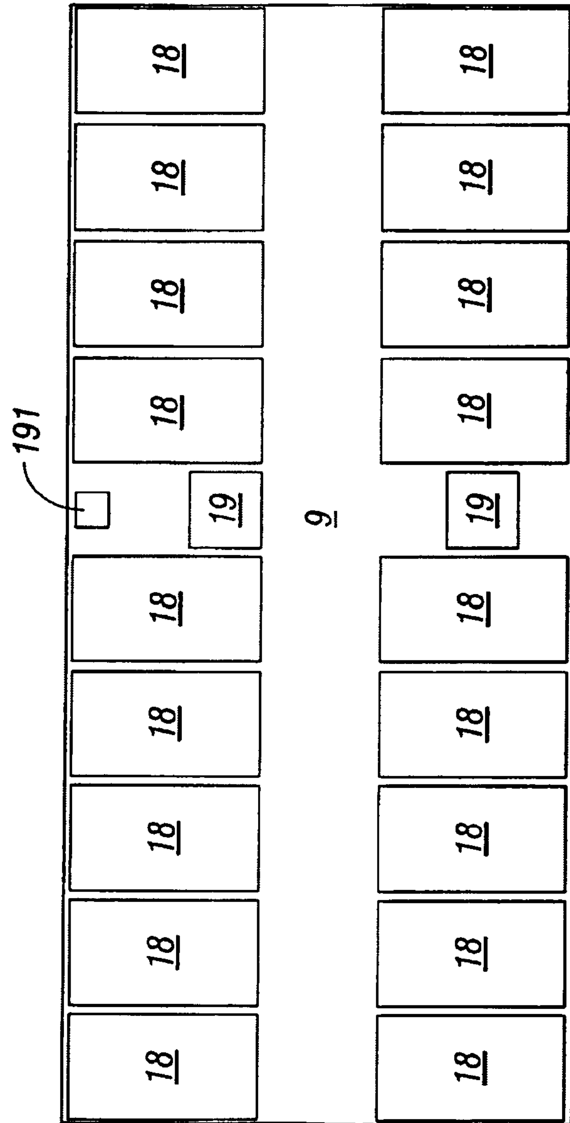


FIG. 35

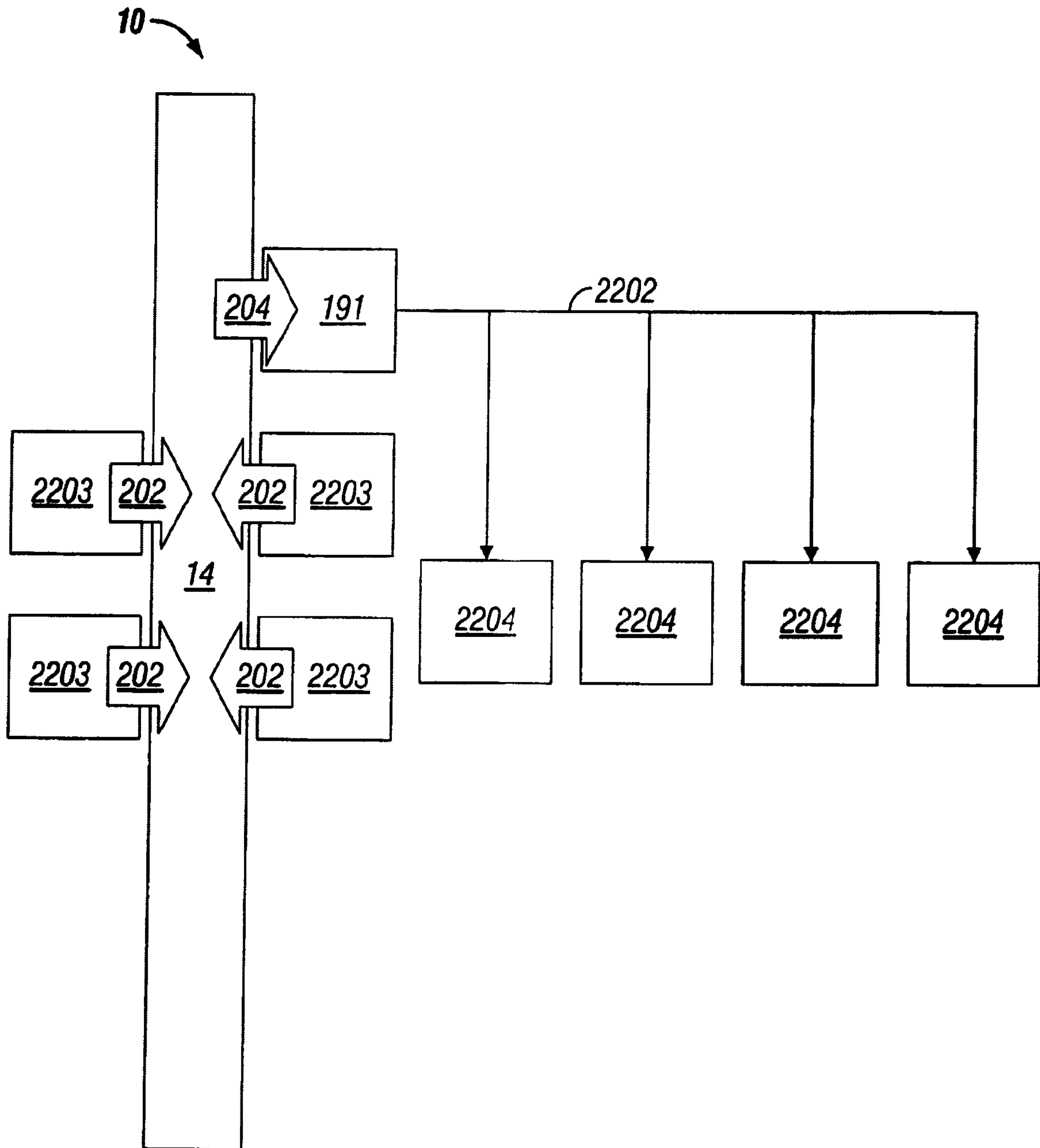
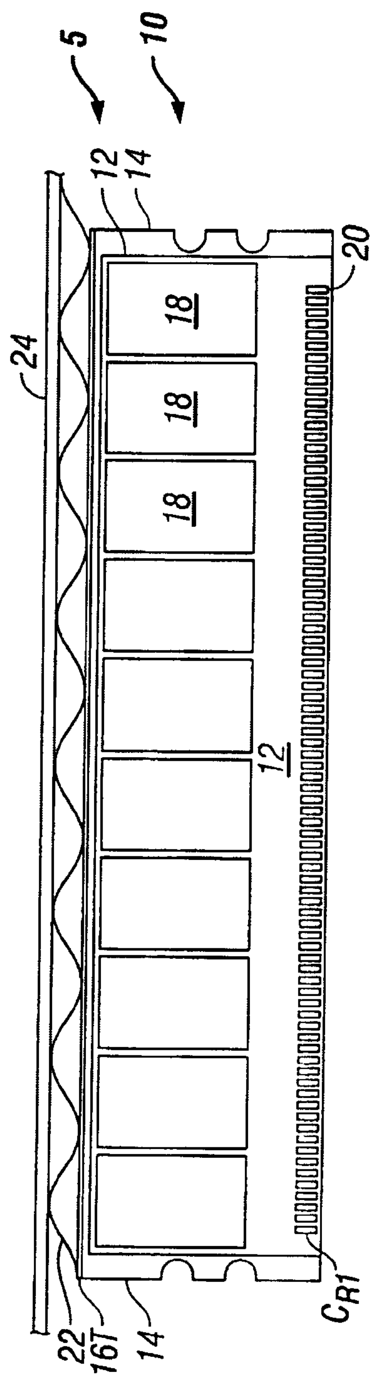


FIG. 36



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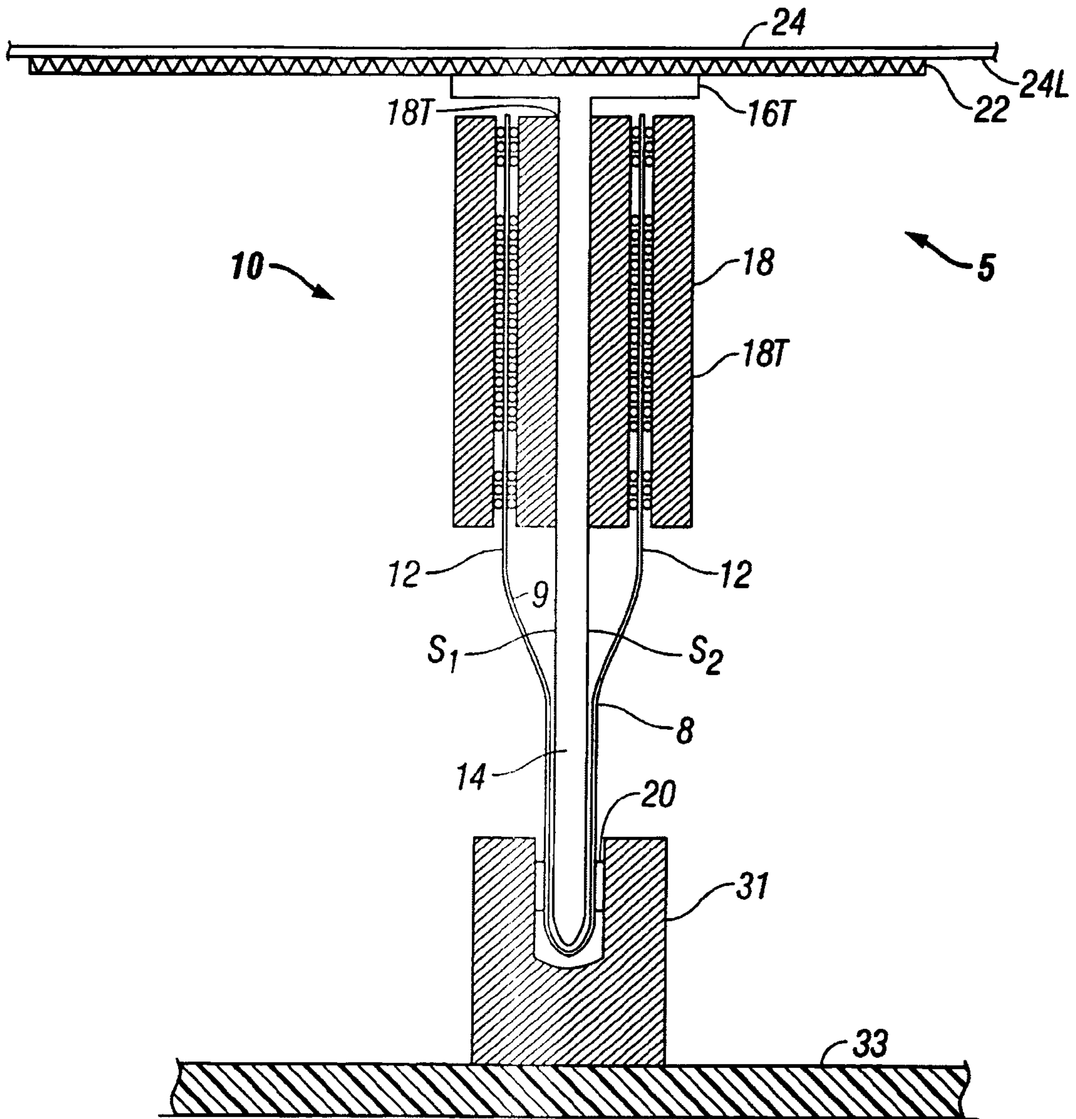


FIG. 38

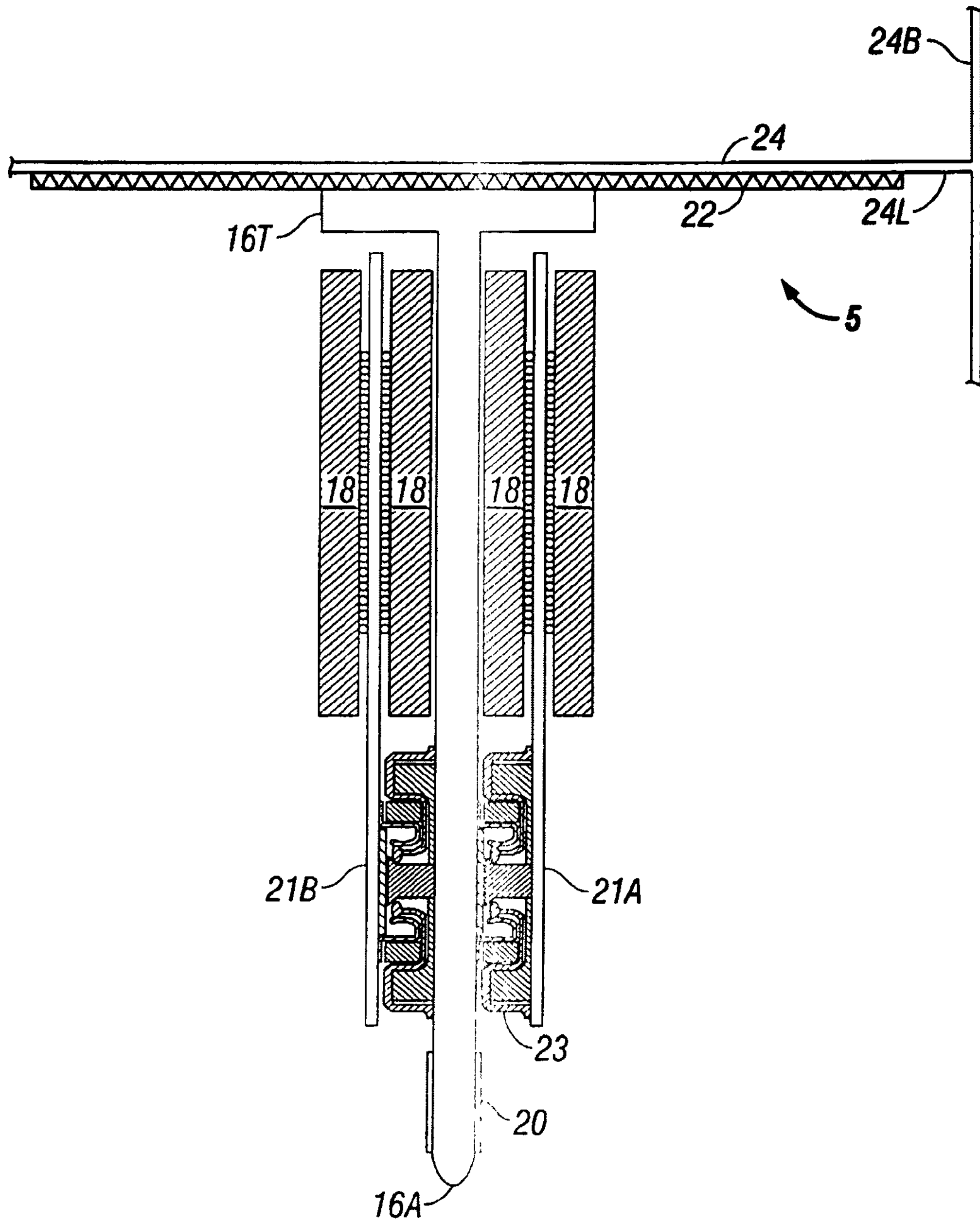
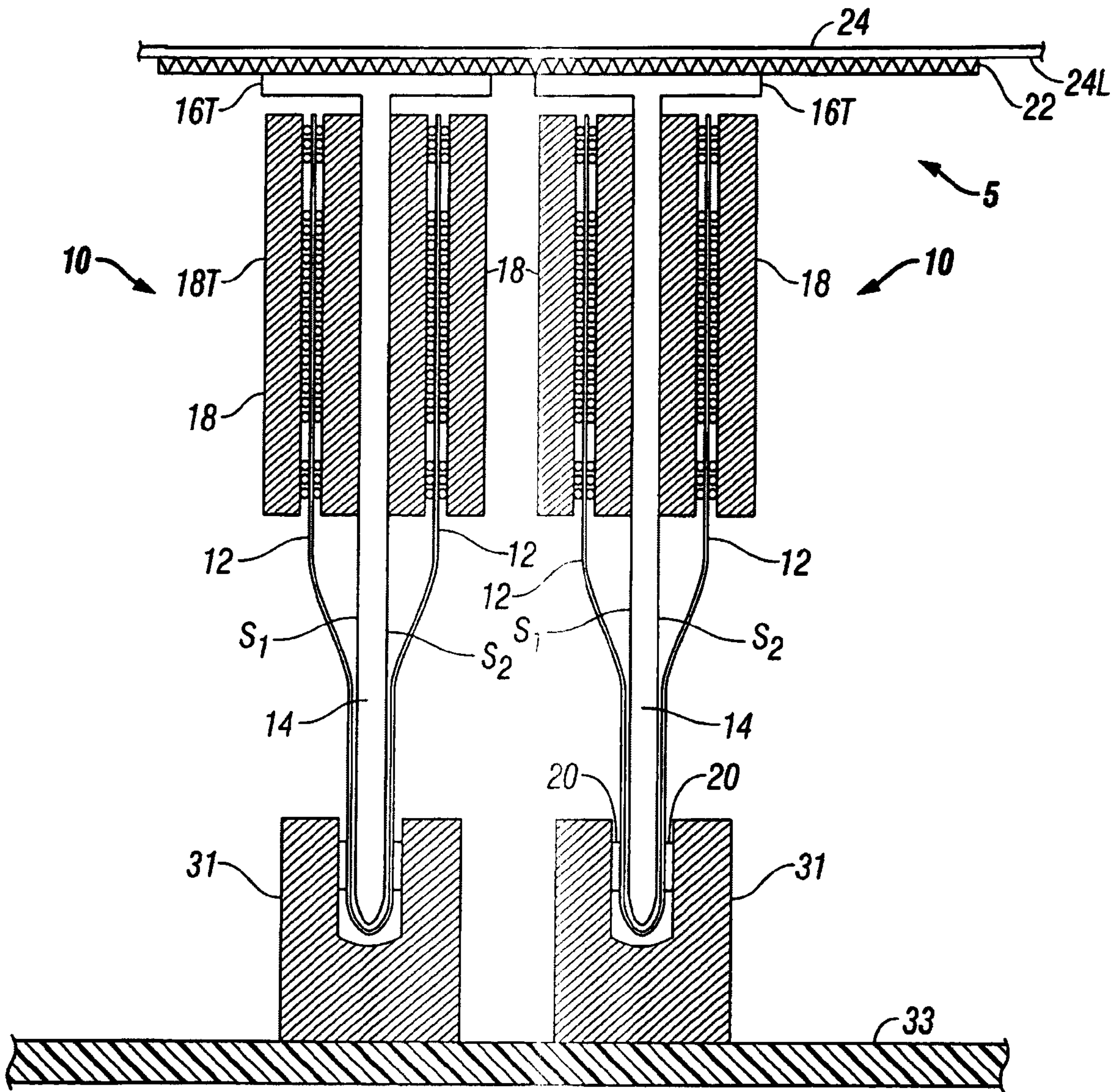


FIG. 39



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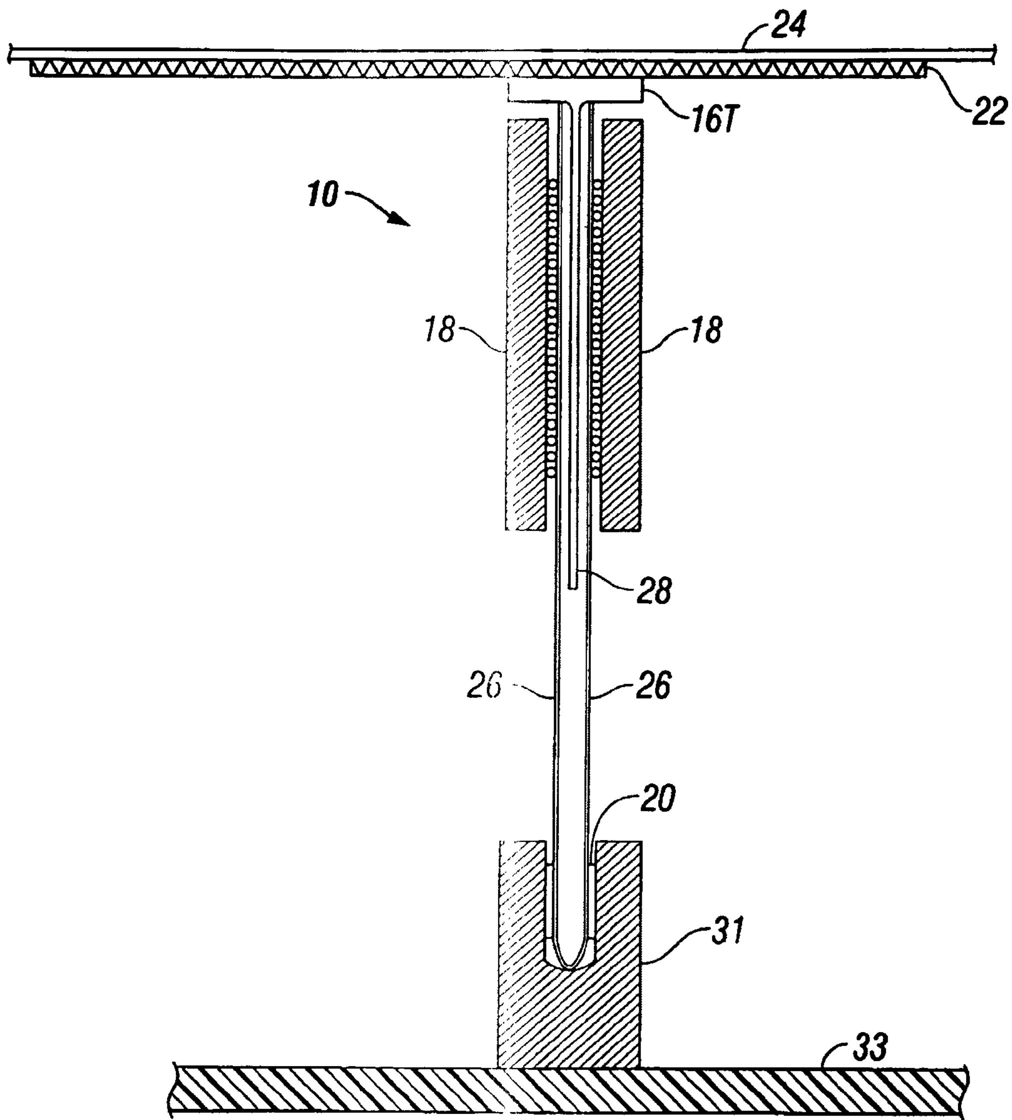
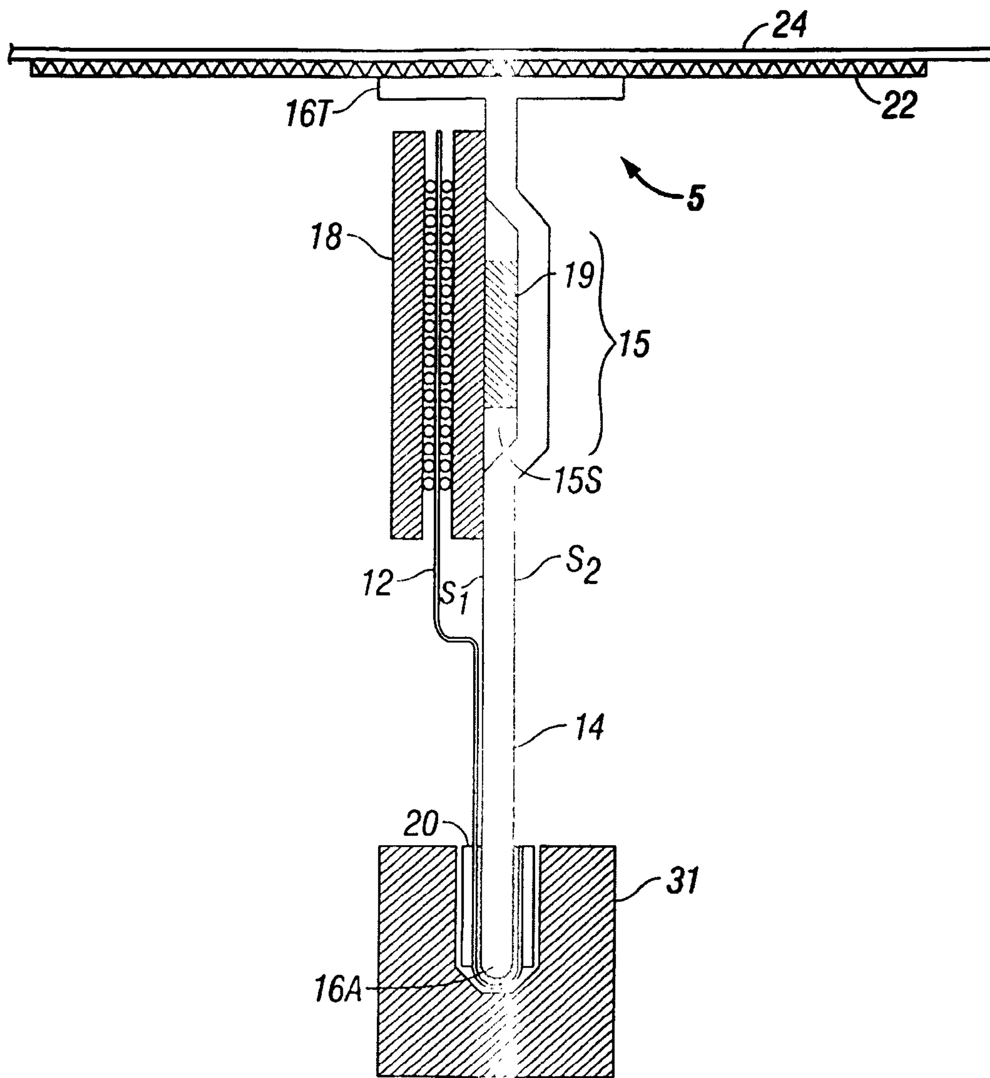


FIG. 41



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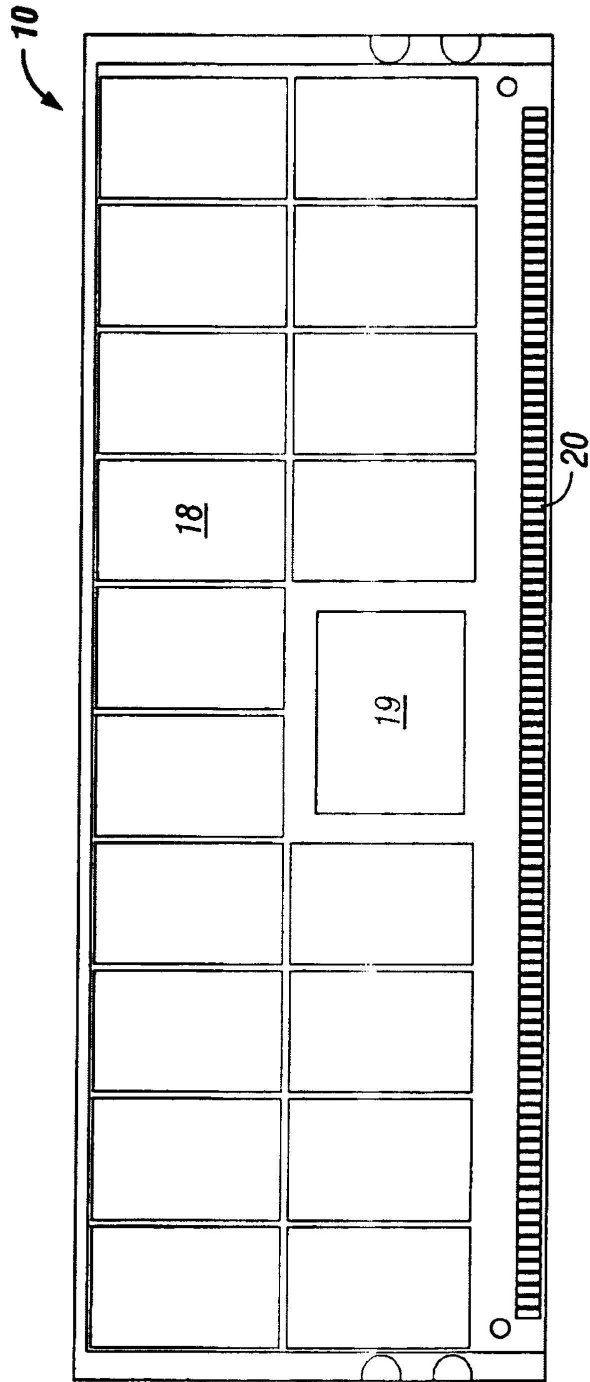


FIG. 43

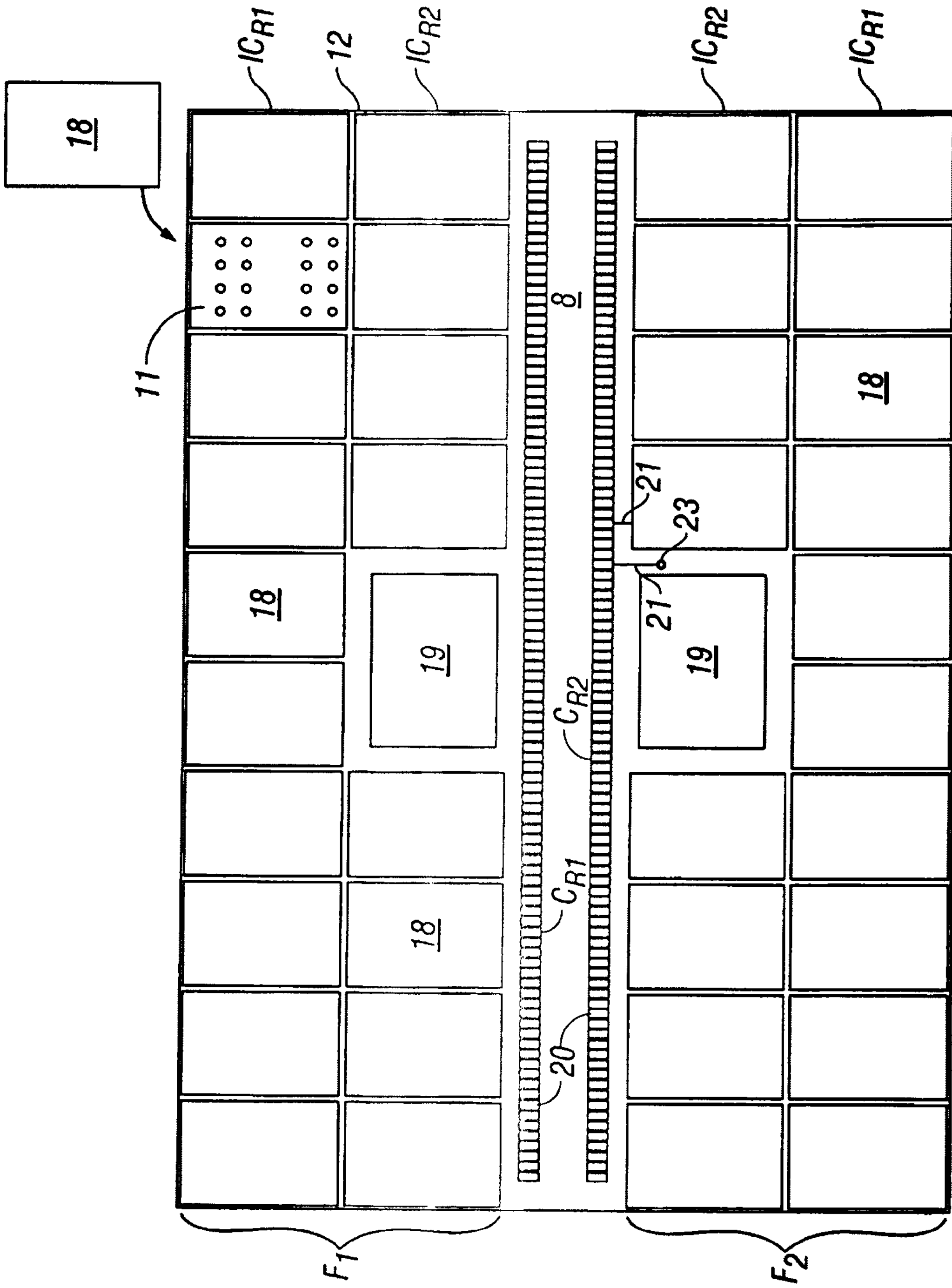
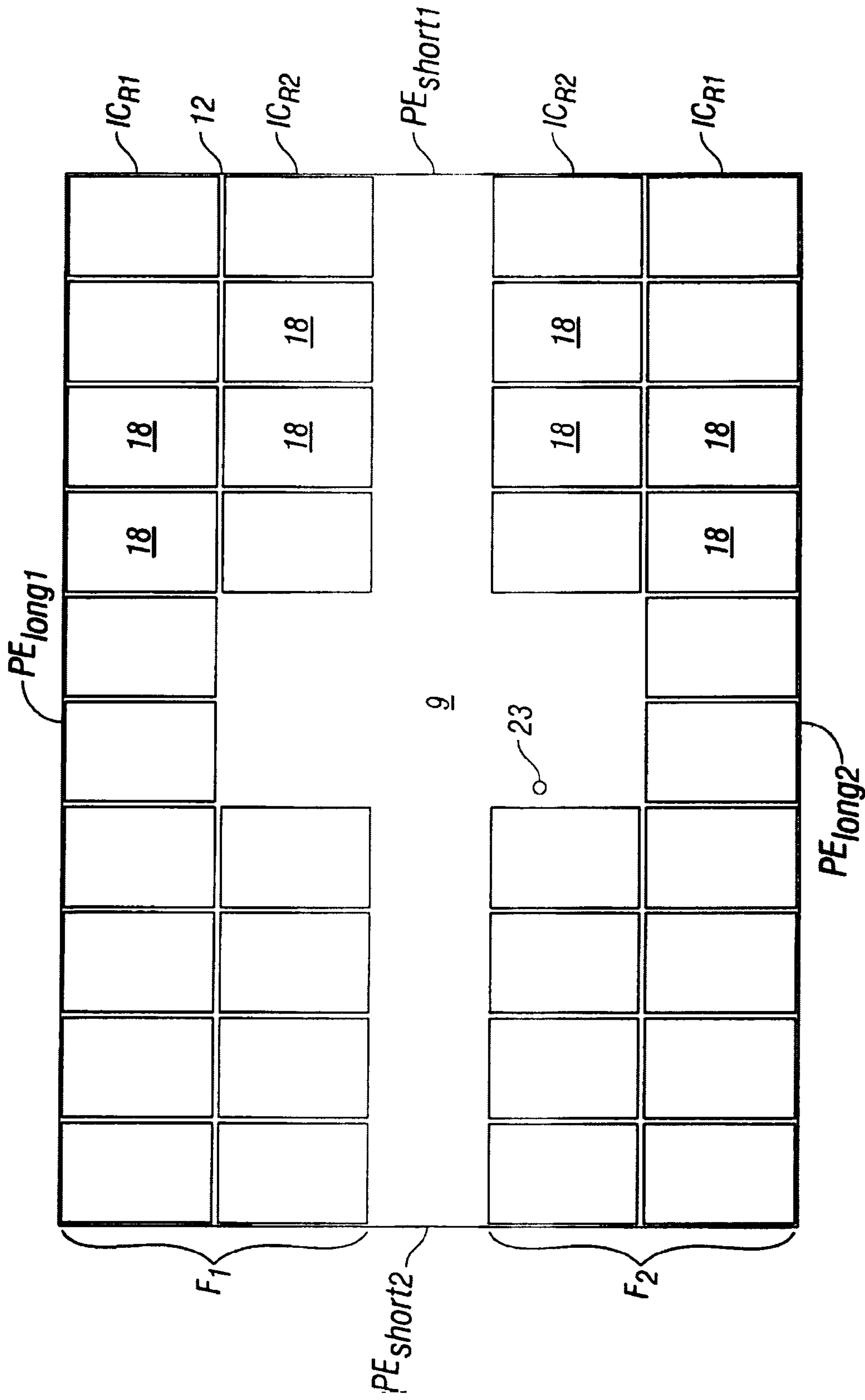


FIG. 44



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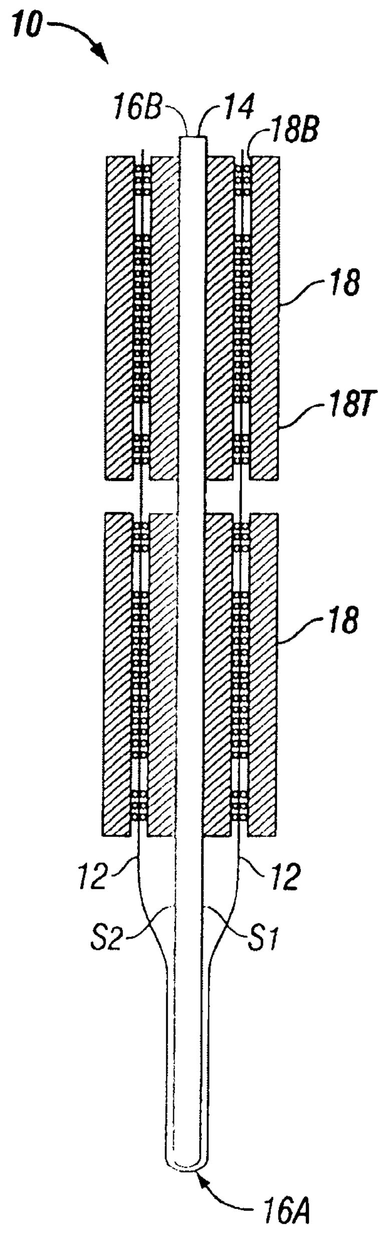

FIG. 46

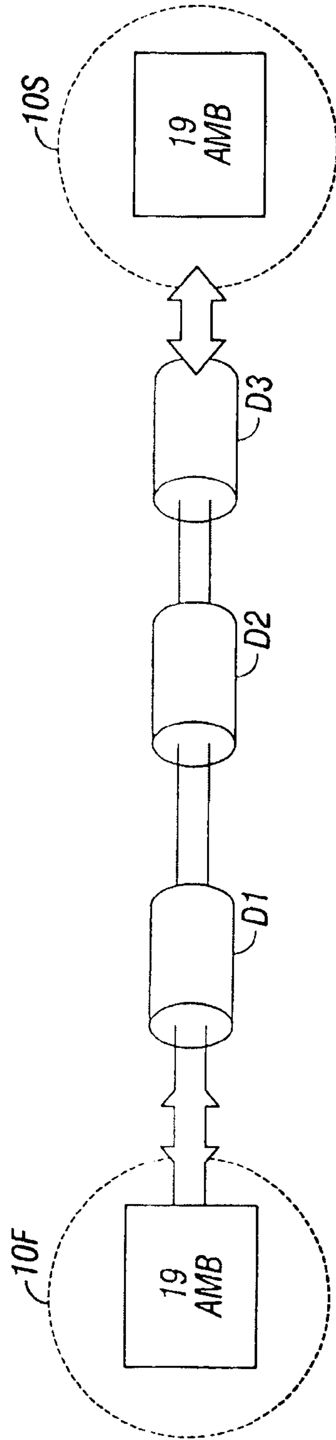

FIG. 47

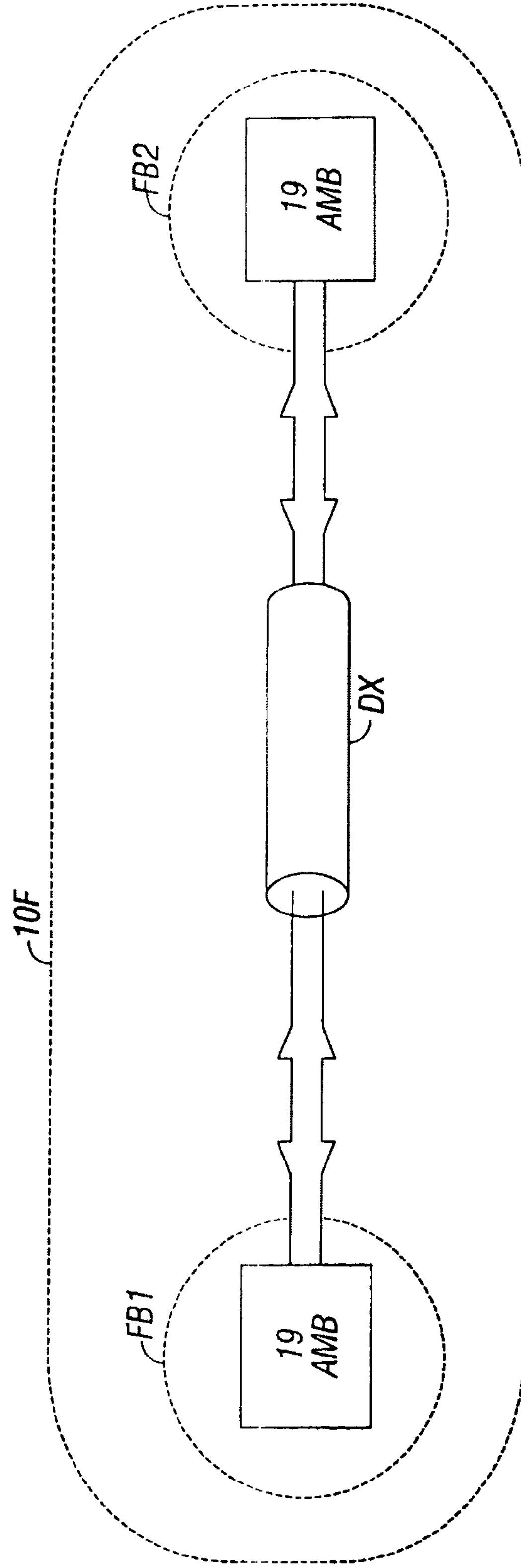

FIG. 48

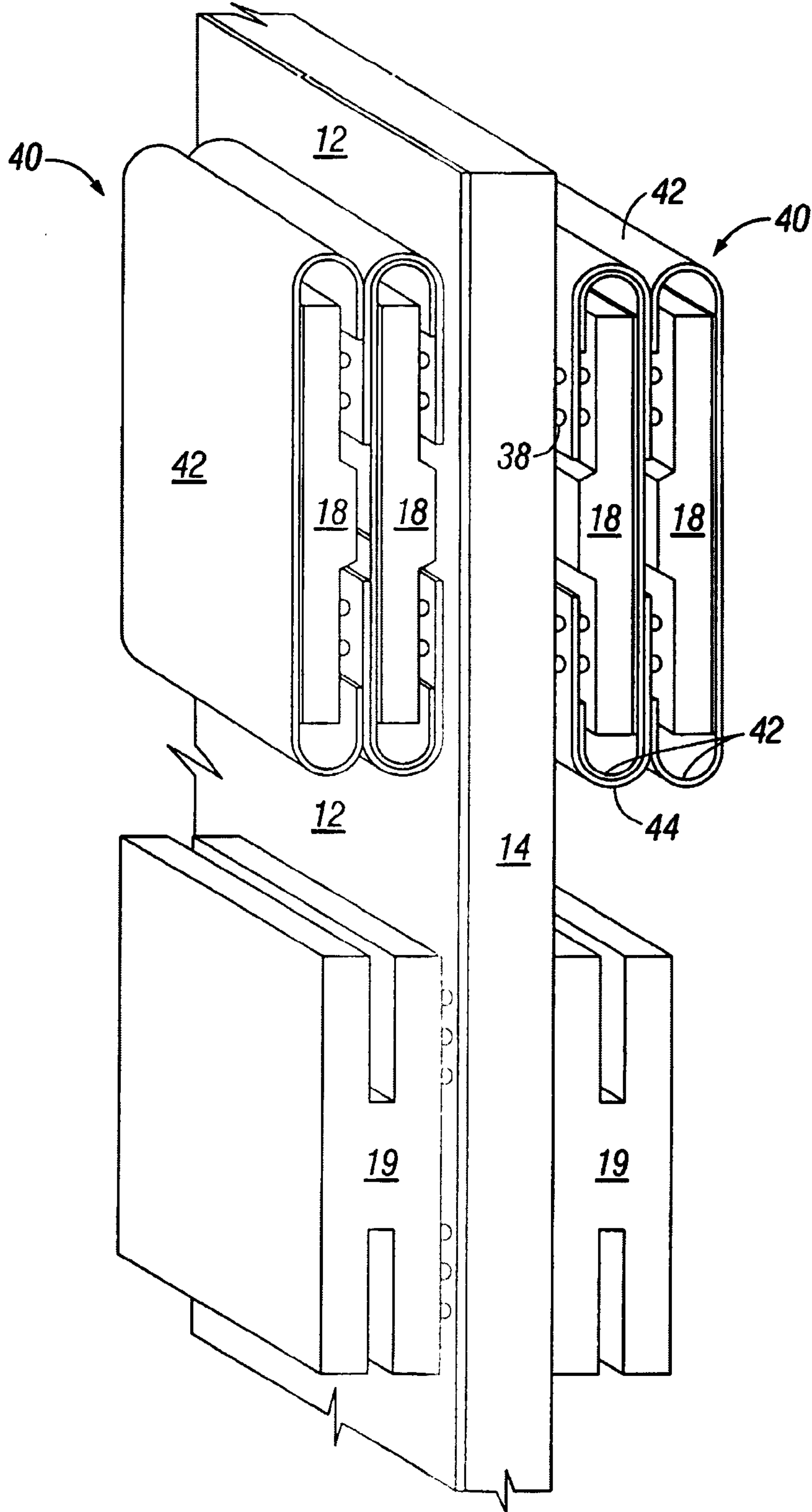

FIG. 49

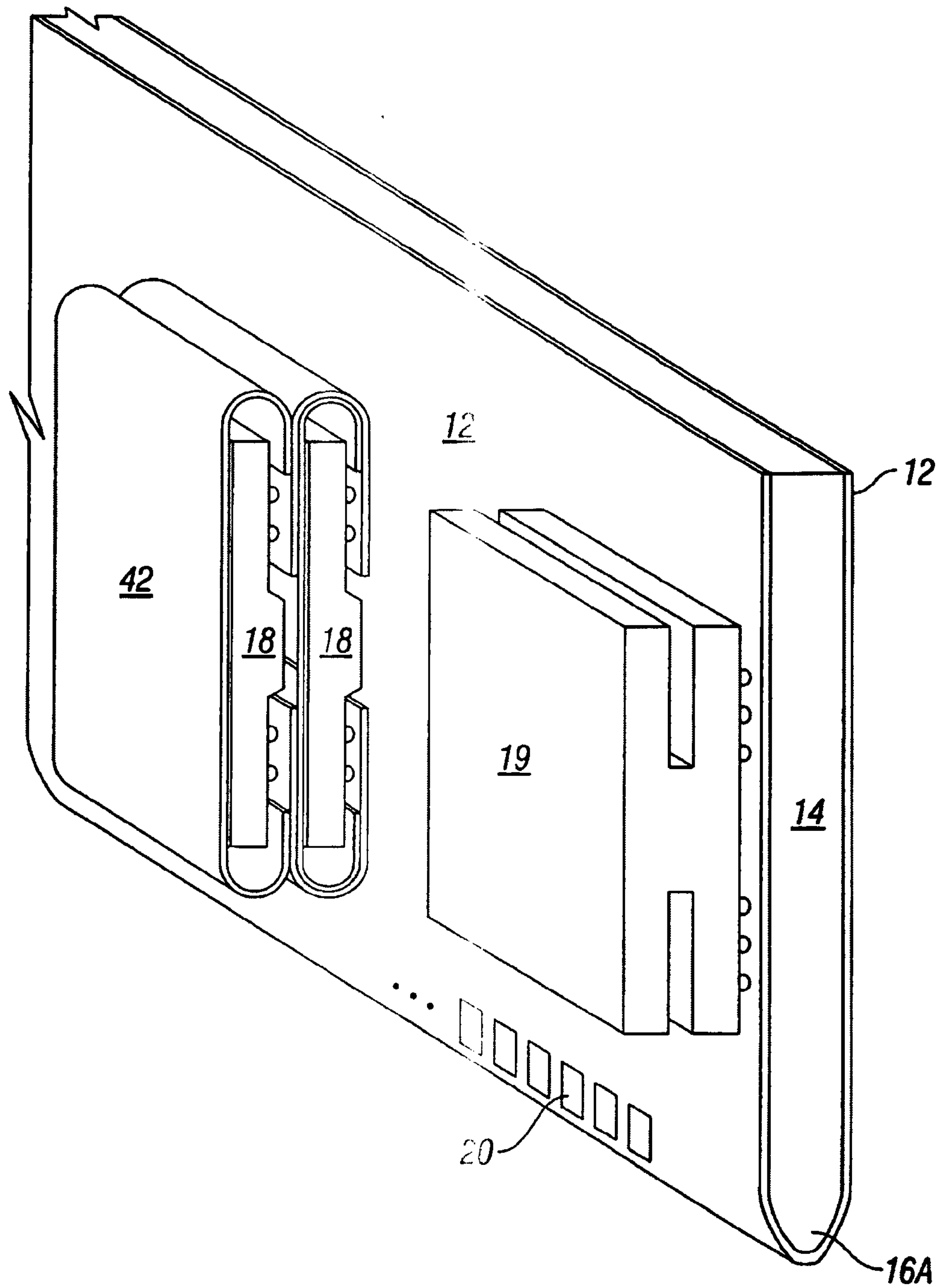

FIG. 50

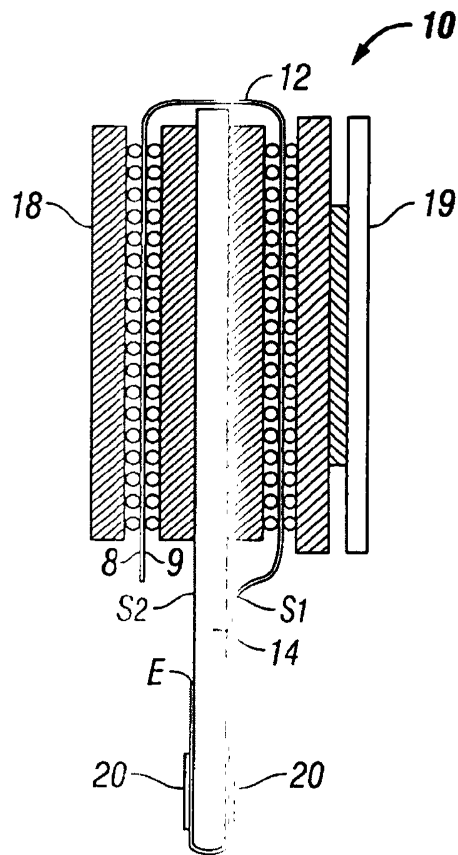

FIG. 51

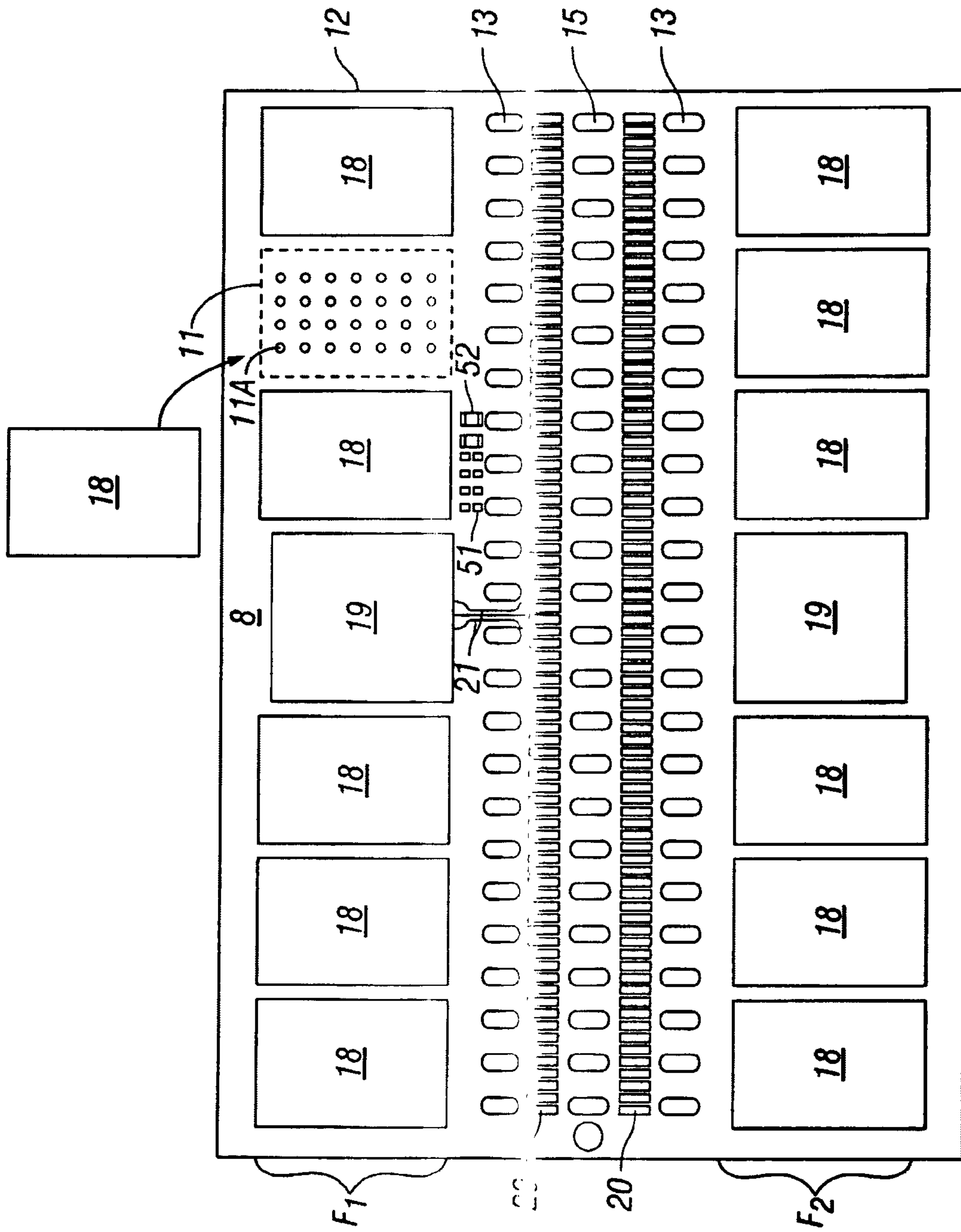

FIG. 52

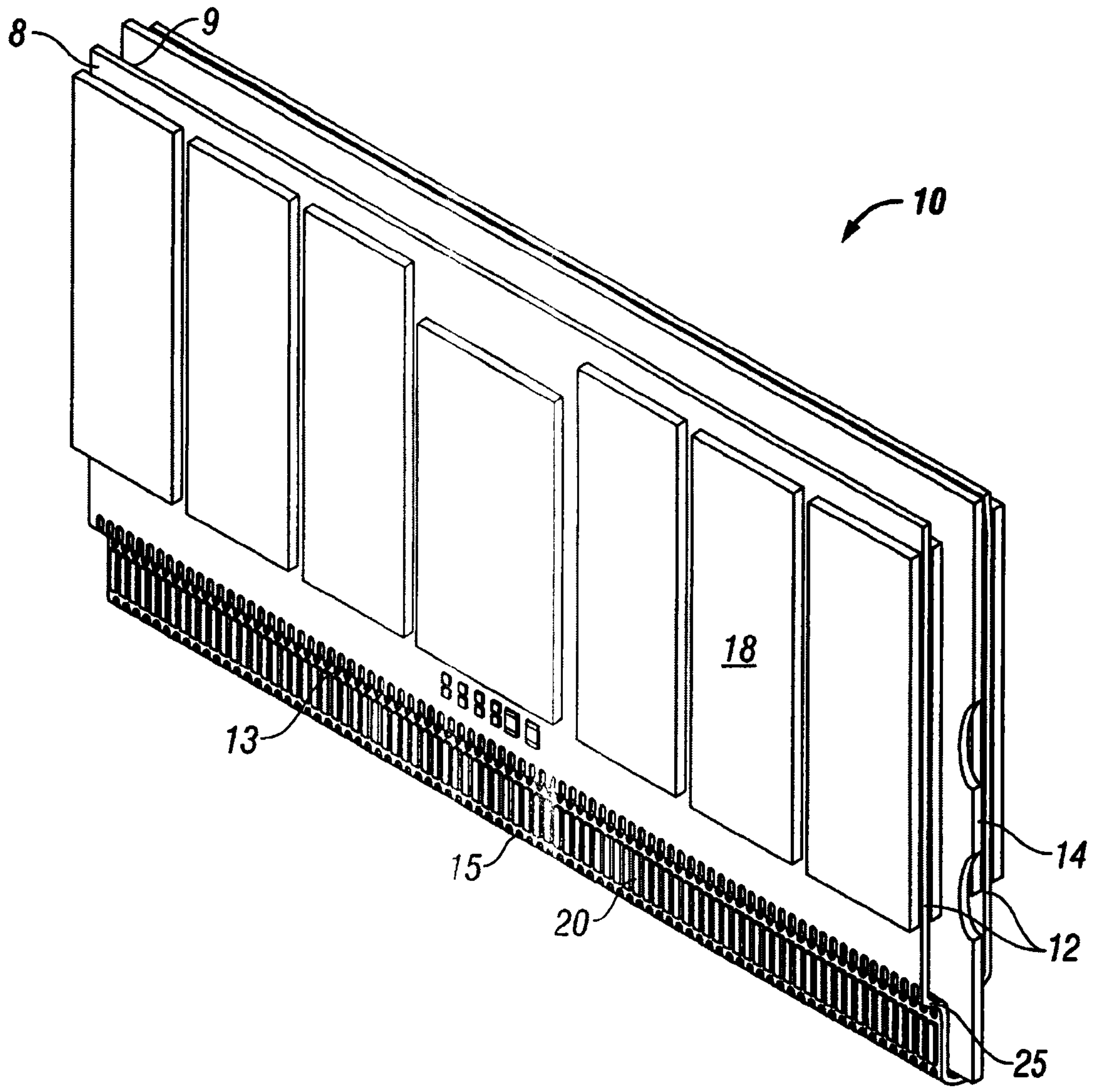

FIG. 53

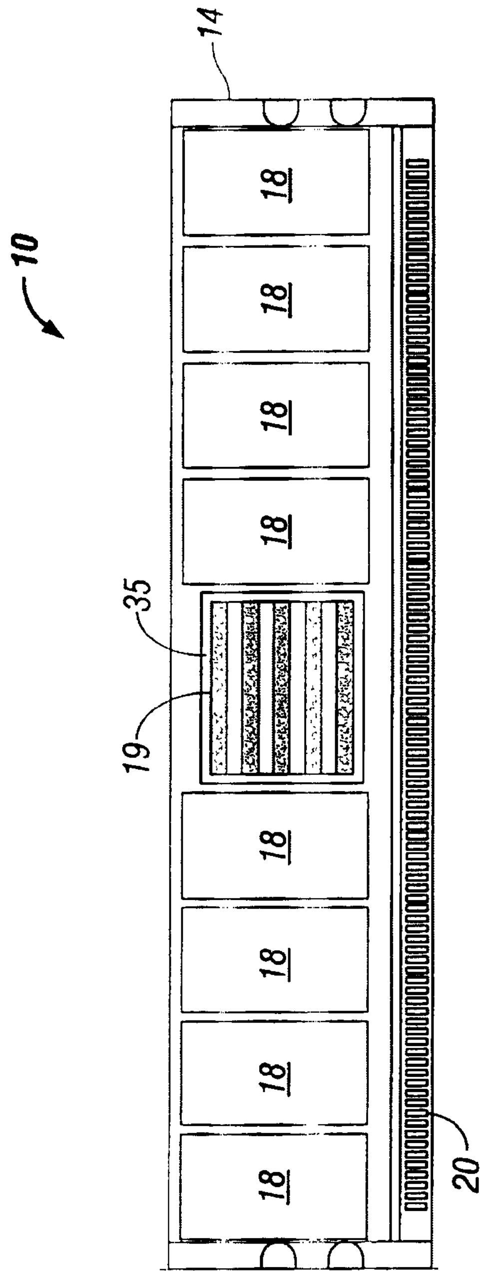

FIG. 54

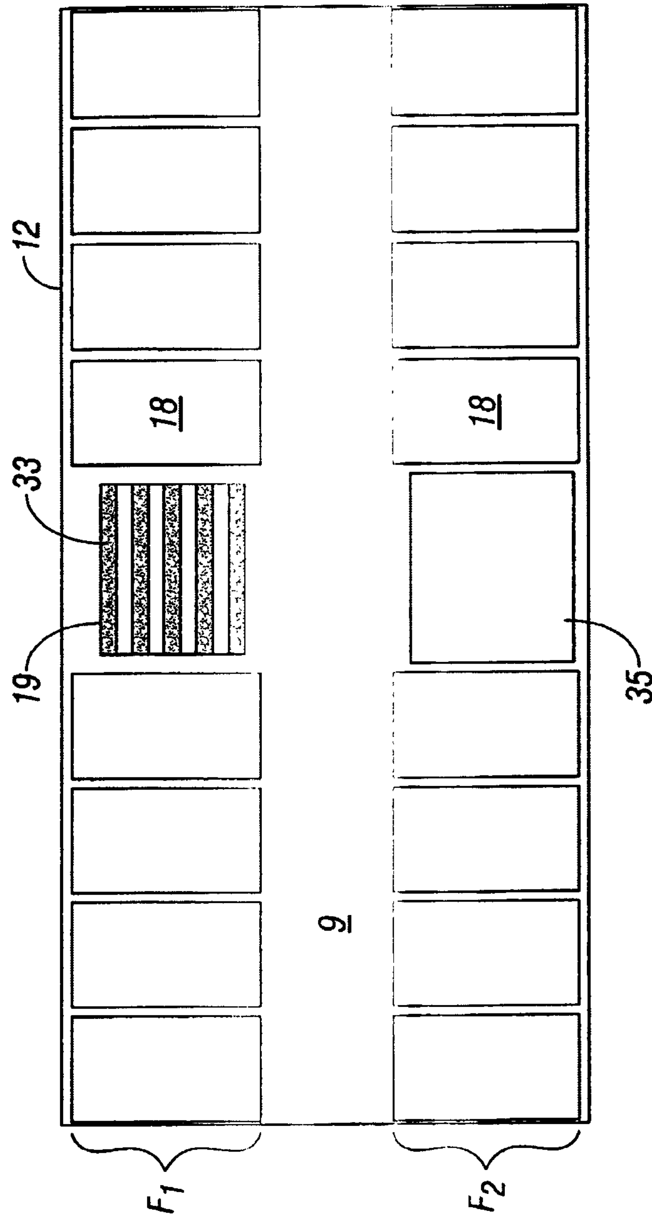

FIG. 55

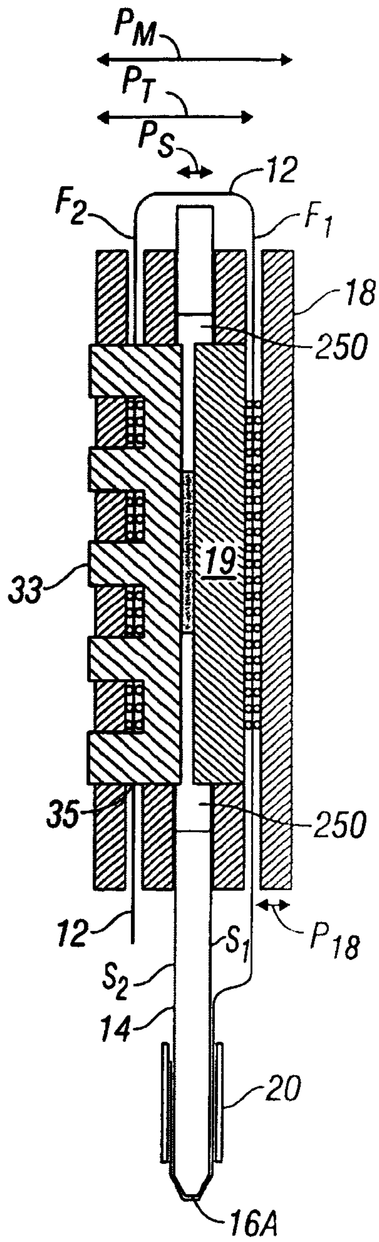

FIG. 56

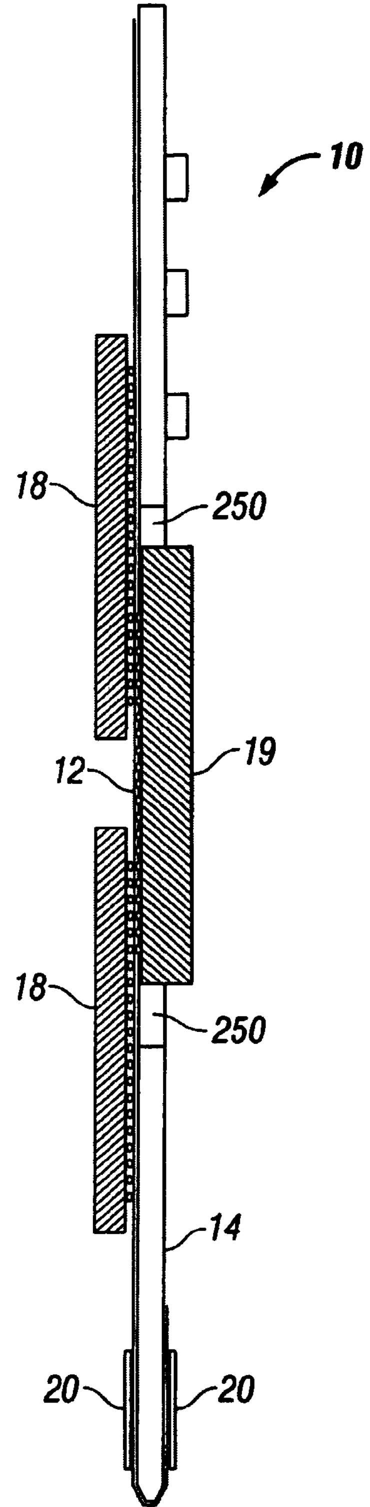

FIG. 57

CIRCUIT MODULE SYSTEM AND METHOD

Field:

The present invention relates to systems and methods for creating
5 high density circuit modules.

Background:

Memory expansion is one of the many fields where high density circuit module solutions provide space-saving advantages. For example,
10 the well-known DIMM (Dual In-Line Memory Module) has been used for years, in various forms, to provide memory expansion. A typical DIMM includes a conventional PCB (printed circuit board) with memory devices and supporting digital logic mounted on both sides. The DIMM is typically mounted in the host computer system by inserting a contact-
15 bearing edge of the DIMM into a card edge connector. Typically, systems that employ DIMMs provide limited profile space for such devices and conventional DIMM-based solutions have typically provided only a moderate amount of memory expansion.

As bus speeds have increased, fewer devices per channel can be
20 reliably addressed with a conventional DIMM-based solution. For example, 288 ICs or devices per channel may be addressed using the SDRAM-100 bus protocol with an unbuffered DIMM. Using the DDR-200 bus protocol, approximately 144 devices may be addressed per channel. With the DDR2-400 bus protocol, only 72 devices per channel
25 may be addressed. This constraint has led to the development of the fully-buffered DIMM (FB-DIMM) with buffered C/A and data in which 288 devices per channel may be addressed. With the FB-DIMM, not only

has capacity increased, pin count has declined to approximately 69 signal pins from the approximately 240 pins previously required.

The FB-DIMM circuit solution is expected to offer practical motherboard memory capacities of up to about 192 gigabytes with six channels and eight DIMMs per channel and two ranks per DIMM using one gigabyte DRAMs. This solution should also be adaptable to next generation technologies and should exhibit significant downward compatibility.

There are several known methods to improve the limited capacity of a DIMM or other circuit board. In one strategy, for example, small circuit boards (daughter cards) are connected to the DIMM to provide extra mounting space. The additional connection may, however, cause flawed signal integrity for the data signals passing from the DIMM to the daughter card while the additional thickness of the daughter card(s) increases the profile of the module.

Multiple die packages (MDP) can also be used to increase DIMM capacity. This scheme increases the capacity of the memory devices on the DIMM by including multiple semiconductor die in a single device package. The additional heat generated by the multiple die typically requires, however, additional cooling capabilities to operate at maximum operating speed. Further, the MDP scheme may exhibit increased costs because of higher yield loss from packaging together multiple die that are not fully pre-tested.

Stacked packages are yet another way to increase module capacity. Capacity is increased by stacking packaged integrated circuits to create a high-density circuit module for mounting on the larger circuit board. In some techniques, flexible conductors are used to selectively interconnect

packaged integrated circuits. Staktek Group L.P., the assignee of the present invention, has developed numerous systems for aggregating CSP (chipscale packaged) devices in space-saving topologies. The increased component height of some stacking techniques may, however, alter system requirements such as, for example, required cooling airflow or the minimum spacing around a circuit board on its host system.

Typically, the known methods raise thermal management issues. For example, when a conventional FBGA packaged DRAM is mounted on a DIMM, the primary thermal path is through the balls into the core of a multilayer DIMM.

What is needed, therefore, are methods and structures for providing high capacity circuit boards in thermally efficient, reliable designs that perform well at higher frequencies but are not too large, yet can be made at reasonable cost.

Summary:

Flexible circuitry is populated with integrated circuits (ICs) disposed along one or both of its major sides. Contacts distributed along the flexible circuitry provide connection to the ICs. Preferably, the flexible circuitry is disposed about an edge of a rigid, thermally-conductive substrate thus placing the integrated circuitry on one or both sides of the substrate with one or two layers of integrated circuitry on one or both sides of the substrate. In alternative, but also preferred embodiments, the ICs on the side of the flexible circuit closest to the substrate are disposed, at least partially, in what are windows, pockets, or cutaway areas in the substrate. Other embodiments may only populate one side of the flexible circuit or may remove substrate material to reduce

module profile. In preferred embodiments, the contacts distributed along the flexible circuitry are configured for insertion into an edge connector socket such as those found in general purpose and server computers. Preferred substrates are comprised of thermally conductive material.
5 Extensions from the substrate in preferred embodiments can be expected to reduce thermal module loading and encourage reduced thermal variations amongst the integrated circuits of the module during operation.

Brief Description of the Drawings:

10 Fig. 1 depicts a side of a flex circuit devised for employment in a module in accordance with a preferred embodiment of the present invention.

Fig. 2 depicts a second side of the flex circuit of Fig. 1.

Fig. 3 depicts a cross-sectional view of a module devised in
15 accordance with a preferred embodiment of the present invention.

Fig. 4 is an enlarged view of the area about a substrate edge in a preferred embodiment.

Fig. 5 is a plan view depicting one side of a module devised in accordance with a preferred embodiment of the present invention.

20 Fig. 6 depicts a pair of modules as may be employed in accordance with the invention.

Fig. 7 depicts an alternative embodiment in accordance with the present invention.

Fig. 8 depicts another embodiment of the present invention having
25 a clip.

Fig. 9 depicts another embodiment having a thinned portion of substrate.

Fig. 10 is a cross-sectional view of another embodiment of the present invention.

Fig. 11 depicts an alternate preferred embodiment having additional layers of ICs.

5 Fig. 12 depicts another alternative embodiment in which flex circuitry is wrapped around opposing edges of a substrate.

Fig. 13 depicts yet another embodiment having a flex circuitry wrapped around opposing edges of a substrate.

Fig. 14 depicts another alternative embodiment in which flex

10 circuitry transits over a substrate.

Fig. 15 depicts an alternative embodiment of the present invention having CSPs on the external side of a flex circuit.

Fig. 16 depicts an alternative embodiment of the present invention having CSPs mounted between a flex circuit and substrate.

15 Fig. 17 depicts another alternative embodiment.

Fig. 18 is a preferred embodiment of the present invention with multiple thermally-radiative extensions.

Fig. 19 depicts an alternative embodiment of the present invention in which a connector provides selective interconnective facility between

20 parts of the flex circuit on opposite lateral sides of the substrate.

Fig. 20 depicts details from the area marked "A" in Fig. 19.

Fig. 21 and 22 depict sides of a flex circuit employed in a module in accordance with the present invention.

Fig. 23 is a view of a substrate employed in an alternative

25 embodiment.

Fig. 24 is a cross-sectional view of an embodiment employing the substrate depicted in Fig. 23.

Fig. 25 is a cross-sectional view of another embodiment.

Fig. 26 is a cross-sectional view of a substrate employed in the module depicted in Fig. 25.

Fig. 27 is an elevation view of a another substrate employable in a
5 module in accord with the invention.

Fig. 28 is a cross-sectional view of part of an alternative embodiment.

Fig. 29 is an exploded cross-section of a flex circuit employed in a preferred embodiment in accord with the invention.

10 Fig. 30 depicts another preferred embodiment.

Fig. 31 depicts sides of a prior art module devised in accord with the "planar" strategy.

Fig. 32 is a schematic map of an embodiment for use in understanding modeled data in tables herein.

15 Fig. 33 depicts a plan view of a module devised in accord with a preferred embodiment of the invention.

Fig. 34 illustrates an enlarged section of a module in accordance with a preferred embodiment illustrating certain thermal flows.

Fig. 35 illustrates a flex circuit employed in an alternative
20 embodiment.

Fig. 36 depicts representative sensor signal flows in an embodiment.

Fig. 37 illustrates an embodiment of a thermal management system devised in accordance with the invention.

25 Fig. 38 is another depiction of a thermal management system in accordance with the invention.

Fig. 39 illustrates another embodiment of a module thermal management system in accordance with the present invention.

Fig. 40 depicts two modules devised in accordance with the present invention and employed in an embodiment of the thermal management
5 system embodiment of the invention.

Fig. 41 illustrates an alternative embodiment employed in an embodiment of the thermal management system embodiment of the invention.

Fig. 42 depicts another embodiment in accordance with the present
10 invention.

Fig. 43 depicts a plan view of another embodiment of the present invention.

Fig. 44 depicts a side of a populated flex circuit employed in a module devised to express multiple instances of an FB-DIMM circuit.

15 Fig. 45 depicts another side of the flex circuitry shown in Fig. 44.

Fig. 46 is a cross-sectional view of an alternative embodiment having four ranks of ICs on each side of the substrate.

Fig. 47 is a schematic illustration of impedance discontinuities between two conventional FB-DIMMs.

20 Fig. 48 is a schematic illustration of certain impedance features in an embodiment having more than one AMB.

Fig. 49 illustrates on part of a FB-DIMM module employing stacks and AMBs.

Fig. 50 illustrates another configuration of a FB-DIMM
25 embodiment in accordance with the invention.

Fig. 51 is yet another FB-DIMM embodiment of the present invention.

Fig. 52 illustrates a side of a flex circuit employed in an embodiment of the present invention.

Fig. 53 is another depiction of a preferred module devised in accordance with the present invention.

5 Fig. 54 is a plan view of a low profile FB-DIMM type embodiment in accord with the invention.

Fig. 55 depicts a flex circuit employed in a low profile FB-DIMM type embodiment.

Fig. 56 is a cross-sectional view of a module in accord with the
10 invention.

Fig. 57 is a cross-sectional view of another module in accord with the invention.

Detailed Description of Preferred Embodiments:

15 Figs. 1 and 2 depict opposing sides 8 and 9 of a preferred flex circuit 12 ("flex", "flex circuitry", "flexible circuitry", "flexible circuit") used in constructing a preferred embodiment of the present invention. Flex circuit 12 is preferably made from plural conductive layers supported by one or more flexible substrate layers as further described.
20 The entirety of the flex circuit 12 may be flexible or, as those of skill in the art will recognize, the flexible circuit structure 12 may be made flexible in certain areas to allow conformability to required shapes or bends, and rigid in other areas to provide rigid and planar mounting surfaces. Preferred flex circuit 12 has openings 17 (or tabs) for use in
25 aligning flex circuit 12 to a substrate during assembly.

ICs 18 on flexible circuit 12 are, in this embodiment, chip-scale packaged memory devices. For purposes of this disclosure, the term

chip-scale or "CSP" shall refer to integrated circuitry of any function with an array package providing connection to one or more die through contacts (often embodied as "bumps" or "balls" for example) distributed across a major surface of the package or die. CSP does not refer to leaded devices that provide connection to an integrated circuit within the package through leads emergent from the periphery of the package such as, for example, a TSOP.

Embodiments of the present invention may be employed with leaded or CSP devices or other devices in both packaged and unpackaged forms but where the term CSP is used, the above definition for CSP should be adopted. Consequently, although CSP excludes leaded devices, references to CSP are to be broadly construed to include the large variety of array devices (and not to be limited to memory only) and whether die-sized or other size such as BGA and micro BGA as well as flip-chip. As those of skill will understand after appreciating this disclosure, some embodiments of the present invention may be devised to employ stacks of ICs each disposed where an IC 18 is indicated in the exemplar Figs.

Multiple integrated circuit die may be included in a package depicted as a single IC 18. While in this embodiment, memory ICs are used to provide a memory expansion board, this is not limiting and various embodiments may include a variety of integrated circuits and other components devised for other primary functions besides or in addition to memory. Such variety may include microprocessors, FPGA's, RF transceiver or other communications circuitry, digital logic, as a list of non-limiting examples, or other circuits or systems which may benefit from a high-density circuit module capability. Circuit 19 depicted between a pair of ICs 18 may be a memory buffer or controller or as later

depicted, an advanced memory buffer (AMB) or may be considered a microprocessor, logic or communications device.

Fig. 1 depicts a top or outer side 8 of flex circuit 12 upon which are mounted ICs 18 disposed in two rows or pluralities IC_{R1} and IC_{R2}. Those of skill will appreciate that mounting of ICs 18 on flex circuit 12 provides straight-forward and efficient manufacturing advantages when examples of module 10 are assembled. Other embodiments may have other numbers of rows or there may be only one such row. Contact arrays are disposed beneath ICs 18 and circuit 19 to provide conductive pads for interconnection to the ICs. An exemplar contact array 11A is shown, as is exemplar IC 18 to be mounted at contact array 11A as depicted. Between the rows IC_{R1} and IC_{R2} of ICs 18, flex circuit 12 has two rows (C_{R1} and C_{R2}) of module contacts 20. When flex circuit 12 is folded as depicted in later Figs., side 8 depicted in Fig. 1 is presented at the outside of module 10. The opposing side 9 of flex circuit 12 (Fig. 2) is on the inside.

Fig. 2 depicts another two pluralities of ICs 18 on side 9 of flex circuit 12 referenced as IC_{R3} and IC_{R4}. Various discrete components such as termination resistors, bypass capacitors, and bias resistors may also be mounted on each of sides 8 and 9 of flex 12. Such discrete components are not shown to simplify the drawing. Flex circuit 12 may also be described with reference to its perimeter edges, two of which are typically long (PE_{long1} and $PE_{long\,2}$) and two of which are typically shorter (PE_{short1} and PE_{short2}). Other embodiments may employ flex circuits 12 that are not rectangular in shape and may be square, in which case the perimeter edges would be of equal size or other convenient shape to adapt to manufacturing particulars.

Fig. 1 depicts exemplar conductive traces 21 connecting rows C_{R1} and C_{R2} of module contacts 20 to ICs 18. Only a few exemplar traces are shown to simplify the drawing. Traces 21 may also connect to vias that may transit to other conductive layers of flex 12 in certain embodiments
5 having more than one conductive layer. A via 23 is shown connecting a signal trace 25 from circuit 19 on another conductive layer of flex 12 as illustrated by the dotted line of trace 25. In a preferred embodiment, vias are part of the connection of ICs 18 on side 9 of flex 12 (Fig. 2) to module contacts 20. Traces 21 and 25 may make other connections
10 between the ICs on either side of flex 12 and may traverse the rows of module contacts 20 to interconnect ICs. Together the various traces and vias make interconnections needed to convey signals to the various ICs. Those of skill will understand that the present invention may be implemented with only a single row of module contacts 20 and may, in
15 other embodiments, be implemented as a module bearing ICs on only one side of the module or on one or both sides of the flex circuitry.

Fig. 3 is a cross-sectional view of a module 10 devised in accordance with a preferred embodiment of the present invention. Module 10 is populated with CSPs 18 having top surfaces 18_T and bottom
20 surfaces 18_B. Substrate 14 has an edge 16A appearing in the depiction of Fig. 3 as an end of substrate 14 about which flex circuit 12 is disposed. Substrate 14 typically has first and second lateral sides S_1 and S_2. Flex 12 is wrapped about perimeter edge 16A of substrate 14 which, near edge 16A in the depicted embodiment, provides the basic shape of a common
25 DIMM board form factor. Preferably, at least a portion of the pocket of flex 12 formed by wrapping the flex circuit about the substrate is laminated or otherwise affixed to substrate 14 on both sides of substrate

14. That portion may vary in length depending on factors such as, for example, the height of ICs 18, the thickness of substrate 14, the length of module contacts 20, and the size and design of the edge connector or computer or expansion board socket into which module 10 is adapted to be inserted. Space where the flex circuit may transition to the area of its connection with ICs 18 may be filled with a conformal or heat conductive underfill, may be left unfilled or, as will be shown in later Fig. 7, may be occupied by a flex support part of substrate 14. Adhesive 30, in a preferred embodiment, is a thermally-conductive material to take advantage of the heat dissipation characteristics that may be provided by use of an appropriately selected thermally-conductive substrate 14 comprised, for example, of a metal such as aluminum.

The inner pair of the four depicted ICs 18 are preferably attached to substrate 14 with a heat conductive adhesive 30. Adhesive 30, in a preferred embodiment, is a thermally-conductive material to take advantage of the heat dissipation characteristics that may be provided by use of an appropriately selected thermally-conductive substrate 14. While in this embodiment, the four depicted ICs are attached to flex circuit 12 in opposing pairs, this is not limiting and more ICs may be connected in other arrangements, such as, for example, staggered or offset arrangements, examples of which are later shown. Further, while only CSP packaged ICs are shown, other ICs (packaged and unpackaged) may be employed as ICs 18. While memory CSPs are the typical IC 18, ICs of other functions may also be employed.

In this embodiment, flex circuit 12 has module contacts 20 positioned in a manner devised to fit in an edge connector or computer or expansion board socket and connect to corresponding contacts in the

connector or socket. While module contacts 20 are shown protruding from the surface of flex circuit 12, this is not limiting and other embodiments may have flush contacts or contacts below the surface level of flex 12. Substrate 14 supports module contacts 20 from behind flex
5 circuit 12 in a manner devised to provide the mechanical form required for insertion into a socket. While the depicted substrate 14 has uniform thickness, this is not limiting and in other embodiments the thickness or surface of substrate 14 may vary. Non-limiting examples of such possible variations are found in later Figs. herein. Substrate 14 in the
10 depicted embodiment is preferably made of a thermally-conductive metallic material such as, for example, aluminum or copper. Substrate 14 may also be comprised of other thermally-conductive materials such as thermally-conductive plastics or carbon-based materials, for example. Where thermal management is less of an issue, materials such as FR4
15 (flame retardant type 4) epoxy laminate, PTFE (poly-tetra-fluoro-ethylene) may be employed in alternative embodiments. In another embodiment, advantageous features from multiple technologies may be combined with use of FR4 having a layer of copper on both sides to provide a substrate 14 devised from familiar materials which may provide
20 heat conduction or a ground plane.

With reference to Fig. 3, depicted module 10 exhibits thermal extension 16T. Although typically depicted and preferably located at an end of substrate 14 where they are most conveniently disposed, a thermal extension off of substrate 14 may also diverge from the main body
25 substrate 14 between the ends of the substrate. Substrate 14 may exhibit one or more such extensions. Thermal extensions 16T may diverge from the central axis of the substrate in any of a variety of orientations and

need not be perpendicular in relation to the main body of the substrate and need not diverge to both sides of module 10. As will be further described, models of module 10 such as that shown in Fig. 3, predict thermal advantages for module 10 when compared to the well-known
5 planar module commonly employed in memory expansion applications. As those of skill will appreciate, thermal extensions 16T provide added surface area for substrate 14 and thus increase the area from which heat may flow or emanate from module 10. The primary vehicle for such thermal flow is convective as airflow typically assists module cooling but
10 those of skill will also recognize that the structure of substrate 14 with thermal extension 16T is likely to be conducive to a variety of means for heat to flow from module 10.

One advantageous methodology for efficiently assembling a circuit module 10 such as described and depicted herein is as follows. In a
15 preferred method of assembling a preferred module assembly 10, flex circuit 12 is placed flat and both sides populated according to circuit board assembly techniques known in the art. Flex circuit 12 is then folded about end 16A of substrate 14. Next, tooling holes 17 may be used to align flex 12 to substrate 14. Flex 12 may be laminated or
20 otherwise attached to substrate 14. Further, top surfaces 18_T of ICs 18 may be attached to substrate 14 in a manner devised to provide mechanical integrity or thermal conduction.

Fig. 4 is an enlarged view of the area around an end 16A of an exemplar module 10. Edge 16A of substrate 14 is preferably rounded for
25 insertion into an edge card connector. While a particular rounded configuration is shown, edge 16A may take on other shapes devised to mate with various connectors or sockets. The form and function of

various edge connectors are well know in the art. The depicted adhesive 30 and flex 12 may vary in thickness and are not drawn to scale to simplify the drawing. When assembled with the flex 12 and adhesive 30, the thickness measured between module contacts 20 falls in the range specified for the mating connector.

Fig. 5 depicts a plan view of module assembly 10 devised in accordance with a preferred embodiment of the present invention. Those of skill will recognize that module assembly 10 may replace traditional DIMMs employed in a large variety of systems. Module assembly 10 has flex circuit 12 wrapped about an edge 16A of substrate 14. ICs 18 are mounted to flex circuit 12 along the depicted side as described with reference to earlier Figs. Module contacts 20 are presented near edge 22 of module assembly 10 for connection to a card edge connector or socket. Optional extension 16T is shown in Fig. 5 along the upper part of depicted module 10.

Fig. 6 depicts a system 5 that employs two modules 10 and illustrates the use of multiple modules 10 in a system 5 in accordance with the present invention.

Modules 10 are shown inserted in card edge connectors 31 which are each deployed on circuit board 33. System 5 thus may be configured to provide memory expansion with features directed to minimization of thermal loading of modules 10.

Fig. 7 illustrates an alternative embodiment of the present invention in which substrate 14 includes flex support 14FS to support flex circuit 12 in its transition to the IC connective areas. Upper end 16B of substrate 14 is identified on the depicted module of Fig. 7 that lacks extensions 16T.

Fig. 8 depicts another embodiment having a clip. In this embodiment, clip 82 is depicted clipped around ICs 18. Clip 82 is preferably made of metal or other heat-conducting material. Preferably, clip 82 has trough 84 devised to mate with an end of substrate 14. The
5 attachment may further be accomplished with adhesive between clip 82 and substrate 14 or ICs 18.

Fig. 9 depicts another embodiment having a thinned portion of substrate 14. In this embodiment, substrate 14 has a first thickness 1 toward edge 16A devised to provide support for an edge and surrounding
10 area of module assembly 10 as may be needed for connection to an edge or other connector. Above the portion of substrate 14 with thickness 1 is a portion 92 having thickness 2. The narrower width of portion 92 is devised to narrow the total width of module assembly 10 and may provide for enhanced cooling airflow or more dense spacing of module
15 assemblies 10 in their operating environment.

Fig. 10 is a cross-sectional view of another preferred embodiment. The depiction is the view from above a module 10 looking downward. Substrate 14 is selectively thinned at portion 102 under device 19. Depicted device 19 has an exposed die 19D mounted on a substrate.
20 Other embodiments may have otherwise packaged or mounted integrated circuits or other devices with heights greater than the typical IC 18. In this embodiment, device 19 is taller or thicker than the other ICs 18 populating the flex 12. Thinned portion 102 of substrate 14 underneath device 19 accommodates the extra height so that flex 12 remains planar
25 and the upper surface of device 19 is in thermal contact with substrate 14. Substrate 14 may be manufactured for this, or other similar embodiments, with a variety of methods such as, for example, by being milled with a

CNC (computer numerical controlled) machine, or being extruded. This, and similar embodiments, may be employed to advantage, for example, to provide advantageous heat performance when device 19 is a FB-DIMM advanced memory buffer (AMB). Device 19 is preferably attached to substrate 14 with heat conductive adhesive.

Fig. 11 depicts another embodiment of the invention having additional layers of ICs 18. Flex circuitry 12 may be provided in this configuration with, for example, a split flex with layers interconnected with vias at portion 24 of flex 12. Further, two flex circuits may be used and interconnected by pad to pad contacts or inter-flex contacts, for example.

Fig. 12 depicts another embodiment having flex portions wrapped around opposing edges of substrate 14. Flex circuit 12 has connecting portion 12C wrapped around extension 16T of substrate 14. In a preferred methodology for assembling this embodiment, the depicted ICs 18 are first mounted to flex circuit 12. Flex portion 26 associated with IC 18A is placed in position relative to the substrate. Flex circuit 12 is then wrapped around edge 16A of substrate 14 a first time. Appropriate adhesive lamination or other techniques are used to attach flex 12 and ICs 18A and 18B to substrate 14. Connecting portion 12C of flex circuit 12 is wrapped around extension 16T. Adhesive may be used to make back-to-back connections between the depicted ICs 18. Lamination or other adhesive or bonding techniques may be used to attach the two layers of flex 12 to each other at flex portions 24. Further, the two layers of flex circuitry 12 wrapped around edge 16A may be interconnected by pad-to-pad contacts or inter-flex contacts. Flex 12 is wrapped again around edge

16A, putting IC 18C into position. IC 18D is positioned back-to-back with IC 18E and attached.

Fig. 13 depicts another embodiment having a flex portion wrapped around opposing edges of substrate 14. Flex circuit 12 has connecting
5 portion 12C wrapped around extension 16T of substrate 14. Connecting portion 12C preferably has more than one conductive layer, and may have three or four or more conductive layers. Such layers may be beneficial to route signals for applications such as, for example, a FB-DIMM which may have fewer DIMM input/output signals than a registered DIMM, but
10 may have more interconnect traces required amongst devices on the DIMM, such as, for example, the C/A copy A and C/A copy B (command/address) signals produced by an FB-DIMM AMB. While two sets of module contacts 20 are shown, other embodiments may have only one set.

15 Fig. 14 depicts a cross-sectional view of another alternative embodiment of the present invention. Flex circuit 12 exhibits contacts 20 proximal to opposing edges 192 of flex circuit 12. Connecting portion 12C of flex circuit 12 is wrapped about extension 16T of substrate 14. In a preferred methodology for assembling this embodiment, the depicted
20 ICs 18 are first mounted to flex circuit 12. Flex circuit 12 is wrapped about extension 16T of substrate 14 and preferably aligned to substrate 14 with tooling holes. Portion 24 of flex circuit 12 is preferably laminated to substrate 14.

Fig. 15 depicts an alternative embodiment of the present invention
25 in which ICs 18 are populated along only one side of flex circuit 12.

Fig. 16 depicts an alternative embodiment of the present invention having CSPs on what becomes the internal side of flex circuit 12 and thus placed between the flex circuit and substrate 14.

Fig. 17 depicts an alternative embodiment of the present invention
5 in which the flex circuit transits over an end 16B of substrate 14 opposite contacts 20.

Fig. 18 is a preferred embodiment of the present invention exhibiting multiple extensions 16T and thinned substrate 14 with indentations 92.

10 Figs. 19 and 20 depict an alternative embodiment of the present invention that employs a connector 200 to provide selective interconnection between portions 202A and 202B of flex circuit 12 associated respectively with lateral sides S_1 and S_2 of substrate 14. The depicted connector 200 has parts 200B and 200A that interconnect in
15 cavity 204 of substrate 14. One example of connector 200 is a 500024/50027 Molex connector but a variety of different connectors may be employed in embodiments of the invention. The depicted connector 200 is disposed in substrate cavity 204 and typically will have a first part 200A and a second part 200B which correspond to portions 202A and
20 202B of flex circuit 12, respectively.

Fig. 21 depicts an exemplar contact-bearing first side of a flex circuit devised in accordance with an alternative preferred embodiment of the present invention. As those of skill will understand, the depiction of Fig. 21 is simplified to show more clearly the principles of the invention.
25 An embodiment with more ICs 18 is shown earlier.

Fig. 22 depicts side 9 of flex circuit 12 of Fig. 21.

Fig. 23 depicts an exemplar substrate formed to be employed with the exemplar flex circuit depicted in Figs. 21 and 22. Flex circuit 12 is folded about substrate 14 shown in Fig. 23 to place ICs 18 along side 9 of flex circuit 12 into the windows 250 arrayed along substrate 14. This
5 results in ICs along rows ICR3 and ICR4 being disposed back to back within windows 250. Preferably, a thermally conductive adhesive or glue is used on the upper sides 18T of ICs 18 to encourage thermal energy flow as well as provide some mechanical advantages. This is merely one relative arrangement between ICs 18 on respective sides of substrate 14.

10 Fig. 24 depicts a view along the line A-A shown in Fig. 23 with flex circuit 12 combined with substrate 14. ICs 18 which are on second side 9 (which in this depiction is the inner side with respect to the module 10) of populated flex circuit 12 are disposed in windows 250 so that the upper surfaces 18_T of ICs 18 of row ICR3 are in close proximity with the
15 upper surfaces 18_T of ICs 18 of row ICR4. Thus, these first and second groups of ICs (CSPs in the depiction) are positioned in the cutaway areas of the first and second lateral sides, respectively, of substrate 14. In this case, the cutaway areas on each lateral side of substrate 14 are in spatial coincidence to create windows 250. Those of skill will recognize that the
20 depiction is not to scale but representative of the interrelationships between the elements and the arrangement results in a profile "P" for module 10 that is significantly smaller than it would have been without fitting ICs 18 along inner side 9 of flex circuit 12 into windows 250. Profile P in this case is approximately the sum of the distances between
25 the upper and lower surfaces of IC 18 plus 4X the diameter of the BGA contacts 63 plus 2X the thickness of flex circuit 12 in addition to any adhesive layers 30 employed to adhere one IC 18 to another. This profile

dimension will vary depending upon whether BGA contacts 63 are disposed below the surface of flex circuit 12 to reach an appropriate conductive layer or contacts which typically are a part of flex circuit 12.

5 Fig. 25 is another depiction of the relationship between flex circuit 12, and a substrate 14 which has been patterned with cutaway areas. The view of Fig. 25 is taken along a line that would intersect the bodies of ICs 18. In Fig. 25, as those of skill will recognize, ICs 18 that comprise row or group ICR3 are staggered relative to those that comprise row or group ICR4 of second side 9 of flex circuit 12 when module 10 is assembled

10 and flex circuit 12 is combined with substrate 14. This staggering may result in some construction benefits providing a mechanical "step" for ICs 18 as they are fitted into substrate 14 and may further provide some thermal advantages increasing the contact area between substrate 14 and the plurality of ICs 18.

15 Fig. 26 depicts exemplar substrate 14 employed in Fig. 25 before being combined with populated flex circuit 12 as viewed along a line through windows 250 of substrate 14. As depicted in Fig. 26, a number of cutaway areas or pockets are delineated with dotted lines and identified with references 250B3 and 250B4, respectively. Those areas identified as

20 250B3 correspond, in this example, to the pockets, sites, or cutaway areas on one side of substrate 14 into which ICs 18 from ICR3 of flex circuit 12 will be disposed when substrate 14 and flex circuit 12 are combined. Those pocket, sites, or cutaway areas identified as references 250B4 correspond to the sites into which ICs 18 from ICR4 will be disposed. In

25 alternate embodiments, there may be more than one row of ICs 18 disposed on a single side of substrate 14.

For purposes herein, the term window may refer to an opening all the way through substrate 14 across span "S" which corresponds to the width or height dimension of packaged IC 18, or it may also refer to that opening where cutaway areas on each of the two sides of substrate 14 overlap.

Fig. 27 depicts a planar view of the substrate 14 previously depicted in Fig. 26. Where cutaway areas 250B3 and 250B4 overlap, there are, as depicted, windows all the way through substrate 14. In some embodiments, cutaway areas 250B3 and 250B4 may not overlap or in other embodiments, there may be pockets or cutaway areas only on one side of substrate 14. Those of skill will recognize that cutaway areas such as those identified with references 250B3 and 250B4 (as well as windows in substrate 14) may be formed in a variety of ways depending on the material of substrate 14 and need not literally be "cut" away but may be formed by a variety of molding, milling and cutting processes as is understood by those in the field.

Fig. 28 is an enlarged view of a portion of one preferred embodiment showing lower IC 18_1 and upper IC 18_2. In this embodiment, conductive layer 66 of flex circuit 12 contains conductive traces connecting module contacts 20 to BGA contacts 63 on ICs 18_1 and 18_2. Where needed, the number of layers may be devised in a manner to achieve the bend radius required in those embodiments that bend flex circuit 12 around edge 16A or 16B, for example, although the assignee has determined that flex circuitry with four conductive layers may be bent as needed about appropriately shaped ends of substrate 14. As will be later shown, holes or vias in appropriate locations of flex 12 assist is creating conformal bends in flex 12 where needed. The number of layers

in any particular portion of flex circuit 12 may also be devised to achieve the necessary connection density given a particular minimum trace width associated with the flex circuit technology used. Some flex circuits 12 may have three or four or more conductive layers. Such layers may be
5 beneficial to route signals for applications such as, for example, a FB-DIMM which may have fewer DIMM input/output signals than a registered DIMM, but may have more interconnect traces required amongst devices on the DIMM.

In this embodiment, there are three layers of flex circuit 12
10 between the two depicted ICs 18_1 and 18_2. Conductive layers 64 and 66 express conductive traces that connect to the ICs and may further connect to other discrete components. Preferably, the conductive layers are metal such as, for example, copper or alloy 110. Vias such as the exemplar vias 23 connect the two conductive layers 64 and 66 and thereby enable
15 connection between conductive layer 64 and module contacts 20. In this preferred embodiment having a three-layer portion of flex circuit 12, the two conductive layers 64 and 66 may be devised in a manner so that one of them has substantial area employed as a ground plane. The other layer may employ substantial area as a voltage reference plane. The use of
20 plural conductive layers provides advantages and the creation of a distributed capacitance intended to reduce noise or bounce effects that can, particularly at higher frequencies, degrade signal integrity, as those of skill in the art will recognize. If more than two conductive layers are employed, additional conductive layers may be added with insulating
25 layers separating conductive layers.

Fig. 29 is an exploded depiction of a flex circuit 12 cross-section according to one preferred embodiment of the present invention. The

depicted flex circuit 12 has four conductive layers 701-704 and seven insulative layers 705-711. The numbers of layers described are merely those used in one preferred embodiment and other numbers of layers and arrangements of layers may be employed. Even a single conductive layer
5 flex circuit 12 may be employed in some embodiments, but flex circuits with more than one conductive layer prove to be more adaptable to more complex embodiments of the invention.

Top conductive layer 701 and the other conductive layers are preferably made of a conductive metal such as, for example, copper or
10 alloy 110. In this arrangement, conductive layers 701, 702, and 704 express signal traces 712 that make various connections by use of flex circuit 12. These layers may also express conductive planes for ground, power or reference voltages.

In this embodiment, inner conductive layer 702 expresses traces
15 connecting to and among various devices mounted on the secondary substrates 21. The function of any one of the depicted conductive layers may be interchanged in function with others of the conductive layers. Inner conductive layer 703 expresses a ground plane, which may be split to provide VDD return for pre-register address signals. Inner conductive
20 layer 703 may further express other planes and traces. In this embodiment, floods or planes at bottom conductive layer 704 provides VREF and ground in addition to the depicted traces.

Insulative layers 705 and 711 are, in this embodiment, dielectric solder mask layers which may be deposited on the adjacent conductive
25 layers for example. Other embodiments may not have such adhesive dielectric layers. Insulating layers 706, 708, and 710 are preferably flexible dielectric substrate layers made of polyimide. However, any

suitable flexible circuitry may be employed in the present invention and the depiction of Fig. 29 should be understood to be merely exemplary of one of the more complex flexible circuit structures that may be employed as flex circuit 12.

5 Fig. 30 depicts an alternate preferred embodiment of a module 10 in accordance with the invention that differs from the embodiment earlier shown in Fig. 3 in that instead of the single flex circuit 12 employed in the embodiment depicted in Fig. 3, the embodiment of Fig. 30 employs two flex circuits identified as 12A and 12B. Each of flex circuits 12A 10 and 12B are populated with ICs 18 on one or both of their respective sides 8 and 9. Either or both of flex circuits 12A and 12B may employ adjunct circuits 19 such as, for example, buffers, sensors, or registers, AMBs, and PLL's for example on either of their respective sides. Those of skill will recognize that modules devised in accord with the principles 15 of the invention may be populated with a variety of ICs including, for example, but not limited to, memory devices, ASICs, microprocessors, video specific microprocessors, RF devices, other logic and FPGAs. As those of skill will recognize, various embodiments may be devised to implement a variety of electrical or topologically-identified modules 20 including but not limited to registered DIMMs, unregistered DIMMs, SO-DIMMs, SIMMs, video modules, FB-DIMMs with AMBs, PCMCIA modules and cards, and other modules. A few of the relevant applications for modules devised in accordance with the invention include servers, desktop computers, video cameras, televisions, and personal 25 communication devices.

Those of skill will therefore recognize that the present invention can be adapted to express iterations of a variety of modules to provide

improved thermal performance and where convenience in manufacturing or minimization of profile are of high value. When a video card or other specialized module that includes a microprocessor or computing logic is devised in accordance with the present invention, one or more of depicted
5 circuits 19 can be considered a microprocessor.

With reference to the embodiment depicted in Fig. 30, each of flex circuits 12A and 12B has module contacts 20 positioned in a manner devised to fit in an edge connector or socket 31 and connect to corresponding contacts in the connector. Edge connector or socket 31 is,
10 as those of skill will recognize, typically a part of a computer 33.

Fig. 31 depicts a conventional DIMM module 11 populated with ICs 18B in a strategy sometimes called "planar" by those of skill in the art. The subsequent tables provide a comparison between an exemplar module 11 such as depicted is Fig. 31 and an exemplar module 10 in
15 accordance with a preferred embodiment of the present invention and devised in accordance with Fig. 3. As the tables demonstrate, there is substantially less thermal variation from IC-to-IC in module 10 (Fig. 3) than is found in a module such as is depicted in Fig. 31 under like conditions. The following data was derived by Staktek Group L.P., the
20 present assignee of this invention using modeling techniques familiar to those in the field.

The following tables should be interpreted with reference to Fig. 32. Fig. 32 depicts a schematic of an embodiment of a module 10 in which the positions of the plural ICs of an exemplar module 10 are
25 identified to assist in understanding the subsequent tables of this disclosure. For example, the IC 18 identified by specific reference in Fig. 32 is located at site 4 (reference "ST4") of the outer side (reference "0")

of side 1 of the module. Airflow 40 is identified in Fig. 32 and will be quantified in subsequent tables. Positions or sites identified in Fig. 32 also identify corresponding sites in the module 11 evaluated in the tables below identified with the suffix "B". The tables are organized to provide
5 ready comparison between an exemplar module 11 (as exemplified by Fig. 31) and an exemplar module 10 (as exemplified by Fig. 3) under the same modeled conditions. Table 1A relates data taken from a model of an exemplar module 10 (exemplified by Fig. 3) while table 1B relates data derived from taken from a model exemplar module 11 exemplified
10 by the depiction of Fig. 31. As the data tables below relate, the models predict surprising and substantial differences in over all temperature and IC-to-IC temperature variation between a model of a module 10 devised in accordance with Fig. 3 (with a thermal extension on the substrate) with CSPs 18 and a model of a module 11 devised in accordance with Fig. 31
15 with ICs 18B under the commonly-known planar strategy. Those of skill will recognize that the predicted improvement in thermal conditions including reduced temperature variation from IC-to-IC in the exemplified and analyzed module 10 over that predicted for the exemplar module 11 should lead to reduced thermally-induced skew variation which would
20 have salutary effects upon timing performance and timing eye tolerances for modules devised in accordance with Fig. 3 with a thermally conductive substrate 14. Models that do not exhibit thermal extension 16T do not show such notable improvement in thermal performance but should exhibit the density and expected durability improvements.
25 Exemplar modules such as those shown in Figs. 18, 19, and 30, for example, can be expected, however, to demonstrate even more enhanced thermal performance characteristics. Those of skill will recognize that

such improvements should also be expected with use of other substrates of thermally conductive and metallic materials such as, for example, copper or copper alloys. In addition to metallic materials, substrate 14 may also be devised from other thermally conductive materials such as,
5 for example, carbon based materials or thermally conductive plastics.

Table 1A below relates thermal data derived from a modeled embodiment devised in accord with module 10 as described herein. The exemplar module 10 was modeled as being populated with plural Micron Technologies DDR2 (11X19) devices as ICs 18. In this instance, two
10 modules 10 were modeled to be operating side to side with a 10 mm module pitch. Substrate 14 was comprised of aluminum and exhibited a topology exemplified by the depiction of Fig. 3. In the model, airflow 40 moved at 2 m/sec. at 35°C while one rank of ICs 18 was operating at 0.38 watts per IC while the other rank was operating at 0.05 watts per IC.

Table 1A

Two Modules 10 (Fig. 3) Side to Side, 10 mm pitch, Aluminum Substrate
.38 W per device on one Rank, .05 W per device on other Rank
35 C air at 2 m/s

DIMM #1											
Side 1	*Site 1*	*Site 2*	*Site 3*	*Site 4*	*Site 5*	*Site 6*	*Site 7*	*Site 8*	*Site 9*	*Registers*	*PLL*
Outer	48.6	51.4	53.2	54.6	59.0	59.6	60.3	61.0	61.2	62.2	
Inner	54.0	55.8	57.5	58.9	62.0	63.0	63.8	64.2	64.2	64.9	68.1
Inner	53.6	55.5	57.2	58.6	61.5	62.6	63.4	63.8	63.8	64.7	
Outer	55.0	58.8	60.8	62.4	63.6	65 9	67.1	67.7	68.0	62.6	
Side 2											

DIMM #2											
Side 1											
Outer	48.4	51.3	53.0	54.3	57.9	58.6	59.4	60.0	60.3	63.3	
Inner	54.1	55.9	57.6	59.1	62.2	63.3	64.1	64.6	64.6	64.6	68.0
Inner	53.7	55.7	57.4	59.0	62.0	63.2	64.1	64.6	64.6	65.2	
Outer	55.5	58.9	61.0	62.8	65.4	67.5	68.8	69.6	69.9	63.4	
Side 2	*Site 1*	*Site 2*	*Site 3*	*Site 4*	*Site 5*	*Site 6*	*Site 7*	*Site 8*	*Site 9*		

Maximum DRAM TEMP, C	69.9
Minimum DRAM TEMP, C	48.4
RANGE, C	21.5

Table 1B below relates thermal data for an exemplar model module 11 devised in accordance with Fig. 31 operating under the same conditions as those modeled in Table 1A.

Table 1B

Two Modules 11 (Planar -DIMM configuration, Fig. 31), Side to Side, 10 mm pitch
.38 W per device on one Rank, .05 W per device on other Rank
35 C air at 2 m/s

DIMM #1 Side 1	*Site 1*	*Site 2*	*Site 3*	*Site 4*	*Site 5*	*Site 6*	*Site 7*	*Site 8*	*Site 9*	*Registers*	*PLL*
TOP	50.6	53.9	56.3	58.5	62.7	63.9	64.9	65.5	65.1	63.3	
BOTTOM	58.2	62.1	64.7	66.6	70.4	72.6	72.9	73.1	73.1	64.3	72.0
TOP	58.2	62.4	64.9	66.9	70.4	72.0	72.9	73.0	72.5	63.9	
BOTTOM	50.4	53.7	56.1	57.8	61.0	63.0	64.1	64.7	64.4	64.4	
Side 2											

DIMM #2 Side 1	*Site 1*	*Site 2*	*Site 3*	*Site 4*	*Site 5*	*Site 6*	*Site 7*	*Site 8*	*Site 9*	*Registers*	*PLL*
TOP	50.5	53.8	56.2	58.3	62.1	63.2	64.1	64.5	63.9	63.0	
BOTTOM	58.0	62.0	64.6	66.4	69.4	71.6	72.8	73.0	72.8	63.8	71.6
TOP	58.3	62.3	64.9	67.0	70.9	72.6	73.0	73.0	73.1	64.0	
BOTTOM	50.4	53.7	56.1	58.0	61.6	63.5	64.8	65.4	65.2	64.8	
Side 2											

Maximum DRAM TEMP, C	73.1
Minimum DRAM TEMP, C	50.4
RANGE, C	22.7

Fig. 33 depicts a module 10 according to another embodiment of the present invention. In this embodiment, module 10 is provided with a thermal sensor 191 mounted along inner side 9 of flex circuit 12. In the depiction of Fig. 33, even though showing side 8 of flex 12, the location of sensor 191 is depicted so that its location is understood in relation to the external view of module 10 provided in Fig. 33. Thermal sensor 191 is thermally coupled to substrate 14 in a manner devised to allow thermal measurements of substrate 14. Such arrangement is used to advantage in embodiments having a thermally-conductive substrate 14, such as those

made of copper, nickel, aluminum, carbon-based materials or thermally conductive plastic, for example. When ICs 18 along inner side 9 of flex circuit 12 are also thermally coupled to substrate 14, the temperature of substrate 14 will tend to match that of ICs 18.

5 In some embodiments, thermal sensor 191 may be integrated into a buffer (such as an AMB, for example) or a register. For example, some FB-DIMM systems may employ one or more AMBs having an integrated thermal sensor. In such a module, one of the AMBs may be mounted along inner side 9 of flex circuit 12 and thermally coupled to substrate 14. 10 The thermal reading taken from such an AMB may be used by the host system as a more accurate indication of module IC temperature than thermal readings taken from AMBs mounted along outer side 8.

In embodiments configured to have more than one DIMM instantiation on a single module, a thermal sensor mounted along inner 15 side 9 of flex circuit 12 may provide readings to be employed for one or more DIMM instantiations mounted along outer side 8. For example, one module may have four DIMM instantiations, two disposed adjacent to substrate 14 and two disposed along an outer side of flex circuitry away from substrate 14. Such a module may have two thermal sensors 191 20 thermally coupled to substrate 14, one on either side. Each thermal sensor may provide a reading for the two DIMM instantiations at their respective sides of substrate 14. Alternatively, one thermal sensor may provide readings for all four DIMM instantiations.

Fig. 34 depicts a cross-section view of another embodiment of the 25 present invention. Thermal sensor 191 and one of the depicted ICs 18 are thermally coupled to substrate 14 with thermally-conductive adhesive 30. Typically, other ICs 18 will be mounted to flex circuit 12 in addition to

thermal sensor 191. In this embodiment, IC 18 and thermal sensor 191 have a similar thickness or height above the depicted flex circuitry 12. Other embodiments may be made with a thermal sensor having a height greater or less than ICs 18. Such a height difference may be adjusted by
5 thermally conductive spacer such as, for example, a piece of copper or other metal. The height difference may also be adjusted by a fill of thermally conductive adhesive, the fill devised to dispose both ICs 18 and thermal sensor 191 in thermal connection to substrate 14. Arrow 202 in Fig. 34 shows flow of heat out of the depicted ICs 18 and into substrate
10 14. Arrow 204 shows flow of heat from substrate 14 to thermal sensor 191. Arrow 205 depicts a flow of thermal energy from an IC 18_1 to an IC 18_2. The disposition of ICs 18_1 and 18_2 opposite each other and separated by the flex circuitry 12 tends to encourage the flow of thermal energy from the one of the pair composed of IC 18_1 and IC 18_2 that is in the ON
15 state to the one of the pair that is in the quiescent or OFF state.

Fig. 35 is an elevation view of inner side 9 of a flex circuit 12 according to another embodiment of the present invention. Thermal sensor 191 is mounted along inner side flex circuit 12, and then flex circuit 12 is wrapped about the edge of substrate 14 to place the depicted
20 side adjacent to the substrate. While in this embodiment only one flex circuit is used, in other embodiments, such as that depicted in Fig. 30, two or more flex circuits may be combined with substrate 14 to form a module. In such embodiments, one or more thermal sensors 191 may be mounted to each flex circuit, or one thermal sensor may adequately
25 measure thermal status for circuitry along both sides of substrate 14 by being thermally coupled to substrate 14.

Fig. 36 is a block diagram depicting sensor signals according to one embodiment of the present invention. Depicted is block 14 representing substrate 14. Arrows 202 and 204 show heat flow from ICs 2203 to substrate 14 and from substrate 14 to thermal sensor 191. ICs 2203 are preferably groups or ranks of ICs, but may be other or single ICs. As described above, ICs 2203 may be coupled directly or indirectly to substrate 14. For example, ICs 2203 may have surfaces thermally adhered to substrate 14 or may be coupled through flexible circuitry and other ICs. ICs 2203 or thermal sensor 191 may also be disposed in cutout portions of substrate 14.

Thermal sensor 191 contains a transducer to transform a temperature signal into an electrical signal. Thus it provides a signal related to a thermal condition of the module. Heat sensor transducers are well known in the art. Many such transducers produce an analog voltage or current proportional to the measured temperature. The analog signal is preferably converted to a digital thermal signal 2202 at the output of thermal sensor 191. Other arrangements may be used. For example, signal 2202 may be an analog signal which is converted for processing elsewhere in module 10 or at circuitry outside of module 10 or a sensor with a digital output may be employed.

The depicted thermal signal 2202 is shown connected to monitoring circuitry 2204 for four DIMM instantiations 2203. In this embodiment, four instantiations of DIMM circuitry such as, for example, FB-DIMM circuitry or registered DIMM circuitry are mounted to flex circuitry in a single module 10. The depicted single thermal sensor provides thermal measurement for controlling and monitoring all four depicted instantiations. In other embodiments, signal 2202 may instead

or additionally connect to a system monitor or other control circuitry for receiving and processing thermal monitoring signals. Such circuitry may be part of module 10 or may be located as part of the system in which module 10 is installed.

5 Those of skill in the art will recognize, after appreciating this specification, that more than one thermal sensor 191 may be arranged to monitor thermal status of circuitry in a module 10. For example, a thermal sensor 191 may supply a thermal measurement signal 2202 for two ranks of ICs, one thermally mounted to each side of substrate 14. 10 Such an embodiment may be used to advantage, for example, in systems having variations in thermal conditions from one location to another or from one IC rank to another. In a system employing FB-DIMM circuitry, DIMM instantiations closer to the system memory controller typically have greater signaling through their AMBs than do DIMM instantiations 15 further from the system memory controller. If such DIMM instantiations are present together on a module 10, there may be control advantages in providing separate thermal measurements associated with each DIMM instantiations, or associated with circuitry along either side of substrate 14.

20 Fig. 37 depicts another preferred embodiment of a module 10 in accordance with the present invention. The depiction of Fig. 37 shows a module 10 similar to that shown earlier in Fig. 3 thermally connected to a chassis or box 24 through thermal conduit 22. Chassis or box 24 functions as a thermal sink for thermal energy from module 10. Thermal 25 conduit 22 participates in the thermal connection between substrate 14 and chassis 24. Thermal conduit 22 may be any material that allows thermal energy to flow between module 10 and chassis or box 24.

Preferably, thermal conduit 22 is comprised of a material that provides some compliance and resilience to compression. This increases the reliability of the thermal path between module 10 and chassis 24 while reducing the possibility of damaging physical forces upon module 10. As shown, thermal conduit 22 is, at least in part, between substrate 14 and chassis component 24.

In the depiction of Fig. 37, thermal conduit 22 is a spring but, as those of skill will recognize upon appreciation of this disclosure, thermal conduit 22 may be any of a variety of thermally conductive materials and thermal conduit 22 need not be compliant. In some embodiments, the system of the invention may even realize contact between substrate 14 of module 10 and chassis 24 without an intermediate thermal conduit. Those of skill will recognize, however, the preference for a compliant intermediary element as a thermal conduit 22. Some examples of appropriate thermal conduit materials include springs, electromagnetic radiation gaskets, thermally conductive materials from the Bergquist company or other suppliers of thermally conductive materials.

In a preferred mode, substrate 14 and its optional, but preferred, extension 16T of module 10 are comprised of thermally conductive materials such as, for example, copper, aluminum, or metallic alloys or carbon-based materials or thermally conductive plastic, for example. The use of metallic materials for substrate 14 has additional advantages such as enhanced strength as well as thermal management advantages. Those of skill will recognize that thermal extension 16T is preferably, but need not be of a contiguous piece with substrate 14 and may, consequently, be considered a part of substrate 14 in either case. As has been shown in earlier cross-sectional views, at least some of the ICs are in direct thermal

communication with substrate 14 and, consequently, can shed thermal energy directly into substrate 14. Other of the resident ICs of module 10 can shed thermal energy into flex 12 which, as those of skill will recognize, may be constructed to enhance thermal conduction into
5 substrate 14.

Fig. 38 is a cross-sectional view of a system 5 devised in accordance with the present invention. The depicted system 5 comprises a module 10 and a chassis component 24 into which thermal energy from module 10 is shunted to chassis component 24 through substrate 14 of
10 module 10 and, in the depicted embodiment, thermal conduit 22 that participates in the thermal connection between substrate 14 and chassis component or box 24. Chassis component 24 will typically be a part of a computing system and may be, for example, a shelf or extension of a larger chassis or box of a computer system such as a general purpose PC.
15 As another example, it may be a part of a server or larger computer chassis or box or it may be a metallic extension, sheet, or bracket connected to a chassis structure in a smaller computing application such as, for example, a notebook computer or a mobile field computer or computing platform of specialized application.

20 The cross-sectional view of Fig. 38 is taken through ICs 18 of module 10 which are disposed in the depicted embodiment on either side of sides S1 and S2 of substrate 14 of module 10. In the depicted system 5, module 10 is shown inserted into edge connector 31 that is resident on board 33. Edge connector 31 is familiar to those of skill in the art and, as
25 shown, it is typically employed on a board 33 such as a motherboard in a computer. As those of skill will recognize, there is some inherent but minor thermal energy flow between module 10 and board 33 through

edge connector 31 but such practitioners should also recognize that such thermal energy flow through edge connector 31 is not the thermal connection highlighted in the present application.

Substrate 14 makes contact with thermal conduit 22 through
5 thermal extension 16T. Thermal conduit 22 is a gasket like material in this depiction and is disposed along the lower side 24L of chassis component 24. The gasket material of the particular thermal conduit 22 shown in this Fig. 38, may be, as an example, an electromagnetic radiation gasket material, for example.

10 Upper surface 18_T of at least some of ICs 18 are employed in the depiction of Fig. 38 to attach the IC-populated flex circuit 12 to substrate 14 of module 10. Preferably, thermal glues or adhesives are used for such attachment. Substrate 14 has a first perimeter edge identified as 16A and a second limit depicted in the depiction of Fig. 38 as thermal
15 extension 16T and those of skill will recognize that a thermal extension 16T can be devised in a variety of shapes. Alternatively, substrate 14 may have merely a second edge with no extension or shaping features.

The thermally conductive material of substrate 14 encourages extraction of thermal energy from the CSPs of the module. Flex circuit
20 12 may be particularly devised to operate as a heat spreader or sink adding to the thermal conduction out of ICs 18 and 19. In another embodiment, advantageous features from multiple technologies may be combined with use of FR4 having a layer of copper on both sides to provide a substrate 14 devised to take advantage of the principles of the
25 invention. Other embodiments may combine in a module 10, traditional construction materials such as FR4 with metallic materials in a substrate

to take better advantage of the benefits of the present invention, but still employ traditional connective strategies.

Fig. 39 depicts a system 5 that employs an alternative embodiment module 10 with secondary substrates 21A and 21B. Such secondary substrates are populated in the depiction with ICs 18 and may be comprised of PCB materials although other materials known in the art may be employed. For example, secondary substrate 21 may be provided by the rigid portion of an integrated rigid flex structure that provides mounting fields for ICs 18, ICs 19 and other circuitry such as registers and PLLs for example and a flexible portion that transits about primary substrate 14 or extends, for example, to flex edge connectors 20. In depicted embodiment, secondary substrates 21A and 21B are connected to connectors 23 which are connected to contacts 20 as will be understood by those of skill in the art with techniques such as flex or layered connectives or even portions of traditional circuit board substrate. Module 10 of system 5 of Fig. 39 is shown in thermal connection with thermal conduit 22 along underside 24L of chassis component 24 which is depicted as a shelf extension of larger chassis body 24B.

Fig. 40 depicts an embodiment of system 5 that employs two modules 10 to illustrate the use of multiple modules 10 in a system 5 in accordance with the invention.

In system 5, thermal extensions 16T of modules 10 are in thermal connection with thermal conduit 22 along underside 24L of a chassis component which may be an extension of a larger chassis body. Thermal conduit 22 may, in preferred modules, be electromagnetic radiation gasket material, for example or, alternatively, modules 10 may be in

direct contact with a part of a chassis within which the modules are employed.

Fig. 41 depicts another embodiment of system 5 that includes a module 10 that employs fewer ICs 18. In the depicted module 10,
5 substrate 14 is made of FR4 but has a copper core and includes copper layers 26 and core 28 that cooperates with thermal extension 16T to shunt thermal energy to chassis or box 24. Such a depiction is offered to help those of skill understand that a large variety of construction combinations for modules can employ the principles of the invention to advantage.

10 Fig. 42 depicts a cross-sectional view of another embodiment of a thermal management system 5 that employs a module 10 inserted into a card edge connector. Module 10 employs an IC 19 and has a deformation, contour, or dimple 15 that creates space 15S which is accommodative of IC 19 which may be, in the depicted embodiment of
15 module 10 a device of taller profile such as, for example, a buffer such as an AMB, for example, in a FB-DIMM or a graphics engine in a graphics module. Substrate 14 need not be of uniform thickness and examples of substrates with thicknesses that vary along the course of the substrate have been shown. Substrate 14 of module 10 of Fig. 42 is in contact with
20 thermal conduit 22 through thermal extension 16T and thermal conduit 22 is shown in contact with chassis or box component 24.

The large capacity provided by some embodiments may be employed to provide multiple DIMM circuits on a single module. For example, the constituent devices including ICs 18 and multiple circuits 19
25 articulated as AMBs can be combined to create dual fully-buffered DIMMs on a single module 10.

Fig. 43 depicts a plan view of a module devised to express more than one instance of a FB-DIMM circuit on a single module 10. Circuit 19 is depicted as an AMB. Those of skill will appreciate that modules 10 configured as a single FB-DIMM will be readily constructed using the
5 principles of the invention.

Fig. 44 illustrates side 8 of a flex circuit 12 as having first and second fields F1 and F2. Each of fields F1 and F2 have at least one mounting contact array for CSPs such as the one depicted by reference 11A. Contact arrays such as array 11 are disposed beneath ICs 18 and
10 circuits 19. An exemplar contact array 11A is shown as is exemplar IC 18 to be mounted at contact array 11A as depicted.

Field F1 of side 8 of flex circuit 12 is shown populated with a first plurality of CSPs IC_{R1} and a second plurality of CSPs IC_{R2}, while second field F2 of side 8 of flex circuit 12 is shown populated with a first
15 plurality of CSPs IC_{R1} and a second plurality of CSPs IC_{R2}. Those of skill will recognize that the identified pluralities of CSPs are, when disposed in the configurations depicted, typically described as "ranks". Between the ranks IC_{R2} of field F1 and IC_{R2} of field F2, flex circuit 12 exhibits a plurality of module contacts allocated, in this embodiment, into
20 two rows (C_{R1} and C_{R2}) of module contacts 20. When flex circuit 12 is folded as later depicted, side 8 depicted in Fig. 44 is presented at the outside of module 10. The opposing side 9 of flex circuit 12 is on the inside in several depicted configurations of module 10 and thus side 9 is closer to the substrate 14 about which flex circuit 12 is disposed than is
25 side 8. As shown, other embodiments may have other numbers of ranks and combinations of plural CSPs connected to create an embodiment of the present invention.

Fig. 45 shows side 9 of flex circuit 12 depicting the other side of the flex circuit shown in Fig. 44. Side 9 of flex circuit 12 is shown as being populated with multiple CSPs 18. Side 9 includes fields F1 and F2 that each include at least one mounting contact array site for CSPs and, in
5 the depicted case, include multiple contact arrays. Each of fields F1 and F2 include, in the depicted preferred embodiment, two pluralities of ICs identified in Fig. 3 as IC_{R1} and IC_{R2}. Thus, each side of flex circuit 12 has, in a preferred embodiment, two fields F1 and F2 each of which fields includes two pluralities or ranks of CSPs IC_{R1} and IC_{R2}. In later Fig. 46,
10 it will be recognized that fields F1 and F2 will be disposed on different sides of substrate 14 in a completed module 10 when ICs 18 are identified according to the organizational identification depicted in Figs. 44 and 45. Those of skill will recognize, however, that the groupings of ICs 18 shown in Figs. 44 and 45 are not dictated by the invention but are
15 provided merely as an exemplar organizational strategy to assist in understanding the present invention. Various discrete components such as termination resistors, bypass capacitors, and bias resistors, in addition to the buffers 19 shown on side 8 of flex circuit 12.

Fig. 44 depicts an exemplar conductive trace 21 connecting row
20 C_{R2} of module contacts 20 to ICs 18. Those of skill will understand that there are many such traces in a typical embodiment. Traces 21 may also connect to vias that may transit to other conductive layers of flex 12 in certain embodiments having more than one conductive layer. In a preferred embodiment, vias connect ICs 18 on side 9 of flex 12 to module
25 contacts 20. An example via is shown as reference 23. Traces 21 may make other connections between the ICs on either side of flex 12 and may traverse the rows of module contacts 20 to interconnect ICs. Together the

various traces and vias make interconnections needed to convey data and control signals amongst the various ICs and buffer circuits.

Fig. 46 is a cross section view of a module 10 devised in accordance with a preferred embodiment of the present invention. 5 Module 10 is populated with ICs 18 having top surfaces 18_T and bottom surfaces 18_B. Substrate or support structure 14 has first and second perimeter edges 16A and 16B appearing in the depiction of Fig. 46 as ends. Substrate or support structure 14 typically has first and second lateral sides S_1 and S_2. Flex 12 is wrapped about perimeter edge 16A of 10 substrate 14.

In a typical FB-DIMM system employing multiple FB-DIMM circuits, the respective AMB's from one FB-DIMM circuit to another FB-DIMM circuit are separated by what can be conceived of as three impedance discontinuities as represented in the system depicted in Fig. 47 15 as D1, D2, and D3. Fig. 47 includes two modules 10F and 10S and includes a representation of the connection between the two modules. Discontinuity D1 represents the impedance discontinuity effectuated by the connector-socket combination associated with the first module 10F. Discontinuity D2 represents the impedance perturbation effectuated by 20 the connection between the connector-socket of first module 10F and the connector-socket of second module 10S, while discontinuity D3 represents the discontinuity effectuated by the connector-socket combination associated with the second module 10S. The AMB is the new buffer technology particularly for server memory and typically 25 includes a number of features including pass-through logic for reading and writing data and commands and internal serialization capability, a data bus interface, a deserialing and decode logic capability and clocking

functions. The functioning of an AMB is the principal distinguishing hard feature of a FB-DIMM module. Upon appreciating this specification, those of skill will understand how to implement the connections between ICs 18 and AMB 19 in FB-DIMM circuits
5 implemented by embodiments of the present invention and will recognize that the present invention provides advantages in capacity as well as reduced impedance discontinuity that can hinder larger implementations of FB-DIMM systems. Further, those of skill will recognize that various principles of the present invention can be employed to realize one or
10 more FB-DIMM circuits on a module.

In contrast to the system represented by Fig. 47, Fig. 48 is a schematic representation of the single impedance perturbation DX effectuated by the connection between a first AMB 19 of a first FB-DIMM "FB1" of a first module 10F and a second AMB 19 of a second
15 FB-DIMM "FB2" of the same first module 10F.

Fig. 49 depicts another embodiment of the present invention illustrating a configuration for a module 10 devised using stacks to create a module 10 presenting two FB-DIMM circuits. Those of skill will appreciate that using stacks such as depicted stacks 40 owned by Staktek
20 Group L.P. allows creating modules with high capacity. Stacks 40 are just one of several stack designs that may be employed with the present invention. Exemplar stacks 40 are devised with mandrels 42 and stack flex circuits 44 as disclosed in U.S. Pat. App. No. 10/453,398, filed June 6, 2003, now US Pat. No. 6,914,324 B2, issued July 5, 2005 which is
25 owned by Staktek Group L.P. and stacks 40 and AMB 19 are mounted on flex circuit 12 which is disposed about substrate 14.

Fig. 50 depicts another embodiment configuration using stacks in an embodiment of the present invention. Such an embodiment presents an FB-DIMM circuit at its contacts 20.

Fig. 51 illustrates another embodiment of the present invention.
5 The depicted module 10 has at least one AMB and associated circuitry such as ICs 18 which in the preferred mode and as illustrated are CSPs and needed support circuitry to create at least one FB-DIMM circuit or instantiation on a module 10 with a relatively low profile. It should be understood that a second AMB in addition to the one shown may be
10 disposed on either side of module 10 but, where employed, a second AMB preferably will be disposed closer to lateral side S2 of substrate 14 than is the depicted AMB 19 but will be preferably disposed on side 8 of flex circuit 12. In this embodiment, contacts 20 are along side 8 of flex circuit 12 and proximal to an edge E of flex circuit 12. The principal
15 circuits that constitute a FB-DIMM circuitry or instantiation (i.e., the CSPs and AMB) may be disposed in single rank file or distributed on both sides of substrate 14. They may be allocated to first and second mounting fields of the first and second sides of flex circuit 12 as earlier described with reference to earlier Figs. Those of skill will recognize that
20 contacts 20 may appear on one or both sides of module 10 depending on the mechanical contact interface particulars of the application.

Fig. 52 depicts a first side 8 of flex circuit 12 used in constructing a module according to another embodiment of the present invention. ICs 18 on flexible circuit 12 are, in this embodiment, chip-scale packaged
25 memory devices of small scale. Circuit 19 depicted between ICs 18 may be a memory buffer or controller such as, for example, an AMB, but in this embodiment is a memory controller or register for a registered

DIMM. This embodiment will preferably have further IC's 18 on an opposite side 9, which is not depicted here. Flex circuit 12 is, in this embodiment, made from four conductive layers and multiple flexible substrate layers as earlier described with reference to Fig. 29.

5 In this embodiment, flex circuit 12 is provided with holes 13, which are devised to allow greater flexibility for bending flex circuit 12 to achieve a desired bend radius for curve 25 (Fig. 53). Holes 13 ("holes", "voids", "partial voids") preferably pass entirely through flex circuit 12, but in other embodiments may be only partial holes or voids 10 that may be exhibited by one or more of the conductive layers of flex circuit 12, and/or one or more of the flexible substrate layers of flex circuit 12. Such partial voids may be devised to allow flexibility while still providing sufficient conductive material to allow the desired connections to contacts 20 and between the depicted ICs in field F1 and 15 field F2.

Holes 13 in this embodiment are spaced to allow traces 21 to pass between them at the level of conductive layers of flex 13. While some preferred embodiments have a dielectric solder mask layer partially covering side 8, traces 21 are depicted along side 8 for simplicity. As 20 those of skill will recognize, traces may be at different layers within the flex circuit.

In this embodiment, flex circuit 12 is further provided with holes 15. Holes 15 are devised to allow flexibility for bending flex circuit 12 to achieve a desired bend radius for around edge 16A or 16B of substrate 25 14, for example. Holes 15 may be expressed as voids or partial voids in the various conductive and non-conductive layers of flex circuit 12. This embodiment of flex circuit 12 is also provided with mounting pads 51

along side 18 of flex circuit 12. Such pads 51 are used for mounting components such as, for example, surface mount resistors 52.

Fig. 53 is a perspective view of a module 10 according to an embodiment of the present invention. Depicted are holes 13 along curve 25. Further, parts of holes 15 can be seen along the lower depicted edge of module 10. Holes 13 may have an extent such that they are present along the entirety of curve 25. Holes 15 may also be sized such that they span the entire bend around the edge of substrate 14. Holes 13 and 15 may have a span greater than the length of their respective curves, or less that such length. For example, holes 13 and 15 may be sized such that they provide an adjusted bend radius for flex circuit 12 only in portions of the bend having a desired bend radius smaller that the radius possible with an unmodified flex circuit 12.

The depicted topology and arrangement of flexible circuitry may be used to advantage to create high capacity and thin-profile circuit modules. For example, a DIMM may be constructed having double device-mounting surface area for a given DIMM height. Such doubling may allow doubling of the number memory devices or enable larger devices that would not fit on traditional DIMMs.

For example, one preferred embodiment provides a 30mm 4-GByte registered DIMM using 512 Mbit parts. Another embodiment provides a 50mm 8-GByte registered DIMM using 1 Gbit parts. Yet another embodiment provides a 2-GByte SO-DIMM using 512 Mbit parts. DIMM modules may be provided having multiple instantiations of DIMM or FB-DIMM circuits, as previously described herein. Also, DIMMs having the usual single instantiation of DIMM circuitry may be provided where the devices employed are too large to fit in the surface

area provided by a typical industry standard DIMM module. Such high-capacity capability and flexibility may be used to advantage to provide high capacity memory for computer systems having a limited number of motherboard DIMM sockets or slots.

5 Fig. 54 illustrates an exemplar module 10 devised to provide a thin profile while employing devices of larger height such as, for example, an AMB. Fig. 54 depicts a preferred embodiment of the present invention and illustrates a module 10 populated with ICs 18 and exhibiting AMB circuit 19 with a resident heat sink 33 emergent from IC opening 35 in
10 flex circuit 12 and further shown in the next Figs.

Fig. 55 depicts side 9 of flex circuit 12. Fields F1 and F2 of depicted flex circuit 12 are each populated with a single rank of ICs 18. Field F2 exhibits IC opening 35 through flex circuit 12. Opening 35 is an opening sufficient in size to allow a selected IC, such as an AMB circuit
15 19, for example, to pass through flex circuit 12. Those of skill will recognize that more than one IC opening 35 may be devised in flex circuit 12 to allow multiple taller profile devices to pass through respective openings.

Fig. 56 depicts another preferred embodiment of the present
20 invention and illustrates a cross-section of a module 10 taken through an iteration of circuit 19. The view of Fig. 56 illustrates module 10 with flex circuit 12 with an opening 35 from which circuit 19 emerges. Flex circuit 12 is wrapped about substrate 14 and IC 19, which is mounted on field F1 of side 9 of flex circuit 12 which, in the depicted embodiment, is
25 the inner side of module 10, passes through window 250 of substrate 12 to emerge in part from IC opening 35 of flex circuit 12. The depicted circuit 19 exhibits a heat radiative element or heat sink 33 and may be

construed to depict an AMB or buffer or logic device, for example. Those of skill will understand that circuit 19 need not emerge from IC opening 35 of flex circuit 12 and that advantages will result merely from placing IC opening 35 of flex circuit 12 substantially in coincidence with
5 circuit 19 to allow thermal energy to be more readily released from circuit 19. However, in many embodiments, circuit 19 will emerge at least in part from opening 35. Other embodiments may be constructed in accordance with the present invention to place, for example, two instantiations of FB-DIMM circuitry on a single module and employ a
10 flex circuit that exhibits two IC openings 35 to coincide with the two AMBs that are either visible through their respective windows in the substrate or actually emerge, at least in part, from the openings 35 of the flex circuit.

As shown in Fig. 56, circuit 19 has a profile depicted by reference
15 "P_T" while module 10 has a profile referenced by "P_M" and ICs 18 each have a profile indicated by the reference "P_{18}" and substrate 14 has a profile of "P_S." As shown, the profile P_M of module 10 is increased less by the profiles for ICs 18 and circuit 19 than would be expected without the use of the techniques disclosed herein. For example, in the
20 embodiment depicted in Fig. 56, P_M is less than four times the profile P_{18} of ICs 18 plus P_T because circuit 19 is disposed into window 250 of substrate 14 and through opening 35 of flex circuit 12.

In this embodiment, the construction places ICs 18 of field F1 on the S_1 side of substrate 14 and ICs 18 of field F2 on the S_2 side of
25 substrate 14 while the taller profile or height of circuit 19, represented by reference P_T, lies substantially within the profile or height P_M of module 10 thus resulting in a lower profile module 10 than would have been

exhibited had circuit 19 been mounted, for example, on side 8 of flex circuit 12 such as the taller profile module 10 shown in previous Fig. 51.

Fig. 57 depicts an alternative embodiment of the present invention and shows module 10 populated with ICs 18 on side 8 of flex circuit 12 and circuit 19 passing through window 250 of substrate 14. The embodiment depicted in Fig. 57 may be employed, for example, in PCI applications where the space allowed for expansion boards is minimal and typically only one-sided conventional boards have been compliant with the space allotted by the application. The principles of the present invention may, therefore, allow greater capacities to be employed in PCI-constrained applications.

Although the present invention has been described in detail, it will be apparent to those skilled in the art that many embodiments taking a variety of specific forms and reflecting changes, substitutions and alterations can be made without departing from the spirit and scope of the invention. The many described embodiments thus illustrate, but do not restrict the scope of the claims.

CLAIMS:

1. A circuit module comprising:

a flex circuit having a first conductive layer comprising signal
5 traces, a second conductive layer comprising signal traces, a first side and a second side and along the first side, and plural expansion board contacts adapted for connection to a circuit board socket;

first and second pluralities of CSPs disposed along the first side of the flex circuit with the first plurality of CSPs being separated from the
10 second pluralities of CSPs by the plural expansion board contacts; and

a substrate having first and second lateral sides and an edge adjacent to which the flex circuit is disposed to place the first side of the flex circuit further from the substrate than is placed the second side of the flex circuit, and to dispose the plural expansion board contacts along at
15 least one of the first and second lateral sides of the substrate.

2. The circuit module of claim 1 wherein the flex circuit further comprises a third conductive layer comprising a ground plane, and a fourth conductive layer comprising signal traces.

20

3. The circuit module of any of the preceding claims further comprising an AMB and the circuit module is configured as an FB-DIMM.

25 4. The circuit module of any of the preceding claims in which the first and second pluralities of CSPs are comprised of stacks.

5. The circuit module of any of the preceding claims in which the flex circuit has at least one bend with at least one row of voids in the flex circuit along the bend.

5 6. The circuit module of claim 5 in which the row of voids is a row of holes through the flex circuit.

7. The circuit module of claim 5 in which the row of voids comprises voids in less than all layers of the flex circuit.

10

8. The circuit module of any of the preceding claims further comprising a first FB-DIMM circuit including CSPs of the first or second pluralities of CSPs and a first AMB mounted on the flex circuit and a second FB-DIMM circuit including CSPs of the first and second

15 pluralities of CSPs and a second AMB mounted on the flex circuit.

9. The circuit module of any of the preceding claims inserted in an edge connector in a computer.

20 10. The circuit module of claim 9 in which the computer is a server computer.

11. The circuit module of claim 8 in which the substrate is patterned to provide cutaway areas into which are disposed selected ones of the

25 pluralities of CSPs on the flex circuit.

12. The circuit module of claim 8 in which the rigid substrate is patterned to provide at least one cutaway area or window into which are disposed one of the first or second AMBs.

13. The circuit module of any of the preceding claims further comprising:

a second flex circuit having a first side and a second side, the first side and second sides each having a first field and a second field, each of the first and second fields of each of the first and second sides having at least one mounting site for CSPs;

first CSPs of the first or second pluralities of CSPs and a first AMB mounted along the first side of the flex circuit and second CSPs mounted along the second side of the flex circuit;

first CSPs and a second AMB mounted along the first side of the second flex circuit and second CSPs mounted along the second side of the second flex circuit;

wherein the first flex circuit is disposed along the first lateral side of the substrate and the second flex circuit is disposed along the second lateral side of the rigid substrate.

14. The circuit module of any of claims 1 to 7 further comprising first and second AMBs with the first AMB being disposed with a first rank of CSPs and the second AMB being disposed with the second rank of CSPs.

15. The circuit module of claim 8 in which the first side of the flex circuit has first and second mounting fields for CSPs and the second side of the flex circuit has first and second mounting fields for CSPs and the

first plurality of CSPs and first AMB of the first FB-DIMM circuitry are disposed along the first mounting field of the first side of the flex circuit and the first field of the second side of the flex circuit while the second plurality of CSPs and the second AMB of the second FB-DIMM circuitry
5 are disposed along the second mounting field of the first side of the flex circuit and the second mounting field of the second side of the flex circuit.

16. The circuit module of claim 15 in which the first plurality of CSPs
10 and first AMB of the first FB-DIMM circuitry are disposed in single lateral rank file along the first mounting field of the first side of the flex circuit and in single lateral rank file along the first field of the second side of the flex circuit while the second plurality of CSPs and the second AMB of the second FB-DIMM circuitry are disposed in single rank file
15 along the second mounting field of the first side of the flex circuit and in single rank file along the second mounting field of the second side of the flex circuit.

17. The circuit module of claim 15 in which the first side of the flex
20 circuit has first and second mounting fields for CSPs and the second side of the flex circuit has first and second mounting fields for CSPs and the first plurality of CSPs and first AMB of the first FB-DIMM circuitry are disposed along the first mounting field of the first side of the flex circuit and the second field of the second side of the flex circuit while the second
25 plurality of CSPs and the second AMB of the second FB-DIMM circuitry are disposed along the second mounting field of the first side of the flex circuit and the first mounting field of the second side of the flex circuit.

18. The circuit module of claim 17 in which the first plurality of CSPs and first AMB of the first FB-DIMM circuitry are disposed in single lateral rank file along the first mounting field of the first side of the flex
5 circuit and in single lateral rank file along the second field of the second side of the flex circuit while the second plurality of CSPs and the second AMB of the second FB-DIMM circuitry are disposed in single rank file along the second mounting field of the first side of the flex circuit and in single rank file along the first mounting field of the second side of the
10 flex circuit.

19. The circuit module of any of the preceding claims, wherein the flex circuit includes an IC opening passing through the flex circuit with the flex circuit being disposed about the substrate to dispose at least one CSP
15 of a first type into the window passing through the rigid substrate.

20. The circuit module of any preceding claims in which the substrate is comprised of thermally conductive material and exhibits at least one thermal extension.

20

21. The circuit module of claim 19 in which the at least one CSP of a first type emerges from the IC window passing through the flex circuit.

22. The circuit module of any of the preceding claims in which a
25 plurality of CSPs of a second type are disposed along the second side of the flex circuit.

23. The circuit module of claim 22 in which the plurality of CSPs of the second type are comprised of memory CSPs.

24. The circuit module of claim 23 in which the plurality of CSPs of
5 the second type which are comprised of stacks.

25. The circuit module of claim 19 in which a plurality of CSPs of a second type are disposed along the first side of the flex circuit.

10 26. The circuit module of claim 25 in which the plurality of CSPs of the second type are comprised of memory circuits.

27. The circuit module of claim 26 in which the plurality of CSPs of the second type are comprised of stacks.

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28. The circuit module of any of the preceding claims connected to a circuit board socket through the plural expansion board contacts of the flex circuit.

20 29. The circuit module of claim 19 in which the second side of the flex circuit has a first field and a second field and the at least one CSP of the first type is mounted on the first field of the second side and a plurality of CSPs of a second type are mounted on the second field of the second side.

25

30. The circuit module of claim 19 in which the at least one CSP of the first type is an AMB.

31. The circuit module of claim 19 in which the first side of the flex circuit is populated with a plurality of CSPs of a second type.

5 32. The circuit module of claim 19 further comprising plural CSPs of a second type in which the substrate is patterned to provide cutaway areas into which are disposed the plural CSPs of the second type.

33. The circuit module of claim 19 further comprising a first plurality 10 of CSPs of a second type, and the first plurality of CSPs of the second type and the at least one CSP of the first type comprise a first FB-DIMM instantiation.

34. The circuit module of claim 33 further comprising a second 15 plurality of CSPs of a second type and the at least one CSP of the first type comprises two AMBs and the second plurality of CSPs of the second type and the at least one CSP of the first type which comprise two AMBs comprise a second FB-DIMM instantiation.

20 35. The circuit module of claim 1 wherein the flex circuit includes an IC opening that passes through the flex circuit, the first side of the flex circuit being populated with plural CSPs of a first type, and the second side being populated with a CSP of a second type, and wherein the substrate includes a window that passes therethrough, the flex circuit 25 being wrapped about the edge of the rigid substrate to dispose the plural CSPs of the first type on the outside of the circuit module and the CSP of the second type into the window of the substrate.

36. The circuit module of claim 35 in which the CSP of the second type emerges in part from the IC opening of the flex circuit.

5 37. The circuit module of claim 1 wherein the flex circuit includes an IC opening and is populated on its first side with memory CSPs and on its second side with at least one IC of a selected type, and the substrate includes a window passing therethrough, and wherein the flex circuit is wrapped to dispose the first side of the flex circuit further from the
10 substrate than is the second side of the flex circuit and dispose the at least one IC of the selected type into the window of the substrate.

38. The circuit module of claim 37 in which the IC of the selected type is disposed through the window of the substrate and emerges in part from
15 the IC opening of the flex circuit.

39. The circuit module of claim 1 wherein:

the first lateral side of the substrate includes one or more cutaway areas and the second lateral side includes one or more cutaway areas, and
20 wherein the flex circuit is disposed about the substrate to position individual ones of a first group of CSPs in the one or more cutaway areas of the first lateral side of the substrate and position individual ones of a second group of CSPs in the one or more cutaway areas of the second lateral side of the substrate.

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40. The circuit module of claim 39 in which the one or more cutaway areas of the first lateral side of the substrate are in spatial coincidence

with respective ones of the one or more cutaway areas of the second lateral side of the substrate.

41. The circuit module of claim 39 in which the one or more cutaway
5 areas of the first lateral side of the substrate are in partial spatial coincidence with respective ones of the one or more cutaway areas of the second lateral side of the substrate.

42. The circuit module of claim 1 wherein the substrate includes a
10 cavity and the flex circuit includes first and second portions, the first portion being adjacent to the first lateral side of the substrate and the second portion being adjacent to the second lateral side of the substrate, and further comprising a connector having first and second parts which are selectively joinable, the first part of the connector corresponding to
15 the first portion of the flex circuitry and the second part of the connector corresponding to the second portion of the flex circuitry, the first and second portions of the flex circuitry being electrically joined in the cavity of the substrate through the first and second parts of the connector.

20 43. A method for devising a circuit module of any of claims 1 to 12 and 14 to 42 comprising:

providing a flex circuit having first and second sides, and first and second long perimeter edges and first and second short perimeter edges with a set of expansion board contacts along the first side, and first and
25 second pluralities of CSPs mounted on the first side of the flex circuit and disposed laterally about the set of edge connector mating contacts to place the first plurality of CSPs nearer the first long perimeter edge of

the flex circuit than is disposed the set of module contacts and the second plurality of CSPs nearer the second long perimeter edge of the flex circuit than is disposed the set of module contacts;

providing a thermally-conductive rigid substrate having first and 5 second lateral sides and a first long perimeter edge and a second long perimeter edge;

wrapping the flex circuit about the thermally-conductive substrate to dispose the second side of the flex circuit closer to the first and second lateral sides of the substrate than is disposed the first side of the flex 10 circuit and to dispose the set of expansion board contacts along the first long perimeter edge of the substrate on both the first and second lateral sides to place the first plurality of CSPs closer to the first lateral side of the thermally-conductive substrate than is disposed the second plurality of CSPs.

15

44. A method for providing increased memory capacity for a computer system comprising inserting a circuit module in accordance with any of claims 1 to 42 into an expansion slot.

20 45. A method of assembling a circuit module in accordance with any of claims 1 to 12 and 14 to 42 comprising:

providing a flex circuit having a first side and a second side, the first side having a plurality of pads for mounting CSPs and a plurality of expansion board contacts for insertion in an expansion board slot, the 25 second side having a plurality of pads for mounting CSPs;

mounting plural CSPs on the first side of the flex circuit;

mounting plural CSPs on the second side of the flex circuit;

mounting an AMB on at least one of the first or second sides of the flex circuit;

providing a thermally-conductive rigid substrate having first and second major surfaces and an edge and a thermal extension; and

5 wrapping the flex circuit about the edge of the rigid substrate, with the first side facing outward, such that the plurality of contacts are disposed proximal to the edge of the thermally-conductive rigid substrate.

46. The method of claim 45 further comprising attaching a heat
10 radiating clip to selected ones of the plural CSPs.

47. The method of claim 45 further comprising inserting the plurality of contacts at least partially into an expansion board slot for connection to an operating environment.

15

48. The method of claim 45 in which the thermally-conductive rigid substrate has first portion and a second portion, the first portion being thinner than the second portion.

20 49. The method of claim 45 in which the thermally-conductive rigid substrate is comprised of a metal.

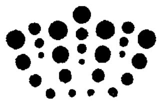
50. The method of claim 45 in which the thermally-conductive rigid substrate is comprised of aluminum.

25

51. The method of claim 41 in which the thermally-conductive rigid substrate is comprised of FR4 and a metallic layer.

52. A circuit module substantially as hereinbefore described with reference to the accompanying drawings.

5 53. A method for devising a circuit module substantially as hereinbefore described with reference to the accompanying drawings.



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Application No: GB0822086.5 **Examiner:** Ian Rees
Claims searched: 1 to 53 **Date of search:** 13 January 2009

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1, 9, 10, 28	JP 11003955 A SHINKO ELECTRIC. See figure 3, EPODOC and WPI abstracts.
A	-	US 4495546 A NAKAMURA. See figure 10.
A	-	US 6232659 B1 CLAYTON. See figure 18C.

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^{X} :

Worldwide search of patent documents classified in the following areas of the IPC

G11C; H05K

The following online and other databases have been used in the preparation of this search report

EPODOC, WPI

International Classification:

Subclass	Subgroup	Valid From
H05K	0001/18	01/01/2006
G11C	0005/00	01/01/2006