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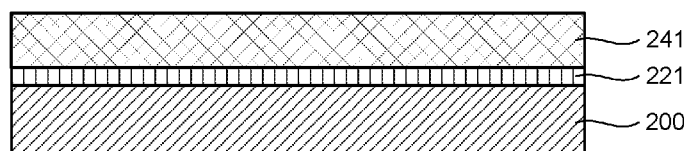


FIG. 2E

(57) Abstract: Dielectric films for semiconductor devices and methods of forming. A processing method includes forming a first film of a first dielectric material on a substrate by performing a first plurality of cycles of atomic layer deposition and, thereafter, heat-treating the first film, where a thickness of the first film is below a threshold thickness needed for spontaneous polarization in the first dielectric material. The processing method further includes forming a second film of a second dielectric material on the substrate by performing a second plurality of cycles of atomic layer deposition and, thereafter, heat-treating the second film, where a thickness of the second film is greater than the thickness of the first film, and the second film is ferroelectric or antiferroelectric. The first and second dielectric materials can include at least one metal oxide, for example zirconium oxide, hafnium oxide, or a laminate or mixture thereof.



METHODS FOR FORMING DIELECTRIC MATERIALS WITH SELECTED POLARIZATION FOR SEMICONDUCTOR DEVICES

[0001] This application is related to and claims priority to United States Provisional Patent Application serial no. 63/063,840 filed on August 10, 2020, the entire contents of which are herein incorporated by reference.

5

FIELD OF THE INVENTION

[0002] The present invention relates to semiconductor processing and semiconductor devices, and more particularly, to substrate processing methods for forming dielectric materials with selected polarization by thin film vapor phase deposition.

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BACKGROUND OF THE INVENTION

[0003] Dielectric materials are used for CMOS-related applications, including field-effect transistor (FET) devices and dynamic random-access memory (DRAM) devices. New methods are needed for forming dielectric materials with selected polarization by thin film vapor phase deposition.

15

SUMMARY OF THE INVENTION

[0004] Embodiments of the invention include methods for forming structures of dielectric films on a substrate, including high-k films that may be used as capacitors and memory cells in semiconductor devices and other devices. According to one embodiment, the method includes forming a first film of a first dielectric material on a substrate by performing a first plurality of cycles of atomic layer deposition and, thereafter, heat-treating the first film, where a thickness of the first film is below a threshold thickness needed for spontaneous polarization in the first dielectric material. The method further includes forming a second film of a second dielectric material on the substrate by performing a second plurality of cycles of atomic layer deposition and, thereafter, heat-treating the second film, where a thickness of the second film is greater than the thickness of the first film, and the second film is ferroelectric or antiferroelectric.

[0005] According to one embodiment, a semiconductor device includes a first film of a first dielectric material on a substrate, where a thickness of the first film is below a threshold thickness needed for spontaneous polarization in the first dielectric material, and a second

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film of a second dielectric material on the substrate, where a thickness of the second film is greater than the thickness of the first film, and the second film is ferroelectric or antiferroelectric.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with a general description of the invention given above, and the detailed description given below, serve to explain the invention.

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[0007] FIG. 1 is a flowchart of an example method of manufacturing a dielectric film structure according to an embodiment of the invention;

[0008] FIGS. 2A – 2E show cross-sectional views of an example dielectric film structure according to an embodiment of the invention;

15 [0009] FIG. 3 shows a cross-sectional view of an example dielectric film structure according to an embodiment of the invention;

[0010] FIG. 4 shows a cross-sectional view of an example dielectric film structure according to an embodiment of the invention;

[0011] FIG. 5 shows a cross-sectional view of an example dielectric film structure according to an embodiment of the invention; and

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[0012] FIGS. 6A and 6B schematically show cross-sectional views of example film structures for semiconductor devices according to embodiments of the invention.

DETAILED DESCRIPTION OF SEVERAL EMBODIMENTS

25 [0013] The present disclosure repeats reference numerals in the various embodiments. This repetition is for the purpose of simplicity and clarity such that repeated reference numerals indicate similar features amongst the various embodiments unless stated otherwise.

[0014] According to one embodiment, schematically shown in FIGS. 1 and 2A-2E, a method in flowchart 1 includes, in 100, providing a substrate 200 in a process chamber. In one example, the process chamber may be configured to perform atomic layer deposition (ALD) of a dielectric material on the substrate 200. The substrate 200 may, for example, include a semiconductor material, including silicon, germanium, silicon germanium, silicon germanium carbide, gallium arsenic phosphide, gallium indium phosphide, silicon carbide, gallium

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arsenic, indium arsenide, or indium phosphide. In one example, the substrate 200 may have an epitaxial layer overlying a bulk semiconductor. Furthermore, the substrate 200 may include a semiconductor-on-insulator (SOI) structure. Still further, the substrate 200 may include a metal layer.

5 **[0015]** The substrate 200 may also include various p-type doped regions and/or n-type doped regions, implemented by a process such as ion implantation and/or diffusion. Those doped regions can include n-well, p-well, light-doped region (LDD) and various channel doping profiles configured to form various integrated circuit (IC) devices, such as a complimentary metal-oxide-semiconductor field-effect transistor (CMOSFET), an imaging sensor, and/or a
10 light emitting diode (LED).

[0016] The substrate 200 may also include various isolation regions. The isolation regions separate various device regions in the substrate 200. The isolation regions include different structures formed by using different processing technologies. For example, the isolation regions may include shallow trench isolation (STI) regions. The formation of an STI region
15 may include etching a trench in the substrate 200 and filling in the trench with insulator materials such as silicon oxide, silicon nitride, and/or silicon oxynitride. The filled trench may have a multi-layer structure such as a thermal oxide liner layer with silicon nitride filling the trench. A chemical mechanical polishing (CMP) may be performed to polish back excessive insulator materials and planarize the top surface of the isolation features.

20 **[0017]** The method further includes, in 110, forming a first film 220 of a first dielectric material on the substrate 200 by performing a first plurality of cycles of atomic layer deposition (ALD). This is schematically shown in FIG. 2B. According to some embodiments, the first film 220 includes a high dielectric constant (high-k) material with a dielectric constant greater than that of SiO₂ (k~4). In the example of a metal oxide, the ALD
25 can include cycles of alternating saturating gaseous exposures of a metal-containing precursor and an oxidizer, where each cycle includes one exposure of the metal-containing precursor, followed by one exposure of the oxidizer. Each cycle deposits one atomic layer or less of the metal oxide, and the number of cycles may selected in order to accurately control the film thickness. Steric hindrance of ligands in the metal-containing precursor and the
30 oxidizer, and a limited number of bonding sites, can limit the chemisorption on the substrate surface, and therefore the film growth per cycle can remain at less than one atomic layer.

[0018] According to some embodiments, the first film 220 can contain zirconium oxide (ZrO₂), hafnium oxide (HfO₂), or laminates or mixtures thereof. The HfO₂ may be doped

with aluminum (Al), gadolinium (Gd), lanthanum (La), silicon (Si), strontium (Sr), or yttrium (Y) dopants.

[0019] In one example, a first film 220 containing ZrO₂ may be deposited by ALD using cycles of alternating gaseous exposures of a zirconium-containing precursor and an oxidizer.

5 In another example, a first film 220 containing a mixture of ZrO₂ and HfO₂ may be deposited by ALD using cycles of alternating gaseous exposures of a zirconium-containing precursor, and oxidizer, a hafnium-containing precursor, and an oxidizer. In yet another example, a first film 220 containing doped HfO₂ may be deposited by ALD using cycles of alternating gaseous exposures of a hafnium-containing precursor, a dopant gas, and an oxidizer. The
10 dopant concentration can, for example, be between about 0.1 atomic % and about 20 atomic %, between about 0.1 atomic % and about 10 atomic %, or between about 0.1 atomic % and about 1 atomic %.

[0020] Embodiments of the invention may utilize a wide variety of zirconium (Zr) and hafnium (Hf) precursors for the vapor phase deposition. For example, representative
15 examples include: Zr(O^tBu)₄ (zirconium tert-butoxide, ZTB), Zr(NEt₂)₄ (tetrakis(diethylamido)zirconium, TDEAZ), Zr(NMeEt)₄ (tetrakis(ethylmethylamido)zirconium, TEMAZ), Zr(NMe₂)₄ (tetrakis(dimethylamido)zirconium, TDMAZ), Hf(O^tBu)₄ (hafnium tert-butoxide, HTB), Hf(NEt₂)₄ (tetrakis(diethylamido)hafnium, TDEAH), Hf(NEtMe)₄
20 (tetrakis(ethylmethylamido)hafnium, TEMAH), and Hf(NMe₂)₄ (tetrakis(dimethylamido)hafnium, TDMAH). In some examples, tris(dimethylaminocyclopentadienyl)hafnium (HfCp(NMe₂)₃) available from Air Liquide as HyALDTM may be used as a hafnium precursor and tris(dimethylaminocyclopentadienyl)zirconium (ZrCp(NMe₂)₃) available from Air Liquide as
25 ZyALDTM may be used as a zirconium precursor. The oxidizer may include an oxygen-containing gas, including plasma-excited O₂, water (H₂O), or ozone (O₃).

[0021] The Al, Gd, La, Si, Sr, and Y dopants may be provided using any dopant gases that have sufficient reactivity, thermal stability, and volatility.

[0022] Examples of Al precursors include Al₂Me₆, Al₂Et₆, [Al(O(sBu))₃]₄,
30 Al(CH₃COCHCOCH₃)₃, AlBr₃, AlI₃, Al(O(iPr))₃, [Al(NMe₂)₃]₂, Al(iBu)₂Cl, Al(iBu)₃, Al(iBu)₂H, AlEt₂Cl, Et₃Al₂(O(sBu))₃, and Al(THD)₃.

[0023] Examples of Gd precursors include Gd(N(SiMe₃)₂)₃, ((iPr)Cp)₃Gd, Cp₃Gd, Gd(THD)₃, Gd[OOCCH(C₂H₅)C₄H₉]₃, Gd(O(iPr))₃, and Gd(acac)₃.

[0024] Examples of La precursors include $\text{La}(\text{N}(\text{SiMe}_3)_2)_3$, $\text{La}(\text{N}(\text{iPr})_2)_3$, $\text{La}(\text{N}(\text{tBu})\text{SiMe}_3)_3$, $\text{La}(\text{TMPD})_3$, $((\text{iPr})\text{Cp})_3\text{La}$, Cp_3La , $\text{Cp}_3\text{La}(\text{NCCH}_3)_2$, $\text{La}(\text{Me}_2\text{NC}_2\text{H}_4\text{Cp})_3$, $\text{La}(\text{THD})_3$, $\text{La}[\text{OOCCH}(\text{C}_2\text{H}_5)\text{C}_4\text{H}_9]_3$, $\text{La}(\text{C}_{11}\text{H}_{19}\text{O}_2)_3 \cdot \text{CH}_3(\text{OCH}_2\text{CH}_2)_3\text{OCH}_3$, $\text{La}(\text{C}_{11}\text{H}_{19}\text{O}_2)_3 \cdot \text{CH}_3(\text{OCH}_2\text{CH}_2)_4\text{OCH}_3$, $\text{La}(\text{O}(\text{iPr}))_3$, $\text{La}(\text{OEt})_3$, $\text{La}(\text{acac})_3$,
 5 $\text{La}(((\text{tBu})_2\text{N})_2\text{CMe})_3$, $\text{La}(((\text{iPr})_2\text{N})_2\text{CMe})_3$, $\text{La}(((\text{tBu})_2\text{N})_2\text{C}(\text{tBu}))_3$, $\text{La}(((\text{iPr})_2\text{N})_2\text{C}(\text{tBu}))_3$, and $\text{La}(\text{FOD})_3$.

[0025] Examples of silicon precursors include silane (SiH_4), disilane (Si_2H_6), monochlorosilane (SiClH_3), dichlorosilane (SiH_2Cl_2), trichlorosilane (SiHCl_3), hexachlorodisilane (Si_2Cl_6), diethylsilane (Et_2SiH_2), and alkylaminosilane compounds.

10 Examples of alkylaminosilane compounds include, but are not limited to, di-isopropylaminosilane ($\text{H}_3\text{Si}(\text{NPr}_2)$), bis(*tert*-butylamino)silane ($((\text{C}_4\text{H}_9(\text{H})\text{N})_2\text{SiH}_2)$), tetrakis(dimethylamino)silane ($\text{Si}(\text{NMe}_2)_4$), tetrakis(ethylmethylamino)silane ($\text{Si}(\text{NEtMe})_4$), tetrakis(diethylamino)silane ($\text{Si}(\text{NEt}_2)_4$), tris(dimethylamino)silane ($\text{HSi}(\text{NMe}_2)_3$), tris(ethylmethylamino)silane ($\text{HSi}(\text{NEtMe})_3$), tris(diethylamino)silane ($\text{HSi}(\text{NEt}_2)_3$), and
 15 tris(dimethylhydrazino)silane ($\text{HSi}(\text{N}(\text{H})\text{NMe}_2)_3$), bis(diethylamino)silane ($\text{H}_2\text{Si}(\text{NEt}_2)_2$), bis(di-isopropylamino)silane ($\text{H}_2\text{Si}(\text{NPr}_2)_2$), tris(isopropylamino)silane ($\text{HSi}(\text{NPr}_2)_3$), and (di-isopropylamino)silane ($\text{H}_3\text{Si}(\text{NPr}_2)$).

[0026] Examples of Sr precursors include Bis(*tert*-butylacetamidinato)strontium (TBAASr), Sr-C, Sr-D, $\text{Sr}(\text{N}(\text{SiMe}_3)_2)_2$, $\text{Sr}(\text{THD})_2$, $\text{Sr}(\text{THD})_2(\text{tetraglyme})$, $\text{Sr}(\text{iPr}_4\text{Cp})_2$, $\text{Sr}(\text{iPr}_3\text{Cp})_2$, and
 20 $\text{Sr}(\text{Me}_5\text{Cp})_2$.

[0027] Examples of Y precursors include $\text{Y}(\text{N}(\text{SiMe}_3)_2)_3$, $\text{Y}(\text{N}(\text{iPr})_2)_3$, $((\text{iPr})\text{Cp})_3\text{Y}$, Cp_3Y , $\text{Y}(\text{THD})_3$, $\text{Y}[\text{OOCCH}(\text{C}_2\text{H}_5)\text{C}_4\text{H}_9]_3$, $\text{Y}(\text{O}(\text{iPr}))_3$, $\text{Y}(\text{acac})_3$, $(\text{C}_5\text{Me}_5)_2\text{Y}$, $\text{Y}(\text{hfac})_3$, and $\text{Y}(\text{FOD})_3$.

[0028] In the above precursors, as well as precursors set forth below, the following common
 25 abbreviations are used: Si: silicon; Me: methyl; Et: ethyl; iPr: isopropyl; nPr: n-propyl; Bu: butyl; nBu: n-butyl; sBu: sec-butyl; iBu: iso-butyl; tBu: tert-butyl; Cp: cyclopentadienyl; THD: 2,2,6,6-tetramethyl-3,5-heptanedionate; TMPD: 2,2,6,6-tetramethylpiperidide; acac: acetylacetonate; hfac: hexafluoroacetylacetonate; and FOD: 6,6,7,7,8,8,8-heptafluoro-2,2-dimethyl-3,5-octanedionate.

30 **[0029]** Following deposition of the first film 220 on the substrate 200, a heat-treating process is performed on the first film 220 using a predetermined substrate temperature and time period to form a heat-treated first film 221. This is schematically shown in FIG. 2C. The heat-treating organizes the atomic elements in the first film 220, reduces the film stress, and

locks in the crystallographic orientation of the first dielectric material. The heat-treating for the first film 220 may be performed at a substrate temperature of about 500°C or lower, between about 200°C and about 500°C, between about 200°C and about 300°C, between about 300°C and about 400°C, or between about 400°C and about 500°C. In one example, the heat-treating may be performed in the same process chamber as the deposition of the first film 220. In another example, the heat-treating may be formed in a different process chamber than the deposition of the first film 220. The heat-treating may be performed under vacuum conditions in the presence of an inert gas, for example argon(Ar) or nitrogen (N₂).

[0030] According to one embodiment of the invention, a thickness of the heat-treated first film 221 can be about 1.5nm, or less. In the case of a first dielectric material containing a metal oxide, this thickness corresponds to only a few atomic monolayers of the metal oxide, and this thickness is below a threshold thickness needed for spontaneous polarization in the metal oxide. This results in a linearly polarizable metal oxide film in the presence of an external electric field. In one example, the heat-treated first film 221 contains textured tetragonal ZrO₂ with (111) crystallographic orientation.

[0031] According to one embodiment, additional heat-treated films of dielectric materials may be formed on the heat-treated first film 221 by repeating the depositing and heat-treating steps at least once. This is schematically shown in FIG. 3, where additional heat-treated films 223, 225 are formed on the heat-treated first film 221 substrate 200 by repeating the depositing and heat-treating steps twice. In general, any number of additional heat-treated films may be formed. Collectively, the heat-treated first film 221 and the additional heat-treated films 223, 225 form a linearly polarizable dielectric material 230.

[0032] Referring back to FIG. 1, the method further includes, in 120, forming a second film 240 of a second dielectric material on the substrate 200 by performing a second plurality of cycles of ALD. This is schematically shown in FIG. 2D. According to embodiments of the invention, a thickness of the second film 240 is greater than a thickness of the first heat-treated first film 221. The second film 240 can include a high-k material. According to some embodiments, the second film 240 can contain ZrO₂, HfO₂, or laminates or mixtures thereof. The HfO₂ may be doped with Al, Gd, La, Si, Sr, or Y dopants. In one example, the heat-treated first film 220 and the second film 240 can contain the same metal oxide.

[0033] Following deposition of the second film 240, a heat-treating process is performed using a predetermined substrate temperature and time period to form a heat-treated second film 241. This is schematically shown in FIG. 2E. The heat-treating organizes the atomic

elements in the second film 240, reduces the film stress, and locks in the crystallographic orientation of the second dielectric material. The heat-treated second 241 and the heat-treated first film 221 can have different crystallographic orientations.

[0034] The heat-treating of the second film 240 may be performed at a substrate temperature of about 500°C or lower, between about 200°C and about 500°C, between about 200°C and about 300°C, between about 300°C and about 400°C, or between about 400°C and about 500°C. According to one embodiment, a cap layer (not shown) may be deposited on the second film 240 prior to the heat-treating. In one example, the cap layer can include titanium nitride (TiN).

[0035] In one example, the heat-treating of the second film 240 may be performed in the same process chamber as the deposition of the second film 240. In another example, the heat-treating may be formed in a different process chamber than the deposition of the second film 240. The heat-treating may be performed under vacuum conditions in the presence of an inert gas, for example Ar or N₂.

[0036] Normally, a thickness of the heat-treated second film 241 is greater than a thickness of the heat-treated first film 221, and the heat-treated second film 241 is ferroelectric or antiferroelectric. In some examples, a thickness of the heat-treated second film 241 is about 5nm, or greater.

[0037] According to another embodiment of the invention, the heat-treated second film 241 is formed on the substrate 200 and, thereafter, the heat-treated first film 221 is formed on the heat-treated second film 241. This is schematically shown in FIG. 4.

[0038] According to one embodiment, additional heat-treated dielectric material may be formed on the heat-treated first film 221 by repeating at least once the depositing and heat-treating steps. This is schematically shown in FIG. 5, where additional heat-treated films 223, 225 are formed on the heat-treated first film 221. Generally, any number of additional heat-treated film may be formed. Collectively, the heat-treated first film 221 and the additional heat-treated films 223, 225 form a linearly polarizable dielectric material 231.

[0039] Embodiments described herein provide methods for forming dielectric materials on a substrate that may be utilized for CMOS-related applications, for example for forming negative capacitance (NC) gate stacks for field-effect transistor (FET) devices or dynamic random-access memory (DRAM) devices. The dielectric materials may, for example, be formed with selected and modulated polarization for use in metal-oxide-semiconductor field-effect transistors (MOSFETs) with very short channel length for ultra-low power computing.

[0040] FIG. 6A schematically shows a cross-sectional view of a film structure 60 for a semiconductor device, where the film structure 60 contains a first conductive layer 600, a first film 602 containing a first dielectric material, a second film 604 containing a second dielectric material, and a second conductive layer 606 on the second film 604. The first and second conductive layers 600, 606 may include metal-containing materials, for example aluminum (Al), copper (Cu), tungsten (W), nickel (Ni), platinum (Pt), alloys thereof, or metal compounds such as titanium nitride (TiN) or tantalum nitride (TaN). The first and second conductive layers 600, 606 may also include a metal silicide or doped silicon. In one example, the first and second conductive layers 600, 606 may be selected to be compatible for n-type and p-type FETs. The first film 602 may be formed as described above for heat-treated first film 221. The first film 602 can have a thickness below a threshold thickness needed for spontaneous polarization in the first dielectric material. Thus, the first film 602 may be linearly polarizable in the presence of an external electric field. The second film 604 may be formed as described above for heat-treated second film 241. The second film 604 can have a thickness that is greater than the thickness of the first film 602, and the second dielectric material has spontaneous polarization. The spontaneous polarization can be ferroelectric or antiferroelectric. A capacitance C of the semiconductor structure 60 is composed of the capacitance of the films and layers shown in FIG. 6A.

[0041] The first film 602 can contain ZrO_2 , HfO_2 , or laminates or mixtures thereof. The HfO_2 may be doped with Al, Gd, La, Si, Sr, or Y dopants. Exemplary methods for forming of the first film 602 and the second film 604 are described in FIGS. 1-5.

[0042] The film structure 61 in FIG. 6B is similar to the film structure 60 and contains a first conductive layer 600, a second film 604 containing a second dielectric material, a first film 602 containing a first dielectric material, and a second conductive layer 606 over the first film 602.

[0043] The film structures 60, 61 may undergo further CMOS or MOS technology processing to form various features and regions known in the art. For example, subsequent processing may form a multilayer interconnection that includes vertical interconnects, such as conventional vias or contacts, and horizontal interconnects, such as metal lines. The various interconnection features may implement various conductive materials including copper, tungsten, and/or silicide to provide electrical routings to couple various devices in the substrate to the input/output power and signals.

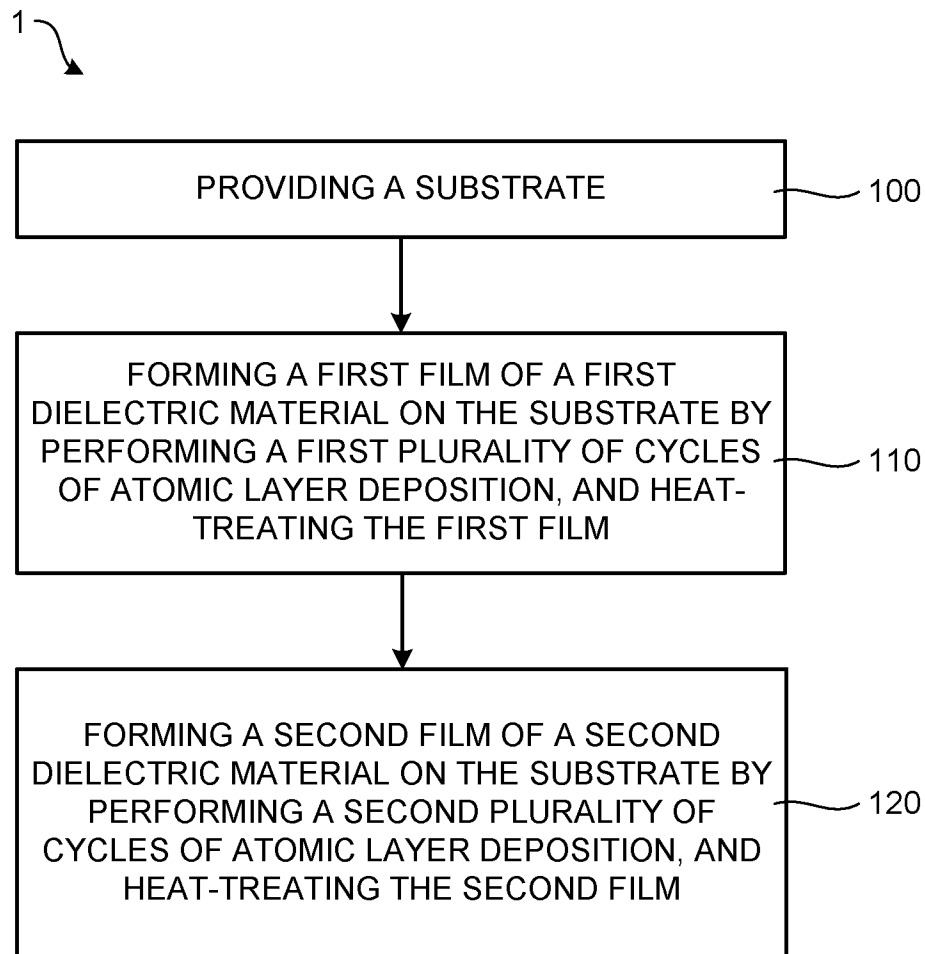
[0044] A plurality of embodiments for forming dielectric materials with selected polarization by thin film vapor phase deposition have been described. The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms that are used for descriptive purposes only and are not to be construed as limiting. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

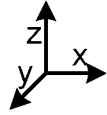
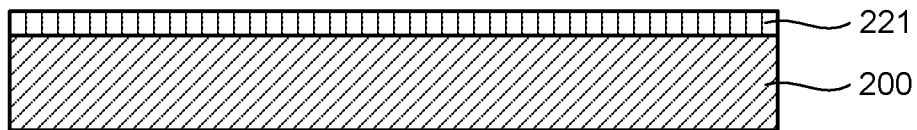
WHAT IS CLAIMED IS:

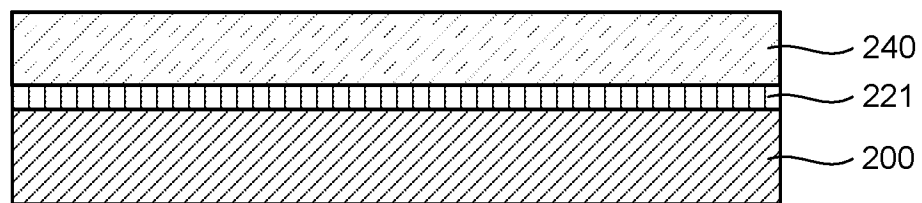
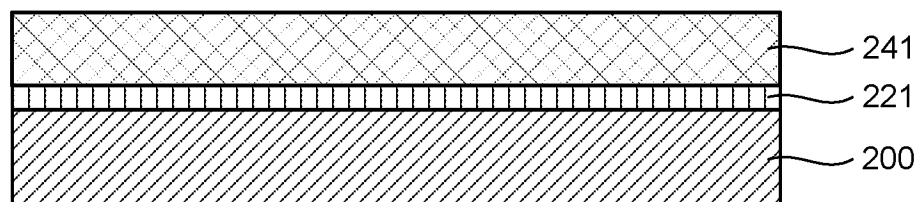
1. A substrate processing method, comprising:
 - forming a first film of a first dielectric material on a substrate by performing a first plurality of cycles of atomic layer deposition and, thereafter, heat-treating the first film, wherein a thickness of the first film is below a threshold thickness needed for spontaneous polarization in the first dielectric material; and
 - forming a second film of a second dielectric material on the substrate by performing a second plurality of cycles of atomic layer deposition and, thereafter, heat-treating the second film, wherein a thickness of the second film is greater than the thickness of the first film, and the second film is ferroelectric or antiferroelectric.
2. The method of claim 1, wherein the second film is formed on the first film.
3. The method of claim 1, wherein the first film is formed on the second film.
4. The method of claim 1, wherein the first and second dielectric materials include at least one metal oxide.
5. The method of claim 4, wherein the at least one metal oxide includes zirconium oxide, hafnium oxide, or a laminate or a mixture thereof.
6. The method of claim 1, wherein the thickness of the first film is about 1.5nm, or less.
7. The method of claim 1, wherein the first film exhibits linear polarization in the presence of an external electric field.
8. The method of claim 1, further comprising:
 - repeating the forming the first film to form an additional film on the first film, wherein the additional film lacks spontaneous polarization.
9. The method of claim 1, further comprising:
 - depositing a cap layer on the second film prior to heat-treating the second dielectric material.

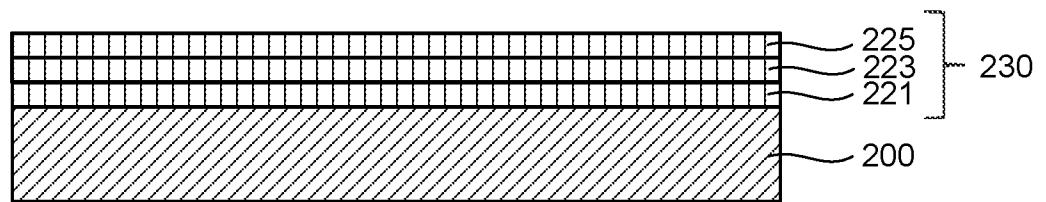
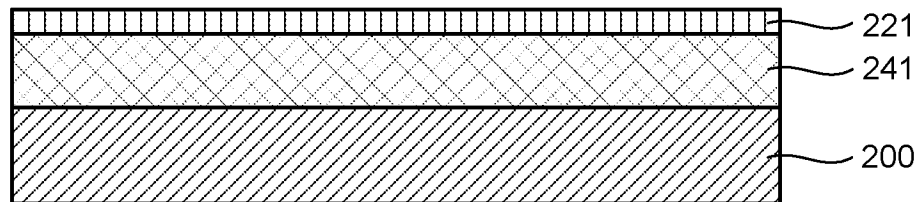
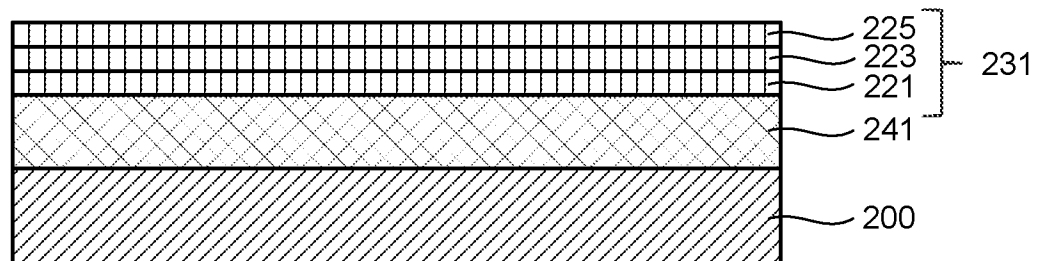
10. The method of claim 1, wherein heat-treating the first film and heat-treating the second film are performed at a substrate temperature between about 650°C and about 900°C in the presence of an inert gas.
11. A substrate processing method, comprising:
- forming a first film of a first zirconium oxide material on a substrate by performing a first plurality of cycles of atomic layer deposition and, thereafter, heat-treating the first film, wherein a thickness of the first film is below a threshold thickness needed for spontaneous polarization in the first zirconium oxide material; and
 - forming a second film of a second zirconium oxide material on the substrate by performing a second plurality of cycles of atomic layer deposition and, thereafter, heat-treating the second film, wherein a thickness of the second film is greater than the thickness of the first film, and the second film is ferroelectric or antiferroelectric.
12. A semiconductor device, comprising:
- a first film containing a first dielectric material on a substrate, wherein a thickness of the first film is below a threshold thickness needed for spontaneous polarization in the first dielectric material; and
 - a second film containing a second dielectric material on the substrate, where a thickness of the second film is greater than the thickness of the first film, and the second film is ferroelectric or antiferroelectric.
13. The device of claim 12, wherein the second film is formed on the first film.
14. The device of claim 12, wherein the first film is formed on the second film.
15. The device of claim 12, wherein the first and second dielectric materials include at least one metal oxide.
16. The device of claim 15, wherein the at least one metal oxide includes zirconium oxide, hafnium oxide, or a laminate or a mixture thereof.

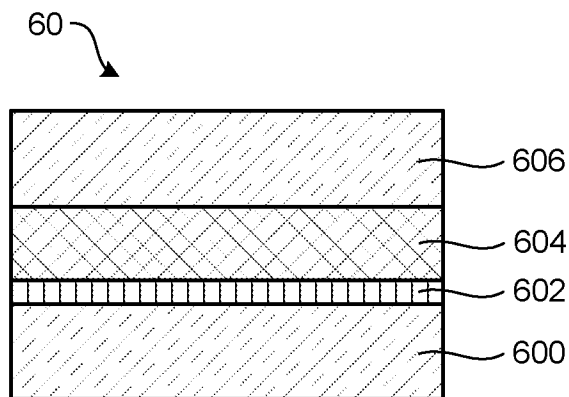
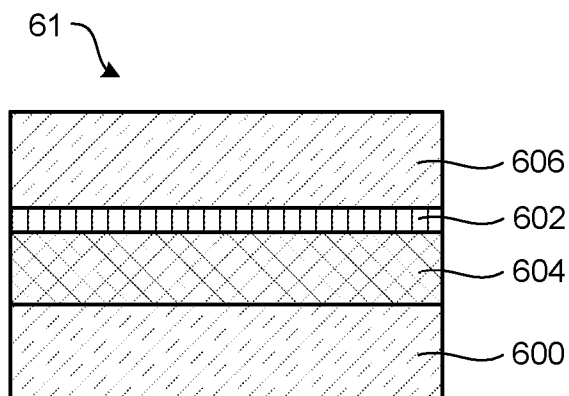
17. The device of claim 12, wherein the thickness of the first film is about 1.5nm, or less.
18. The device of claim 12, wherein the first film exhibits linear polarization in the presence of an external electric field.
19. The device of claim 12, further comprising:
 - an additional film on the first film, wherein the additional film lacks spontaneous polarization.
20. The device of claim 12, wherein the first film has tetragonal (111) crystallographic orientation.

**FIG. 1**

**FIG. 2A****FIG. 2B****FIG. 2C**

**FIG. 2D****FIG. 2E**

**FIG. 3****FIG. 4****FIG. 5**

**FIG. 6A****FIG. 6B**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2021/043952

A. CLASSIFICATION OF SUBJECT MATTER H01L 21/02(2006.01)i; C23C 16/40(2006.01)i; C23C 16/455(2006.01)i; C23C 16/56(2006.01)i According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L 21/02(2006.01); H01L 27/115(2006.01); H01L 29/423(2006.01); H01L 29/51(2006.01); H01L 29/66(2006.01) Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: ferroelectric material, spontaneous polarization, atomic layer deposition, dielectric material, heat		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2016-0181091 A1 (INTERMOLECULAR, INC.) 23 June 2016 (2016-06-23) paragraphs [0048]-[0058], claims 11-20 and figures 11-17	1-20
A	US 2020-0203499 A1 (NATIONAL CHIAO TUNG UNIVERSITY) 25 June 2020 (2020-06-25) paragraphs [0038]-[0049] and figures 4A-4E	1-20
A	US 2017-0103988 A1 (UNIVERSITY OF FLORIDA RESEARCH FOUNDATION, INC.) 13 April 2017 (2017-04-13) the entire document	1-20
A	US 2016-0308021 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD. et al.) 20 October 2016 (2016-10-20) the entire document	1-20
A	US 2015-0214322 A1 (GLOBALFOUNDRIES INC.) 30 July 2015 (2015-07-30) the entire document	1-20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
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Date of the actual completion of the international search 17 November 2021		Date of mailing of the international search report 17 November 2021
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer PARK, Hye Lyun Telephone No. +82-42-481-3463

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Information on patent family members

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