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(54) **Title**: FLIP-CHIP LIKE INTEGRATED PASSIVE PREPACKAGE FOR SIP DEVICE

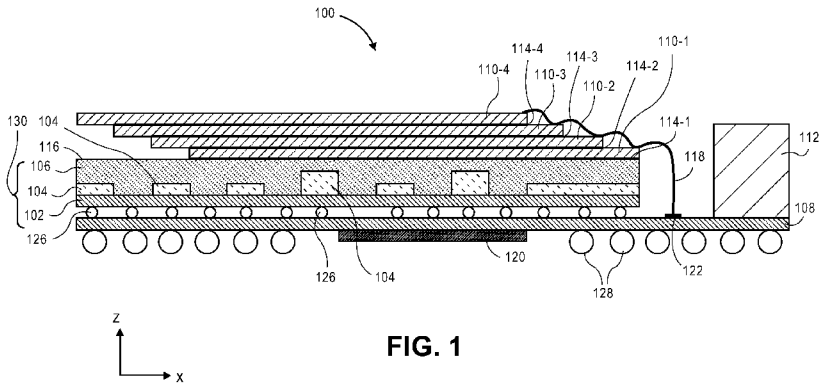


FIG. 1

(57) **Abstract**: A system in package and method for making a system in package. A plurality of passive devices are coupled to an interposer. A molding compound envelopes the plurality of passive devices and defines a platform having a substantially planar surface. The interposer is coupled to a substrate. A plurality of integrated circuit dies are coupled in a stack to the planar surface.

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FLIP-CHIP LIKE INTEGRATED PASSIVE PREPACKAGE FOR SIP DEVICE

FIELD

Embodiments of the invention relate to systems in package (SIPs). More specifically, embodiments of the invention relate to reduced area SIPs.

BACKGROUND

Systems in package (SIPs) are becoming increasingly popular as a result of improved performance in small form factors. SIPs integrate active integrated circuit (IC) dies and discrete components, also referred to as passives or passive devices, in a single package. The assembly process for SIPs is quite complex, and that complexity is exacerbated where large numbers of passive devices are needed. In some cases, there may be as many as 200 passive devices in a single SIP. Passive devices, also referred to herein as "passives", include capacitors, inductors, resistors, voltage regulators, transformers and the like.

Historically, the active ICs are coupled onto the surface of the printed circuit board and wire bonded thereto. The passives are distributed around the ICs on the circuit board. As a result, the requirement of large numbers of passives significantly increases the SIP dimension in x and y. Increasingly, the SIPs are used in smaller and thinner form factors such as smart phones, tablets and other mobile devices. As a result, size, both in x and y and also in z, becomes a critical factor.

In an effort to reduce the size, some have tried to embed a percentage of the passives in the printed circuit board (PCB) so that fewer are on the surface, thereby reducing the x and y dimension. However, this possible solution significantly increases the cost and complexity of manufacturing the substrate, increasing costs and reducing yields.

Another proposed solution is to use an interposer to mount passive devices and application-specific integrated circuits (ASICs). The routing requirement for ASIC and passives combined typically requires a six or greater level interposer, which significantly increases z-dimension. The interposer may then be attached on top of a stack of other active ICs and wire bonded to the substrate. The wire bonding and length of the signal path can negatively affect signal quality. Additionally, the cost of the interposer, coupled with the significant increase in z dimension, renders this solution unsuitable for many applications.

Another proposal has been to place the IC dies directly above the passives. To accomplish this, the passives that support the die need to be substantially co-planar. It is quite difficult to ensure a level height of the plurality of passives. There is a significant concern posed by possible tilt during the wire bond process. Additionally, the initial die and the die-attach film attaching the surface of the die to the passives must be thick enough to avoid cracking of that die or other dies in the stack. Generally, high volume manufacturing using this technique has not been found feasible.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings in which like references indicate similar elements. It should be noted that different

references to "an" or "one" embodiment in this disclosure are not necessarily to the same embodiment, and such references mean at least one.

Figure 1 is a sectional side view of a system in a package (SIP) according to one embodiment of the invention.

Figure 2 is a schematic top view of the SIP of Figure 1.

Figure 3 is a flow diagram for producing a system in a package according to one embodiment of the invention.

Figure 4 is a block diagram of a system according to one embodiment of the invention.

DETAILED DESCRIPTION

Figure 1 is a sectional side view of a system in package (SIP) according to one embodiment of the invention. In this view, the x and z dimensions of the SIP 100 are shown. As used herein, the x y dimensions refer to length and width (the long dimensions of the device) and z refers to the height or thickness (the shortest dimension) of the device.

An interposer 102 is used to mount a plurality of passive devices 104 directly thereon. The passive devices 104 are selected from the passive devices required in the SIP 100 having a z dimension below a threshold. The threshold is determined based on the maximum desired z dimension of the overall SIP. Interposer 102 may be quite simple because the routing requirements for passives tend to be relatively simple. Therefore, to control the z dimension, an interposer 102 of four layers or fewer is typically used. In one embodiment, interposer 102 has only two layers.

Interposer 102 may be a land grid array interposer; that is, the conductive connection points 126 are formed as a land grid array. In other embodiments, a ball grid array or any other suitable technology for providing electric

connectivity to the interposer may be used. It is desirable to select the x and y dimensions of interposer 102 carefully to minimize overall system size. Appropriate selection of interposer dimensions is discussed in more detail below with reference to Figure 2.

After the passive devices 104 are coupled to the interposer, molding material 106 is introduced to envelope the passive devices 104 and form a substantially planar upper surface that can be used for mounting integrated circuit (IC) dies, as discussed below. The interposer 102, passive devices 104 and molding material 106 collectively form a prepackage that is independently testable prior to installation as part of the SIP 100. Thus, after formation, the individual units may be tested to ensure the passives are functioning properly for continued with inclusion in the SIP 100. Molding material 106 is typically an epoxy resin, and the molding can be performed using substantially any conventional low pressure molding, including, without limitation, channel flow molding, pin gate molding and the like. To the extent that there are any substantial non-planarities of the upper surface after molding, the surface of molding material 106 can be planarized using various grinding techniques. However, many molding techniques will yield a perfectly satisfactory substantially planar surface without additional post-processing.

SIP 100 has a primary substrate 108 to which the prepackage 130 is attached. Interposer 102 may be reflowed to couple prepackage 130 to substrate 108. Substrate 108 has a plurality of contacts 128 that may be arranged as a ball grid array, pin grid array or other arrange suitable to provide conductive communication in the system containing the SIP 100.

A layer of die-attach film 114-1 is placed between platform surface 116 and a first IC die 110-1, thereby attaching the IC die 110-1 to platform surface 116. In one embodiment, the IC die 110-1 is attached to the prepackage 116 to be substantially flush with an edge of the prepackage 116. Successive layers of

die-attach film 114-2, 114-3 and 114-4 couple successive IC dies 110-2, 110-3, 110-4 (generically 110) into a stair-stepped stack. That is, each successive die 110-2, 110-3 and 110-4 is staggered from the one below it so that all dies 110 can be wire bonded to the substrate 108 in a single bonding area 122. In one embodiment, the number of dies 114 in a stack coupled with the offset causes the stack collectively to have an x dimension equal to the x dimension of the prepackage. While four ICs 110 are shown, more or fewer ICs may be used in other embodiments of the invention. In some embodiment of the invention, the ICs in the stack are memory ICs. Memory dies tend to be the largest dies in use in SIP manufacture.

In some embodiments, additional passive devices 112, particularly those having z dimensions greater than the threshold, are coupled directly to substrate 108. In some embodiments, application-specific integrated circuit (ASIC) 120 may be coupled directly to an opposing side of substrate 108. This direct coupling shortens the signal path and thereby improves the signal quality. ASICs tend to be smaller than the memory dies. Accordingly, the ASICs tend not to be the limiting factor on SIP x-y dimensions. By using the opposing side of the substrate for direct connection of the ASIC 120, a reduction of ultimate z-dimension is achieved.

Figure 2 is a schematic top view of the SIP of Figure 1. In this view, the x and y dimensions of the SIP are visible. Substrate 108 has the plurality of additional passive devices 112 coupled directly thereto. However, in this view, it can be seen that the die 110 stack has dimensions in x and y that are substantially equal to those of the prepackage 130. Thus, in this manner, the x and y dimensions of the system as a whole are substantially reduced.

Figure 3 is a flow diagram for producing a system in a package according to one embodiment of the invention. At block 302, the passive devices required for the system in a package are selected. The passives are

grouped by z dimension at block 304. Passives with a z less than a threshold are mounted onto an interposer at block 306. At block 308, a platform is molded over the interposer enveloping the passive devices on the interposer. The platform may be molded using, e.g., pin-gate molding, channel flow molding, or other type of low pressure molding techniques. Suitable epoxy resins are widely commercially available. The interposer assembly (also referred to as a prepackage) may be tested independently at block 310. This testing can ensure that all contacts are present and all the passive devices are functioning as expected.

Assuming that the interposer passes the test at block 310, the interposer is attached to a substrate such as a printed circuit board (PCB) flush with at least one edge of the PCB. The PCB-interposer relationship may be selected such that the y dimension of the substrate and the interposer are substantially equal while the x dimension of the interposer is somewhat less than the x dimension of the PCB. The reduced x dimension leaves unoccupied space on the substrate for wired bonding of the ICs and coupling of additional required devices. The attachment of the interposer may be performed by reflowing the interposer once it is correctly positioned on the PCB.

Once the PCB and interposer are coupled together, Then, at block 314, additional passive devices with a large z are mounted on the PCB. And then die-attach film is applied to the platform at block 316. The first circuit die may then be attached to the die-attach film on the platform at block 318. Preferably, the first die is attached substantially flush with an edge of a platform adjacent to a portion of the substrate that remains exposed after attachment of the interposer. At block 320, additional circuit die are attached using die-attach film such that they have a stair-step configuration. The dies are then wire bonded to the PCB at block 322. After wire bonding, at block 324, molding material is introduced to envelop all components, dies and wires at top side of

the substrate. This molding can be performed using any conventional low pressure molding with epoxy resin. At block 326, an ASIC may be attached to the opposite side of the PCB, providing a short, high-quality signal path for the ASIC to the other system components. In this way, a SIP efficiently using x, y, and z dimensions is created.

Figure 4 is a block diagram of a system according to one embodiment of the present invention. The computer system 1000 (also referred to as the electronic system 1000) as depicted can embody a SIP, according to any of the several disclosed embodiments and their equivalents as set forth in this disclosure. The computer system 1000 may be a mobile device such as a netbook computer. The computer system 1000 may be a mobile device such as a wireless smart phone. The computer system 1000 may be a desktop computer. The computer system 1000 may be a hand-held reader. The computer system 1000 may be a server system. The computer system 1000 may be a supercomputer or high-performance computing system.

In an embodiment, the electronic system 1000 is a computer system that includes a system bus 1020 to electrically couple the various components of the electronic system 1000. The system bus 1020 is a single bus or any combination of busses according to various embodiments. The electronic system 1000 includes a voltage source 1030 that provides power to the integrated circuit 1010. In some embodiments, the voltage source 1030 supplies current to the integrated circuit 1010 through the system bus 1020.

The integrated circuit 1010 is electrically coupled to the system bus 1020 and includes any circuit, or combination of circuits according to an embodiment. In an embodiment, the integrated circuit 1010 includes a processor 1012 that can be of any type. As used herein, the processor 1012 may mean any type of circuit such as, but not limited to, a microprocessor, a microcontroller, a graphics processor, a digital signal processor, or another

processor. In an embodiment, the processor 1012 includes, or is coupled with, a SIP as disclosed herein. In an embodiment, SRAM embodiments are found in memory caches of the processor. Other types of circuits that can be included in the integrated circuit 1010 are a custom circuit or an application-specific integrated circuit (ASIC), such as a communications circuit 1014 for use in wireless devices such as cellular telephones, smart phones, pagers, portable computers, two-way radios, and similar electronic systems, or a communications circuit for servers. In an embodiment, the integrated circuit 1010 includes on-die memory 1016 such as static random-access memory (SRAM). In an embodiment, the integrated circuit 1010 includes embedded on-die memory 1016 such as embedded dynamic random-access memory (eDRAM).

In an embodiment, the integrated circuit 1010 is complemented with a subsequent integrated circuit 1011. Useful embodiments include a dual processor 1013 and a dual communications circuit 1015 and dual on-die memory 1017 such as SRAM. In an embodiment, the dual integrated circuit 1010 includes embedded on-die memory 1017 such as eDRAM.

In an embodiment, the electronic system 1000 also includes an external memory 1040 that in turn may include one or more memory elements suitable to the particular application, such as a main memory 1042 in the form of RAM, one or more hard drives 1044, and/or one or more drives that handle removable media 1046, such as diskettes, compact disks (CDs), digital variable disks (DVDs), flash memory drives, and other removable media known in the art. The external memory 1040 may also be embedded memory 1048 such as the first die in a die stack, according to an embodiment.

In an embodiment, the electronic system 1000 also includes a display device 1050, an audio output 1060. In an embodiment, the electronic system 1000 includes an input device such as a controller 1070 that may be a keyboard,

mouse, trackball, game controller, microphone, voice-recognition device, or any other input device that inputs information into the electronic system 1000. In an embodiment, an input device 1070 is a camera. In an embodiment, an input device 1070 is a digital sound recorder. In an embodiment, an input device 1070 is a camera and a digital sound recorder. In an embodiment, an input device is a touch screen that may be part of display device 1050.

As shown herein, the integrated circuit 1010 can be implemented in a number of different embodiments, including a SIP, according to any of the several disclosed embodiments and their equivalents, an electronic system, a computer system, one or more methods of fabricating an integrated circuit, and one or more methods of fabricating an electronic assembly that includes a SIP, according to any of the several disclosed embodiments as set forth herein in the various embodiments and their art-recognized equivalents. The elements, materials, geometries, dimensions, and sequence of operations can all be varied to suit particular I/O coupling requirements including array contact count, array contact configuration for a microelectronic die embedded in a processor mounting substrate according to any of the several disclosed SIP embodiments and their equivalents. A foundation substrate may be included, as represented by the dashed line of Figure 4. Passive devices may also be included, as is also depicted in Figure 4.

The following examples pertain to further embodiments. The various features of the different embodiments may be variously combined with some features included and others excluded to suit a variety of different applications. Some embodiments relate to a system in package having an interposer with a plurality of passive devices coupled to the interposer. A molding compound envelopes the plurality of passive devices and defines a platform having a substantially planar surface. The interposer is coupled to a substrate. A plurality of integrated circuit dies are coupled in a stack to the planar surface.

In a further embodiment, an application-specific integrated circuit (ASIC) is coupled to an opposing surface of the substrate from the interposer.

In a further embodiment, a plurality of layers of die attach film (DAF) are applied to couple the circuit dies to the platform and to each other. In one embodiment, one layer of DAF resides between the planar surface and a first of the plurality of integrated circuit dies, and one layer resides between each pair of dies in the stack.

In a further embodiment, the stack of dies has a stair-step profile and the substrate has a wire bonding area adjacent to a bottom step.

In a further embodiment, a second group of passive devices are coupled directly to the substrate. At least some of the passive devices coupled directly to the substrate have z dimension greater than a maximum z dimension of the platform.

In a further embodiment, the interposer, first plurality of passive devices, and platform form a pre-package that can be independently tested before attachment to the substrate.

In a further embodiment, the interposer has fewer than four layers.

In a further embodiment, the platform has dimensions in x and y substantially equal to the dimensions of the stack in x and y.

In a further embodiment, wherein the interposer has a land grid array.

Some embodiments relate to a method of creating a system in package by mounting a plurality of passive devices onto an interposer and molding a platform of mold material on the interposer to enveloping the passive devices. The interposer is then coupled to a substrate. A die stack is attached to the platform on the interposer.

In a further embodiment, an application-specific integrated circuit (ASIC) is coupled to an opposing side of the substrate from the interposer.

In a further embodiment, a second plurality of passive devices are mounted directly on the substrate.

In a further embodiment, the set of passive devices used in the system in package are grouped into a first plurality and a second plurality based on a z dimension of the devices.

In a further embodiment, a layer of die attach film (DAF) is applied to a surface of the platform. A first integrated circuit die is placed substantially flush with the edge of the platform nearest a set of bonding pads on the substrate. A second layer of DAF is applied to a surface of the first integrated circuit die. A second integrated circuit die is placed offset from the edge of the platform.

In a further embodiment, the first and second integrated circuit dies are wire bonded to the bonding pads.

In a further embodiment, the interposer is coupled to the substrate by aligning the interposer with an edge of the substrate and then reflowing connection points of the interposer.

In a further embodiment, the passive devices and interposer are tested after molding and before coupling to the substrate.

Some embodiments relate to a system with interactive display having a system in package as part of the larger system. Some such embodiment include a system in package having an interposer with a plurality of passive devices coupled to the interposer. A molding compound envelopes the plurality of passive devices and defines a platform having a substantially planar surface. The interposer is coupled to a substrate. A plurality of integrated circuit dies are coupled in a stack to the planar surface. The system in package is coupled to and drives a display. The display has a touch screen interface coupled thereto.

In a further embodiment, the system in a package has an application-specific integrated circuit (ASIC) coupled to an opposing side of the substrate relative to the interposer.

In a further embodiment, the platform has its dimensions in x and y substantially equal to the dimensions in x and y of the integrated die stack.

Some embodiments relate to a system in package having a substrate. The system in package also includes a means for encapsulating passive devices as a pre-testable unit while defining a planar platform that is distinct from the substrate. A plurality of integrated circuit dies are coupled to the platform.

In a further embodiment, the pre-testable unit includes an interposer with a plurality of passive devices coupled to it. A molding material is molded over the interposer enveloping the passive devices.

In a further embodiment, the pre-testable unit is coupled to a first side of the substrate and an application-specific integrated circuit (ASIC) is coupled a second side of the substrate.

While embodiments of the invention are discussed above in the context of flow diagrams reflecting a particular linear order, this is for convenience only. In some cases, various operations may be performed in a different order than shown or various operations may occur in parallel. It should also be recognized that some operations described with respect to one embodiment may be advantageously incorporated into another embodiment. Such incorporation is expressly contemplated.

In the foregoing specification, the invention has been described with reference to the specific embodiments thereof. It will, however, be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A system in package comprising:

an interposer;

a plurality of passive devices coupled to the interposer;

a molding compound enveloping the plurality of passive devices, the molding compound defining a platform having a substantially planar surface;

a substrate to which the interposer is coupled; and

a plurality of integrated circuit dies coupled in a stack to the planar surface.

2. The system in package of claim 1, further comprising:

an application-specific integrated circuit (ASIC) coupled to an opposing surface of the substrate from the interposer.

3. The system in package of claim 1, further comprising:

a plurality of layers of die attach film (DAF), one layer between the planar surface and a first of the plurality of integrated circuit dies, and one layer between each pair of dies in the stack.

4. The system in package of claim 1, wherein the stack has a stair-step profile, and wherein the substrate has a wire bonding area adjacent to a bottom step.

5. The system in package of claim 1, further comprising:

a second plurality of passive devices coupled directly to the substrate, at least some of the passive devices in the second plurality having a z dimension greater than a maximum z dimension of the platform.

6. The system in package of claim 1, wherein the interposer, first plurality of passive devices, and platform form a free package that is independently testable from the substrate.

7. The system in package of claim 1, wherein the interposer has fewer than four layers.

8. The system in package of claim 1, wherein the platform has dimensions in x and y substantially equal to the dimensions of the stack in x and y..

9. The system in package of claim 1, wherein the interposer comprises:
a land grid array.

10. A method of creating a system in package comprising:
mounting a plurality of passive devices onto an interposer;
molding a platform of mold material on the interposer, the platform enveloping the passive devices;
coupling the interposer to a substrate; and
attaching a die stack to the platform.

11. The method of claim 10, further comprising:
coupling an application-specific integrated circuit (ASIC) to an opposing side of the substrate from the interposer.

12. The method of claim 10, further comprising:

mounting a second plurality of passive devices directly on the substrate.

13. The method of claim 12, further comprising:

grouping the passive devices into a first plurality and a second plurality based on a z dimension of the devices.

14. The method of claim 10, wherein attaching the die stack comprises:

applying a layer of die attach film (DAF) to a surface of the platform;

placing a first integrated circuit die substantially flush with the edge of the platform nearest the set of bonding pads on the substrate;

applying a second layer of DAF to a surface of the first integrated circuit die; and

placing a second integrated circuit die offset from the edge of the platform.

15. The method of claim 14, further comprising:

wire bonding the first and second integrated circuit dies to bonding pads on the substrate.

16. The method of claim 10, wherein coupling the interposer comprises aligning the interposer with an edge of the substrate; and

reflowing connection points of the interposer.

17. The method of claim 10, further comprising:

testing the passive devices and interposer after molding and before coupling to the substrate.

18. A system with interactive display comprising:

a system in package including:

an interposer;

a plurality of passive devices coupled to the interposer;

a molding compound enveloping the plurality of passive devices, the molding compound defining a platform having a substantially planar surface;

a substrate to which the interposer is coupled;

a plurality of integrated circuit dies coupled in a stack to the planar surface;

a display driven by the system in package; and

a touchscreen interface coupled to the display.

19. The system of claim 18, further comprising an application-specific integrated circuit (ASIC) coupled to an opposing side of the substrate relative to the interposer.

20. The system of claim 19 wherein the platform has its dimensions in x and y substantially equal to the dimensions in x and y of the integrated die stack.

21. A system in package comprising:

a substrate;

means for encapsulating passive devices as a pre-testable unit while defining a planar platform; and

a plurality of integrated circuit dies coupled to the platform.

22. The system of claim 21, wherein the means for defining further comprises:

an interposer;

a plurality of passive devices coupled to the interposer; and

molding material enveloping the passive devices.

23. The system in package of claim 21, wherein the means for encapsulating is coupled to a first side of the substrate and an application-specific integrated circuit (ASIC) is coupled a second side of the substrate.

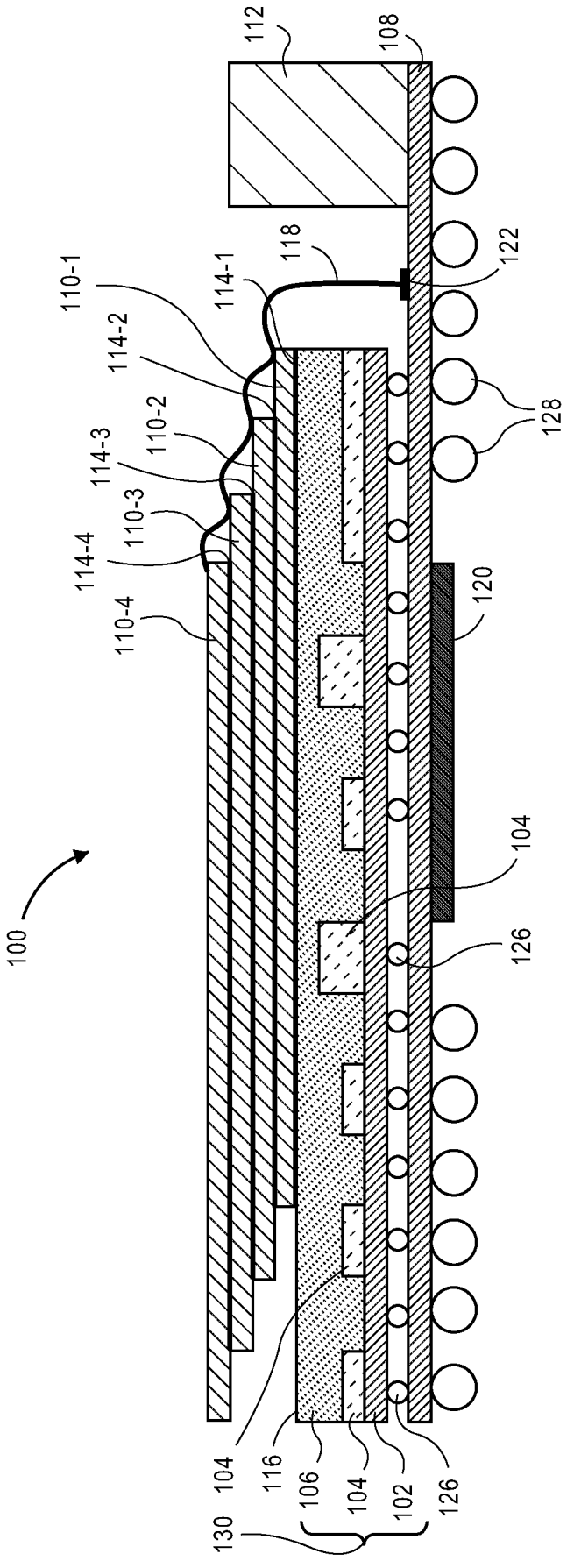

112
108
118
122
110-1
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FIG. 1

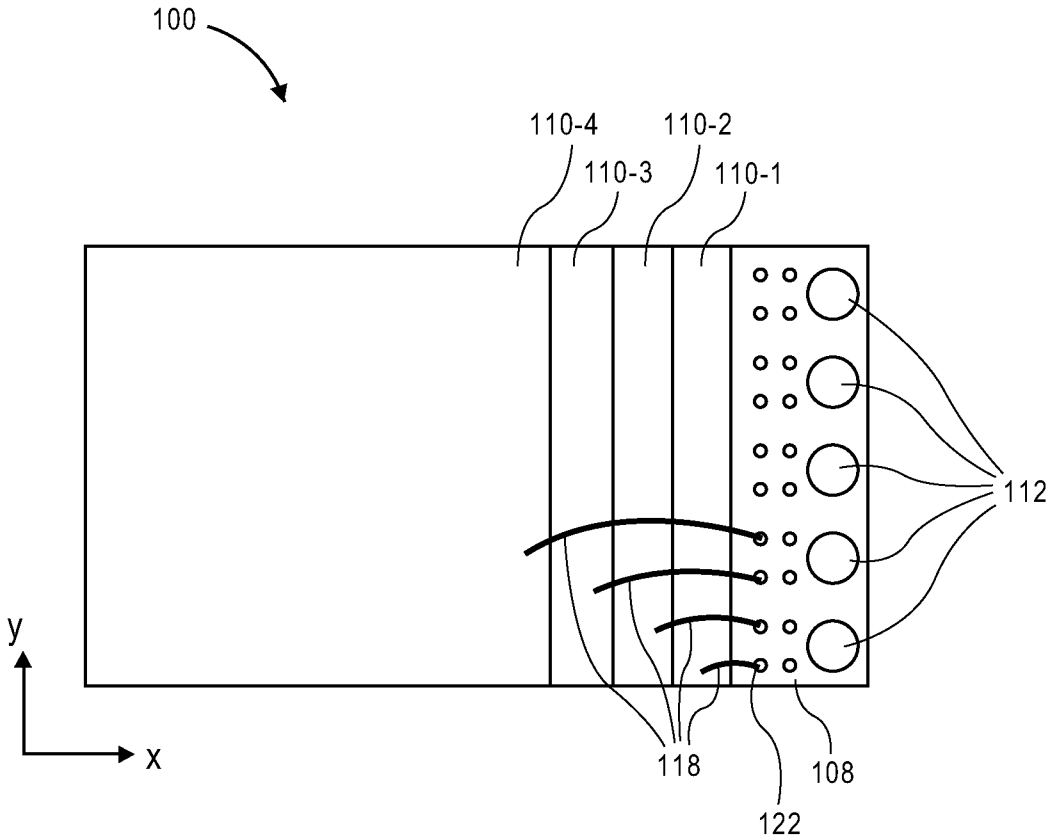


FIG. 2

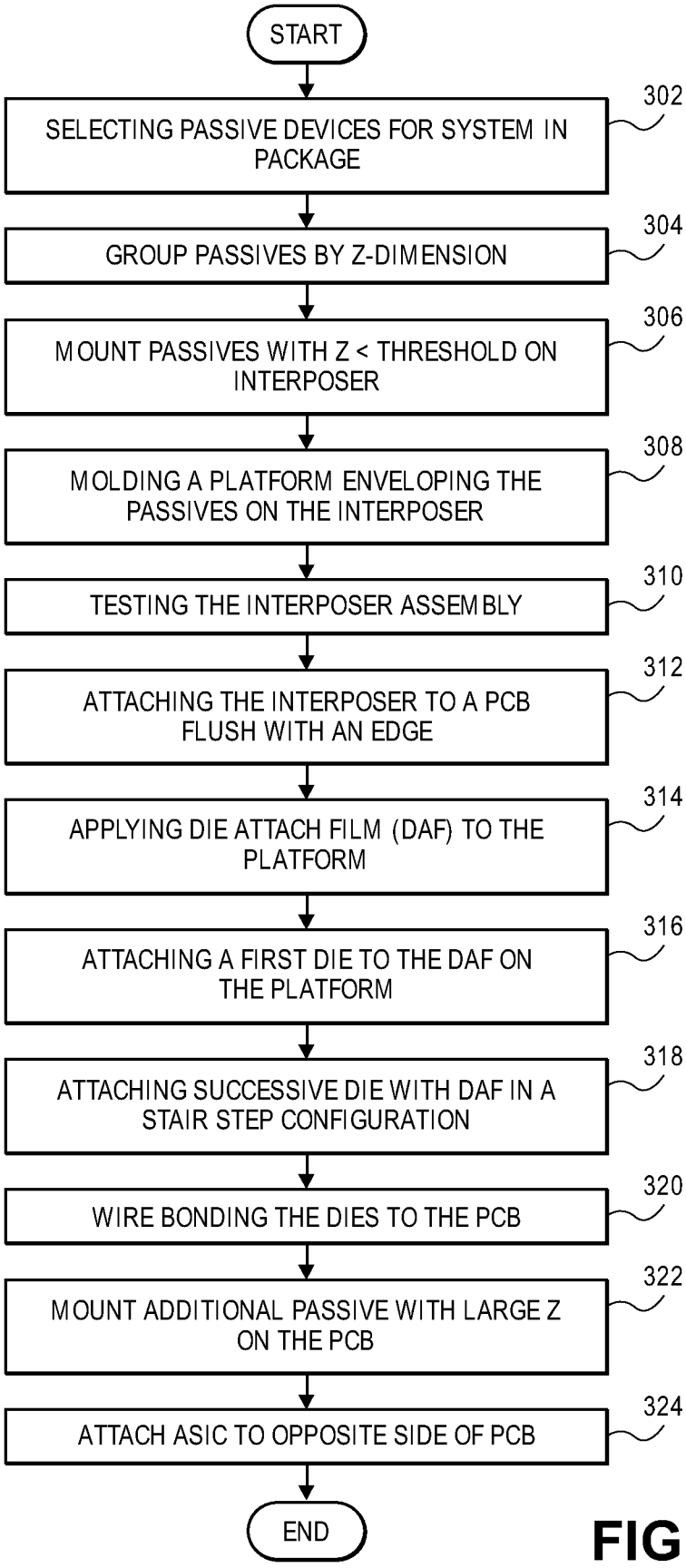

START
SELECTING PASSIVE DEVICES FOR SYSTEM IN PACKAGE
302
GROUP PASSIVES BY Z-DIMENSION
304
MOUNT PASSIVES WITH Z < THRESHOLD ON INTERPOSER
306
MOLDING A PLATFORM ENVELOPING THE PASSIVES ON THE INTERPOSER
308
TESTING THE INTERPOSER ASSEMBLY
310
ATTACHING THE INTERPOSER TO A PCB FLUSH WITH AN EDGE
312
APPLYING DIE ATTACH FILM (DAF) TO THE PLATFORM
314
ATTACHING A FIRST DIE TO THE DAF ON THE PLATFORM
316
ATTACHING SUCCESSIVE DIE WITH DAF IN A STAIR STEP CONFIGURATION
318
WIRE BONDING THE DIES TO THE PCB
320
MOUNT ADDITIONAL PASSIVE WITH LARGE Z ON THE PCB
322
ATTACH ASIC TO OPPOSITE SIDE OF PCB
324
END

FIG. 3

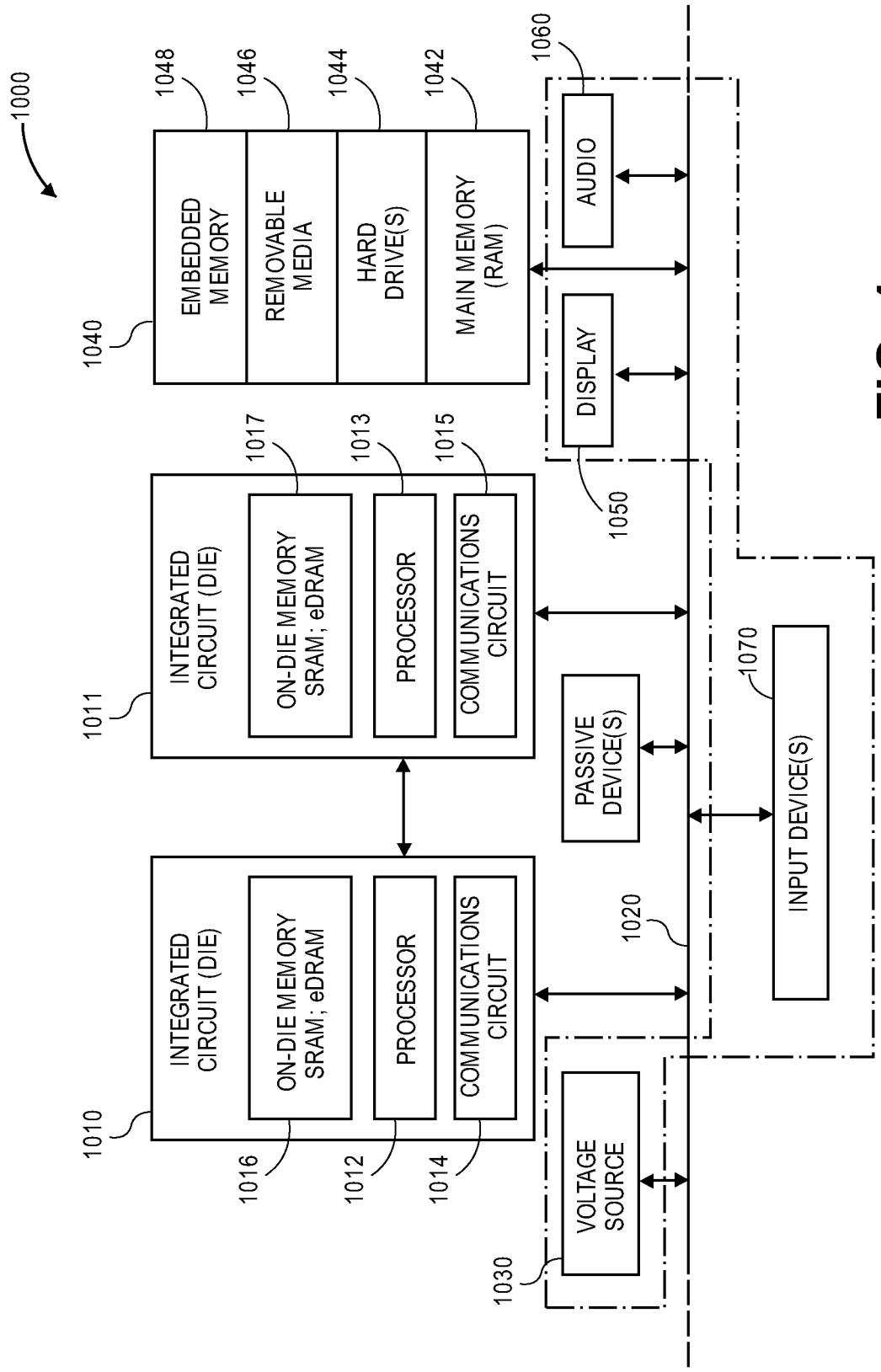

1000
1048
1046
1044
1042
1060
EMBEDDED MEMORY
REMOVABLE MEDIA
HARD DRIVE(S)
MAIN MEMORY (RAM)
AUDIO
1040
DISPLAY
1050
1017
1013
1015
INTEGRATED CIRCUIT (DIE)
ON-DIE MEMORY SRAM; eDRAM
PROCESSOR
COMMUNICATIONS CIRCUIT
1011
PASSIVE DEVICE(S)
1070
INPUT DEVICE(S)
1020
1010
1016
1012
1014
1030
VOLTAGE SOURCE

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/098867

A. CLASSIFICATION OF SUBJECT MATTER

H01L 25/16(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,WPI,EPODOC,CNKI,IEEE: substrate, pcb, interpose+, regulator, active, encapsulate, transformer, planar, plane, wrap +, passive, reduc+, pack+, insulat+, resin, transistor, chip, die, dice, resistor, cover+, clad+, decreas+, dimension, middle, coat +, second, stack, inductor, envelop+, encapsulat+, dielectric, compound, surface, SIP, capacitor, step, mold+, insert+, INTEL, TING CHIH-CHENG

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010047965 A1 (INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE) 25 February 2010 (2010-02-25) description, paragraphs [0001]-[0009] and Figure 2	1-23
Y	US 2014203395 A1 (SILICONWARE PREC. INDUSTRIES CO., LTD.) 24 July 2014 (2014-07-24) description, paragraphs [0030]-[0036] and Figure 3	1-23
Y	US 6376904 B1 (RAMBUS INC.) 23 April 2002 (2002-04-23) description, column 5, line 15 to column 7, line 10 and Figure 3	1-23
A	CN 101017811 A (SILICONWARE PREC. INDUSTRIES CO., LTD.) 15 August 2007 (2007-08-15) the whole document	1-23
A	CN 1617315 A (SILICONWARE PREC. INDUSTRIES CO., LTD.) 18 May 2005 (2005-05-18) the whole document	1-23

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 May 2015	**01 June 2016**
Name and mailing address of the ISA/CN **STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China** Facsimile No. **(86-10)62019451**	Authorized officer **ZHOU,Zhongtang** Telephone No. **(86-10)53318981**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/098867

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2015/098867

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				US	7638875	B2	29 December 2009
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				US	7851322	B2	14 December 2010
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				TW	I499013	B	01 September 2015
				TW	201431009	A	01 August 2014
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				US	6621155	B1	16 September 2003
CN	101017811	A	15 August 2007		None		
CN	1617315	A	18 May 2005	CN	1333449	C	22 August 2007
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