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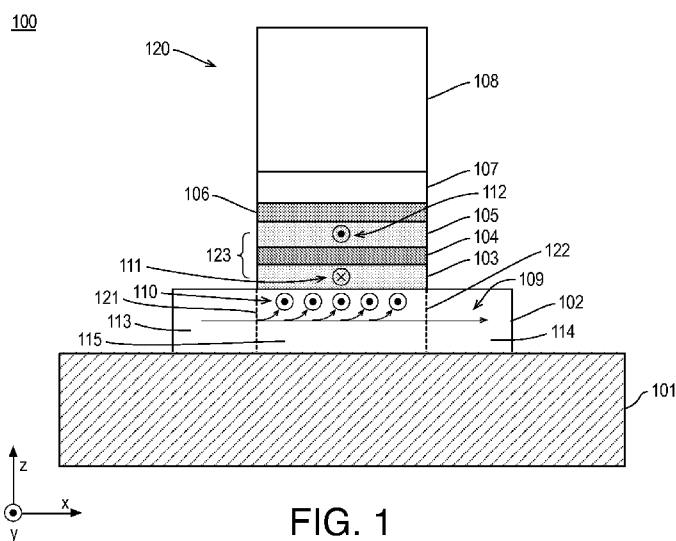


FIG. 1

(57) Abstract: Embodiments related to magnetic tunnel junction devices including a spin Hall effect metal layer having a first portion with a first crystallographic phase adjacent to a free magnetic layer and a second portion with a second crystallographic phase having a lower conductivity than the first crystallographic phase extending away from the first portion and the free magnetic layer, systems incorporating such devices, and methods for forming them are discussed.



FLASH ANNEAL OF A SPIN HALL EFFECT SWITCHED MAGNETIC TUNNEL JUNCTION DEVICE TO REDUCE RESISTIVITY OF METAL INTERCONNECTS

TECHNICAL FIELD

Embodiments of the invention generally relate to magnetic tunnel junction devices with reduced resistivity metal interconnects, and more particularly relate to magnetic tunnel junction
5 devices having spin Hall effect metal layer with a first crystallographic phase adjacent to a free magnetic layer and a second, lower resistivity crystallographic phase extending away from the first crystallographic phase.

BACKGROUND

In some implementations, magnetic tunnel junction (MTJ) devices, such as
10 magnetoresistive random-access memory (MRAM) devices may include a tunnel barrier layer between a fixed magnetic layer and a free magnetic layer. As its name suggests, the fixed magnetic layer may be set to a particular magnetic polarity. The free magnetic layer may be changed and a characteristic such as an electrical resistance may be detected to read the device (e.g., to read a bit cell of the device). The free magnetic layer may be changed or written by
15 passing current through the device to induce a magnetic field or using spin transfer torque (STT) techniques. For example, such spin transfer torque techniques may include providing a charge current flowing through a material adjacent to the free magnetic layer to create a spin current orthogonal to the direction of the charge current. The spin current may, via spin transfer torque, change the magnetic state or polarity of the free magnetic layer.

20 As discussed, spin transfer torque may be used to change or flip the polarity of the free magnetic layer in a magnetic tunnel junction device such as magnetic random access memory. Such spin transfer torque memory may offer advantages such as lower power consumption and better scalability over conventional magnetic random access memory as well as advantages over other conventional memory devices. However, significant improvements are still needed in the
25 implementation of such devices.

BRIEF DESCRIPTION OF THE DRAWINGS

The material described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements. In the figures:

FIG. 1 is a side view of an example magnetic tunnel junction device;

FIG. 2 illustrates example phase boundaries between a high resistance portion and low resistance portions of a spin Hall effect metal layer;

FIG. 3 is a side view of an example integrated circuit including magnetic tunnel junction devices;

FIG. 4 is a flow diagram illustrating an example process for forming magnetic tunnel junction devices having reduced resistivity metal interconnects;

FIGS. 5A, 5B, 5C, 5D, 5E, 5F, and 5G are side views of example magnetic tunnel junction device structures as particular fabrication operations are performed;

FIG. 6 illustrates an example MRAM cell implementing a magnetic tunnel junction device having reduced resistivity metal interconnects;

FIG. 7 is an illustrative diagram of a mobile computing platform employing a magnetic tunnel junction device having reduced resistivity metal interconnects; and

FIG. 8 is a functional block diagram of a computing device, all arranged in accordance with at least some implementations of the present disclosure.

DETAILED DESCRIPTION

One or more embodiments or implementations are now described with reference to the enclosed figures. While specific configurations and arrangements are discussed, it should be
5 understood that this is done for illustrative purposes only. Persons skilled in the relevant art will recognize that other configurations and arrangements may be employed without departing from the spirit and scope of the description. It will be apparent to those skilled in the relevant art that techniques and/or arrangements described herein may also be employed in a variety of other systems and applications other than what is described herein.

Reference is made in the following detailed description to the accompanying drawings,
10 which form a part hereof, wherein like numerals may designate like parts throughout to indicate corresponding or analogous elements. It will be appreciated that for simplicity and/or clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements
15 for clarity. Further, it is to be understood that other embodiments may be utilized and structural and/or logical changes may be made without departing from the scope of claimed subject matter. It should also be noted that directions and references, for example, up, down, top, bottom, over, under, and so on, may be used to facilitate the discussion of the drawings and embodiments and are not intended to restrict the application of claimed subject matter. Therefore, the following
20 detailed description is not to be taken in a limiting sense and the scope of claimed subject matter defined by the appended claims and their equivalents.

In the following description, numerous details are set forth, however, it will be apparent to one skilled in the art, that the present invention may be practiced without these specific details. In some instances, well-known methods and devices are shown in block diagram form, rather
25 than in detail, to avoid obscuring the present invention. Reference throughout this specification to “an embodiment” or “in one embodiment” means that a particular feature, structure, function, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrase “in an embodiment” in various places throughout this specification are not necessarily referring to the same embodiment of the
30 invention. Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment

may be combined with a second embodiment anywhere the two embodiments are not specified to be mutually exclusive.

The terms “coupled” and “connected,” along with their derivatives, may be used herein to describe structural relationships between components. It should be understood that these terms
5 are not intended as synonyms for each other. Rather, in particular embodiments, “connected” may be used to indicate that two or more elements are in direct physical or electrical contact with each other. “Coupled” may be used to indicate that two or more elements are in either direct or indirect (with other intervening elements between them) physical or electrical contact with each other, and/or that the two or more elements co-operate or interact with each other (e.g., as in a
10 cause an effect relationship).

The terms “over,” “under,” “between,” “on”, and/or the like, as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between
15 two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening features.

Magnetic tunnel junction devices, memory, integrated circuits, apparatuses, computing
20 platforms, and methods are described below related to magnetic tunnel junction devices having reduced resistivity metal interconnects.

As described above, magnetic tunnel junction devices such as magnetoresistive random-access memory devices that utilize spin transfer torque to change or flip the free magnetic layer may offer advantages over other magnetoresistive random-access memory devices. For example,
25 the magnetic tunnel junction devices may offer lower power consumption and better scalability. In an embodiment, a magnetic tunnel junction device may include an insulator layer between a fixed magnetic layer and a free magnetic layer and a spin Hall effect metal layer having a first portion adjacent to the free magnetic layer and a second portion extending away from the first portion and the free magnetic layer. For example, the first portion may include a first
30 crystallographic phase of the spin Hall effect metal layer and the second portion may include a second crystallographic phase of the spin Hall effect metal layer having a lower conductivity

than the first crystallographic phase. As is discussed further herein the first crystallographic phase of the spin Hall effect metal layer may, in response to a charge current, provide a spin current to switch a polarization of the free magnetic layer via spin transfer torque. The second crystallographic phase of the spin Hall effect metal layer may be incapable of providing such a spin transfer torque but may provide a substantially lower resistivity with respect to the first crystallographic phase.

Such a magnetic tunnel junction device may be formed using any suitable technique or techniques. In an embodiment, a free magnetic layer may be disposed over a first portion of a spin Hall effect metal layer having a first crystallographic phase, an insulator layer may be disposed over the free magnetic layer, a fixed magnetic layer may be disposed over the insulator layer, and a contact layer may be disposed over the fixed magnetic layer such that a second portion of the spin Hall effect metal layer is exposed, and the second portion of the spin Hall effect metal layer may be transformed from the first crystallographic phase to a second crystallographic phase having a lower conductivity than the first crystallographic phase. For example, the transforming of the exposed second portion may include a flash annealing operation.

The spin Hall effect metal layer may include any suitable material or materials. In some embodiments, the spin Hall effect metal layer includes or consists of tantalum or tungsten. For example, the first crystallographic phase may be a beta phase of tantalum and the second crystallographic phase may be an alpha phase of tantalum or the first crystallographic phase may be a beta phase of tungsten and the second crystallographic phase may be an alpha phase of tungsten. In some embodiments, the spin Hall effect metal layer includes or consists of platinum.

Such magnetic tunnel junction devices may be implemented via circuits or systems such as non-volatile magnetoresistive random-access memory circuits or systems or the like. In an embodiment, a non-volatile MRAM bit cell may include a selection transistor and a magnetic tunnel junction device coupled to the selection transistor such that the magnetic tunnel junction device includes an insulator layer between a fixed magnetic layer and a free magnetic layer and a spin Hall effect metal layer having a first portion adjacent to the free magnetic layer and a second portion extending away from the first portion and the free magnetic layer such that the first portion has a first crystallographic phase of the spin Hall effect metal layer and the second portion has a second crystallographic phase of the spin Hall effect metal layer having a lower conductivity than the first crystallographic phase as discussed above.

FIG. 1 is a side view of an example magnetic tunnel junction device 100, arranged in accordance with at least some implementations of the present disclosure. For example, magnetic tunnel junction device 100 may have reduced resistivity interconnects and may therefore advantageously provide for lower power devices. As shown, magnetic tunnel junction device 100 may include a substrate 101, a spin Hall effect metal layer 102, a free magnetic layer 103, an insulator layer 104 (e.g., a tunnel barrier), a fixed magnetic layer 105, an antiferromagnetic layer 106, and contact layers 107, 108. For example, material stack 120 may include any of spin Hall effect metal layer 102, free magnetic layer 103, insulator layer 104, fixed magnetic layer 105, antiferromagnetic layer 106, and contact layers 107, 108. For example, as discussed herein, material stack 120 may include free magnetic layer 103, insulator layer 104, fixed magnetic layer 105, antiferromagnetic layer 106, and contact layers 107, 108. Furthermore, as shown, free magnetic layer 103, insulator layer 104, and fixed magnetic layer 105 may provide for a magnetic tunnel junction 123.

In operation, fixed magnetic layer 105 may have a fixed magnetic polarity 112. In the illustrated example, magnetic polarity 112 is in a direction extending out of the page (e.g., in a y-direction); however any suitable fixed magnetic polarity 112 such as extending into the page or in a vertical (e.g., in a z-direction) may be provided. Furthermore, as shown, a magnetic polarity 111 of free magnetic layer 103 may be flipped, switched, changed, or modified or the like by applying a charge current 109 via spin Hall effect metal layer 102.

For example, spin Hall effect metal layer 102 may include low resistance portions 113, 114 and a high resistance portion 115. Low resistance portions 113, 114 may include a particular crystallographic phase of spin Hall effect metal layer 102 and high resistance portion 115 may include a different crystallographic phase of spin Hall effect metal layer 102. For example, the crystallographic phase of high resistance portion 115 may provide for the capability of spin Hall effect metal layer 102 to provide spin transfer torque to flip or switch magnetic polarity 111 of free magnetic layer 103 while the crystallographic phase of low resistance portions 113, 114 may not provide such functionality or may severely limit such functionality. As shown, in some embodiments, high resistance portion 115 may be in direct contact with free magnetic layer 103. In other embodiments, an intervening layer or layer may be provided between high resistance portion 115 and free magnetic layer 103 so long as high resistance portion 115 may provide for switching free magnetic layer 103 as discussed herein.

As shown, via high resistance portion 115 of spin Hall effect metal layer 102, charge current 109 may provide a spin current 110 orthogonal to the direction of charge current 109 due to a spin Hall effect (SHE). In an embodiment, a charge current 109 in the x-direction may provide a spin current 110 in the y-direction and a charge current 109 in the negative x-direction may provide a spin current 110 in the negative y-direction. For example, high resistance portion 115 of spin Hall effect metal layer 102 may include beta phase tantalum, beta phase tungsten, or beta phase platinum, which may provide a spin Hall effect to generate spin current 110. Spin current 110 may flip, switch, change, or modify magnetic polarity 111 via spin transfer torque (STT). By switching the direction of charge current 109, an opposite direction spin current 110 may be generated and an opposite polarity of magnetic polarity 111 may be provided. Such differences in polarity of magnetic polarity 111 may be detected via a change in resistance through magnetic tunnel junction device 100 or the like such that a memory cell may be provided (e.g., the memory cell may be written via changing polarity of magnetic polarity 111 and read via detection of resistance or the like).

For example, the discussed crystallographic phases of particular materials (e.g., beta phases of tantalum, tungsten, or platinum) may provide the capability of switching the state of magnetic tunnel junction device 100 based on a spin Hall effect. However, as discussed, such crystallographic phases may provide high electrical resistance (e.g., such phases may be high resistivity phases), which may make them poor interconnects. However, low resistance portions 113, 114 may advantageously offer lower electrical resistance and, therefore, better characteristics as interconnect portions of spin Hall effect metal layer 102. For example, low resistance portions 113, 114 may be different crystallographic phases with respect to high resistance portion 115. In an embodiment, spin Hall effect metal layer 102 may include or consist entirely of tantalum, high resistance portion 115 may be beta phase tantalum and low resistance portions 113, 114 may be alpha phase tantalum. In another embodiment, spin Hall effect metal layer 102 may include or consist entirely of tungsten, high resistance portion 115 may be beta phase tungsten and low resistance portions 113, 114 may be alpha phase tungsten. In yet another embodiment, spin Hall effect metal layer 102 may include or consist entirely of platinum, high resistance portion 115 may be beta phase platinum and low resistance portions 113, 114 may be alpha phase platinum.

Such low resistance crystallographic phases may, as discussed, offer better characteristics as interconnects; however, they may not be capable of providing spin current 110. Therefore,

spin Hall effect metal layer 102 may include high resistance portion 115 to provide for the spin Hall effect discussed above and low resistance portions 113, 114 to provide lower electrical resistance. For example, low resistance portions 113, 114 may extend away from high resistance portion 115 and free magnetic layer 103 and may include, as discussed, a crystallographic phase having a lower conductivity than the crystallographic phase of high resistance portion 115. In some embodiments, high resistance portion 115 may be characterized as a spin Hall effect portion, a high resistance crystallographic phase portion, a spin Hall effect crystallographic phase portion, or the like and/or low resistance portions 113, 114 may be characterized as interconnect portions, low resistance crystallographic phase portions, interconnect crystallographic phase portions or the like. In some embodiments, the electrical resistance of high resistance portion 115 may be about 5 to 10 or times greater than low resistance portions 113, 114. For example, the resistivities of beta phase tantalum and tungsten are about 10 times greater than the resistivities of alpha phase tantalum and tungsten.

Furthermore, FIG. 1 illustrates two low resistance portions 113, 114 each extending away from high resistance portion 115 and free magnetic layer 103 along substrate 101. However, magnetic tunnel junction device 100 may include any number of low resistance portions 113, 114 such as one low resistance portion or three or more low resistance portions. Low resistance portions 113, 114 may extend along a top of substrate 101 as shown or low resistance portions 113, 114 may extend within substrate 101 such as a channel formed in substrate 101 or the like.

As discussed, spin Hall effect metal layer 102 may include high resistance portion 115 and one or more low resistance portions 113, 114 extending away from high resistance portion 115. High resistance portion 115 and low resistance portions 113, 114 may meet at phase boundaries such as phase boundary 121 between high resistance portion 115 and low resistance portion 113 and phase boundary 122 between high resistance portion 115 and low resistance portion 114 having any suitable shape. In the embodiment of FIG. 1, phase boundaries 121, 122 extend substantially vertically downwardly from corners of free magnetic layer 103 to an edge of spin Hall effect metal layer 102. However, as discussed, phase boundaries 121, 122 may have any suitable shapes.

FIG. 2 illustrates example phase boundaries 201, 202 between high resistance portion 115 and low resistance portions 113, 114 of spin Hall effect metal layer 102, arranged in accordance with at least some implementations of the present disclosure. As shown, in some embodiments, phase boundaries 201, 202 between high resistance portion 115 and low resistance portions 113,

114 may have profiles that extend away from corners 203, 204 of free magnetic layer 103 to an edge of spin Hall effect metal layer 102. For example, phase boundary 201 may extend from corner 203 of free magnetic layer 103 to a bottom edge 207 of spin Hall effect metal layer 102 at a location 205 that is outside of free magnetic layer 103 and phase boundary 202 may extend
5 from corner 204 of free magnetic layer 103 to bottom edge 207 of spin Hall effect metal layer 102 at a location 206 that is outside of free magnetic layer 103. In the illustrated example, phase boundaries 201, 202 have concave curved profiles. However, phase boundaries 201, 202 may have any suitable shape such as linear profiles.

Returning to FIG. 1, as discussed, magnetic tunnel junction device 100 may include
10 substrate 101. Substrate 101 may include any suitable material, materials, and devices. In an embodiment, substrate 101 may include a semiconductor material such as monocrystalline silicon (Si), germanium (Ge), silicon germanium (SiGe), a III-V materials based material (e.g., gallium arsenide (GaAs)), a silicon carbide (SiC), a sapphire (Al₂O₃), or any combination thereof. In an embodiment, substrate 101 may include silicon having a (100) crystal orientation.
15 In various examples, substrate 101 may include metallization interconnect layers for integrated circuits or electronic devices such as transistors, memories, capacitors, resistors, optoelectronic devices, switches, or any other active or passive electronic devices separated by an electrically insulating layer, for example, an interlayer dielectric, a trench insulation layer, or the like. For example, substrate 101 may include metal contacts and interconnects as discussed further herein
20 with respect to FIG. 3.

As shown, magnetic tunnel junction device 100 may include spin Hall effect metal layer 102 having low resistance portions 113, 114 each extending away from high resistance portion 115 over substrate 101. In some embodiments, spin Hall effect metal layer 102 comprises tantalum, tungsten, or platinum with low resistance portions 113, 114 and high resistance portion
25 115 having different crystallographic phases discussed herein. Spin Hall effect metal layer 102 may have any suitable thickness such as a thickness of about 8 nm or more. Furthermore, magnetic tunnel junction device 100 may include free magnetic layer 103 disposed over high resistance portion 115 of spin Hall effect metal layer 102 such that low resistance portions 113, 114 are exposed with respect to free magnetic layer 103 and other components of material stack
30 120. As will be appreciated, exposed low resistance portions 113, 114 may be covered by a dielectric layer or passivation layer or the like such that exposed low resistance portions 113, 114 may be exposed with respect to material stack 120 but covered with a dielectric layer or

passivation layer or the like. Free magnetic layer 103 may include any suitable material or materials such as a ferromagnetic material of any suitable thickness such as a thickness in the range of about 0.4 to 3 nm. In an embodiment, free magnetic layer 103 is cobalt iron boron (CoFeB).

5 Also, as shown, magnetic tunnel junction device 100 may include insulator layer 104 (e.g., a tunnel barrier) over free magnetic layer 103. Insulator layer 104 may include any suitable material or materials such as magnesium oxide having any suitable thickness such as a thickness in the range of about 0.4 to 3 nm. Fixed magnetic layer 105 may be disposed over insulator layer 104 and fixed magnetic layer 105 may include any suitable material or materials such as a
10 ferromagnetic material of any suitable thickness such as a thickness in the range of about 0.4 to 3 nm. In an embodiment, fixed magnetic layer 105 is cobalt iron boron (CoFeB). The thicknesses of free magnetic layer 103 and fixed magnetic layer 105 may be the same or they may be different. Magnetic tunnel junction device 100 may also include antiferromagnetic layer 106 over fixed magnetic layer 105 and contact layers 107, 108 over antiferromagnetic layer 106.
15 Antiferromagnetic layer 106 and contact layers 107, 108 may include any suitable material or materials of any suitable thicknesses. In an embodiment, antiferromagnetic layer 106 is a synthetic antiferromagnetic (SAF) layer. In an embodiment, contact layers 107, 108 may include tantalum and ruthenium, respectively. In some embodiments, contact layers 107, 108 include two layers as shown; however any number of contact layers such as one contact layer may be used. In
20 some embodiments, contact layer 107 and/or contact layer 108 may be characterized as an electrode such as a fixed electrode and spin Hall effect metal layer 102 may be characterized as an electrode such as a free electrode.

As shown, in some embodiments, free magnetic layer 103, insulator layer 104, fixed magnetic layer 105, antiferromagnetic layer 106, and contact layers 107, 108 of material stack
25 120 may have substantially vertical sidewalls. However, in some embodiments, such sidewalls may be tapered. Furthermore, material stack 120 may have any suitable dimensions. For example, free magnetic layer 103, insulator layer 104, fixed magnetic layer 105, antiferromagnetic layer 106, and contact layers 107, 108 of material stack 120 may have a width (e.g., in the x-direction) of about 50 to 70 nm and a depth (e.g., in the y direction) of about 120 to
30 200 nm.

FIG. 3 is a side view of an example integrated circuit 300 including magnetic tunnel junction device 100 and a magnetic tunnel junction device 301, arranged in accordance with at

least some implementations of the present disclosure. For example, integrated circuit 300 may include a memory circuit, a processor having integrated memory, a system on a chip, or the like. As shown, integrated circuit 300 may include magnetic tunnel junction device 100 and magnetic tunnel junction device 301 having any characteristics discussed herein. For example, magnetic tunnel junction device 100 may include material stack 120 including spin Hall effect metal layer 102 with high resistance portion 115 and low resistance portions 113, 114. Furthermore, magnetic tunnel junction device 301 may include material stack 320 including spin Hall effect metal layer 302 with high resistance portion 315 and low resistance portions 313, 314. Magnetic tunnel junction device 301 may have any characteristics as discussed herein with respect to magnetic tunnel junction device 100. In some embodiments, magnetic tunnel junction devices 100, 301 may have the same characteristics and, in other embodiments, they may have one or more different characteristics.

As shown, substrate 101 may include contacts 331–334 disposed within an interlayer dielectric 341 (ILD). For example, contacts 331–334 may interconnect magnetic tunnel junction devices 100, 301 to devices formed within lower levels of substrate 101 such as logic transistors, other devices, or the like. For example, as shown, low resistance portions 113, 114 of spin Hall effect metal layer 102 may extend to contacts 331, 332, respectively, and low resistance portions 313, 314 of spin Hall effect metal layer 302 may extend to contacts 333, 334, respectively. Such low resistance portions may provide for desirable interconnect characteristics such as low resistivity and high resistance portions 115, 315 may provide for operation of magnetic tunnel junction devices 100, 301 as discussed herein. In the illustrated example, contacts 331–334 are below magnetic tunnel junction devices 100, 301. In other examples, one or more of contacts 331–334 may be beside or above magnetic tunnel junction devices 100, 301.

Additional details associated with the described features of magnetic tunnel junction devices 100, 301 are provided herein with respect to FIGS. 5A–5G and the associated discussion, which provides additional details related to the formation of magnetic tunnel junction devices 100, 301. Furthermore, magnetic tunnel junction devices 100, 301 may be implemented in an electronic device structure such as a logic device incorporating memory, an MRAM, or the like, as is discussed further herein.

FIG. 4 is a flow diagram illustrating an example process 400 for forming magnetic tunnel junction devices having reduced resistivity metal interconnects, arranged in accordance with at least some implementations of the present disclosure. For example, process 400 may be

implemented to magnetic tunnel junction device 100 and/or magnetic tunnel junction device 301 as discussed herein. In the illustrated implementation, process 400 may include one or more operations as illustrated by operations 401–403. However, embodiments herein may include additional operations, certain operations being omitted, or operations being performed out of the order provided.

Process 400 may begin at operation 401, “Dispose a Free Magnetic Layer over a First Portion of a Spin Hall Effect Metal Layer having a First Crystallographic Phase”, where a free magnetic layer may be disposed over a first portion of a spin Hall effect metal layer having a first crystallographic phase. For example, the first crystallographic phase may be a phase operable to switch the free magnetic layer (e.g., the first crystallographic phase may be beta phase tantalum, beta phase tungsten, beta phase platinum, or the like). In an embodiment, free magnetic layer 103 of material stack 120 and/or a free magnetic layer of material stack 320 may be formed over portions of spin Hall effect metal layers 503, 504, respectively as discussed further herein with respect to FIGS. 5A–5E and elsewhere herein. In an embodiment, the free magnetic layer may be disposed over the first portion of the spin Hall effect metal layer using a bulk deposition technique and subsequent patterning technique.

Process 400 may continue at operation 402, “Dispose an Insulator Layer, a Fixed Magnetic Layer, and a Contact Layer Over the Free Magnetic Layer such that a Second Portion of the Spin Hall Effect Metal Layer is Exposed”, where an insulator layer may be disposed over the free magnetic layer, a fixed magnetic layer may be disposed over the insulator layer, and a contact layer may be disposed over the fixed magnetic layer such that a second portion of the spin Hall effect metal layer is exposed. In an embodiment, insulator layer 104, fixed magnetic layer 105, and one or both of contact layers 107, 108 of material stack 120 may be disposed over free magnetic layer 103 and/or an insulator layer, a fixed magnetic layer, and one or both of contact layers of material stack 320 may be disposed over a free magnetic layer of material stack 320 as discussed further herein with respect to FIGS. 5C–5E and elsewhere herein. In an embodiment, the insulator layer may be disposed over the free magnetic layer, the fixed magnetic layer may be disposed over the insulator layer, and the contact layer may be disposed over the fixed magnetic layer using bulk deposition techniques and a subsequent patterning technique.

Process 400 may continue at operation 403, “Transform the Second Portion of the Spin Hall Effect Metal Layer from the First Crystallographic Phase to a Second Crystallographic Phase”, where the exposed second portion of the spin Hall effect metal layer may be transformed

from the first crystallographic phase to a second crystallographic phase having a lower conductivity than the first crystallographic phase. The exposed second portion of the spin Hall effect metal layer may be transformed using any suitable technique or techniques. In an embodiment, the second portion of the spin Hall effect metal layer may be transformed from the first crystallographic phase to the second crystallographic phase via a flash annealing operation as discussed further herein with respect to FIG. 5F and elsewhere herein.

As discussed, process 400 may be implemented to fabricate magnetic tunnel junction device 100 and/or magnetic tunnel junction device 301. Further details associated with such fabrication techniques are discussed herein in particular, with respect to FIGS. 5A–5G. Any one or more of the operations of process 400 (or the operations discussed herein with respect to FIGS. 5A–5G) may be undertaken in response to instructions provided by one or more computer program products. Such program products may include signal bearing media providing instructions that, when executed by, for example, a processor, may provide the functionality described herein. The computer program products may be provided in any form of computer readable medium. Thus, for example, a processor including one or more processor core(s) may undertake one or more of the described operations in response to instructions conveyed to the processor by a computer readable medium.

FIGS. 5A–5G are side views of example magnetic tunnel junction device structures as particular fabrication operations are performed, arranged in accordance with at least some implementations of the present disclosure. FIG. 5A illustrates a side view of magnetic tunnel junction device structure 501. As shown in FIG. 5A, magnetic tunnel junction device structure 501 includes substrate 101 having contacts 331–334 disposed with interlayer dielectric 341. For example, contacts 331–334 may interconnect subsequently formed magnetic tunnel junction devices 100, 301 to devices previously formed within lower levels of substrate 101 such as logic transistors, other devices, or the like. In an embodiment, contacts 331–334 may provide connection to a metal 2 layer of devices formed within substrate 101. Substrate 101 may be formed using any suitable technique or techniques.

FIG. 5B illustrates a magnetic tunnel junction device structure 502 similar to magnetic tunnel junction device structure 501, after the formation of spin Hall effect metal layers 503, 504. Spin Hall effect metal layers 503, 504 may be formed using any suitable technique or techniques. In an embodiment, spin Hall effect metal layers 503, 504 may be formed by providing a bulk material layer (e.g., via electroplating or deposition or the like) and subsequent patterning (e.g.,

via photolithography patterning and etch techniques, or the like). Spin Hall effect metal layers 503, 504 may include any material or materials operable to provide spin transfer torque to a subsequently formed free magnetic layer as discussed herein. In an embodiment, spin Hall effect metal layers 503, 504 comprise or consist entirely of beta phase tantalum. In another embodiment, spin Hall effect metal layers 503, 504 comprise or consist entirely of beta phase tungsten. In yet another embodiment, spin Hall effect metal layers 503, 504 comprise or consist entirely of beta phase platinum. Although illustrated with spin Hall effect metal layers 503, 504 having the same compositions, in some embodiments, spin Hall effect metal layers 503, 504 may have different compositions. As discussed, spin Hall effect metal layers 503, 504 may extend from contacts 331, 332 and from contacts 333, 334, respectively. Furthermore, spin Hall effect metal layers 503, 504 may have any suitable thickness such as a thickness of 8 nm or more.

FIG. 5C illustrates a magnetic tunnel junction device structure 505 similar to magnetic tunnel junction device structure 502, after the formation of a bulk free magnetic layer 506, a bulk insulator layer 507, a bulk fixed magnetic layer 508, a bulk antiferromagnetic layer 508, a bulk contact layer 510, and a bulk contact layer 511. Bulk free magnetic layer 506, bulk insulator layer 507, bulk fixed magnetic layer 508, bulk antiferromagnetic layer 508, bulk contact layer 510, and bulk contact layer 511 may be formed using any suitable technique or techniques such as electroplating, deposition, or the like. Furthermore, free magnetic layer 506, bulk insulator layer 507, bulk fixed magnetic layer 508, bulk antiferromagnetic layer 508, bulk contact layer 510, and bulk contact layer 511 may have any suitable thicknesses. For example, free magnetic layer 506 may have a thickness over spin Hall effect metal layers 503, 504 in the range of about 0.4 to 3 nm, bulk insulator layer 507 may have a thickness in the range of about 0.4 to 3 nm, and bulk fixed magnetic layer 508 may have a thickness in the range of about 0.4 to 3 nm.

FIG. 5D illustrates a magnetic tunnel junction device structure 512 similar to magnetic tunnel junction device structure 505, after the formation of a mask 513 and material stacks 120, 320. Mask 513 may be formed using any suitable technique or techniques such as photolithography techniques. In some embodiments, mask 513 may include a hardmask material (e.g., silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, or the like). Mask 513 may be any material that provides for patterning selectivity with respect to bulk free magnetic layer 506, bulk insulator layer 507, bulk fixed magnetic layer 508, bulk antiferromagnetic layer 509, bulk contact layer 510, and/or bulk contact layer 511. In some embodiments, the formation

of material stacks 120, 320 may include material removal techniques such as etch techniques or the like.

FIG. 5E illustrates a magnetic tunnel junction device structure 514 similar to magnetic tunnel junction device structure 512, after the removal of mask 513. Mask 513 may be removed
5 using any suitable technique or techniques such as ash techniques, etch techniques, or the like.

FIG. 5F illustrates a magnetic tunnel junction device structure 515 similar to magnetic tunnel junction device structure 514, during the transformation of exposed portions of spin Hall effect metal layers 503, 504 from a first crystallographic phase to a second crystallographic phase having a lower conductivity than the first crystallographic phase. As discussed, the second
10 crystallographic phase may have a lower conductivity than the first crystallographic phase to provide for advantageous interconnect characteristics and such that the second crystallographic phase may not be capable of switching free magnetic layers via spin transfer torque as discussed herein. As discussed, the exposed portions of spin Hall effect metal layers 503, 504 may be transformed from the first crystallographic phase to the second crystallographic phase using any
15 suitable technique or techniques.

In the example of FIG. 5F, the exposed portions of spin Hall effect metal layers 503, 504 may be transformed using a flash annealing operation. For example, a flash lamp 516 may provide radiation 517 that may flash anneal the exposed portions of spin Hall effect metal layers 503, 504 to transform them from the first to second crystallographic phase. In an embodiment,
20 the exposed portions may be beta phase tantalum and the flash anneal may anneal the exposed portions to form alpha phase tantalum low resistance portions 113, 114, 313, 314 and leaving beta phase tantalum high resistance portions 115, 315. In such embodiments, the flash anneal may anneal the exposed portions to or at a temperature of not less than 750°C. In another embodiment, the exposed portions may be beta phase tungsten and the flash anneal may anneal
25 the exposed portions to form alpha phase tungsten low resistance portions 113, 114, 313, 314 and leaving beta phase tungsten high resistance portions 115, 315. In such embodiments, the flash anneal may anneal the exposed portions to or at a temperature of not less than 850°C. In yet another embodiment, the exposed portions may be beta phase platinum and the flash anneal may anneal the exposed portions to form alpha phase platinum low resistance portions 113, 114, 313,
30 314 and leaving beta phase platinum high resistance portions 115, 315. In such embodiments, the flash anneal may anneal the exposed portions to or at a temperature of not less than 750°C.

As discussed, the flash anneal may leave high resistance portions 115, 315. For example, the material stacks 120, 320 may block exposure of high resistance portions 115, 315 to radiation 517 and thereby maintaining the crystallographic phase of high resistance portions 115, 315. The discussed flash anneal may be performed using any suitable technique or techniques. For example, the flash anneal may include a flash or radiation intensity or power and/or a flash or radiation duration. One or both of such intensity or power and/or duration may be adjusted to provide the discussed flash anneal temperatures and/or crystallographic phase changes. In some embodiments, radiation 517 may be provided from flash lamp 516 in the range of microseconds to milliseconds.

FIG. 5G illustrates a magnetic tunnel junction device structure 518 similar to magnetic tunnel junction device structure 515, after the formation of low resistance portions 113, 114, 313, 314. Magnetic tunnel junction device structure 518 may have any characteristics as discussed herein such as those discussed with respect to FIGS. 1–3. Furthermore, as will be appreciated, magnetic tunnel junction device structure 518 may be subjected to further processing such as back end processing for the generation of additional interconnect layers (e.g., metal layers and contact or via layers), passivation, packaging, and the like. Such back end processing may include limitations on processing temperature (e.g., a temperature limit of not more than 400°C or the like) that may ensure high resistance portions 115, 315 do not undergo crystallographic phase changes (e.g., such that high resistance portions 115, 315 may be operable to switch free magnetic layers as discussed herein).

FIGS. 5A–5G illustrate an example process flow for fabricating magnetic tunnel junction device 100 and/or magnetic tunnel junction device 301 as discussed herein. In various examples, additional operations may be included or certain operations may be omitted.

FIG. 6 illustrates an example MRAM cell 600 implementing a magnetic tunnel junction device 601 having reduced resistivity metal interconnects, arranged in accordance with at least some implementations of the present disclosure. As shown, MRAM cell 600 may include magnetic tunnel junction device 601, a selection transistor 605, a word line 604, a source line 606, a bit line 603, and a reference line 602. As shown, magnetic tunnel junction device 601 may be coupled to selection transistor 605 such that magnetic tunnel junction device 601 may be selected for reading and writing. For example, magnetic tunnel junction device 601 may be read by providing a current through magnetic tunnel junction device 601 via bit line 603 and source line 606 when magnetic tunnel junction device 601 is selected via selection transistor 605 as

asserted by word line 604. For example, a resistance of magnetic tunnel junction device 601 may be evaluated to determine the bit of information stored therein. Furthermore, magnetic tunnel junction device 601 may be written by providing a current through high resistance portion 115 of spin Hall effect metal layer 102 as discussed herein and as provided via bit line 603 and reference line 602. For example, reference line 602 may be held at a reference potential such as ground and may provide a reference plane or the like. MRAM cell 600 may include additional read and write circuitry (not shown), a sense amplifier (not shown), a bit line reference (not shown), or the like, as will be understood by those skilled in the art, for the operation of MRAM cell 600. MRAM cell 600 may be characterized as a bit cell, an MRAM bit cell, a spin Hall effect magnetic tunnel junction (SHE-MTJ) bit cell, or the like.

Referring to FIG. 6, magnetic tunnel junction device 601 may include any characteristics as discussed with respect to magnetic tunnel junction device 100 or elsewhere herein. For example, magnetic tunnel junction device 601 may include an insulator layer between a fixed magnetic layer and a free magnetic layer and a spin Hall effect metal layer having a first portion adjacent to the free magnetic layer and a second portion extending away from the first portion and the free magnetic layer such that the first portion comprises a first crystallographic phase of the spin Hall effect metal layer and the second portion comprises a second crystallographic phase of the spin Hall effect metal layer having a lower conductivity than the first crystallographic phase. In an embodiment, the spin Hall effect metal layer comprises tantalum, the first phase comprises an beta phase of tantalum, and the second phase comprises an alpha phase of tantalum. In another embodiment, the spin Hall effect metal layer comprises tungsten, the first phase comprises an beta phase of tungsten, and the second phase comprises an alpha phase of tungsten. In yet another embodiment, the spin Hall effect metal layer consists of tantalum or tungsten, the magnetic fixed layer and the magnetic free layer comprise cobalt iron boron, and the insulator layer comprises magnesium oxide.

FIG. 7 is an illustrative diagram of a mobile computing platform 700 employing a magnetic tunnel junction device having reduced resistivity metal interconnects, arranged in accordance with at least some implementations of the present disclosure. For example, mobile computing platform 700 may include a magnetic tunnel junction device including a spin Hall effect metal layer having a first portion with a first crystallographic phase adjacent to a free magnetic layer and a second portion with a second crystallographic phase having a lower conductivity than the first crystallographic phase. The magnetic tunnel junction device may be

any magnetic tunnel junction device discussed herein such as magnetic tunnel junction device 100 or magnetic tunnel junction device 301 or the like. In some examples, the magnetic tunnel junction device and transistors may be implemented together as an integrated circuit. Mobile computing platform 700 may be any portable device configured for each of electronic data display, electronic data processing, wireless electronic data transmission, or the like. For example, mobile computing platform 700 may be any of a tablet, a smart phone, a netbook, a laptop computer, etc. and may include a display screen 705, which in the exemplary embodiment is a touchscreen (e.g., capacitive, inductive, resistive, etc. touchscreen), a chip-level (SoC) or package-level integrated system 710, and a battery 715.

Integrated system 710 is further illustrated in the expanded view 720. In the exemplary embodiment, packaged device 750 (labeled “Memory/Processor” in FIG. 7) includes at least one memory chip (e.g., MRAM), and/or at least one processor chip (e.g., a microprocessor, a multi-core microprocessor, or graphics processor, or the like). In an embodiment, packaged device 750 is a microprocessor including an MRAM cache memory. In an embodiment, packaged device 750 includes one or more of magnetic tunnel junction device 100 or magnetic tunnel junction device 301 or both. For example, an employed memory cell may include magnetic tunnel junction device 100 or magnetic tunnel junction device 301. Packaged device 750 may be further coupled to (e.g., communicatively coupled to) a board, a substrate, or an interposer 760 along with, one or more of a power management integrated circuit (PMIC) 730, RF (wireless) integrated circuit (RFIC) 725 including a wideband RF (wireless) transmitter and/or receiver (TX/RX) (e.g., including a digital baseband and an analog front end module further comprises a power amplifier on a transmit path and a low noise amplifier on a receive path), and a controller thereof 735. In general, packaged device 750 may be also be coupled to (e.g., communicatively coupled to) display screen 705.

Functionally, PMIC 730 may perform battery power regulation, DC-to-DC conversion, etc., and so has an input coupled to battery 715 and an output providing a current supply to other functional modules. In an embodiment, PMIC 730 may perform high voltage operations. As further illustrated, in the exemplary embodiment, RFIC 725 has an output coupled to an antenna (not shown) to implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated

as 3G, 4G, 5G, and beyond. In alternative implementations, each of these board-level modules may be integrated onto separate ICs coupled to the package substrate of packaged device 750 or within a single IC (SoC) coupled to the package substrate of the packaged device 750.

FIG. 8 is a functional block diagram of a computing device 800, arranged in accordance with at least some implementations of the present disclosure. Computing device 800 may be found inside platform 800, for example, and further includes a motherboard 802 hosting a number of components, such as but not limited to a processor 801 (e.g., an applications processor) and one or more communications chips 804, 805. Processor 801 may be physically and/or electrically coupled to motherboard 802. In some examples, processor 801 includes an integrated circuit die packaged within the processor 801. In general, the term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

In various examples, one or more communication chips 804, 805 may also be physically and/or electrically coupled to the motherboard 802. In further implementations, communication chips 804 may be part of processor 801. Depending on its applications, computing device 800 may include other components that may or may not be physically and electrically coupled to motherboard 802. These other components may include, but are not limited to, volatile memory (e.g., DRAM) 807, 808, non-volatile memory (e.g., ROM) 810, a graphics processor 812, flash memory, global positioning system (GPS) device 813, compass 814, a chipset 806, an antenna 816, a power amplifier 809, a touchscreen controller 811, a touchscreen display 817, a speaker 815, a camera 803, and a battery 818, as illustrated, and other components such as a digital signal processor, a crypto processor, an audio codec, a video codec, an accelerometer, a gyroscope, and a mass storage device (such as hard disk drive, solid state drive (SSD), compact disk (CD), digital versatile disk (DVD), and so forth), or the like.

Communication chips 804, 805 may enable wireless communications for the transfer of data to and from the computing device 800. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. Communication chips 804, 805 may implement any of a number of wireless standards or protocols, including but not limited to those described

elsewhere herein. As discussed, computing device 800 may include a plurality of communication chips 804, 805. For example, a first communication chip may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA,
5 WiMAX, LTE, Ev-DO, and others.

As used in any implementation described herein, the term “module” refers to any combination of software, firmware and/or hardware configured to provide the functionality described herein. The software may be embodied as a software package, code and/or instruction set or instructions, and “hardware”, as used in any implementation described herein, may include,
10 for example, singly or in any combination, hardwired circuitry, programmable circuitry, state machine circuitry, and/or firmware that stores instructions executed by programmable circuitry. The modules may, collectively or individually, be embodied as circuitry that forms part of a larger system, for example, an integrated circuit (IC), system on-chip (SoC), and so forth.

While certain features set forth herein have been described with reference to various
15 implementations, this description is not intended to be construed in a limiting sense. Hence, various modifications of the implementations described herein, as well as other implementations, which are apparent to persons skilled in the art to which the present disclosure pertains are deemed to lie within the spirit and scope of the present disclosure.

The following examples pertain to further embodiments.

20 In one or more first embodiments, a magnetic tunnel junction device comprises an insulator layer between a fixed magnetic layer and a free magnetic layer and a spin Hall effect metal layer having a first portion adjacent to the free magnetic layer and a second portion extending away from the first portion and the free magnetic layer, wherein the first portion comprises a first crystallographic phase of the spin Hall effect metal layer and the second portion
25 comprises a second crystallographic phase of the spin Hall effect metal layer having a lower conductivity than the first crystallographic phase.

Further to the first embodiments, the spin Hall effect metal layer comprises tantalum, the first phase comprises an beta phase of tantalum, and the second phase comprises an alpha phase of tantalum.

Further to the first embodiments, the spin Hall effect metal layer comprises tungsten, the first phase comprises an beta phase of tungsten, and the second phase comprises an alpha phase of tungsten.

5 Further to the first embodiments, the spin Hall effect metal layer consists of tantalum or tungsten.

Further to the first embodiments, the magnetic fixed layer and the magnetic free layer comprise cobalt iron boron and the insulator layer comprises magnesium oxide.

10 Further to the first embodiments, the spin Hall effect metal layer consists of tantalum or tungsten, the magnetic fixed layer and the magnetic free layer comprise cobalt iron boron, and the insulator layer comprises magnesium oxide.

Further to the first embodiments, the first portion of the spin Hall effect metal layer is in contact with the free magnetic layer.

15 Further to the first embodiments, in response to a charge current, the first portion of the spin Hall effect metal layer is to provide a spin current to switch a polarization of the free magnetic layer via a spin transfer torque.

Further to the first embodiments, the first portion of the spin Hall effect metal layer is in contact with the free magnetic layer and/or, in response to a charge current, the first portion of the spin Hall effect metal layer is to provide a spin current to switch a polarization of the free magnetic layer via a spin transfer torque.

20 Further to the first embodiments, the magnetic tunnel junction device further comprises an antiferromagnetic layer in contact with the fixed magnetic layer and a metal contact layer in contact with the antiferromagnetic layer.

Further to the first embodiments, the first and second crystallographic phases meet at a phase boundary having a profile extending away from a corner of the free magnetic layer.

25 Further to the first embodiments, the second portion of the spin Hall effect metal layer extends from the first portion along a substrate to a contact disposed within the substrate.

In one or more second embodiments, a method for fabricating a magnetic tunnel junction device comprises disposing a free magnetic layer over a first portion of a spin Hall effect metal

layer having a first crystallographic phase, disposing an insulator layer over the free magnetic layer, a fixed magnetic layer over the insulator layer, and a contact layer over the fixed magnetic layer, wherein a second portion of the spin Hall effect metal layer is exposed, and transforming the second portion of the spin Hall effect metal layer from the first crystallographic phase to a second crystallographic phase having a lower conductivity than the first crystallographic phase.

Further to the second embodiments, transforming the second portion of the spin Hall effect metal layer comprises a flash annealing operation.

Further to the second embodiments, transforming the second portion of the spin Hall effect metal layer comprises a flash annealing operation, the spin Hall effect metal layer comprises tantalum, and the flash annealing operation anneals the second portion of the spin Hall effect metal layer to a temperature not less than 750°C.

Further to the second embodiments, transforming the second portion of the spin Hall effect metal layer comprises a flash annealing operation, the spin Hall effect metal layer comprises tungsten, and the flash annealing operation anneals the second portion of the spin Hall effect metal layer to a temperature not less than 850°C.

Further to the second embodiments, transforming the second portion of the spin Hall effect metal layer comprises a flash annealing operation, the spin Hall effect metal layer comprises tantalum and the flash annealing operation anneals the second portion of the spin Hall effect metal layer to a temperature not less than 750°C or the spin Hall effect metal layer comprises tungsten and the flash annealing operation anneals the second portion of the spin Hall effect metal layer to a temperature not less than 850°C.

Further to the second embodiments, the method further comprises disposing an antiferromagnetic layer between the fixed magnetic layer and the contact.

In one or more third embodiments, a non-volatile MRAM bit cell comprises a selection transistor and a magnetic tunnel junction device coupled to the selection transistor, the magnetic tunnel junction device including an insulator layer between a fixed magnetic layer and a free magnetic layer and a spin Hall effect metal layer having a first portion adjacent to the free magnetic layer and a second portion extending away from the first portion and the free magnetic layer, wherein the first portion comprises a first crystallographic phase of the spin Hall effect

metal layer and the second portion comprises a second crystallographic phase of the spin Hall effect metal layer having a lower conductivity than the first crystallographic phase.

Further to the third embodiments, the spin Hall effect metal layer comprises tantalum, the first phase comprises an beta phase of tantalum, and the second phase comprises an alpha phase of tantalum.

Further to the third embodiments, the spin Hall effect metal layer comprises tungsten, the first phase comprises an beta phase of tungsten, and the second phase comprises an alpha phase of tungsten.

Further to the third embodiments, the spin Hall effect metal layer consists of tantalum or tungsten, the magnetic fixed layer and the magnetic free layer comprise cobalt iron boron, and the insulator layer comprises magnesium oxide.

Further to the third embodiments, the first portion of the spin Hall effect metal layer is in contact with the free magnetic layer.

In one or more fourth embodiments, a mobile computing platform comprises any of the example structures discussed with respect to the first or second embodiments.

It will be recognized that the invention is not limited to the embodiments so described, but can be practiced with modification and alteration without departing from the scope of the appended claims. For example, the above embodiments may include specific combination of features. However, the above embodiments are not limited in this regard and, in various implementations, the above embodiments may include the undertaking only a subset of such features, undertaking a different order of such features, undertaking a different combination of such features, and/or undertaking additional features than those features explicitly listed. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

25

CLAIMS

What is claimed is:

- 5 1. A magnetic tunnel junction device comprising:
an insulator layer between a fixed magnetic layer and a free magnetic layer; and
a spin Hall effect metal layer having a first portion adjacent to the free magnetic layer and
a second portion extending away from the first portion and the free magnetic layer,
wherein the first portion comprises a first crystallographic phase of the spin Hall effect
10 metal layer and the second portion comprises a second crystallographic phase of the spin Hall
effect metal layer having a lower conductivity than the first crystallographic phase.
2. The magnetic tunnel junction device of claim 1, wherein the spin Hall effect metal layer
comprises tantalum, the first phase comprises an beta phase of tantalum, and the second phase
15 comprises an alpha phase of tantalum.
3. The magnetic tunnel junction device of claim 1, wherein the spin Hall effect metal layer
comprises tungsten, the first phase comprises an beta phase of tungsten, and the second phase
comprises an alpha phase of tungsten.
20
4. The magnetic tunnel junction device of claim 1, wherein the spin Hall effect metal layer
consists of tantalum or tungsten.
5. The magnetic tunnel junction device of claim 1, wherein the magnetic fixed layer and the
25 magnetic free layer comprise cobalt iron boron and the insulator layer comprises magnesium
oxide.

6. The magnetic tunnel junction device of claim 1, wherein the first portion of the spin Hall effect metal layer is in contact with the free magnetic layer.

7. The magnetic tunnel junction device of claim 1, wherein, in response to a charge current,
5 the first portion of the spin Hall effect metal layer is to provide a spin current to switch a polarization of the free magnetic layer via a spin transfer torque.

8. The magnetic tunnel junction device of claim 1, further comprising an antiferromagnetic layer in contact with the fixed magnetic layer and a metal contact layer in contact with the
10 antiferromagnetic layer.

9. The magnetic tunnel junction device of claim 1, wherein the first and second crystallographic phases meet at a phase boundary having a profile extending away from a corner of the free magnetic layer.

15

10. The magnetic tunnel junction device of claim 1, wherein the second portion of the spin Hall effect metal layer extends from the first portion along a substrate to a contact disposed within the substrate.

20 11. A method for fabricating a magnetic tunnel junction device comprising:
disposing a free magnetic layer over a first portion of a spin Hall effect metal layer having a first crystallographic phase;
disposing an insulator layer over the free magnetic layer, a fixed magnetic layer over the insulator layer, and a contact layer over the fixed magnetic layer, wherein a second portion of the
25 spin Hall effect metal layer is exposed; and

transforming the second portion of the spin Hall effect metal layer from the first crystallographic phase to a second crystallographic phase having a lower conductivity than the first crystallographic phase.

5 12. The method of claim 11, wherein transforming the second portion of the spin Hall effect metal layer comprises a flash annealing operation.

13. The method of claim 12, wherein the spin Hall effect metal layer comprises tantalum and the flash annealing operation anneals the second portion of the spin Hall effect metal layer to a
10 temperature not less than 750°C.

14. The method of claim 12, wherein the spin Hall effect metal layer comprises tungsten and the flash annealing operation anneals the second portion of the spin Hall effect metal layer to a temperature not less than 850°C.

15

15. The method of claim 11, further comprising disposing an antiferromagnetic layer between the fixed magnetic layer and the contact.

16. A non-volatile MRAM bit cell comprising:
20 a selection transistor and a magnetic tunnel junction device coupled to the selection transistor, the magnetic tunnel junction device including:

an insulator layer between a fixed magnetic layer and a free magnetic layer; and
a spin Hall effect metal layer having a first portion adjacent to the free magnetic layer and a second portion extending away from the first portion and the free magnetic
25 layer,

wherein the first portion comprises a first crystallographic phase of the spin Hall effect metal layer and the second portion comprises a second crystallographic phase of the spin Hall effect metal layer having a lower conductivity than the first crystallographic phase.

5

17. The non-volatile MRAM bit cell of claim 16, wherein the spin Hall effect metal layer comprises tantalum, the first phase comprises an beta phase of tantalum, and the second phase comprises an alpha phase of tantalum.

10 18. The non-volatile MRAM bit cell of claim 16, wherein the spin Hall effect metal layer comprises tungsten, the first phase comprises an beta phase of tungsten, and the second phase comprises an alpha phase of tungsten.

15 19. The non-volatile MRAM bit cell of claim 16, wherein the spin Hall effect metal layer consists of tantalum or tungsten, the magnetic fixed layer and the magnetic free layer comprise cobalt iron boron, and the insulator layer comprises magnesium oxide.

20. The non-volatile MRAM bit cell of claim 16, wherein the first portion of the spin Hall effect metal layer is in contact with the free magnetic layer.

20

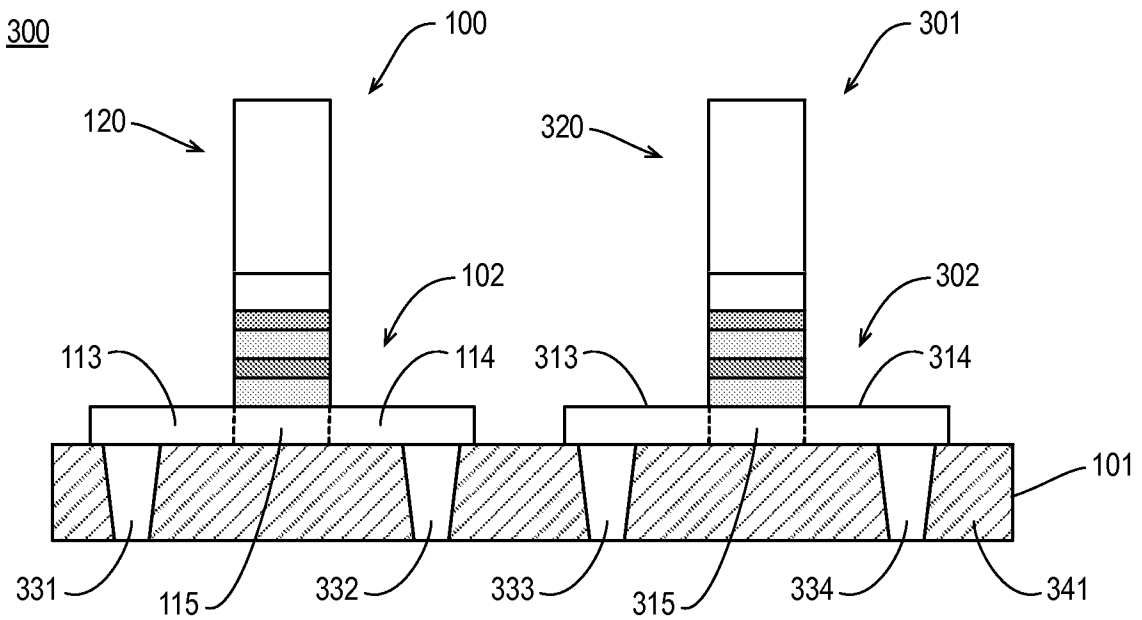


FIG. 3

400

Dispose a Free Magnetic Layer over a First Portion of a Spin Hall Effect Metal Layer having a First Crystallographic Phase

401

Dispose an Insulator Layer, a Fixed Magnetic Layer, and a Contact Layer Over the Free Magnetic Layer such that a Second Portion of the Spin Hall Effect Metal Layer is Exposed

402

Transform the Second Portion of the Spin Hall Effect Metal Layer from the First Crystallographic Phase to a Second Crystallographic Phase

403

FIG. 4

501

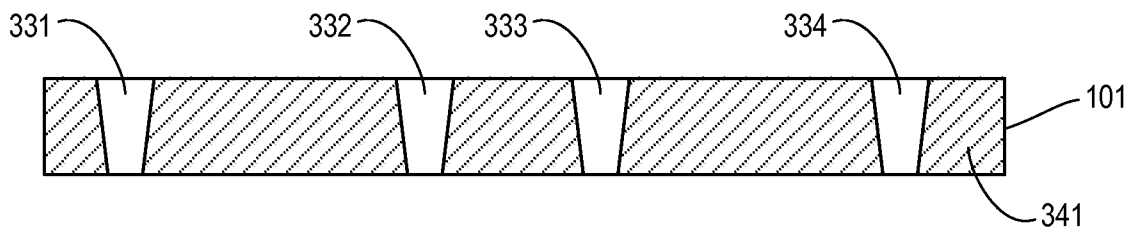


FIG. 5A

502

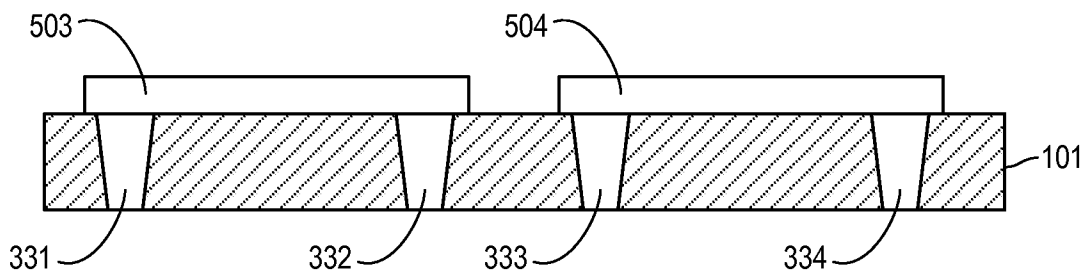


FIG. 5B

505

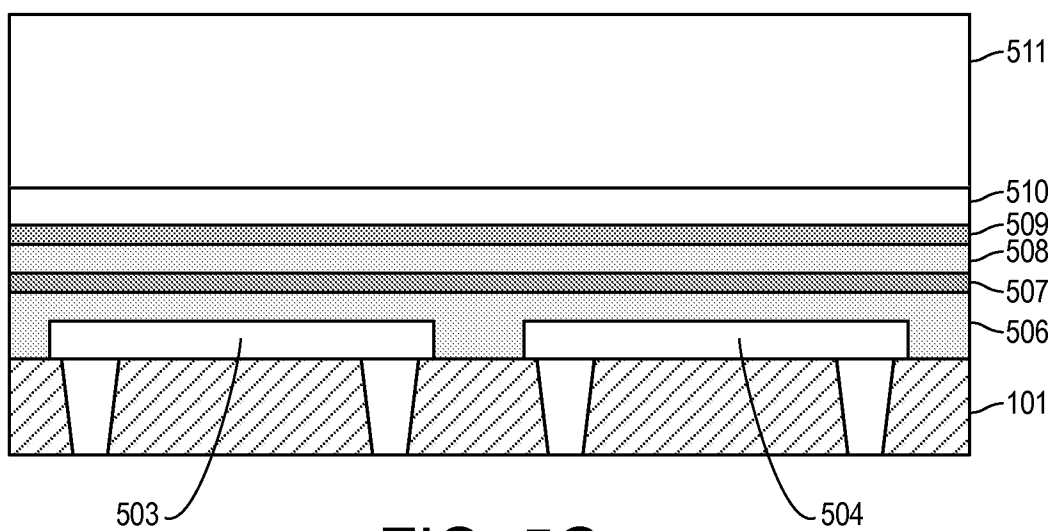


FIG. 5C

512

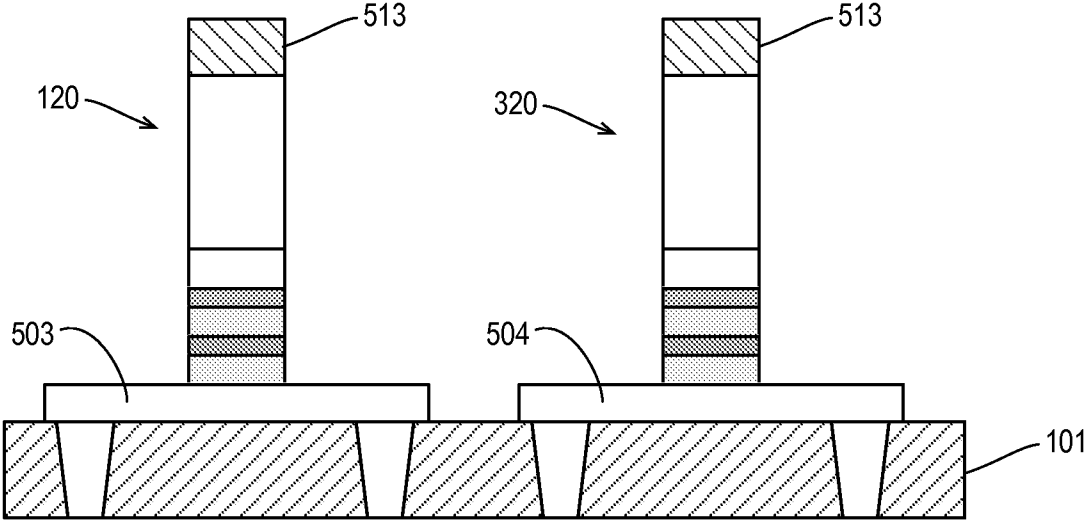


FIG. 5D

514

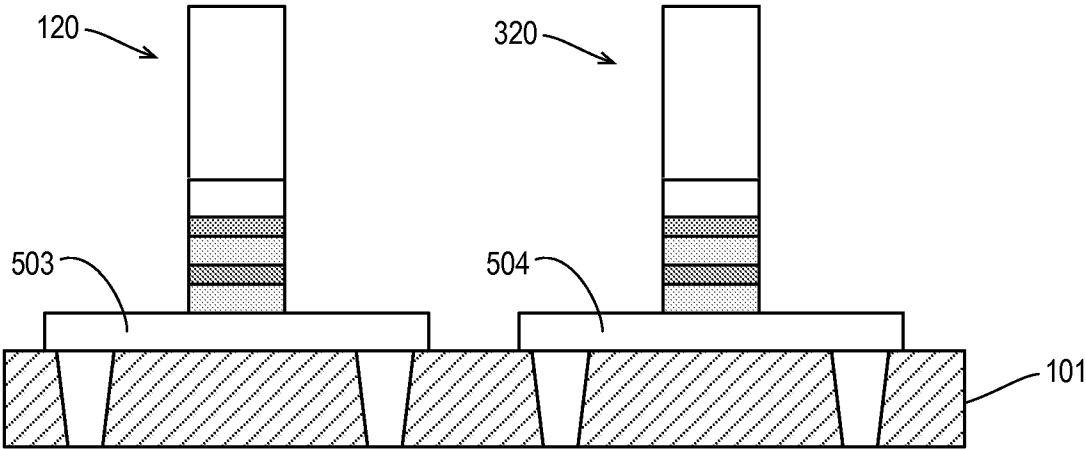


FIG. 5E

515

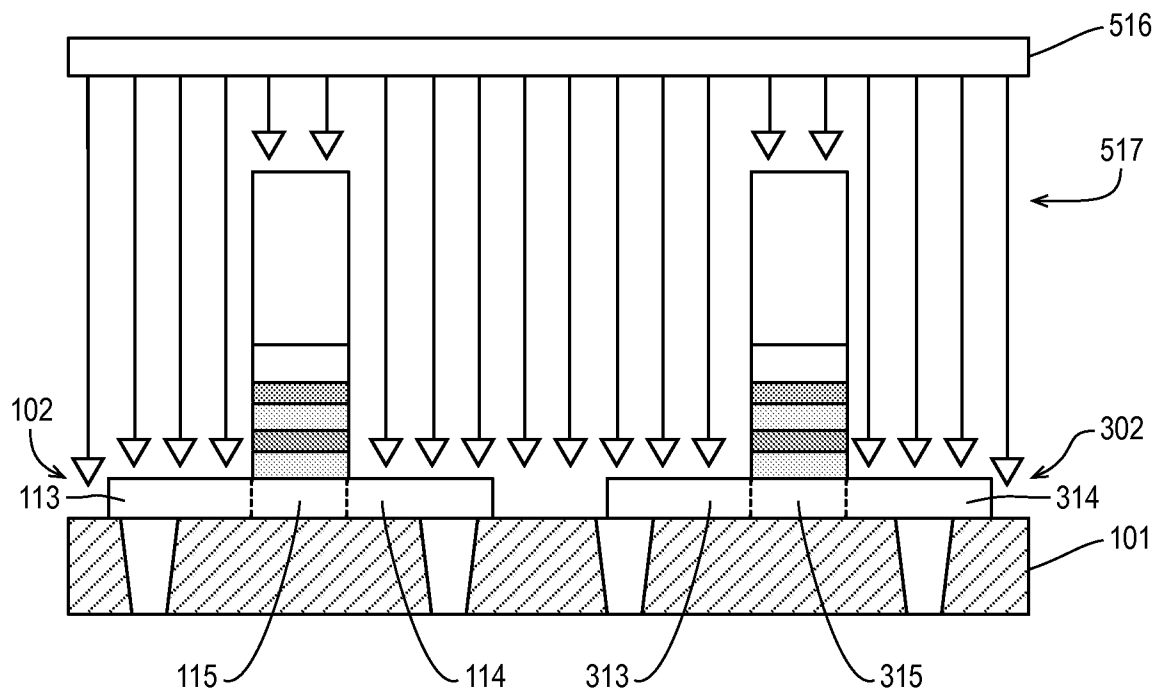


FIG. 5F

518

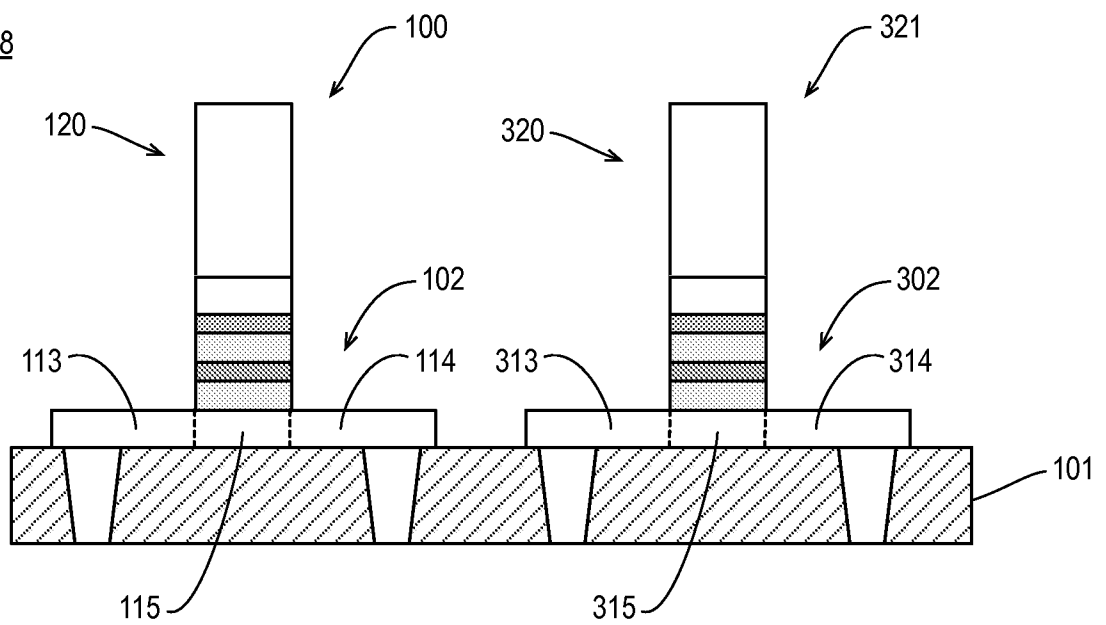


FIG. 5G

600

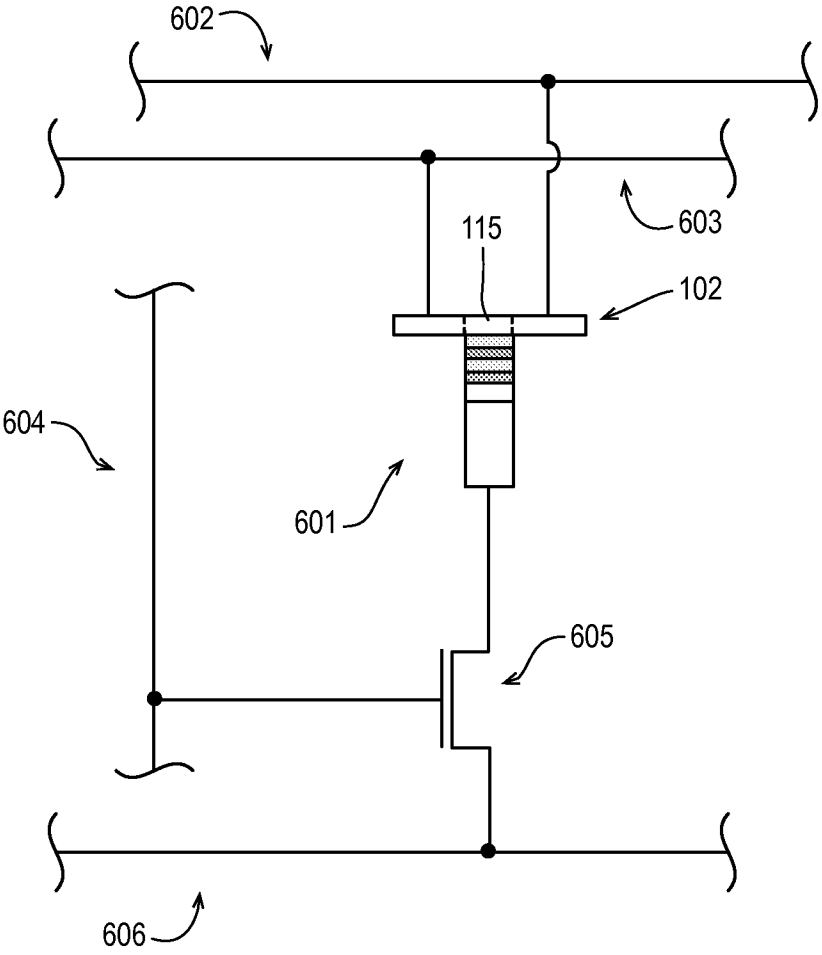


FIG. 6

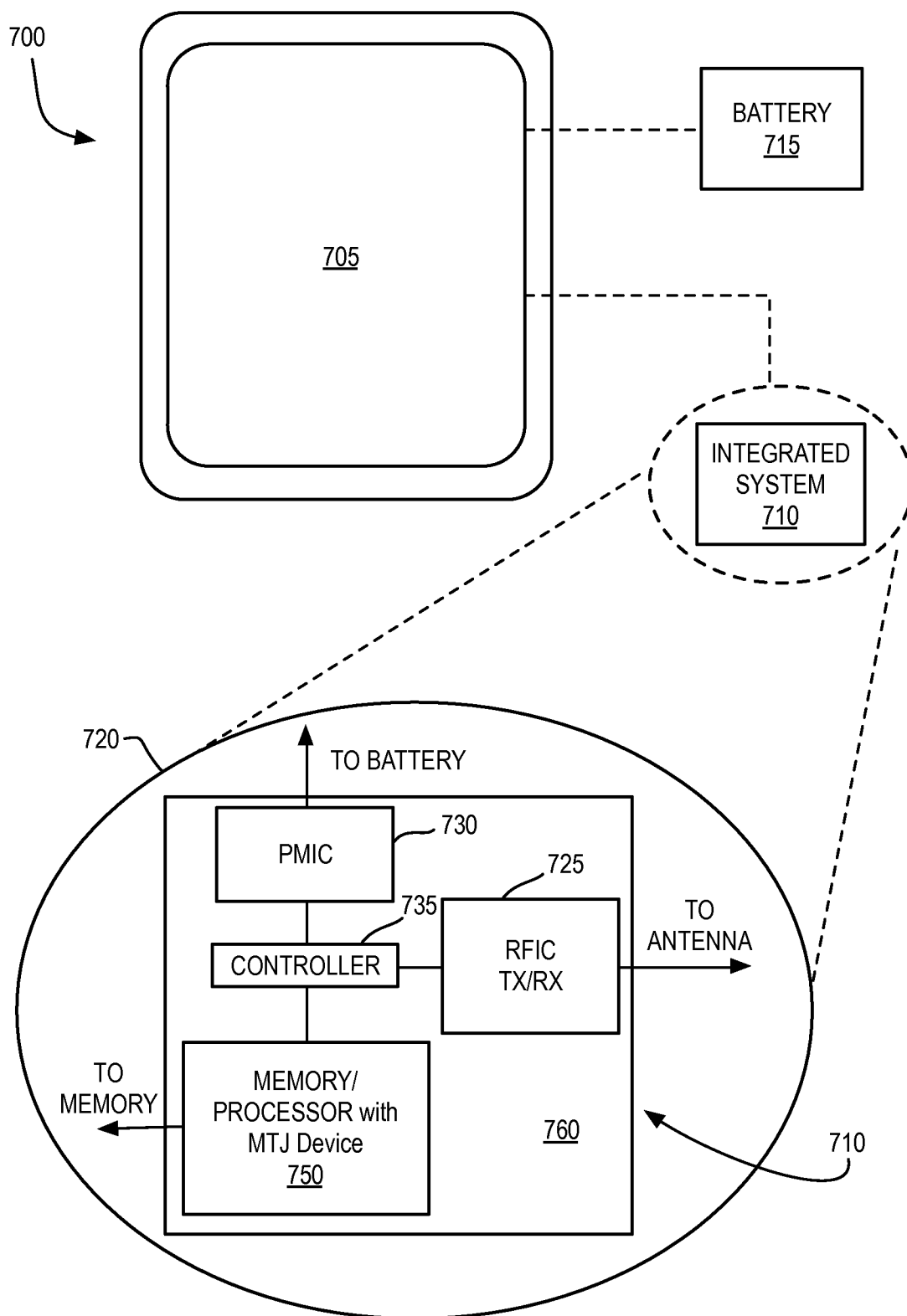


FIG. 7

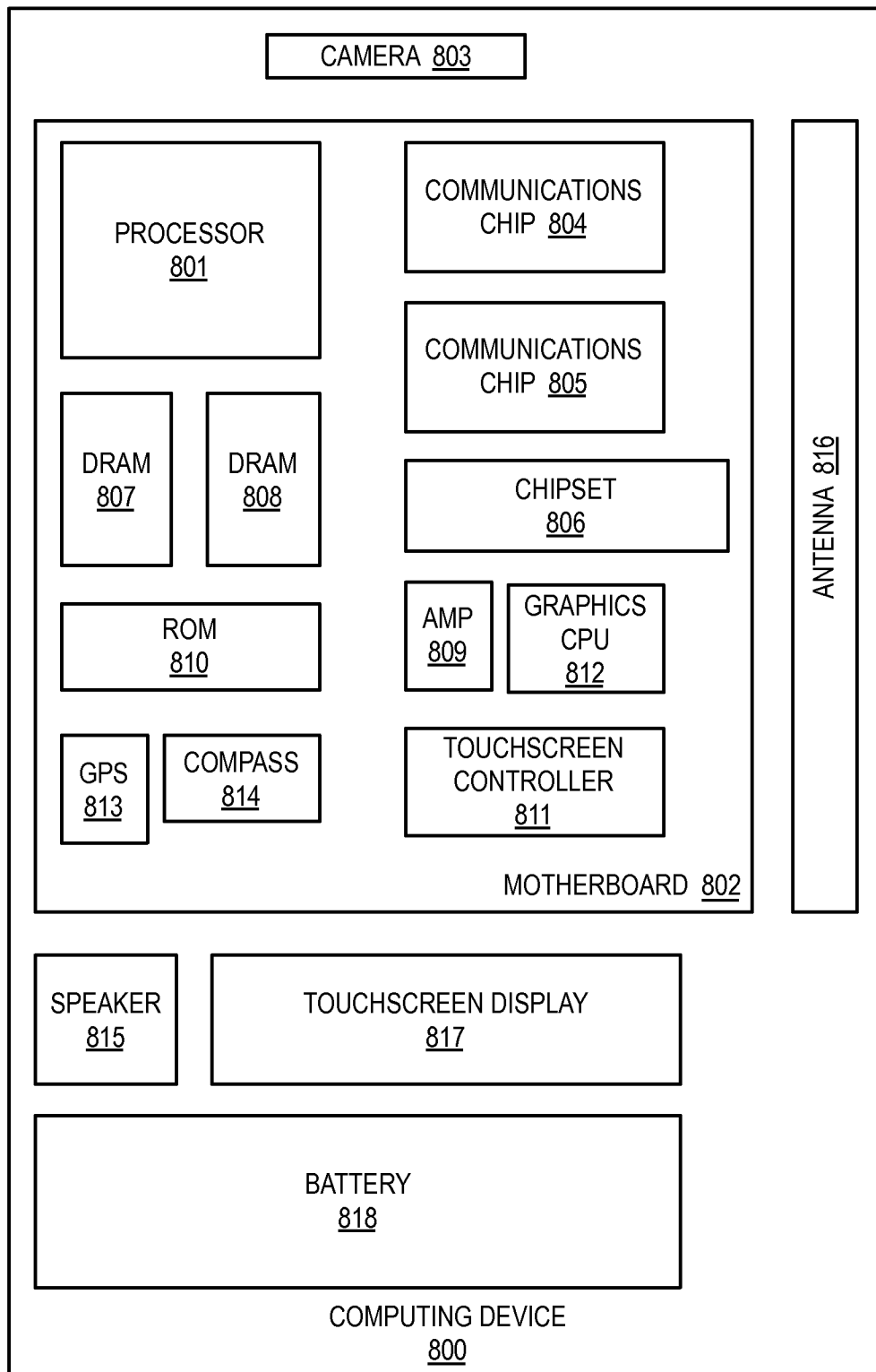


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/051177**A. CLASSIFICATION OF SUBJECT MATTER****H01L 43/04(2006.01)i, H01L 43/06(2006.01)i, H01L 43/02(2006.01)i, H01L 43/10(2006.01)i, H01L 43/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 43/04; G11C 16/30; H01L 21/8246; C23F 1/00; H03K 3/356; H01L 43/14; H01L 27/10; H01L 43/06; H01L 43/02; H01L 43/10; H01L 43/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: magnetic tunnel junction, resistivity, flash anneal, α -Ta, β -Ta**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0169088 A1 (ROBERT A. BUHRMAN et al.) 19 June 2014 See paragraphs [0013]-[0079], claim 1 and figure 18.	1-11, 15-20
Y		12-14
Y	US 2011-0174770 A1 (JOHN J. HAUTALA) 21 July 2011 See paragraphs [0026]-[0032], claim 1 and figure 1.	12-14
A	JP 2012-257206 A (SEMICONDUCTOR ENERGY LAB CO., LTD.) 27 December 2012 See paragraphs [0148]-[0161], claim 1 and figure 1.	1-20
A	US 2014-0252439 A1 (YIMIN GUO) 11 September 2014 See paragraphs [0044]-[0058], claim 1 and figure 1.	1-20
A	US 2010-0047929 A1 (LIUBO HONG et al.) 25 February 2010 See paragraphs [0055]-[0067], claim 1 and figure 8.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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