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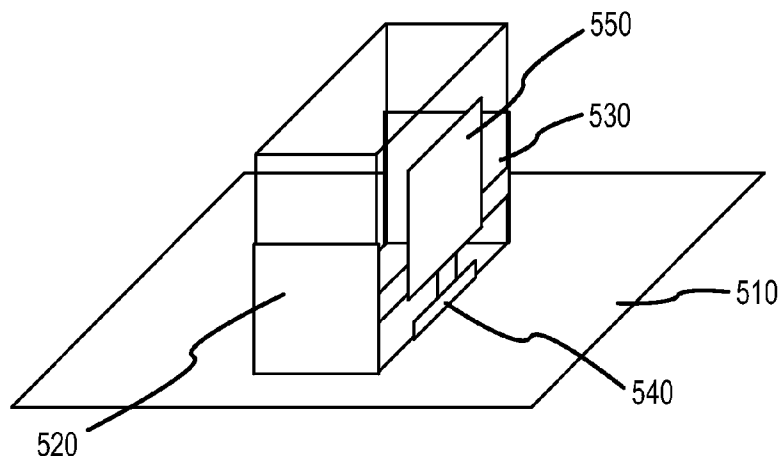


FIG. 5B

(57) Abstract: A device according to various aspects of the present invention generally includes a surface mount device having a top side, a bottom side, a plurality of sidewalls, and a circuit comprising one or more layers. The device includes a first conductive surface covering a portion of one of the sidewalls for providing an input to the circuit, a second conductive surface covering a portion of one of the sidewalls for providing an output from the circuit, and a third conductive surface covering a portion of one of the sidewalls for providing an electrical ground to the circuit. When the surface mount device is mounted to a provided mounting surface, at least one layer of the circuit is orthogonal to the provided mounting surface.

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SURFACE MOUNT DEVICES WITH MINIMUM LEAD INDUCTANCE AND METHODS OF MANUFACTURING THE SAME

DESCRIPTION OF THE INVENTION

Field of the Invention

The present invention relates to surface mount devices, and more particularly, to surface mount devices with minimum lead inductance and methods of manufacturing the same.

Background of the Invention

Surface mount devices (SMDs) are electronic components used in a wide variety of applications. Traditionally, SMDs use side terminals, also known as leads or terminals, for electrical connection to a mounting surface on a printed circuit board (PCB), substrate, or the like. Figure 1 depicts a prior art SMD having a plurality of side terminals 110. Typically, conventional SMDs, such as the one shown in Figure 1, include a circuit (not shown) residing in or on one of more upper layers of the SMD. The bottom surface of the SMD is mounted to a mounting surface (not shown). As shown in Figure 1, side terminals 110 extend from the top surface of the SMD to the bottom surface of the SMD, thereby connecting the circuit on or near the top of the SMD to conductors on the mounting surface. Consequently, all side terminals 110 connecting the circuit to a mounting surface have a length 130 that is at least the height of the substrate 120.

Side terminals 110 have inherent inductances associated with the length and thickness of the side terminals 110. Such inherent inductance can cause signal distortion and performance degradation, particularly in high frequency SMD applications. Conventional methods of reducing side terminal inductance include reducing the length of the side terminal 110 and using wider and thicker metal traces for the side terminal 110. However, modification of the dimensions of the side terminal 110 may be restricted by factors such as substrate thickness, minimum physical strength requirements, and process requirements. The dimensions of the side terminal 110 may also be restricted by the dimensions of the SMD itself.

Lead inductance can have a detrimental effect on a wide range of SMDs, including Integrated Passive Devices (IPDs). In the case of IPD filters, for example, the associated parasitic inductance due to the length of the leads 110 can seriously deteriorate the filter's out-band rejection performance. Additionally, as SMDs are used at higher frequencies, the effect of the lead inductance is even more significant. Reducing the thickness of the wafer substrate 120 thickness may be helpful to reduce associated lead inductance in these cases, but this technique is of limited use since the substrate 120 must have a minimum thickness to maintain the requisite

physical strength for assembly, handling, and system reliability. These and other issues are addressed by the embodiments of the present invention.

SUMMARY OF THE INVENTION

5 A device according to various aspects of the present invention comprises a surface mount device having a top side, a bottom side, a plurality of sidewalls, and a circuit comprising one or more layers. The device includes a first conductive surface covering a portion of one of the sidewalls for providing an input to the circuit, a second conductive surface covering a portion of one of the sidewalls for providing an output from the circuit, and a third conductive surface
10 covering a portion of one of the sidewalls for providing an electrical ground to the circuit. When the surface mount device is mounted to a provided mounting surface, at least one layer of the circuit is orthogonal to the provided mounting surface.

 In another device according to various aspects of the present invention, at least two of the first conductive surface, the second conductive surface, and the third conductive surface cover
15 respective portions of the same sidewall.

 In another device according to various aspects of the present invention, each of the first conductive surface, the second conductive surface and the third conductive surface covers a portion of a different one of the plurality of sidewalls.

 In another device according to various aspects of the present invention, the third
20 conductive surface is for bonding to the provided mounting surface.

 In another device according to various aspects of the present invention, a majority of the third conductive surface is for bonding to the provided mounting surface.

 In another device according to various aspects of the present invention, a portion of at least one of the first conductive surface and the second conductive surface is coplanar with the
25 majority of the third conductive surface for bonding to the provided mounting surface.

 In another device according to various aspects of the present invention, one of the sidewalls of the surface mount device is for bonding to the provided mounting surface.

 In another device according to various aspects of the present invention, the circuit comprises an integrated passive device.

30 In another device according to various aspects of the present invention, the circuit comprises an integrated active device.

 In another device according to various aspects of the present invention, the circuit comprises a filter.

Another device according to various aspects of the present invention further comprises a passivation layer covering at least a portion of the circuit.

A method for manufacturing a device according to various aspects of the present invention comprises providing a surface mount device, wherein the surface mount device
5 comprises a top side, a bottom side, a plurality of sidewalls, and a circuit comprising one or more layers; covering a portion of one of the sidewalls with a first conductive surface, the first conductive surface for providing an input to the circuit; covering a portion of one of the sidewalls with a second conductive surface, the second conductive surface for providing an
10 output from the circuit; and covering a portion of one of the sidewalls with a third conductive surface, the third conductive surface for providing an electrical ground to the circuit, wherein when the surface mount device is mounted to a provided mounting surface, at least one layer of the circuit is orthogonal to the provided mounting surface.

In another method for manufacturing a device according to various aspects of the present invention, at least two of the first conductive surface, second conductive surface, and the third
15 conductive surface cover respective portions of the same sidewall.

In another method for manufacturing a device according to various aspects of the present invention, each of the first conductive surface, the second conductive surface and the third conductive surface covers a portion of a different one of the plurality of sidewalls.

In another method for manufacturing a device according to various aspects of the present
20 invention, the third conductive surface is for bonding to the provided mounting surface.

In another method for manufacturing a device according to various aspects of the present invention, a majority of the third conductive surface is for bonding to the provided mounting surface.

In another method for manufacturing a device according to various aspects of the present
25 invention, a portion of at least one of the first conductive surface and the second conductive surface is coplanar with the majority of the third conductive surface for bonding to the provided mounting surface.

In another method for manufacturing a device according to various aspects of the present invention, one of the sidewalls of the surface mount device is for bonding to the provided
30 mounting surface.

In another method for manufacturing a device according to various aspects of the present invention, the circuit comprises an integrated passive device.

In another method for manufacturing a device according to various aspects of the present invention, the circuit comprises an integrated active device.

In another method for manufacturing a device according to various aspects of the present invention, the circuit comprises a filter.

Another method for manufacturing a device according to various aspects of the present invention further comprises covering at least a portion of the circuit with a passivation layer.

5 A system according to various aspects of the present invention comprises an apparatus including a mounting surface; and a surface mount device mounted to the mounting surface, the surface mount device comprising: a top side, a bottom side, a plurality of sidewalls, and a circuit comprising one or more layers; a first conductive surface covering a portion of one of the sidewalls, the first conductive surface for providing an input to the circuit; a second conductive
10 surface covering a portion of one of the sidewalls, the second conductive surface for providing an output from the circuit; and a third conductive surface covering a portion of one of the sidewalls, the third conductive surface for providing an electrical ground to the circuit, wherein when the surface mount device is mounted to the mounting surface, at least one layer of the circuit is orthogonal to the mounting surface.

15 In another system according to various aspects of the present invention, at least two of the first conductive surface, the second conductive surface, and the third conductive surface cover respective portions of the same sidewall.

 In another system according to various aspects of the present invention, each of the first conductive surface, the second conductive surface and the third conductive surface covers a
20 portion of a different one of the plurality of sidewalls.

 In another system according to various aspects of the present invention, the third conductive surface is for bonding to the provided mounting surface.

 In another system according to various aspects of the present invention, a majority of the third conductive surface is for bonding to the provided mounting surface.

25 In another system according to various aspects of the present invention, a portion of at least one of the first conductive surface and the second conductive surface is coplanar with the majority of the third conductive surface for bonding to the provided mounting surface.

 In another system according to various aspects of the present invention, one of the sidewalls of the surface mount device is for bonding to the provided mounting surface.

30 In another system according to various aspects of the present invention, the circuit comprises an integrated passive device.

 In another system according to various aspects of the present invention, the circuit comprises an integrated active device.

In another system according to various aspects of the present invention, the circuit comprises a filter.

Another system according to various aspects of the present invention, further comprises a passivation layer covering at least a portion of the circuit.

5 It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

10 The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

Figure 1 is a perspective view of a prior art surface mount device (SMD).

Figure 2 is a perspective view of a prior art SMD providing a filter circuit.

Figure 3 is a schematic of the filter circuit in Figure 2.

15 Figure 4 depicts the frequency response of the filter circuit in Figure 2, with and without ground lead inductance.

Figure 5A is a perspective view of a prior art SMD.

Figure 5B is a perspective view of an exemplary embodiment of an SMD in accordance with aspects of the present invention.

20 Figure 5C is a perspective view of an exemplary embodiment of an SMD in accordance with aspects of the present invention.

Figure 6A is a perspective view of a prior art SMD providing a filter circuit.

Figure 6B is a perspective view of an exemplary embodiment of an SMD providing a filter circuit in accordance with aspects of the present invention.

25 Figure 7 depicts the frequency response of the circuits in Figures 6A and 6B.

Figure 8 is a side view of an SMD according to aspects of the present invention.

Figures 9A, 9B, and 10 depict exemplary processes for constructing an SMD according to aspects of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

30 Figure 2 depicts a prior art SMD providing a filter circuit 210 residing on or near the top side of the SMD. The filter circuit 210 includes four sidewall terminals 110: an input terminal 220, an output terminal 230, and two ground terminals 240. In this example, only the ground terminal 240 in the foreground is connected to the filter circuit 210.

The schematic diagram for the filter circuit 210 in Figure 2 is depicted in Figure 3. The filter circuit 210 includes three resonators (L1/C1; L2/C2; and L3/C3). The inductance attributable to the ground lead 240 is represented by the inductor L4. In the case of an exemplary filter fabricated with thin-film processes to provide an SMD with side-wall terminations as depicted in Figure 2, and having a case size of 1mm by 0.5mm and a substrate thickness of 0.3mm., this ground inductance L4 is about 0.16nH. Figure 4 shows the frequency response for the filter circuit 210 with (410) and without (420) the 0.16nH ground inductance L4. It can be seen that out-band rejection performance with the ground inductance L4 is considerably worse than that of the out-band rejection of the filter circuit 210 without the ground inductance L4.

An SMD may be constructed according to various aspects of the present invention to minimize lead inductance. Figure 5A depicts a prior art SMD having an input terminal 220, an output terminal 230, and a ground terminal 240 connected to a circuit 210. In contrast, an embodiment of an SMD according to the present invention is depicted in Figure 5B. In this exemplary embodiment, a first conductive surface serves as an input terminal 520, a second conductive surface serves as an output terminal 530, and a third conductive surface serves as a ground terminal 540. The SMD comprises a circuit 550 on or near the top surface of the SMD. The SMD is rotated such that the circuit 550 (and thus the top of the SMD) is orthogonal to the mounting surface 510.

Each conductive surface 520, 530, or 540 may cover any portion of the SMD. In the exemplary embodiment depicted in Figure 5B, the conductive surface for the input terminal 520 covers a portion of the sidewall in the foreground (orthogonal to the mounting surface 110) and a portion of the bottom sidewall adjacent to, and coplanar with, the mounting surface 510. The conductive surface for the output terminal 530 covers a portion of the sidewall shown in Figure 5B as the rear sidewall, as well as a portion of the sidewall adjacent to, and coplanar with, the mounting surface 510. The conductive surface for the ground terminal 540 covers a portion of the top of the SMD to connect with the circuit 550, as well as covering the sidewall of the SMD adjoining the mounting surface 510. In this exemplary embodiment, the ground terminal 540 is connected directly to the mounting surface 510, avoiding the ground inductance L4 associated with the ground terminal 540 in the conventional SMD.

Any circuit 550 may be used in conjunction with an SMD according to the present invention. The circuit 550 may serve any number of functions, have any number of leads, and may be configured in any suitable manner. For example, referring to Figure 5C, a circuit 550 may connect to an input terminal 520, an output terminal 530, and a ground terminal 540, each

comprising conductive surfaces each covering portions of the same sidewall adjacent and coplanar with the mounting surface 510 in order to minimize the inherent inductance of all three terminals 520, 530, and 540.

The present invention may provide various other benefits. For example, in the case of a circuit 550 comprising a filter, having the bottom of the SMD in contact with air instead of the mounting surface 510 (as depicted in Figures 5B and 5C) may increase the quality factor (Q) of the filter to reduce insertion loss in the passband of the filter. Additionally, referring to Figure 5C, by having leads 520, 530, and 540 on the sidewall adjacent to, and coplanar with, the mounting surface 510 may allow the dimensions of each lead to be reduced to allow additional leads to be connected to the circuit 550, where such connections may not be physically possible on a conventional SMD. The circuit may be designed and configured in any appropriate manner to operate in accordance with the present invention. For example, a circuit 550 that would connect to multiple ground terminals 240 in a conventional SMD may be configured to connect to a single ground terminal 540 for use with an SMD in accordance with the present invention.

Any type of SMD may utilize aspects of the present invention to minimize lead inductance. For example, Figure 6A depicts a prior art SMD comprising an integrated passive device (IPD) providing a filter circuit 610 connected to an input terminal 220, an output terminal 230, and a ground terminal 240 in the foreground of the figure. Figure 6B depicts an SMD providing the same filter circuit 610, but oriented to attach to a mounting surface (like mounting surface 510 shown in Figure 5B) through an input terminal 620, an output terminal 630, and a ground terminal 640. In this example, by connecting the ground terminal 640 to the mounting surface in this manner, the inherent inductance associated with the ground terminal 640 is minimized. As shown in Figure 7, the out-band rejection performance of the filter circuit 610 with the inductance associated with the ground terminal 240 (710) is considerably worse than that of the out-band rejection without ground terminal inductance (720). The former frequency response plot is for the filter depicted in Figure 6A, while the latter frequency response plot is for the filter depicted in Figure 6B. Any SMD, regardless of the type of circuitry embodied in the SMD, may utilize aspects of the present invention to minimize lead inductance.

An SMD according to aspects of the present invention may be constructed in any manner using any appropriate materials, and may include any desired features. For example, referring to Figure 8, an SMD according to the present invention may comprise a wafer substrate 120, a first metal layer 810, a dielectric layer 820, an insulation layer 830, and a second metal layer 840. The wafer substrate 120 may comprise any material or materials suitable for use in constructing an SMD, such as silicon, alumina, or any other appropriate material. The first and second metal

layers 810, 840 may comprise any desired conductive materials, such as copper, gold, aluminum, and/or the like. The dielectric layer 820 may comprise any suitable dielectric material, such as silicon dioxide, silicon nitride, and/or the like. The insulation layer 830 may comprise any desired insulating material, such as polyimide.

5 An SMD according to aspects of the present invention may be constructed in any manner. An exemplary process for constructing an SMD according to the present invention is depicted in Figures 9A and 9B. In this exemplary process, a first metal layer 810 may be deposited on an alumina substrate 120 (910). The first metal layer 810 is patterned and etched (920), and a dielectric layer 820 added (930). The dielectric layer 820 is patterned and etched (940), and an
10 insulation layer 830 is added (950). The insulator layer 830 is patterned, etched, and cured (960) and a second metal layer 840 is added (970). The second metal layer 840 is patterned and etched (980). The exemplary process depicted in Figures 9A and 9B may be employed to fabricate an SMD comprising a capacitor 982, an inductor 984, and two grounding points 986. More generally, the above-depicted process may be employed to fabricate any circuit that is embodied
15 in an SMD, including the previously-shown and described conductive surfaces to connect the circuit to a mounting surface.

Referring to Figure 10, an SMD according to the present invention may include a passivation layer 1010 protecting a circuit 550 supported by a substrate 120. The passivation layer 1010 may comprise any composition, such as Si_3N_4 , Al_2O_3 , and/or any other suitable
20 material. In one exemplary embodiment, the passivation layer 1010 is a solder mask to prevent solder from spreading onto the circuit. The passivation layer 1010 may be used to achieve any other suitable purpose.

The passivation layer 1010 may be added to an SMD as part of the manufacturing process for the SMD. For example, referring again to Figure 10, the passivation layer 1010 may
25 be added to an SMD and patterned and etched (1020). The wafer substrate 120 may be thinned to any appropriate thickness and then diced (1030). Sidewall terminations 1050 may be added onto the SMD (1040) at any time desired. The sidewall terminations 1050 depicted in the last of the three cross-sectional views in Figure 10 are analogous to those shown in Figures 5b and 5C. The processes described in Figures 9A, 9B and 10 are exemplary only. Elements of an SMD
30 according to the present invention may be constructed in any other suitable manner.

An SMD according to the present invention may be mounted on any desired mounting surface 510. For example, in one embodiment of the present invention the SMD connects to a printed circuit board, however, the mounting surface 510 may comprise any mounting surface, such as a substrate. The mounting surface 510 may be of any dimension and may be constructed

using any method of manufacture. The mounting surface 510 may operate as part of a larger system and/or in conjunction with any number of other systems and devices. Any number of SMDs in accordance with the present invention may be utilized in conjunction with a mounting surface 510.

- 5 Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

WHAT IS CLAIMED IS:

1. A device, comprising:
a surface mount device having a top side, a bottom side, a plurality of sidewalls, and a circuit comprising one or more layers;
5 a first conductive surface covering a portion of one of the sidewalls, the first conductive surface for providing an input to the circuit;
a second conductive surface covering a portion of one of the sidewalls, the second conductive surface for providing an output from the circuit; and
a third conductive surface covering a portion of one of the sidewalls, the third conductive
10 surface for providing an electrical ground to the circuit, wherein when the surface mount device is mounted to a provided mounting surface, at least one layer of the circuit is orthogonal to the provided mounting surface.
2. The device of claim 1, wherein at least two of the first conductive surface, the second conductive surface, and the third conductive surface cover respective portions of the
15 same sidewall.
3. The device of claim 1, wherein each of the first conductive surface, the second conductive surface and the third conductive surface covers a portion of a different one of the plurality of sidewalls.
4. The device of claim 1, wherein the third conductive surface is for bonding to the
20 provided mounting surface.
5. The device of claim 1, wherein a majority of the third conductive surface is for bonding to the provided mounting surface.
6. The device of claim 5, wherein a portion of at least one of the first conductive surface and the second conductive surface is coplanar with the majority of the third conductive
25 surface for bonding to the provided mounting surface.
7. The device of claim 1, wherein one of the sidewalls of the surface mount device is for bonding to the provided mounting surface.
8. The device of claim 1, wherein the circuit comprises an integrated passive device.
9. The device of claim 1, wherein the circuit comprises an integrated active device.
- 30 10. The device of claim 1, wherein the circuit comprises a filter.
11. The device of claim 1, further comprising a passivation layer covering at least a portion of the circuit.
12. A method for manufacturing a device, comprising:

providing a surface mount device, wherein the surface mount device comprises a top side, a bottom side, a plurality of sidewalls, and a circuit comprising one or more layers;

covering a portion of one of the sidewalls with a first conductive surface, the first conductive surface for providing an input to the circuit;

5 covering a portion of one of the sidewalls with a second conductive surface, the second conductive surface for providing an output from the circuit; and

covering a portion of one of the sidewalls with a third conductive surface, the third conductive surface for providing an electrical ground to the circuit, wherein when the surface mount device is mounted to a provided mounting surface, at least one layer of the circuit is
10 orthogonal to the provided mounting surface.

13. The method of claim 12, wherein at least two of the first conductive surface, second conductive surface, and the third conductive surface cover respective portions of the same sidewall.

14. The method of claim 12, wherein each of the first conductive surface, the second
15 conductive surface and the third conductive surface covers a portion of a different one of the plurality of sidewalls.

15. The method of claim 12, wherein the third conductive surface is for bonding to the provided mounting surface.

16. The method of claim 15, wherein a majority of the third conductive surface is for
20 bonding to the provided mounting surface.

17. The method of claim 16, wherein a portion of at least one of the first conductive surface and the second conductive surface is coplanar with the majority of the third conductive surface for bonding to the provided mounting surface.

18. The method of claim 12, wherein one of the sidewalls of the surface mount device
25 is for bonding to the provided mounting surface.

19. The method of claim 12, wherein the circuit comprises an integrated passive device.

20. The method of claim 12, wherein the circuit comprises an integrated active device.

30 21. The method of claim 12, wherein the circuit comprises a filter.

22. The method of claim 12, further comprising covering at least a portion of the circuit with a passivation layer.

23. A system, comprising:

an apparatus including a mounting surface; and

a surface mount device mounted to the mounting surface, the surface mount device comprising:

a top side, a bottom side, a plurality of sidewalls, and a circuit comprising one or more layers;

5 a first conductive surface covering a portion of one of the sidewalls, the first conductive surface for providing an input to the circuit;

a second conductive surface covering a portion of one of the sidewalls, the second conductive surface for providing an output from the circuit; and

10 a third conductive surface covering a portion of one of the sidewalls, the third conductive surface for providing an electrical ground to the circuit, wherein when the surface mount device is mounted to the mounting surface, at least one layer of the circuit is orthogonal to the mounting surface.

24. The system of claim 23, wherein at least two of the first conductive surface, the second conductive surface, and the third conductive surface cover respective portions of the
15 same sidewall.

25. The system of claim 23, wherein each of the first conductive surface, the second conductive surface and the third conductive surface covers a portion of a different one of the plurality of sidewalls.

26. The system of claim 23, wherein the third conductive surface is for bonding to the
20 provided mounting surface.

27. The system of claim 26, wherein a majority of the third conductive surface is for bonding to the provided mounting surface.

28. The system of claim 27, wherein a portion of at least one of the first conductive surface and the second conductive surface is coplanar with the majority of the third conductive
25 surface for bonding to the provided mounting surface.

29. The system of claim 23, wherein one of the sidewalls of the surface mount device is for bonding to the provided mounting surface.

30. The system of claim 23, wherein the circuit comprises an integrated passive device.

30 31. The system of claim 23, wherein the circuit comprises an integrated active device.

32. The system of claim 23, wherein the circuit comprises a filter.

33. The system of claim 23, further comprising a passivation layer covering at least a portion of the circuit.

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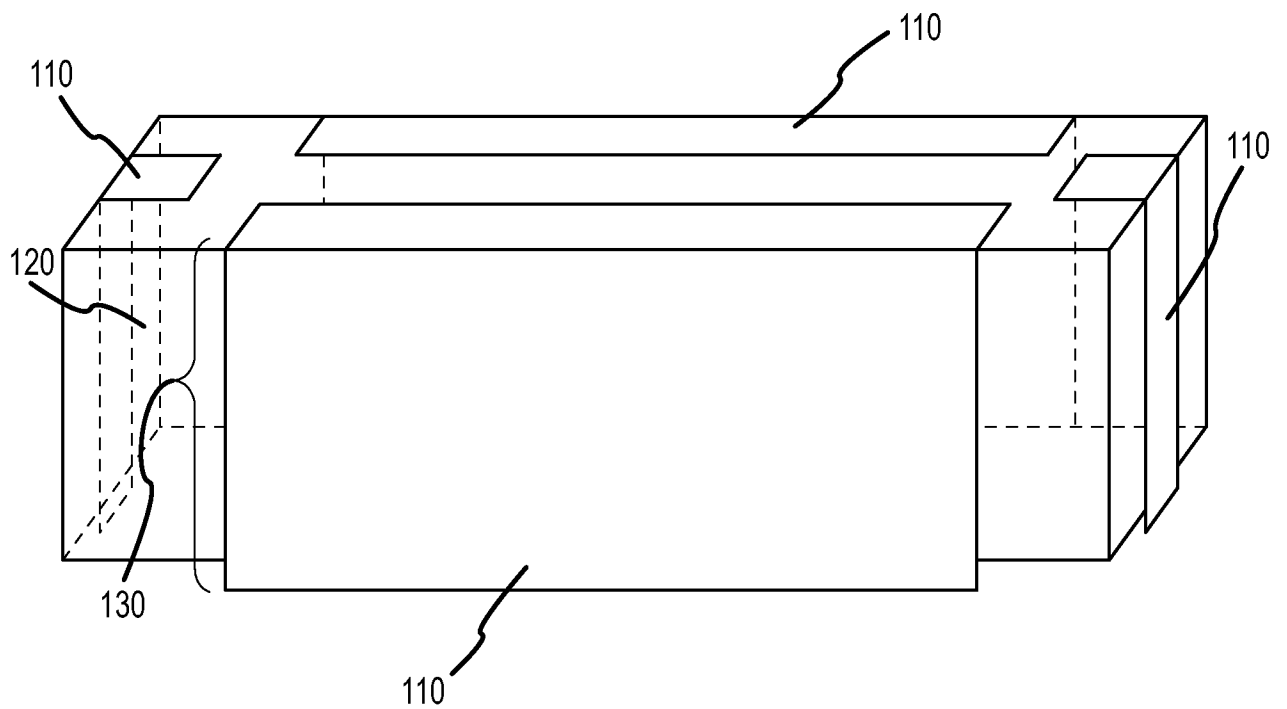


FIG.1

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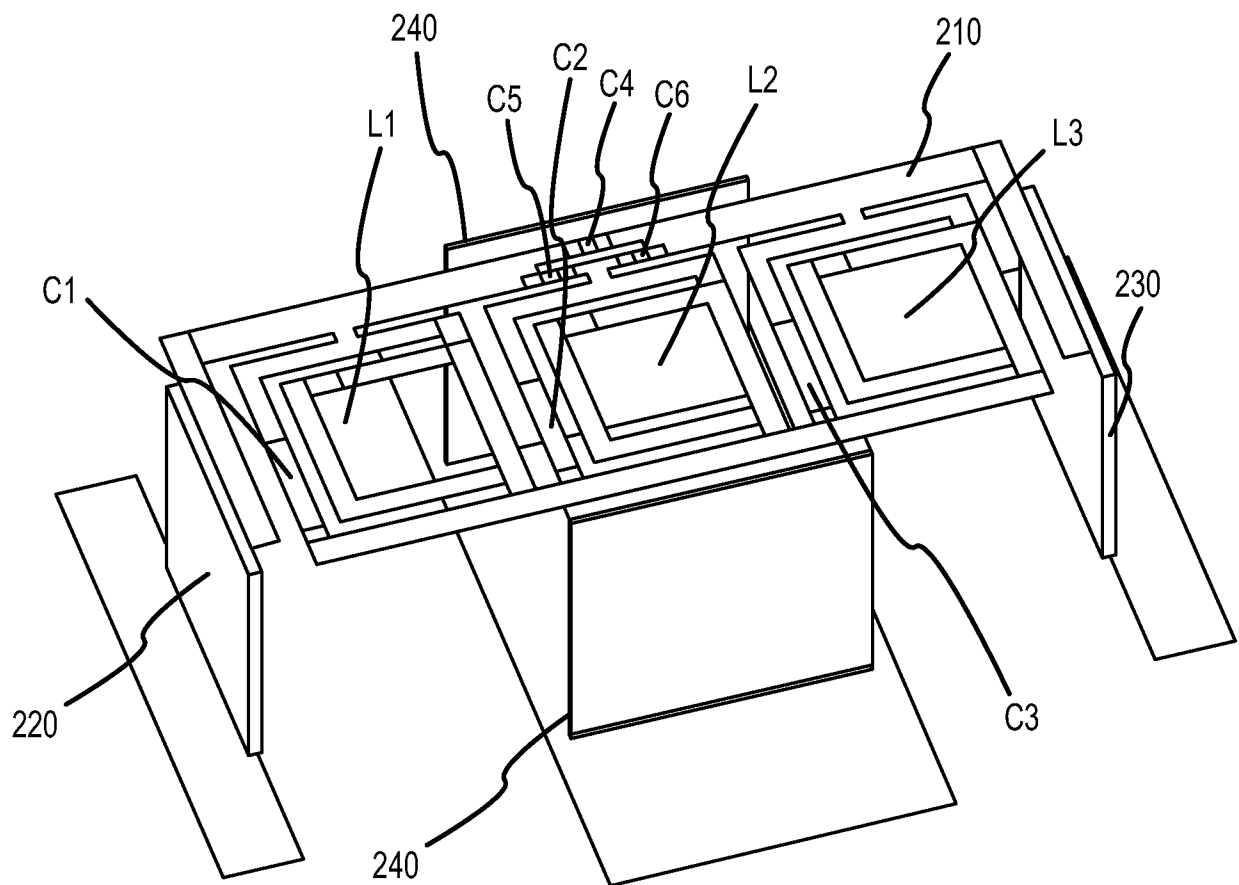


FIG.2

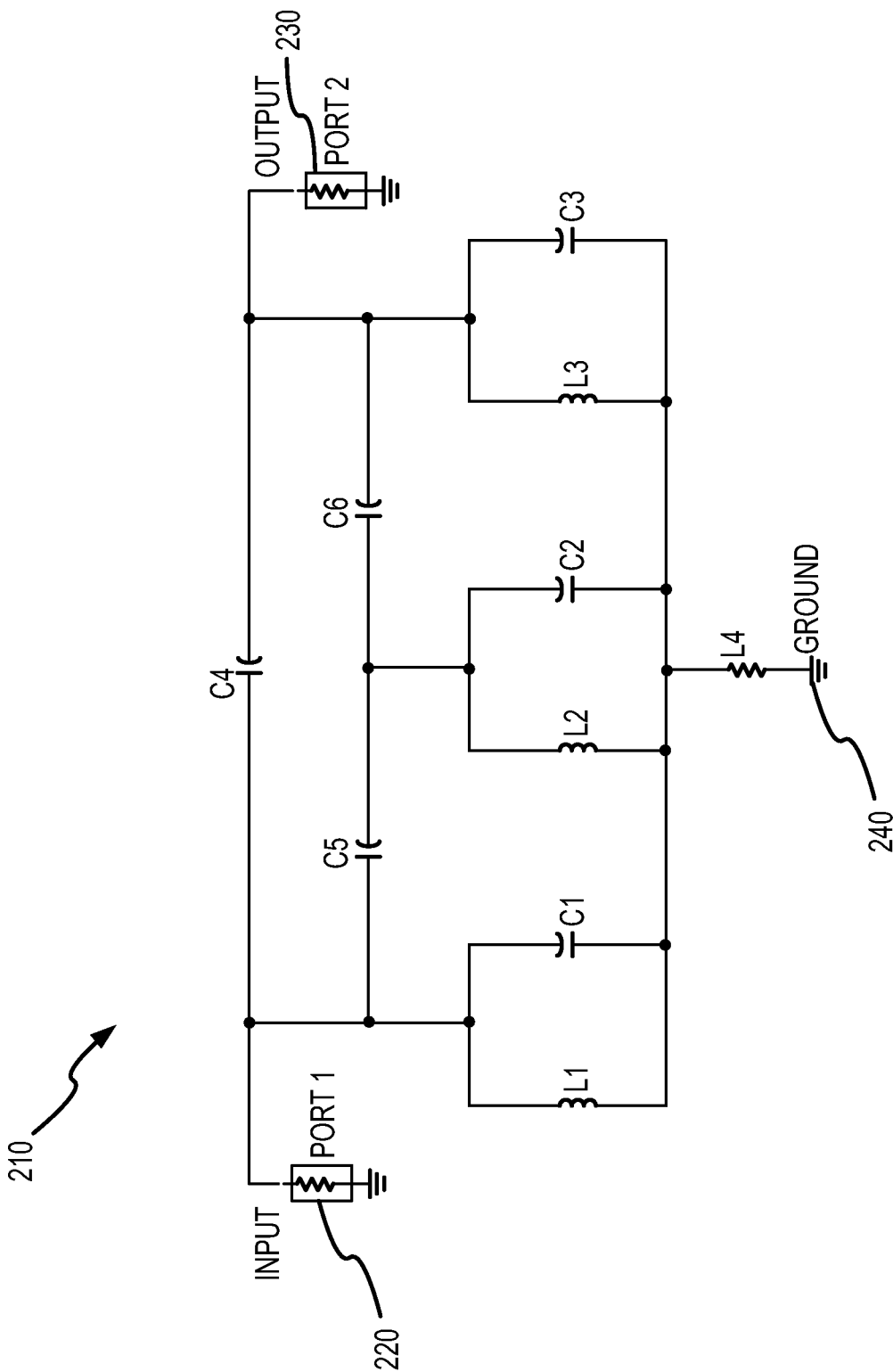


FIG.3

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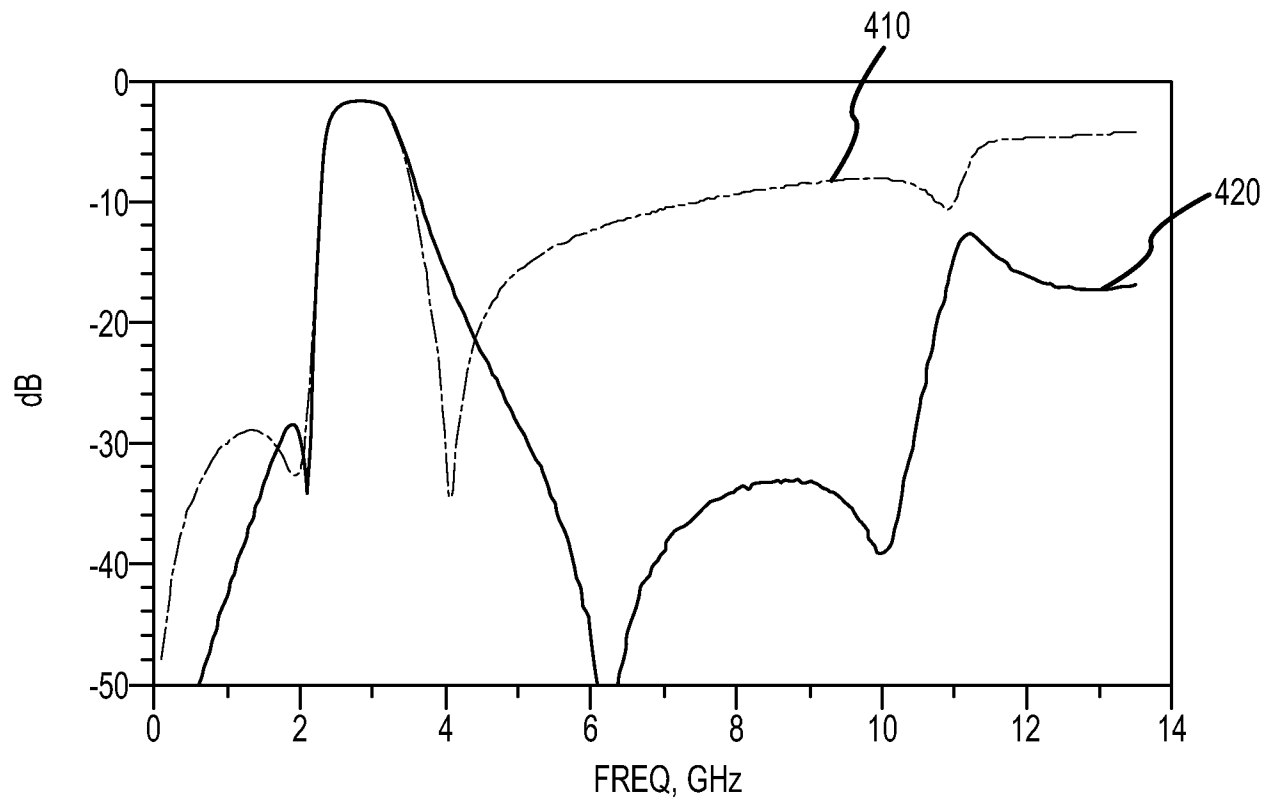


FIG.4

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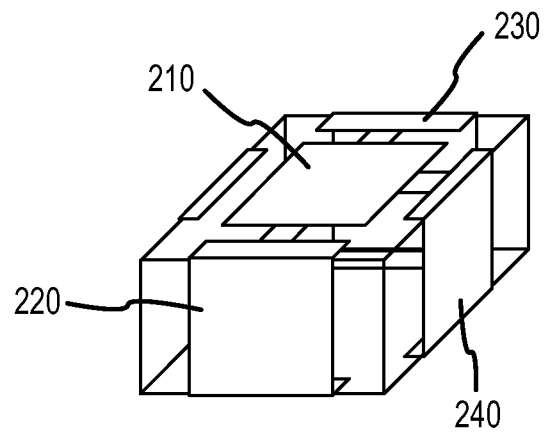


FIG. 5A

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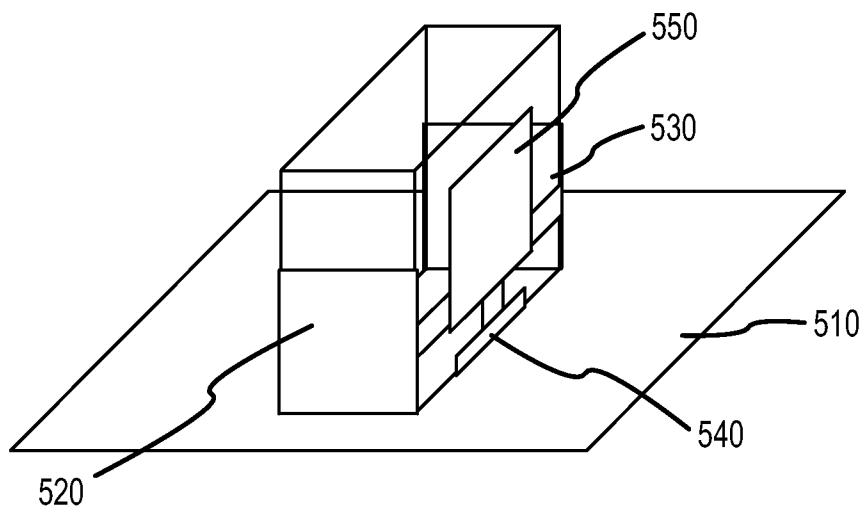


FIG.5B

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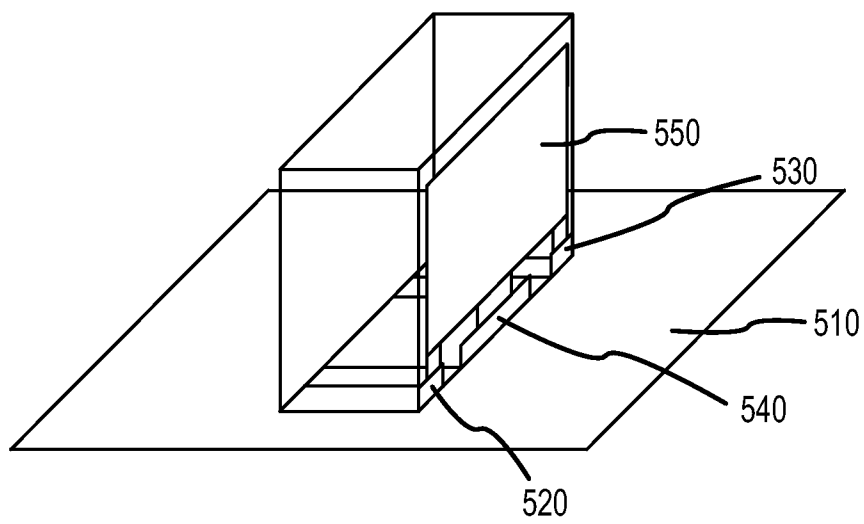


FIG. 5C

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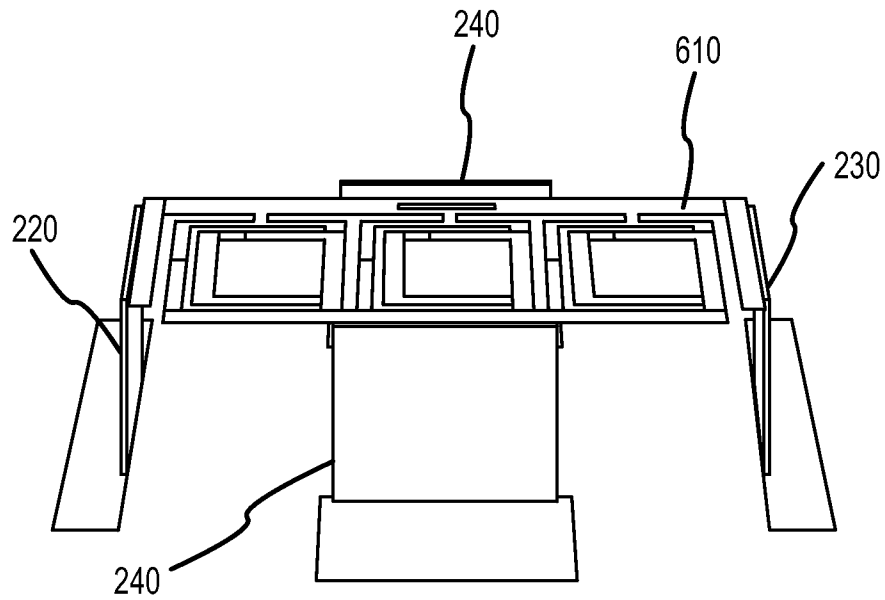


FIG. 6A

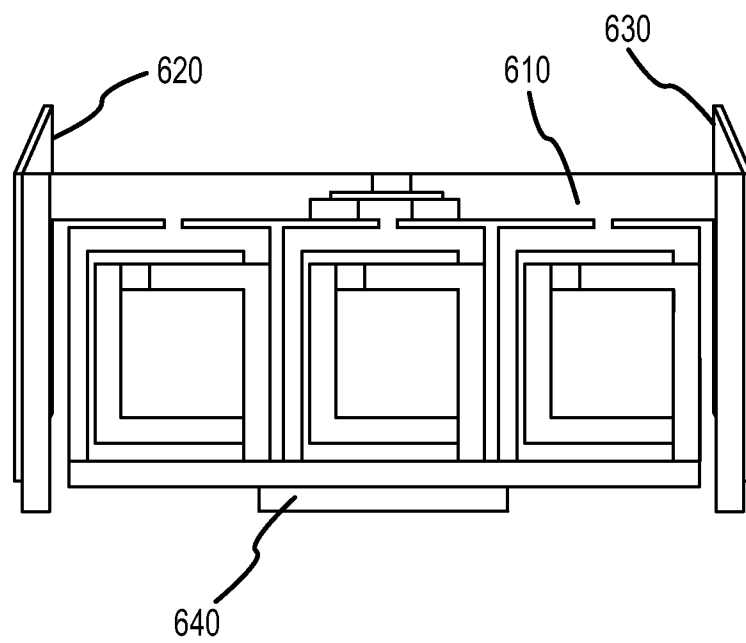


FIG. 6B

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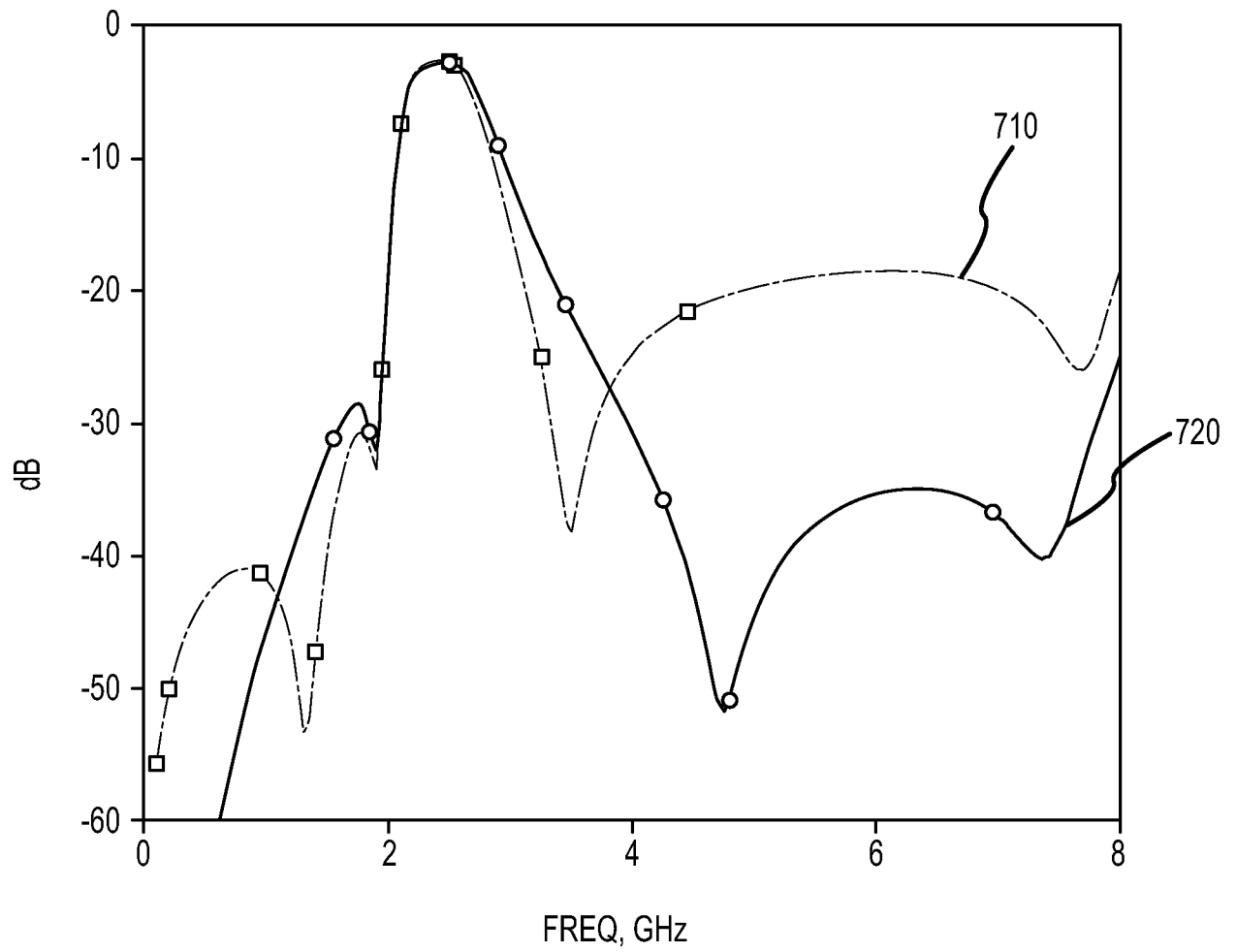


FIG.7

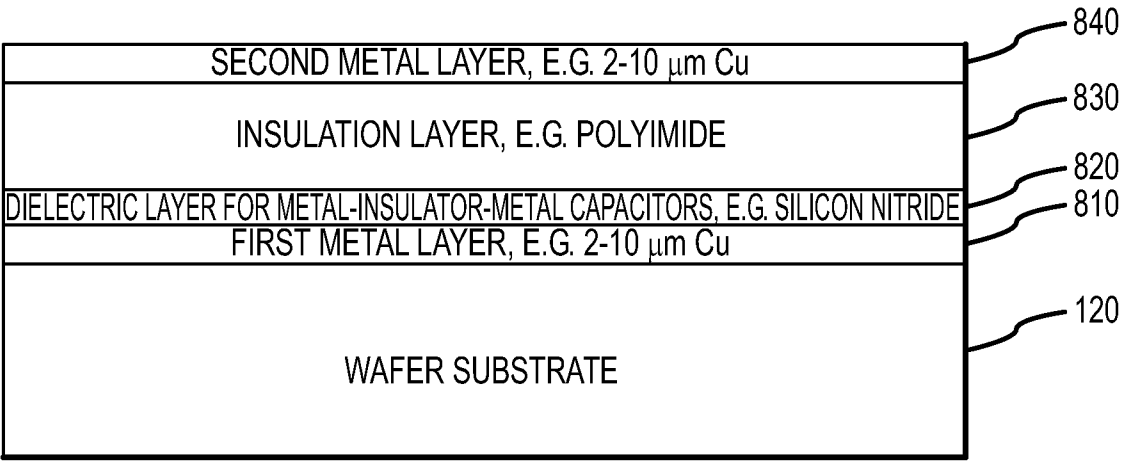


FIG.8

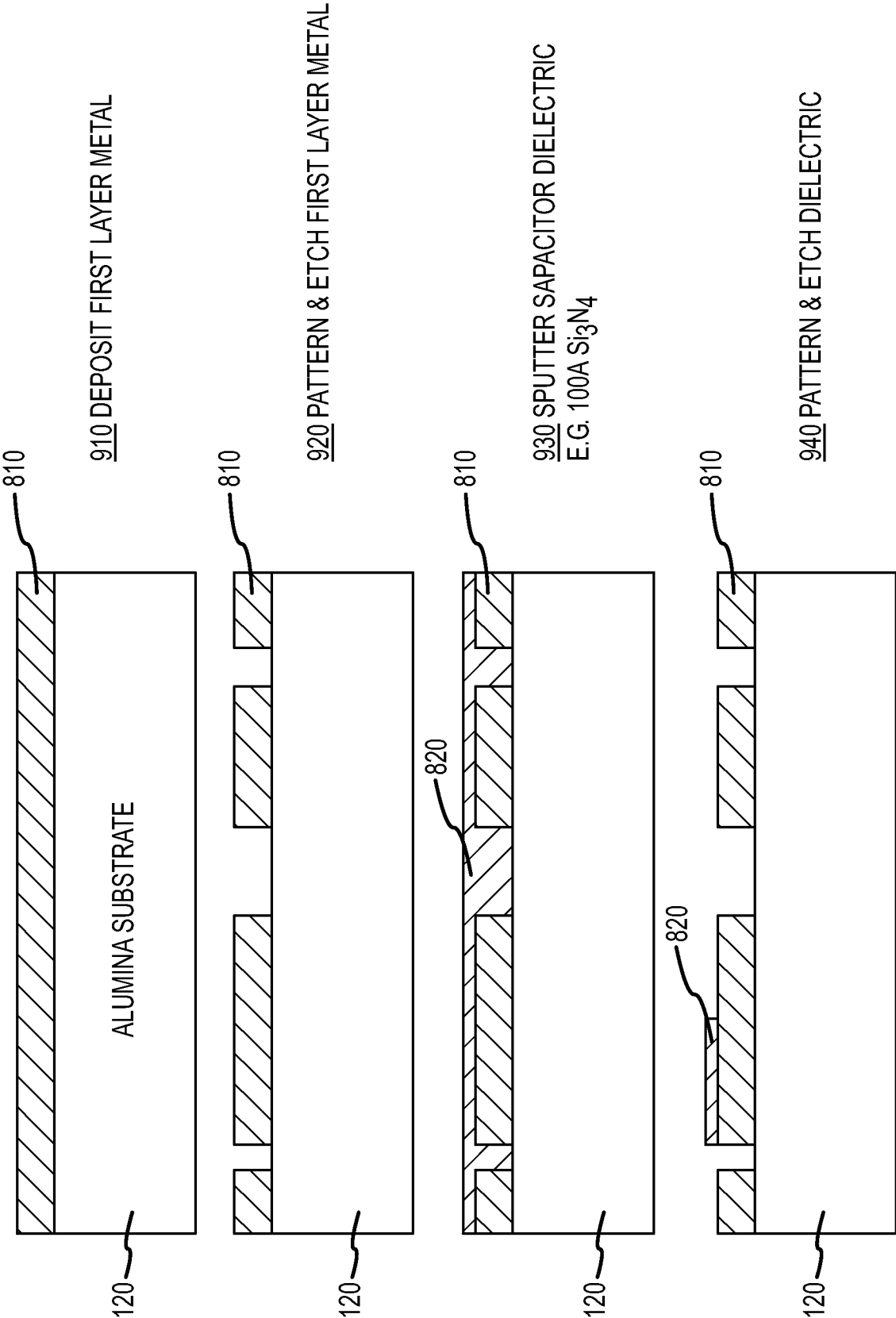
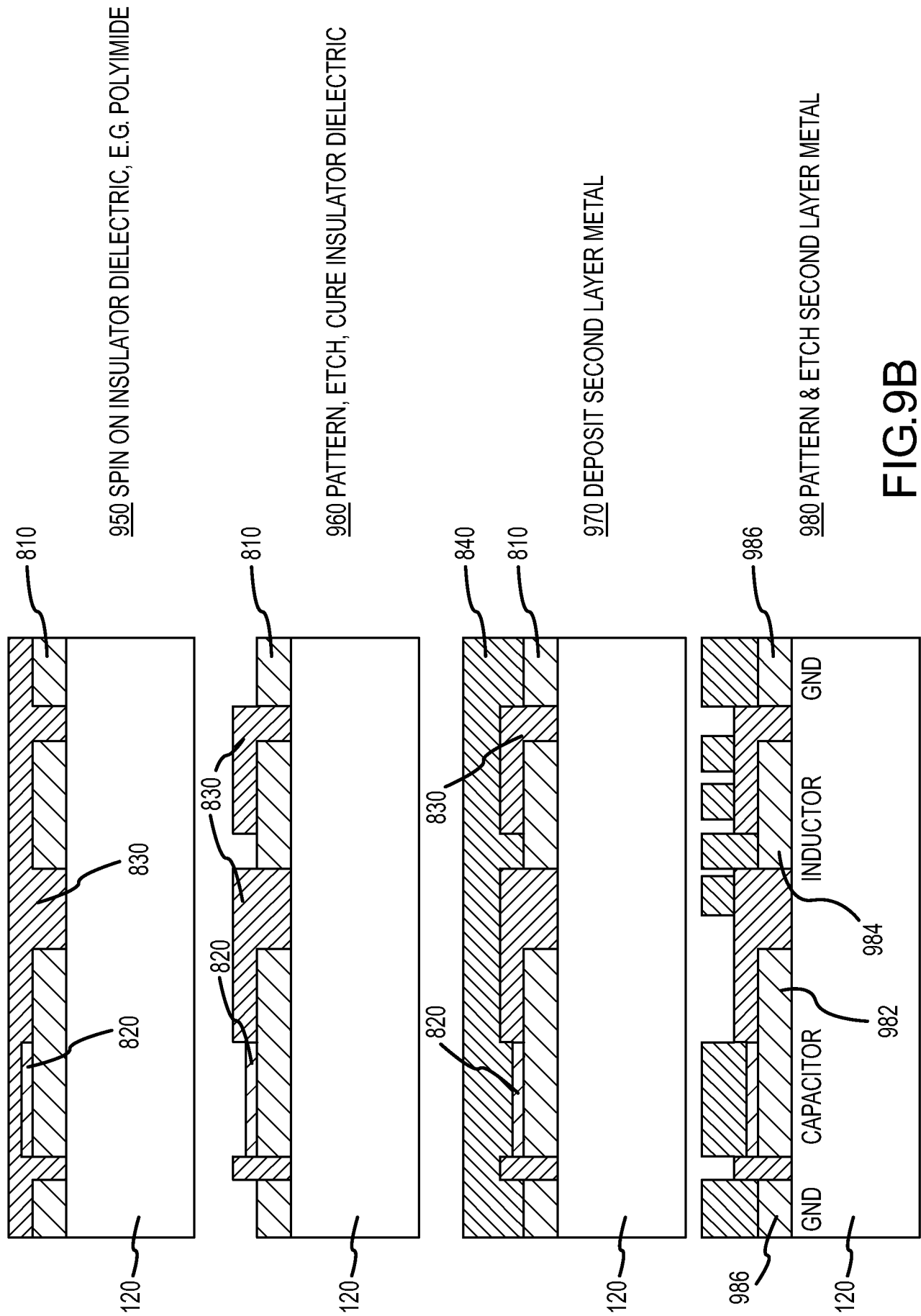


FIG.9A



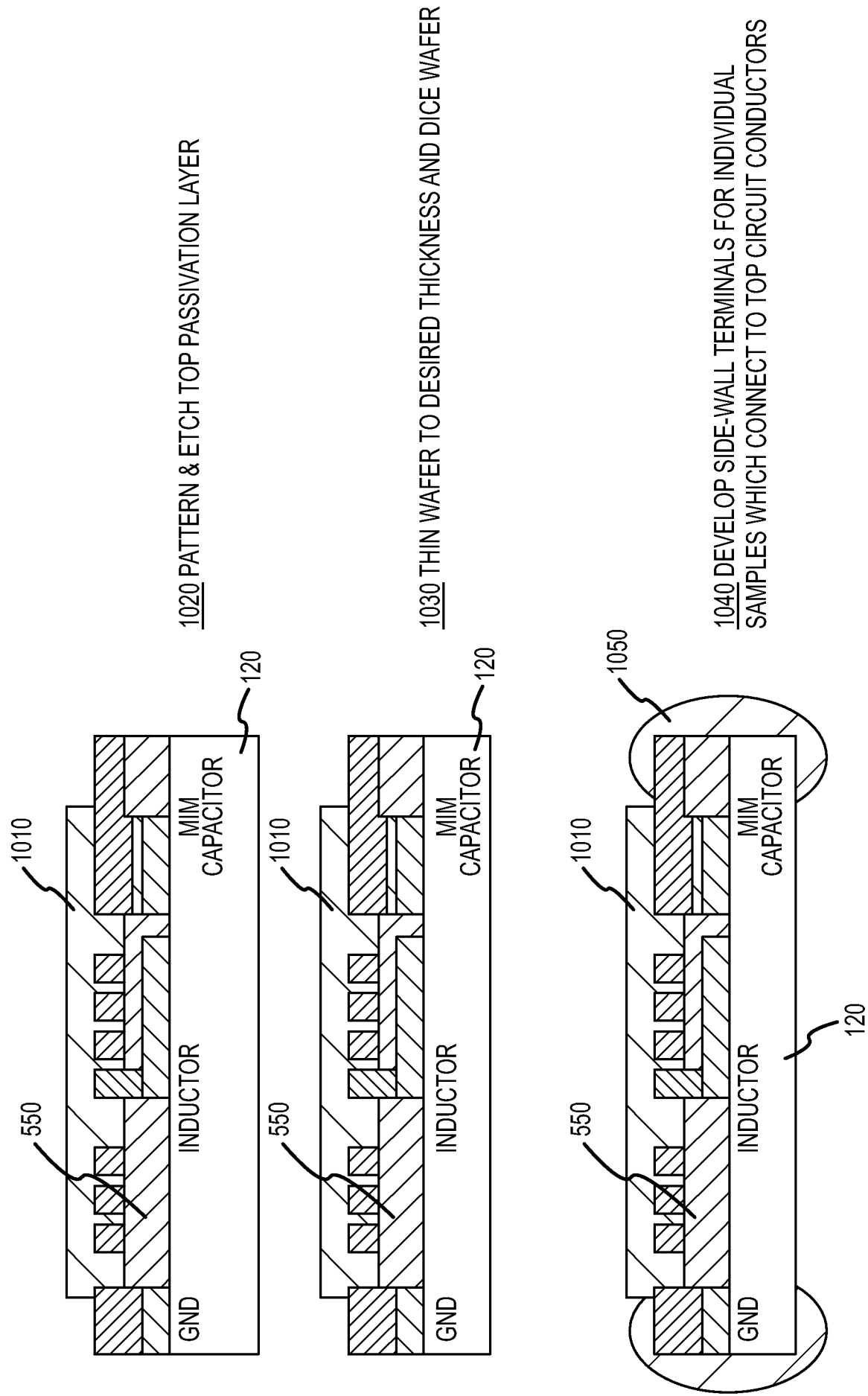


FIG.10

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/057382

A. CLASSIFICATION OF SUBJECT MATTER
INV. H05K1/18 H01L27/01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05K H03H H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 985 414 A (FUKUDA YOSHIHIRO [JP] ET AL) 16 November 1999 (1999-11-16) column 3, line 57 - column 4, line 50; figures 5-8	1-7, 10-18, 21-29, 32, 33
A	US 5 173 670 A (NAITO YASUYUKI [JP] ET AL) 22 December 1992 (1992-12-22)	
A	US 5 519 366 A (KANEKO TOSHIMI [JP] ET AL) 21 May 1996 (1996-05-21)	
A	US 6 444 920 B1 (KLEE MAREIKE K [DE] ET AL) 3 September 2002 (2002-09-03)	
A	US 2002/011596 A1 (YOSHISATO AKIYUKI [JP] ET AL) 31 January 2002 (2002-01-31)	

☐

Further documents are listed in the continuation of Box C.

☒

See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

20 August 2008

Date of mailing of the international search report

27/08/2008

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/057382

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