SPEECH PROCESSOR FOR CHANGING VOICE PITCH

21 Claims, 4 Drawing Fgs.

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Field of Search 179/100.2 T

References Cited

UNITED STATES PATENTS

2,352,023 6/1944 Schuller 179/100.2 R
2,886,650 5/1959 Fairbanks et al. 179/100.2 T
2,903,521 9/1959 Ellison 179/100.2 T
2,909,616 10/1959 Marty 179/100.2 T

ABSTRACT: By utilizing the speech processor of the invention, the speech of a diver in a helium-oxygen atmosphere is made intelligible, or a normal recording played at higher speeds is made intelligible thereby providing a speed hearing capability, or a voice signal is compressed for transmission over low bandwidth communication lines. The invention makes use of the fact that normal speech may be chopped or segmented at certain rates and still retain its intelligibility. The basic principle of the invention is accomplished in either an electronic or electromechanical embodiment wherein the following steps are performed. The speech to be processed is segmented into very small and, in some applications, equal pieces. Every other piece is discarded and the remaining pieces are recombined. The recombined pieces are played back at a slower speed dependent on the length of the discarded pieces.
FIG. 1.

FIG. 2.
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SPEECH PROCESSOR FOR CHANGING VOICE PITCH

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to speech-processing techniques and is more particularly concerned with apparatus for reproducing the speech of a diver in a helium-oxygen atmosphere in intelligible form, restoring to normal sounding a normal recording played at a higher speed and providing compression of a voice signal for transmission over a low-grade transmission line.

2. Description of the Prior Art

In the prior art there are a number of techniques commonly employed for speech processing in the areas of improving the intelligibility of speech in helium-oxygen atmospheres, in speed hearing especially for the blind and in data compression for transmission over low bandwidth communication lines.

In the field of speech processing, prior art devices have generally included speech processing apparatus which progressively speed up the pitch of the speech signal as the speed of the signal is increased. In the prior art devices mentioned above, the signal is speeded up by a compression process, and the modulation signal is speeded up by a compression process. The two speeded signals are then mixed and the reconstructed speech is reproduced.

One prior art method of accomplishing this speed hearing is known as a harmonic compressor. In the harmonic compressor, speech is fed to a band of 36 band-pass filters which separately the speech into its different frequency components. The output of the bank of filters is sent, in turn, to 36 frequency dividers which halve the frequencies of the narrow-band signals from the filters. The output of the dividers, the halved frequency signals go to networks which remove distortion and combine the halved signals into one signal. The frequency components of this signal are then half of the original input values. This halved frequency signal is then compressed on magnetic tape. The halved frequencies are then restored to their original values by doubling the playback speed. This prior art device does not operate in real time, i.e., the speech must first be recorded and played back later and is so voluminous that it takes up the space of a 6-foot high cabinet.

In a third application, the voice signal is compressed for transmission over low bandwidth communication lines. The prior art devices mentioned above might be adapted to provide for this application.

2. SUMMARY AND OBJECTS OF THE INVENTION

Accordingly, a primary object of the invention is to provide an improved speech processor.

Another object of the invention is to provide a speech processor which utilizes a relatively small amount and simple arrangement of components and which utilizes a small amount of power and which can operate in real time.

Still another object of the invention is to provide a speech processor which segments the speech into small pieces, discards every other piece, and recombines the remaining pieces.

Yet another object of the invention is to provide an electronic embodiment comprising two tone registers into which voice signals, having been digitized, are loaded, and the means for switching back and forth between these registers after each loading cycle so that there is no pause in the output signal as one register is loaded.

A further object of the invention is to provide an electromechanical embodiment wherein a magnetic tape loop is moved past a recording head into which the voice signal is applied, which tape loop is played by several playback heads moving in the same direction as the tape, but slower.

The invention accordingly comprises the features of construction, combination of elements and arrangement of parts which will be exemplified in the construction hereinafter set forth and the scope of the invention will be indicated in the claims.

The basis for the apparatus of the invention is based on the fact that normal speech can be chopped or interrupted at certain rates and still retain its intelligibility. This factor is supported in an article of The Journal of the Acoustical Society of America, Volume 22, No. 2, pages 167 to 173, dated Mar. 1950, and entitled, "The Intelligibility of Interrupted Speech." Both the electronic and electromechanical embodiments of the invention take full advantage of this factor.

Briefly, an electronic embodiment of the apparatus of the invention digitizes the voice signal. This voice signal might be that of a diver in a helium-oxygen atmosphere, or might be a recording of normal voice played back at higher speed or might be simply a voice signal being transmitted over a communications line. By all electronic means, the digitized voice signal is shifted into a first shift register at a first frequency. When this first register is fully loaded this condition is detected thereupon shifting the digitized voice signal out of the first register at a second frequency. This second frequency is lower that the first frequency. Simultaneously with shifting out of the digitized voice signal from the first register, subsequent and now digitized voice signals are shifted into the second register at the first frequency. When the second register is fully loaded, this condition is detected and thereupon a digitized voice signal is shifted out of the second register at the second frequency. This cycling as described above continues in an alternate manner until the input voice signal is fully processed. This fully processed digital signal is continually restored to an analog signal, which may then be relayed through a speaker.

In an electromechanical embodiment, a magnetic tape loop is moved past a recording head into which the input voice signal is applied. The tape is played back by several playback heads moving in the same direction as the tape, but slower. These playback heads are equally spaced on the circumference of a rotating wheel with each head sequentially making contact with the tape. The tape between the heads during changeover does not get played, thus segmenting the input signal with ever other segment, i.e., the tape not played, being discarded.

The aforesaid prior art apparatus are disadvantaged in that they either require an excessive amount of electronics, a multiplicity of special purpose and accurate components, especially filters, a very large and expensive configuration with an excessive power requirement, or they do not operate in real time. Because of these deficiencies in the prior art apparatus, the application set forth are not fully realized, for example, a person would be limited to access of a speed hearing device.
The loss of information from the discarded segments in the embodiments mentioned hereinabove is negligible when the chopping rate, i.e., the segment length is optimized for the characteristics of human speech and hearing. The segments ideally should be long compared with voice pitch waveform periods of 5 to 10 milliseconds and short compared with voice syllabic periods of 100 to 200 milliseconds. For example, a segment period of 20 milliseconds has been used.

Thus, the apparatus of the invention segments the incoming voice signal, discards alternate segments and reads out the segments signal at a lower rate, thereby keeping the same time base as the input signal. It should be noted that with the first frequency being double that of the second frequency the pitch of the incoming voice signal will be reduced by one-half and that although 50 percent of the input signal has been lost at this point the articulation will still be satisfactory.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of the preferred embodiments of the invention as illustrated in the accompanying drawings in which:

FIG. 1 illustrates a block diagram of an electronic embodiment of the speech processor of the invention;

FIG. 2 illustrates the timing waveforms at signal points indicated in the block diagram illustrated in FIG. 1;

FIG. 3 illustrates a block diagram of an electromechanical embodiment of the speech processor of the invention; and

FIG. 4 illustrates a modification of the processor shown in FIG. 3.

**DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Now referring to FIG. 1 there is illustrated a block diagram of an all electronic embodiment of the apparatus for processing the aforementioned signals. An electromechanical embodiment will be discussed later. The signal which is analog in nature is coupled to the input of an analog to digital (A/D) converter 10 which converter digitizes the input signal. The converter 10 might be a simple clipper or limiter thereby producing a chopped signal at the output of converter 10, or might be a delta modulator thereby producing a binary pulse pattern which is representative of the input signal. Converter 10 might also binary code the amplitude of the input signal which embodiment will be discussed hereinafter. The output of converter 10 is connected to the inputs of shift registers 16 and 18, which registers receive their respective clock pulses by way of switch 22 from either "A" clock 14 or "B" clock 12. Clock 14 operates at a higher frequency than clock 12, although both clocks are shown separately it should be understood that the pulse train out of clock 12 could have been derived from divider means connected to the output of clock 14.

Switch 20, as well as switch 24, might include a well-known combination of logic gates and/or flip-flops and switch 20 is initially set so that terminal a is connected to terminal c while terminal b is connected to terminal d. After switch 20 is initially toggled, a is connected to d and b is connected to c. Subsequent toggling alternately changes the connections cited above.

The toggle signal may be generated by a counter 22 which generates a pulse each time clock 14 produces that number of pulses as registers 16 and 18 have signal storage positions. The toggle signal might also be generated by a monostable multivibrator, not shown, whose time constant approximates the time for loading a register at the higher frequency of clock 14. Counter 22 also toggles switch 24 which is initially set so that terminal a is connected to terminal b. The output of shift register 16 is connected to terminal b of switch 24 while the output of shift register 18 is connected to terminal c.

The combination of switches 20 and 24 initially allows register 18 to clock in the digitized signal at the clock 14 frequency while register 16 has its signal stored therein clocked out of terminal a of switch 24 at the clock 12 frequency. Note that usually there is no signal stored in register 16 initially. When counter 22 generates a toggle signal the above condition will change so that now the signal just stored in register 18 will be clocked out of switch 24 at the clock 12 frequency while subsequent digitized signals will be clocked into register 16 at the clock 14 frequency. This process will continue in the alternate manner noted above.

Further, the signal at terminal a of switch 24 is processed by a digital to analog (D/A) converter 26 and then filtered by means of filter 28 thereby providing the output signal of the apparatus of the invention.

It can be seen then that the signal is always clocked into a register at the higher frequency of clock 14 and clocked out of the registers at the lower frequency of clock 12. It can also be seen that the processed signal is lower in frequency than the digitized signal out of converter 10 and that such processed signal has been chopped thus resulting in some loss of information of the input signal. It can also be seen that two registers are used so that there is no pause in the output as one register is loaded.

In operation and for ease of explanation reference should now be made to FIG. 1 in combination with the waveforms of FIG. 2. The waveforms are represented by the letters A to E. Waveform A is representative of the digitized signal output of A/D converter 10. Waveforms B and C are representative of the clock pulses produced by clocks 14 and 12 respectively. As illustrated, waveform B is twice the frequency of waveform C. Waveform D is the toggle signal from counter 22 which signal has been shown for illustration purposes as occurring every sixth pulse of clock 14. Waveform E is the processed signal occurring at the output of switch 24.

Shift registers 16 and 18 each have, in this example, six storage positions. Since counter 22 produces a toggle signal every six pulses of clock 14, it can be seen that each time a register loads up at the higher clock rate it is then switched to output the stored signals at the lower clock rate.

Let us now assume for initial condition that shift registers 16 and 18 are clear of any stored signals; that switch 20 is set so that terminals a and c are connected together and terminals b and d are so connected; and that switch 24 is set so that terminal a is connected to terminal b.

Let us also assume that the digitized input signal, whether it be a recorded voice replayed at higher speed, or a diver breathing in a helium-oxygen atmosphere, etc., is clipped and converted to pulses as indicated in waveform A. Note that this conversion to pulses is not necessary since the clipped waveform could have been directly sampled. At time 1, as illustrated FIG. 2, a pulse of higher frequency than clock 12 is indicated, while at time 2, no pulse or a binary zero is indicated, etc. Waveform A is clocked into shift register 18 at the rate shown by waveform B, and at the same time register 16 is receiving the clock pulses indicated by waveform C. Initially, however, no signals are clocked out of register 16 since no signals had been stored therein.

It should be understood that although no signal is being clocked out of shift register 16, signals from counter 10 as indicated by waveform A will be clocked into register 16 at the lower clock rate indicated by waveform C. It will be observed, however, that any such data clocked into either of the registers at the lower clock rate, i.e., the clock rate of clock 12, will not be used since switch 24 will be connected in such a manner as to discard such clocked in signals.

At time 6 therefore, register 18 will now have stored in it pulses indicated in waveform A as numbers 1 through 6. At this point in time counter 22 will emit a pulse as indicated by waveform D toggling the connections of switch 20 and of switch 24 such that now signals as indicated by waveform A beginning with the binary zero at time 7 will be clocked into register 16 at the waveform B rate. At the same time the signals now stored in register 18 will be clocked out of register 18 at the waveform C rate and through the connections of switch 24 into the D/A converter 26 and out via filter 28. The signal emitted from the a terminal of switch 24 is indicated by
waveform E. At time 7 a binary one pulse is shown which is identical to the signal as shown in waveform A at time 1. At time 9 a binary zero is emitted which binary zero is identical to the binary zero indicated at time 2 in waveform A. In a similar fashion the binary one indicated at time 11 in waveform E is identical to the binary one shown in waveform A at time 3. Because the output clock rate as shown by this example is one-half the frequency of the input clock rate, counter 22 is ready to emit its next toggle signal. Accordingly, the binary ones or zeros shown in waveform A at times 4, 5, and 6 will be discarded such that one-half of the input signal is no longer used. This condition is agreeable with the fact that the speech may be chopped at certain rates and still retain its intelligibility.

At time 12 when counter 22 emits its next toggle signal as indicated in waveform D, now stored in register 16 are the pulses of waveform A as indicated at times 7 through 12. Upon toggling, switch 24 will emit these signals as indicated at times 13, 15 and 17 in waveform E. Pulses 13, 15 and 17 of waveform E are identical to pulses 7, 8 and 9 respectively of waveform A. The signals of waveform A as indicated at times 10, 11 and 12 are not used. This operation continues alternatively until the last signal as indicated by waveform A at time 24 is processed. It can be seen that waveform E now contains the first three signals of every group of six signals originally received and indicated by waveform A. Accordingly, the signals indicated at times 25, 27 and 29 of waveform E are identical to the signals of waveform A at times 19, 20 and 21 respectively.

It should be understood that the length of registers 16 and 18 as well as the toggle frequency have been picked for purposes of explanation only and that much length and frequency may have been any number which would be determined by the application involved. The process as described above compresses the input signal by a factor of two and provides a sampling factor of 50 percent. These ratios may be varied from unity to any factor desired by changing the length of the discarded signals and the frequency of clock 12.

It should be additionally noted that as the frequency of clock 12 is lowered the pitch frequency is lowered. When the frequency of clock 12 is one-half the frequency of clock 14, the pitch has been reduced to one-half. Although 50 percent of the input information has been lost at this point the articulation will still be satisfactory as shown by the reference cited hereinbefore entitled, "The Intelligibility of Interrupted Speech." The length of the shift registers and the clocking rates are determined by the voice pitch period and audio bandwidth.

Higher frequency clocks can be used for improved frequency response of the audio output but the shift registers will also have to be lengthened. In actual practice shift registers 16 and 18 were built to each include 400 storage positions and counter 22 emitted a toggle signal every 400 clock pulses of clock 14. Clock 14 had a frequency of 20 kilohertz while clock 12 had a frequency of 10 kilohertz.

Thus, the processing technique of the invention may be utilized for improving the intelligibility of speech in a helium-oxygen atmosphere, i.e., in that circumstance where a diver is at considerable water depth and is breathing a helium-oxygen mixture. The voice of the diver for example at 200 feet is of high pitch and unintelligible. By chopping this voice and playing it back slower than it was spoken, the pitch of the voice becomes lower, i.e., the pitch is restored to normal, and the speech is now intelligible. In an application of speech hearing, especially for the blind person, a normal recording might for example be played at twice the normal speed. At this higher speed the voice on the recording would be unintelligible. By chopping this voice, the pitch would be lowered but is now intelligible, and the frequency of the voice recording would be doubled thus resulting in information being absorbed at a faster rate.

In a further application of this invention it would be possible to use this processor to reduce the bandwidth of voice before transmitting it over a communications channel. With a ratio of clock frequencies of 2 to 1, a 50 percent reduction in the radiofrequency bandwidth may be possible. Another similar device on the receiving end would be utilized to reconvert the voice to its original pitch. In this application it would not be necessary to use the converter 26 and filter 28, transmission could be in digital form. The receiving device would then incorporate a similar device as shown in the apparatus of the invention, however, the positions of clock 12 and clock 14 would be interchanged. That is to say the incoming processed digital signals from switch 24 of the transmitting device would be clocked into the receiving device at the lower frequency and clocked out at the higher frequency. This higher frequency output signal would then be converted into analog form and filtered thereby producing the received output signal. Further the receiving device would not require an A/D converter similar to converter 10 in FIG. 1.

As herebefore stated converter 10, illustrated in FIG. 1, might have produced a binary code of the amplitude of the input signal. For example, if the amplitude of the input signal is divided into 8 levels then the converter 10 would have at its output three binary lines corresponding to 20, 21 and 22 and thereby giving eight possible binary indications of the level of the input signal. To provide for these three binary lines at the output of converter 10, shift register 16 would now be replaced by three identical and parallel shift registers. These sets of registers would be coupled as shown in FIG. 1 and the operation would remain substantially identical to that previously discussed. The clock line from terminal C of switch 20 would clock the parallel registers replacing shift register 16 and the clock line from terminal D of switch 20 would clock the parallel registers replacing shift register 18. The D/A converter 26 would recombine the signals as switched by switch 24.

Now referring to FIG. 3, there is illustrated an electromechanical embodiment of the invention. The speech to be processed is applied to input terminal 74. Input terminal 74 is connected to record head 42. Between record head 42 and pressure pad 44 a magnetic tape loop 40 which is driven in a clockwise direction by capstan 56 and pincher roller 54. Capstan 56 is driven in a counterclockwise direction, as shown by the arrow, by a suitable motor, not shown. Tape loop 40 passes along the circumference of playback assembly 41 which assembly 41 is driven in a clockwise direction by another suitable motor, not shown.

Playback assembly 41 includes in this illustration two playback heads 62 and 64 and 72 and 74 apart along the circumference. The two playback heads are coupled to output terminal 72 by means of their slip rings 68 and brush 66. The output 76 of brush 66 is coupled to a playback amplifier 70, whose output is coupled to output terminal 72. The tape loop 40 is guided along the circumference of playback assembly 41 by means of roller bearings 60, which are utilized to reduce friction between the tape loop 40 and assembly 41.

After the tape loop 40 passes assembly 41 and capstan 56, it passes between erase head 46 and pressure pad 48. The loop 40 is held tight by means of rollers 50 and 52. Roller 52 has coupled to it a spring mechanism 58 for increased tension of the tape loop 40.

Playback assembly 41 might have included more than two playback heads spaced equally along the circumference. In any such arrangement as well as the two playback head arrangements shown, only one playback head is coupled to the output terminal 72 at a time. As illustrated, the tape behind playback head 64 to just in front of playback head 62 will not get played back thereby resulting in segmenting of the speech and discarding every other segment of the speech which is fed into record head 42. If only one playback head were used, the basic concept of the invention could still be achieved, however, the playback would not be continuous. It should be understood that the block diagram of FIG. 3, is a simple schematic representation of the invention and does not include all the mechanical and electrical details but is sufficient to describe the invention. These details may be accomplished in any convenient manner. 3,621,150
The operation of the embodiment of FIG. 3 is as follows. The closed magnetic tape loop 40 moves past the record head 42 at a fixed speed determined by the capstan 56. A short distance before the tape loop 40 passes the record head 42 it passes an erase head 46 where all previous signals are erased. The signal to be processed is applied to the record head 42 through the input terminal 74. The recorded tape then passes over a playback housing 41 in the shape of a wheel which housing includes two or more playback heads 62 and 64 equally spaced along the circumference of the wheel. The operation will be described with two heads but more than two may be desirable. For instance, the less the circumferential distance between heads the slower need be the speed of the tape and wheel for a given quality reproduction. Only one head at a time can be played back. This can be accomplished by limiting the length of arc that the tape makes contact with the wheel or by the brush and slip ring arrangement. Both methods are shown for the two head arrangement. It should be noted that for a given quality reproduction the erase head 46 should be employed, but that nevertheless the system would still operate satisfactorily without the erase head so long as the record head is energized.

With the housing 41 or (wheel) stationary, one head, will be in contact with the tape 49 (or if more than one, only one will be coupled with the electronics through its slip ring). The playback channel will play back exactly what was recorded but delayed by a fraction of a second. If the wheel is moved slowly in the same direction as the tape the relative speed of the tape across the playback head will become less than it was when the wheel was stationary. This lowers the pitch of the speech. After the head, which was making contact with the tape, rotates 180° it loses contact with the tape and the other head starts making contact. The tape between the two heads during head changeover does not get played, since it is in front of the head just going on the tape and in back of the head which has left the tape. The head never makes contact with any tape in front of it, since the tape is moving faster than the wheel.

The speed of the wheel is variable from 0 r.p.m. to an r.p.m. equal to the tape speed. With the speed 0 there is no pitch reduction; as the speed increases to one-half the speed of the tape, the pitch decreases by one-half. At this point the size of the tape segments played back become equal to the segments not played back. As the speed of the wheel is increased further the pitch is lowered further and smaller segments are played back relative to those not played. With a speed control for the wheel the pitch frequency will be adjustable.

After the tape loop 40 passes over the wheel, it passes by the capstan 56 which drives the tape at a constant speed. It then passes the erase head 46 and guide rollers 50 and 52 and returns to the record head.

A spring is shown on one of the guide rollers to hold the tape loop tight against the playback heads. It also simplifies the replacement of the tape loop. If additional pressure is needed to hold the tape in contact with the playback heads a semicircular shoe could press against the tape. Another suggestion for holding the tape tight against the heads is shown in FIG. 4.

In FIG. 4, playback housing 41 is illustrated with a flexible tape pressure means generally indicated at 92. Playback housing 41 now includes a cylinder 80 which has coated on its outer surface a friction-reducing substance such as that sold under the trademark “TEFLON.” This essentially frictionless cylinder 80 replaces the roller bearings 60 of FIG. 3. Tape loop 40 passes around and is pressed against cylinder 80 by means of flexible tape pressure means 92.

Pressure means 92 includes flexible pressure tape 90 which is held tightly against recording tape 40 as it passes over the wheel or cylinder 80. Pressure tape 90 is held in position by means of guide rollers 82 and 84 and is kept tight by means of roller 86 and spring tension means 88. The pressure tape 90 is free to move around the rollers 82, 84 and 86 thus reducing the drag on the recording tape 40 as it passes over the cylinder 80. If it is required to reduce the drag further, a capstan, not shown, could be used to drive the flexible pressure tape 90 at the same speed as the recording tape 40.

This embodiment of the invention might be utilized in a communication system in which case the receiving end would include apparatus as shown in FIG. 3. However, since the incoming speech is now lower in pitch than normal, the speed of revolution of the playback housing 41 would be greater than the speed of the tape loop 40.

It has thus been seen that the on electromechanical embodiment of the invention as illustrated in FIG. 3 segments, discards every other segment, and combines the remaining segments by means of a tape loop which is fed by the speech to be processed and which is driven at a constant speed past a playback housing which for best results includes at least two playback heads spaced substantially 180° apart, the playback housing rotating at some adjustable slower speed so as to reduce the tape loop to playback head speed.

Other methods of reducing the effective playback head to tape speed involve oscillating heads or dual capstan drives. It will thus be seen that the objects set forth above among those made apparent from the preceding description, are efficiently attained, and since certain changes may be made in the above construction without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

Having described the invention, what is claimed as new and secured by Letters Patent is:

1. Apparatus for processing speech signals, comprising:
   A. an input terminal for receiving said speech signals;
   B. an analog-to-digital converter coupled to said input terminal;
   C. first and second storage means coupled to said analog-to-digital converter;
   D. means for alternately reading said signals into said first and second storage means at a first rate;
   E. an output terminal;
   F. means for alternately reading out said first and second storage means at a second rate, said signals being read out at said second rate being coupled to said output terminal; and
   G. a digital-to-analog converter coupled to the output of said storage means.

2. Apparatus as defined in claim 1, wherein said speech signals are that of a diver speaking in a helium-oxygen atmosphere.

3. Apparatus as defined in claim 1 wherein said speech signals are that of a normal voice recording played back at a higher speed than the original recording speed.

4. Apparatus as defined in claim 1 wherein said first and second storage means comprises first and second shift registers.

5. Apparatus as defined in claim 4 wherein said readin and readout means includes:
   A. clock means for generating pulses at a first frequency and for generating pulses at a second frequency, said second frequency being lower in frequency than said first frequency; and
   B. first switch means for coupling said pulses of said first frequency to the clock input of said first shift register whereby signals are loaded into said first shift register at said first frequency and for simultaneously coupling said pulses of said second frequency to the clock input of said second shift register whereby signals are unloaded from said second shift register at said second frequency.

6. Apparatus as defined in claim 5 wherein said readin and readout means further includes:
   A. means for sensing the loading of a predetermined amount of signal into said first shift register;
   B. means connecting said sensing means to said first switch means for toggling said first switch means upon said sensing such that said pulses of said first frequency are coupled to the clock input of said second shift register.
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whereby signals are loaded into said second shift register at said first frequency and such that said pulses of said second frequency are coupled to the clock input of said first shift register whereby signals are unloaded from said first shift register at said second frequency; and

C. second shift register means for coupling the register being unloaded to said output terminal.

7. Apparatus as defined in claim 6 wherein said second shift register means is toggled by said sensing means.

8. Apparatus as defined in claim 6 wherein said second shift register means is variable.

9. Apparatus as defined in claim 6 wherein said analog-to-digital converter includes a clipping network.

10. Apparatus as defined in claim 6 wherein said analog-to-digital converter produces a binary pulse pattern of the speech signals on said output lines.

11. Apparatus as defined in claim 6, further including:
   a filter network coupled to receive a signal from said digital-to-analog converter.

12. Apparatus as defined in claim 6 wherein said analog-to-digital converter includes a delta modulator.

13. Apparatus as defined in claim 12 wherein said first and second shift registers are each comprised of n parallel connected shift registers, each of which n parallel shift registers is coupled to a corresponding line of said output lines.

14. Apparatus for processing speech signals, comprising:
   A. an input terminal for receiving said speech signals;
   B. means for converting said speech signals into digital signals;
   C. a pair of shift registers coupled to receive said digital signals;
   D. means for alternately clocking said digital signals into one of said shift registers at a first frequency;
   E. means for alternately clocking said digital signals out of the other of said shift registers at a second frequency which is lower than said first frequency; and
   F. means for converting said digital signals clocked out of said shift registers at said second frequency to analog form.

15. Signal-processing apparatus having a processor output terminal, said apparatus comprising:
   A. analog-to-digital conversion means;
   B. means for generating first clock pulses at a first frequency;
   C. means for generating second clock pulses at a second frequency, said second frequency being lower in frequency than said first frequency;
   D. first and second shift register means
      1. each having a signal input and output terminal,
      2. each coupled to said conversion means at said signal input terminal,
      3. each having m storage positions, and
      4. each having a clock input for shifting the signal into said signal input terminal through each of said m storage positions, and out of said signal output terminal;
   E. means for sensing the occurrence of m of said first clock pulses;
   F. means for alternately coupling said first clock pulses to said clock input of said first register means and then to said clock input of said second register means each time said sensing means senses the occurrence of m of said first clock pulses;
   G. means for alternately coupling said second clock pulses to said clock input of one of said register means which is not connected to said first clock pulses;
   H. means for coupling said signal output terminal of one of said register means which has its clock input coupled to said second clock pulses, to said processor output terminal, and
   I. digital-to-analog conversion means coupling said shift register means to said processor output terminal whereby the signal is loaded into said register means at a higher rate than the signal is unloaded from said register means and whereby the signal at said processor output terminal is proportional to the ratio of the frequencies of the second clock pulses over the first clock pulses times that amount of signal in the signal from the conversion means.

16. Apparatus as defined in claim 15 wherein said signal is that of a diver submerged in water whereby said signal is made intelligible.

17. Apparatus as defined in claim 15 wherein said signal is that of a normal voice recording played back at a higher speed thereby resulting in an intelligible, speed hearing playback.

18. Apparatus as defined in claim 15 wherein
   A. said analog-to-digital converter produces a binary pulse pattern of said signal on n output lines; and
   B. said first and second shift register means are each comprised of n parallel connected shift registers, each of which n parallel shift registers is coupled to a corresponding line of said n output lines.

19. Apparatus as defined in claim 18 wherein said means for converting a digital signal to an analog signal includes a filter network for further restoring said signal to analog form.

20. A method for processing voice signals comprising the steps of:
   A. converting said speech signals into digital signals;
   B. segmenting said digital signals;
   C. discarding every other segment of said segmented signals;
   D. combining the remaining segments of said segmented signals; and
   E. converting said digital signals to an analog signal.

21. A method for processing signals comprising the steps of:
   A. converting said signals into digital form;
   B. shifting said digital signals into a first register at a first frequency;
   C. detecting a cycle of said shifting whereby said first register is fully loaded;
   D. shifting, upon said detecting of said fully loaded first register, said digital signals out of said first register at a second frequency, said second frequency being lower than said first frequency, and simultaneously shifting said digital signals into a second register at said first frequency;
   E. detecting a cycle of said shifting whereby said second register is fully loaded;
   F. shifting, upon said detecting of said fully loaded second register, said digital signals out of said second register at said second frequency, and
   G. restoring said digital signals shifted out of said registers to analog signals.