



- (51) International Patent Classification:
H01L 21/768 (2006.01) *H01L 29/78* (2006.01)
H01L 21/762 (2006.01)
- (21) International Application Number:
PCT/US2016/032436
- (22) International Filing Date:
13 May 2016 (13.05.2016)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
62/162,640 15 May 2015 (15.05.2015) US
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- (81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,

[Continued on next page]

(54) Title: RADIO FREQUENCY ISOLATION USING SUBSTRATE OPENING

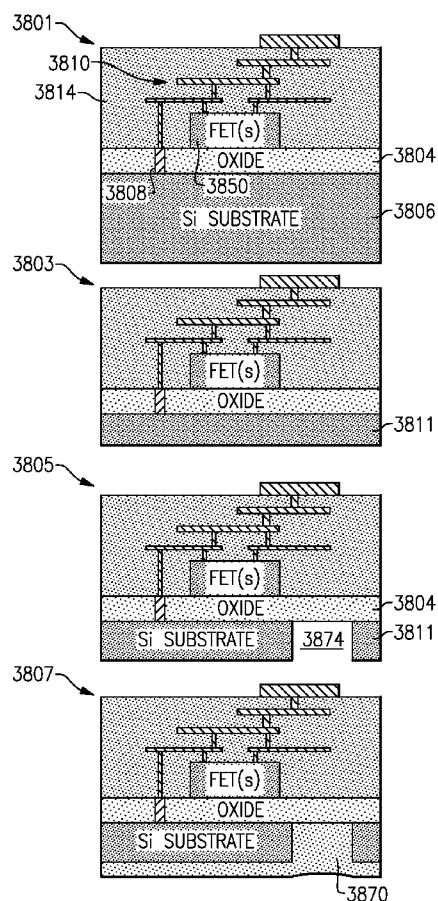


FIG. 69B

(57) Abstract: Radio-frequency (RF) devices are fabricated by providing a field-effect transistor (FET) formed over a an oxide layer formed on a substrate layer and removing at least a portion of the substrate layer to form an opening exposing at least a portion of a backside of the oxide layer, the opening being positioned to enhance RF performance for one or more components of the RF device.





DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,

DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

— *with international search report (Art. 21(3))*

RADIO FREQUENCY ISOLATION USING SUBSTRATE OPENING

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to U.S. Provisional Application No. 62/162,640, filed May 15, 2015, and entitled RADIO FREQUENCY ISOLATION USING SUBSTRATE OPENING, the disclosure of which is hereby incorporated by reference in its entirety.

BACKGROUND

Field

[0002] The present disclosure relates to field-effect transistor (FET) devices such as silicon-on-insulator (SOI) devices.

Description of the Related Art

[0003] In electronics applications, field-effect transistors (FETs) can be utilized as switches. Such switches can allow, for example, routing of radio-frequency (RF) signals in wireless devices.

SUMMARY

[0004] In accordance with a number of implementations, the present disclosure relates to a method for fabricating a radio-frequency (RF) device. The method comprises providing a field-effect transistor (FET) formed over an oxide layer formed on a substrate layer and removing at least a portion of the substrate layer to form an opening exposing at least a portion of a backside of the oxide layer, the opening being positioned to enhance RF performance for one or more components of the RF device.

[0005] In certain embodiments, the method further comprises thinning the substrate layer prior to removing the at least a portion of the substrate layer. The method may comprise covering at least a portion of the substrate layer and the opening with a covering to form a cavity. The covering may be a laminate film, a plastic lid structure, an additional replacement substrate layer, or the like.

[0006] In certain embodiments, the method comprises at least partially filling the opening with a dielectric filler. The method may further comprise covering at least a portion

of a backside of the substrate layer with the dielectric filler to form a dielectric layer. The method may further comprise applying a replacement substrate layer to the dielectric layer to provide mechanical stability for the RF device. In certain embodiments, the method comprises applying a handle wafer to the RF device to provide mechanical stability for the RF device.

[0007] In accordance with a number of implementations, the present disclosure relates to a radio-frequency (RF) device comprising a field-effect transistor (FET) implemented over an oxide layer, a patterned semiconductor substrate layer on which the oxide layer is formed, the substrate layer including a backside trench defined at least in part by side wall portions of the substrate layer, and one or more electrical connections connected to the FET.

[0008] In certain embodiments, the substrate layer is a thinned substrate layer. The RF device may further comprise a replacement substrate layer disposed on a backside of the substrate layer and covering the trench to form a cavity. The RF device may further comprise a dielectric filler material contained within the trench. In certain embodiments, the RF device further comprises a dielectric layer disposed on a backside of the substrate layer.

[0009] In accordance with a number of implementations, the present disclosure relates to a wireless device comprising a transceiver configured to process radio-frequency (RF) signals and an RF module in communication with the transceiver, the RF module including a switching device having a field-effect transistor (FET) implemented over an oxide layer and a patterned semiconductor substrate layer including an opening defined at least in part by a side wall of the substrate layer and a portion of a backside of the oxide layer, the switching device further including one or more electrical connections connected to the FET. The wireless device further comprises an antenna in communication with the RF module, the antenna configured to facilitate transmitting and/or receiving of the RF signals.

[0010] In certain embodiments, the substrate layer is a thinned substrate layer. The wireless device may further comprise a replacement substrate layer disposed on a backside of the substrate layer that covers the opening to form a cavity. The wireless

device may comprise a dielectric filler contained within the opening. A dielectric layer may be disposed on a backside of the substrate layer.

[0011] In accordance with a number of implementations, the present disclosure relates to a radio-frequency (RF) module comprising a packaging substrate configured to receive a plurality of devices and a switching device mounted on the packaging substrate, the switching device including a field-effect transistor (FET) implemented over an oxide layer and a patterned semiconductor substrate layer including an opening defined at least in part by a side wall of the substrate layer and a portion of a backside of the oxide layer, the switching device further including one or more electrical connections connected to the FET.

[0012] In certain embodiments, the substrate layer is a thinned substrate layer. The RF module may comprise a replacement substrate layer disposed on a backside of the substrate layer and covering the opening to form a cavity. In certain embodiments, the RF module comprises a dielectric filler contained within the opening. A dielectric layer may be disposed on a backside of the substrate layer.

[0013] In accordance with a number of implementations, the present disclosure relates to a method of fabricating a radio-frequency (RF) device. The method may comprise providing a field-effect transistor (FET) formed over an oxide layer, forming one or more electrical connections to the FET, forming one or more dielectric layers over at least a portion of the electrical connections, electrically coupling an electrical element to the FET via the one or more electrical connections, and disposing a handle wafer layer on at least a portion of the one or more dielectric layers, the handle wafer layer being at least partially over the electrical element. The method further comprises removing at least a portion of the handle wafer layer to form an opening exposing at least a portion of the electrical element.

[0014] In certain embodiments, the method comprises thinning the handle wafer layer prior to said removing the at least a portion of the handle wafer layer. The method may comprise covering at least a portion of the handle wafer layer and the opening with a covering to form a cavity. In certain embodiments, the covering may be a laminate film, a plastic lid structure, an additional replacement substrate layer, or other type of covering.

[0015] The method may comprise at least partially filling the opening with a dielectric material. The method may further comprise covering at least a portion of the

handle wafer layer with the dielectric material to form a dielectric layer. The method may further comprise applying a replacement substrate layer to the dielectric layer to provide mechanical stability for the RF device.

[0016] The electrical element may be a surface acoustic wave (SAW) device, a bulk acoustic wave (BAW) device, or other type of electrical device, such as a passive device (e.g., inductor).

[0017] In certain embodiments, the method comprises at least partially removing the substrate layer to expose at least a portion of a backside of an oxide layer disposed between the FET and the substrate layer. The method may further comprise disposing an electrical contact structure on the backside of the oxide layer to provide electrical contact to the one or more electrical connections through a through-oxide via. The method may comprise disposing a substrate contact layer on the backside of the oxide layer.

[0018] In accordance with a number of implementations, the present disclosure relates to a radio-frequency (RF) device comprising a field-effect transistor (FET) implemented over an oxide layer, one or more electrical connections to the FET, one or more dielectric layers formed over at least a portion of the electrical connections, an electrical element electrically coupled to the FET via the one or more electrical connections, and a handle wafer layer disposed on at least a portion of the one or more dielectric layers, the handle wafer layer including a topside trench defined at least in part by sidewall portions of the handle wafer layer, the trench exposing at least a portion of the electrical element.

[0019] In certain embodiments, the RF device further comprises a covering that covers at least a portion of the handle wafer layer and the trench to form a cavity. The covering may be a laminate film, for example. In certain embodiments, the RF device comprises a dielectric material that fills the trench. The RF device may further comprise a replacement substrate layer applied to the dielectric material to provide mechanical stability for the RF device.

[0020] In accordance with a number of implementations, the present disclosure relates to a wireless device comprising a transceiver configured to process radio-frequency (RF) signals and an RF module in communication with the transceiver, the RF module including a switching device having a field-effect transistor (FET) implemented over an

oxide layer, one or more electrical connections to the FET, one or more dielectric layers formed over at least a portion of the electrical connections, an electrical element electrically coupled to the FET via the one or more electrical connections, a handle wafer layer disposed on at least a portion of the one or more dielectric layers, the handle wafer layer including a topside trench defined at least in part by sidewall portions of the handle wafer layer, the trench exposing at least a portion of the electrical element. The wireless device further comprises an antenna in communication with the RF module, the antenna configured to facilitate transmitting and/or receiving of the RF signals.

[0021] In certain embodiments, the RF module includes a covering that covers at least a portion of the handle wafer layer and the trench to form a cavity. The RF module may include a dielectric material that at least partially fills the trench.

[0022] In accordance with a number of implementations, the present disclosure relates to a method of fabricating a radio-frequency (RF) device. The method comprises providing a field-effect transistor (FET) formed over an oxide layer, forming one or more electrical connections to the FET, forming one or more dielectric layers over at least a portion of the electrical connections, disposing a handle wafer layer on at least a portion of the one or more dielectric layers, and removing at least a portion of the handle wafer layer to form an opening at least partially above the FET.

[0023] In certain embodiments, the method comprises thinning the handle wafer layer prior to removing the at least a portion of the handle wafer layer. The method may comprise covering at least a portion of the handle wafer layer and the opening with a covering to form a cavity. For example, the covering may comprise a laminate film, a plastic lid structure, an additional replacement substrate layer, or other type of covering.

[0024] In certain embodiments, the method comprises at least partially filling the opening with a dielectric material. The method may further comprise covering at least a portion of the handle wafer layer with the dielectric material to form a dielectric layer. The method may further comprise applying a replacement substrate layer to the dielectric layer to provide mechanical stability for the RF device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Figure 1 shows an example of a field-effect transistor (FET) device having an active FET implemented on a substrate, and a region below the active FET configured to include one or more features to provide one or more desirable operating functionalities for the active FET.

[0026] Figure 2 shows an example of a FET device having an active FET implemented on a substrate, and a region above the active FET configured to include one or more features to provide one or more desirable operating functionalities for the active FET.

[0027] Figure 3 shows that in some embodiments, a FET device can include both of the regions of Figures 1 and 2 relative an active FET.

[0028] Figure 4 shows an example FET device implemented as an individual silicon-on-insulator (SOI) unit.

[0029] Figure 5 shows that in some embodiments, a plurality of individual SOI devices similar to the example SOI device of Figure 4 can be implemented on a wafer.

[0030] Figure 6A shows an example wafer assembly having a first wafer and a second wafer positioned over the first wafer.

[0031] Figure 6B shows an unassembled view of the first and second wafers of the example of Figure 6A.

[0032] Figure 7 shows a terminal representation of an SOI FET having nodes associated with a gate, a source, a drain, a body, and a substrate.

[0033] Figures 8A and 8B show side sectional and plan views, respectively, of an example SOI FET device having a node for its substrate.

[0034] Figure 9 shows a side sectional view of an SOI substrate that can be utilized to form an SOI FET device having an electrical connection for a substrate layer.

[0035] Figure 10 shows a side sectional view of an SOI FET device having an electrical connection for a substrate layer.

[0036] Figure 11 shows an example SOI FET device that is similar to the example of Figure 10, but in which a trap-rich layer is substantially absent.

[0037] Figure 12 shows that in some embodiments, an electrical connection to a substrate can be implemented without being coupled to other portions of an active FET.

[0038] Figure 13 shows that in some embodiments, a handle wafer can include a plurality of doped regions implemented to provide one or more functionalities similar to a trap-rich interface layer in the example of Figure 10.

[0039] Figures 14A and 14B show side sectional and plan views of an example SOI FET having a contact layer implemented underneath an insulator layer such as a buried oxide (BOX) layer.

[0040] Figure 15 shows an example SOI FET device that is similar to the example of Figure 11, but with a contact layer implemented underneath a BOX layer.

[0041] Figure 16 shows an example SOI FET device that is similar to the example of Figure 12, but with a contact layer implemented underneath a BOX layer.

[0042] Figure 17 shows an example SOI FET device that is similar to the example of Figure 10, but with a contact layer implemented underneath a BOX layer.

[0043] Figure 18 shows an example SOI FET device that is similar to the example of Figure 13, but with a contact layer implemented underneath a BOX layer.

[0044] Figure 19 shows another example SOI FET device that is similar to the example of Figure 13, but with a perforated contact layer implemented underneath a BOX layer.

[0045] Figure 20 shows a process that can be implemented to facilitate fabrication of an SOI FET device having one or more features as described herein.

[0046] Figure 21 shows examples of various stages of the fabrication process of Figure 20.

[0047] Figures 22A and 22B show a process that can be implemented to fabricate an SOI FET device having one or more features as described herein.

[0048] Figures 23A and 23B show examples of various stages of the fabrication process of Figures 22A and 22B.

[0049] Figure 24 shows that in some embodiments, a contact layer having one or more features as described herein can be implemented with, for example, desired dimensions and/or separation from an active FET to provide one or more functionalities.

[0050] Figures 25A and 25B show examples of how a contact layer having one or more features as described herein can be dimensioned to provide one or more desirable functionalities.

[0051] Figures 26A-26F show non-limiting examples of how contact layers can be implemented relative to circuit elements.

[0052] Figure 27 shows an example of a contact layer that can be implemented in the example SOI FET device of Figure 19.

[0053] Figure 28 shows that in some embodiments, an SOI FET device can have its contact layer having one or more features as described herein biased by, for example, a substrate bias network.

[0054] Figure 29 shows an example of a radio-frequency (RF) switching configuration having an RF core and an energy management (EM) core.

[0055] Figure 30 shows an example of the RF core of Figure 29, in which each of the switch arms includes a stack of FET devices.

[0056] Figure 31 shows an example of the biasing configuration of Figure 28, implemented in a switch arm having a stack of FETs as described in reference to Figure 30.

[0057] Figure 32 shows that a pattern of one or more conductive layers can be implemented to be electrically connected to a bias circuit such as a substrate bias circuit.

[0058] Figure 33 shows an example configuration in which a pattern of one or more conductive layers can generally form a ring shaped perimeter substantially around an entire die having an RF core and an energy management core ("EM core").

[0059] Figure 34 shows an example configuration in which a pattern of one or more conductive layers can generally form a ring shaped distribution implemented substantially around each of an RF core and an EM core of a switching die.

[0060] Figure 35 shows an example configuration in which a pattern of one or more conductive layers can generally form a ring shaped distribution implemented substantially around an assembly of series arms and shunt arms.

[0061] Figure 36 shows an example configuration in which a pattern of one or more conductive layers can generally form a ring shaped distribution implemented substantially around each of series arms and shunt arms.

[0062] Figure 37 shows an example configuration in which a pattern of one or more conductive layers can generally form a ring shaped distribution implemented substantially around each FET in a given arm.

[0063] Figures 38A-38E show non-limiting examples of patterns of one or more conductive layers that can be implemented around a circuit element.

[0064] Figures 39A and 39B show that in some embodiments, there may be more than one pattern of one or more conductive layers implemented relative a circuit element.

[0065] Figure 40 shows an example in which a conductive layer of an SOI FET device can be electrically connected to a substrate bias network.

[0066] Figure 41 shows another example in which a conductive layer of an SOI FET device can be electrically connected to a substrate bias network.

[0067] Figure 42 shows an example in which a conductive layer of an SOI FET device can be electrically connected to a gate node of the SOI FET device.

[0068] Figure 43 shows an example in which a conductive layer of an SOI FET device can be electrically connected to a gate node of the SOI FET device through a phase-shift circuit.

[0069] Figure 44 shows an example in which a conductive layer of an SOI FET device can be electrically connected to a gate node of the SOI FET device through a phase-shift circuit, similar to the example of Figure 43, and in which a substrate bias network can be configured to allow application of a DC control voltage to the conductive layer.

[0070] Figure 45A shows an example that is similar to the example of Figure 42, but with a diode D in series with a resistance R.

[0071] Figure 45B shows that in some embodiments, the polarity of the diode D can be reversed from the example of Figure 45A.

[0072] Figure 46 shows an example that is similar to the example of Figure 43, but with a diode D in parallel with a phase-shifting circuit.

[0073] Figure 47 shows an example that is similar to the example of Figure 42, but with a diode D in series with a resistance R.

[0074] Figure 48 shows an example that is similar to the example of Figure 46, but with biasing.

[0075] Figure 49 shows an SOI FET device having a conductive layer as described herein.

[0076] Figures 50A-50D show examples of how a conductive layer of an SOI FET device can be coupled to other nodes of the SOI FET device.

[0077] Figures 51A-51D show examples of how a conductive layer of an SOI FET device can be coupled to other nodes of the SOI FET device through a phase-shifting circuit.

[0078] Figures 52A-52D show examples that are similar to the examples of Figures 50A-50D, and in which a bias signal can be applied to the conductive layer.

[0079] Figures 53A-53D show examples that are similar to the examples of Figures 51A-51D, and in which a bias signal can be applied to the conductive layer.

[0080] Figures 54A-54D show examples of how a conductive layer of an SOI FET device can be coupled to other nodes of the SOI FET device through a diode D.

[0081] Figures 55A-55D show examples of how a conductive layer of an SOI FET device can be coupled to other nodes of the SOI FET device through a diode D and a phase-shifting circuit.

[0082] Figures 56A-56D show examples that are similar to the examples of Figures 54A-54D, and in which a bias signal can be applied to the conductive layer.

[0083] Figures 57A-57D show examples that are similar to the examples of Figures 55A-55D, and in which a bias signal can be applied to the conductive layer.

[0084] Figure 58 shows a switch assembly implemented in a single-pole-single-throw (SPST) configuration utilizing an SOI FET device.

[0085] Figure 59 shows that in some embodiments, the SOI FET device of Figure 58 can include a conductive layer feature as described herein.

[0086] Figure 60 shows an example of how two SPST switches having one or more features as described herein can be utilized to form a switch assembly having a single-pole-double-throw (SPDT) configuration.

[0087] Figure 61 shows that the switch assembly of Figure 60 can be utilized in an antenna switch configuration.

[0088] Figure 62 shows an example of how three SPST switches having one or more features as described herein can be utilized to form a switch assembly having a single-pole-triple-throw (SP3T) configuration.

[0089] Figure 63 shows that the switch assembly of Figure 62 can be utilized in an antenna switch configuration.

[0090] Figure 64 shows an example of how four SPST switches having one or more features as described herein can be utilized to form a switch assembly having a double-pole-double-throw (DPDT) configuration.

[0091] Figure 65 shows that the switch assembly of Figure 64 can be utilized in an antenna switch configuration.

[0092] Figure 66 shows an example of how nine SPST switches having one or more features as described herein can be utilized to form a switch assembly having a 3-pole-3-throw (3P3T) configuration.

[0093] Figure 67 shows that the switch assembly of Figure 66 can be utilized in an antenna switch configuration.

[0094] Figures 68A-68E show examples of how a DPDT switching configuration such as the examples of Figures 64 and 65 can be operated to provide different signal routing functionalities.

[0095] Figure 69A shows a process for forming a cavity in accordance with one or more embodiments disclosed herein.

[0096] Figure 69B shows examples of various structures associated with a cavity formation processes in accordance with one or more embodiments disclosed herein.

[0097] Figure 70 shows a process for forming a cavity in accordance with one or more embodiments disclosed herein.

[0098] Figure 71 shows examples of various structures associated with a cavity formation processes in accordance with one or more embodiments disclosed herein.

[0099] Figure 72 shows a process for forming a cavity in accordance with one or more embodiments disclosed herein.

[0100] Figure 73 shows examples of various structures associated with a cavity formation processes in accordance with one or more embodiments disclosed herein.

[0101] Figure 74 shows a process for forming a cavity in accordance with one or more embodiments disclosed herein.

[0102] Figure 75 shows examples of various structures associated with a cavity formation processes in accordance with one or more embodiments disclosed herein.

[0103] Figures 76A-76C show embodiments of die structures in accordance with one or more embodiments.

[0104] Figures 77A-77C show embodiments of die structures in accordance with one or more embodiments.

[0105] Figures 78A-78D depict non-limiting examples of switching circuits and bias/coupling circuits as described herein can be implemented on one or more semiconductor die.

[0106] Figures 79A and 79B show plan and side views, respectively, of a packaged module having one or more features as described herein.

[0107] Figure 80 shows a schematic diagram of an example switching configuration that can be implemented in the module of Figures 70A and 70B.

[0108] Figure 81 depicts an example wireless device having one or more advantageous features described herein.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

[0109] The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

Introduction

[0110] Disclosed herein are various examples of a field-effect transistor (FET) device having one or more regions relative to an active FET portion configured to provide a desired operating condition for the active FET. In such various examples, terms such as FET device, active FET portion, and FET are sometimes used interchangeably, with each other, or some combination thereof. Accordingly, such interchangeable usage of terms should be understood in appropriate contexts.

[0111] Figure 1 shows an example of a FET device 100 having an active FET 101 implemented on a substrate 103. As described herein, such a substrate can include one or more layers configured to facilitate, for example, operating functionality of the active FET, processing functionality for fabrication and support of the active FET, etc. For example, if the FET device 100 is implemented as a silicon-on-Insulator (SOI) device, the substrate 103 can include an insulator layer such as a buried oxide (BOX) layer, an interface layer, and a handle wafer layer.

[0112] Figure 1 further shows that in some embodiments, a region 105 below the active FET 101 can be configured to include one or more features to provide one or more desirable operating functionalities for the active FET 101. For the purpose of description, it will be understood that relative positions above and below are in the example context of the active FET 101 being oriented above the substrate 103 as shown. Accordingly, some or all of the region 105 can be implemented within the substrate 103. Further, it will be understood that the region 105 may or may not overlap with the active FET 101 when viewed from above (e.g., in a plan view).

[0113] Figure 2 shows an example of a FET device 100 having an active FET 101 implemented on a substrate 103. As described herein, such a substrate can include one or more layers configured to facilitate, for example, operating functionality of the active FET 100, processing functionality for fabrication and support of the active FET 100, etc. For example, if the FET device 100 is implemented as a silicon-on-Insulator (SOI) device, the substrate 103 can include an insulator layer such as a buried oxide (BOX) layer, an interface layer, and a handle wafer layer.

[0114] In the example of Figure 2, the FET device 100 is shown to further include an upper layer 107 implemented over the substrate 103. In some embodiments, such an upper layer can include, for example, a plurality of layers of metal routing features and dielectric layers to facilitate, for example, connectivity functionality for the active FET 100.

[0115] Figure 2 further shows that in some embodiments, a region 109 above the active FET 101 can be configured to include one or more features to provide one or more desirable operating functionalities for the active FET 101. Accordingly, some or all of the region 109 can be implemented within the upper layer 107. Further, it will be understood that the region 109 may or may not overlap with the active FET 101 when viewed from above (e.g., in a plan view).

[0116] Figure 3 shows an example of a FET device 100 having an active FET 101 implemented on a substrate 103, and also having an upper layer 107. In some embodiments, the substrate 103 can include a region 105 similar to the example of Figure 1, and the upper layer 107 can include a region 109 similar to the example of Figure 2.

[0117] Examples related to some or all of the configurations of Figures 1-3 are described herein in greater detail.

[0118] In the examples of Figures 1-3, the FET devices 100 are depicted as being individual units (e.g., as semiconductor die). Figures 4-6 show that in some embodiments, a plurality of FET devices having one or more features as described herein can be fabricated partially or fully in a wafer format, and then be singulated to provide such individual units.

[0119] For example, Figure 4 shows an example FET device 100 implemented as an individual SOI unit. Such an individual SOI device can include one or more active FETs 101 implemented over an insulator such as a BOX layer 104 which is itself implemented over a handle layer such as a silicon (Si) substrate handle wafer 106. In the example of Figure 4, the BOX layer 104 and the Si substrate handle wafer 106 can collectively form the substrate 103 of the examples of Figures 1-3, with or without the corresponding region 105.

[0120] In the example of Figure 4, the individual SOI device 100 is shown to further include an upper layer 107. In some embodiments, such an upper layer can be the upper layer 103 of Figures 2 and 3, with or without the corresponding region 109.

[0121] Figure 5 shows that in some embodiments, a plurality of individual SOI devices similar to the example SOI device 100 of Figure 4 can be implemented on a wafer 200. As shown, such a wafer can include a wafer substrate 103 that includes a BOX layer 104 and a Si handle wafer layer 106 as described in reference to Figure 4. As described herein, one or more active FETs can be implemented over such a wafer substrate.

[0122] In the example of Figure 5, the SOI device 100 is shown without the upper layer (107 in Figure 4). It will be understood that such a layer can be formed over the wafer substrate 103, be part of a second wafer, or any combination thereof.

[0123] Figure 6A shows an example wafer assembly 204 having a first wafer 200 and a second wafer 202 positioned over the first wafer 200. Figure 6B shows an unassembled view of the first and second wafers 200, 202 of the example of Figure 6A.

[0124] In some embodiments, the first wafer 200 can be similar to the wafer 200 of Figure 5. Accordingly, the first wafer 200 can include a plurality of SOI devices 100 such as the example of Figure 4. In some embodiments, the second wafer 202 can be configured to provide, for example, a region (e.g., 109 in Figures 2 and 3) over a FET of each SOI device 100, and/or to provide temporary or permanent handling wafer functionality for process steps involving the first wafer 200.

Examples of SOI Implementation of FET Devices

[0125] Silicon-on-Insulator (SOI) process technology is utilized in many radio-frequency (RF) circuits, including those involving high performance, low loss, high linearity switches. In such RF switching circuits, performance advantage typically results from building a transistor in silicon, which sits on an insulator such as an insulating buried oxide (BOX). The BOX typically sits on a handle wafer, typically silicon, but can be glass, borosilicon glass, fused quartz, sapphire, silicon carbide, or any other electrically-insulating material.

[0126] Typically, an SOI transistor is viewed as a 4-terminal field-effect transistor (FET) device with gate, drain, source, and body terminals. However, an SOI FET can be represented as a 5-terminal device, with an addition of a substrate node. Such a substrate node can be biased and/or be coupled one or more other nodes of the transistor to, for example, improve both linearity and loss performance of the transistor. Various examples related to such a substrate node and biasing/coupling of the substrate node are described herein in greater detail.

[0127] In some embodiments, such a substrate node can be implemented with a contact layer having one or more features as described herein to allow the contact layer to provide a desirable functionality for the SOI FET. Although various examples are described in the context of RF switches, it will be understood that one or more features of the present disclosure can also be implemented in other applications involving FETs.

[0128] Figure 7 shows a terminal representation of an SOI FET 100 having nodes associated with a gate, a source, a drain, a body, and a substrate. It will be understood that in some embodiments, the source and the drain can be reversed.

[0129] Figures 8A and 8B show side sectional and plan views of an example SOI FET device 100 having a node for its substrate. Such a substrate can be, for example, a silicon substrate associated with a handle wafer 106 as described herein. Although described in the context of such a handle wafer, it will be understood that the substrate does not necessarily need to have functionality associated with a handle wafer.

[0130] An insulator layer such as a BOX layer 104 is shown to be formed over the handle wafer 106, and a FET structure is shown to be formed based on an active silicon device 102 over the BOX layer 104. In various examples described herein, and as

shown in Figures 8A and 8B, the FET structure can be configured as an NPN or PNP device.

[0131] In the example of Figures 8A and 8B, terminals for the gate, source, drain and body are shown to be configured and provided so as to allow operation of the FET. A substrate terminal is shown to be electrically connected to the substrate (e.g., handle wafer) 106 through an electrically conductive feature 108 extending through the BOX layer 104. Such an electrically conductive feature can include, for example, one or more conductive vias, one or more conductive trenches, or any combination thereof. Various examples of how such an electrically conductive feature can be implemented are described herein in greater detail.

[0132] In some embodiments, a substrate connection can be connected to ground to, for example, avoid an electrically floating condition associated with the substrate. Such a substrate connection for grounding typically includes a seal-ring implemented at an outermost perimeter of a given die.

[0133] In some embodiments, a substrate connection such as the example of Figures 8A and 8B can be utilized to bias the substrate 106, to couple the substrate with one or more nodes of the corresponding FET (e.g., to provide RF feedback), or any combination thereof. Such use of the substrate connection can be configured to, for example, improve RF performance and/or reduce cost by eliminating or reducing expensive handle-wafer treatment processes and layers. Such performance improvements can include, for example, improvements in linearity, loss and/or capacitance performance.

[0134] In some embodiments, the foregoing biasing of the substrate node can be, for example, selectively applied to achieve desired RF effects only when needed or desired. For example, bias points for the substrate node can be connected to envelope-tracking (ET) bias for power amplifier (PA) to achieve distortion cancelation effects.

[0135] In some embodiments, a substrate connection for providing the foregoing example functionalities can be implemented as a seal-ring configuration similar to the grounding configuration, or other connection configurations. Examples of such substrate connections are described herein in greater detail.

[0136] Figure 9 shows a side sectional view of an SOI substrate 10 that can be utilized to form an SOI FET device 100 of Figure 10 having an electrical connection for a

substrate layer 106 (e.g., Si handle layer). In Figure 9, an insulator layer such as a BOX layer 104 is shown to be formed over the Si handle layer 106. An active Si layer 12 is shown to be formed over the BOX layer 104. It will be understood that in some embodiments, the foregoing SOI substrate 10 of Figure 9 can be implemented in a wafer format, and SOI FET devices having one or more features as described herein can be formed based on such a wafer.

[0137] In Figure 10, an active Si device 102 is shown to be formed from the active Si layer 12 of Figure 9. One or more electrically conductive features 108 such as vias are shown to be implemented through the BOX layer 104, relative to the active Si device 102. In some embodiments, such conductive features (108) can allow the Si handle layer 106 to be coupled to the active Si device (e.g., a FET), be biased, or any combination thereof. Such coupling and/or biasing can be facilitated by, for example, a metal stack 110. In some embodiments, such a metal stack can allow the conductive features 108 to be electrically connected to a terminal 112. In the example of Figure 10, one or more passivation layers, one or more dielectric layers, or some combination thereof (collectively indicated as 114) can be formed to cover some or all of such a metal stack.

[0138] In some embodiments, a trap-rich layer 14 can be implemented between the BOX layer 104 and the Si handle layer 106. However, and as described herein, the electrical connection to the Si handle layer 106 through the conductive feature(s) 108 can eliminate or reduce the need for such a trap-rich layer which is typically present to control charge at an interface between the BOX layer 104 and the Si handle layer 106, and which can involve costly process steps.

[0139] Aside from the foregoing example of eliminating or reducing the need for a trap-rich layer, the electrical connection to the Si handle layer 106 can provide a number of advantageous features. For example, the conductive feature(s) 108 can allow forcing of excess charge at the BOX/Si handle interface to thereby reduce unwanted harmonics. In another example, excess charge can be removed through the conductive feature(s) 108 to thereby reduce the off-capacitance (C_{off}) of the SOI FET. In yet another example, the presence of the conductive feature(s) 108 can lower the threshold of the SOI FET to thereby reduce the on-resistance (R_{on}) of the SOI FET.

[0140] Figure 11 shows an example FET device 100 that is similar to the example of Figure 10, but in which a trap-rich layer (14 in Figure 10) is substantially absent. Accordingly, in some embodiments, the BOX layer 104 and the Si handle layer 106 can be in substantially direct engagement with each other.

[0141] In the example of Figure 11, the conductive features (e.g., vias) 108 are depicted as extending through the BOX layer 104 and contacting the Si handle layer 106 generally at the BOX/Si handle interface. It will be understood that in some embodiments, such conductive features can extend deeper into the Si handle layer 106.

[0142] In the examples of Figures 10 and 11, the conductive features 108 are depicted as being coupled to other electrical connections associated with the active Si device 102. Figure 12 shows that in some embodiments, an electrical connection to a substrate (e.g., Si handle layer 106) can be implemented without being coupled to such other electrical connections associated with the active Si device 102. For example, a conductive feature 108 such as a via is shown to extend through the BOX layer 104 so as to form a contact with the Si handle layer 106. The upper portion of the through-BOX conductive feature 108 is shown to be electrically connected to a terminal 113 that is separate from a terminal 112.

[0143] In some embodiments, the electrical connection between the separate terminal 113 and the Si handle layer 106 (through the conductive feature 108) can be configured to allow, for example, separate biasing of a region in the substrate (e.g., Si handle layer 106) to achieve a desired operating functionality for the active Si device 102. Such an electrical connection between the separate terminal 113 and the Si handle layer 106 is an example of a non-grounding configuration utilizing one or more through-BOX conductive features 108.

[0144] In the examples of Figures 10-12, the through-BOX conductive features (108) are depicted as either being coupled to electrical connections associated with the active Si device 102, or as being separate from such electrical connections. It will be understood that other configurations can also be implemented. For example, one or more through-BOX conductive features (108) can be coupled to one node of the active Si device 102 (e.g., source, drain or gate), but not other node(s). Non-limiting examples of circuit

representations of such coupling (or non-coupling) between the substrate node and other nodes of the active Si device are disclosed herein in greater detail.

[0145] In the example of Figure 10, the trap-rich layer 14 can be implemented as an interface layer between the BOX layer 104 and the Si handle layer 106, to provide one or more functionalities as described herein. In the examples of Figures 11 and 12, such a trap-rich interface layer 14 can be omitted as described herein.

[0146] Figure 13 shows that in some embodiments, a handle wafer 106 (e.g., Si handle layer) can include a plurality of doped regions 117 implemented to provide one or more functionalities similar to a trap-rich interface layer (e.g., 14 in Figure 10). Such doped regions can be, for example, generally amorphous and have relatively high resistivity when compared to other portions of the handle wafer 106. In some embodiments, such doped regions can include crystalline structure, amorphous structure, or any combination thereof.

[0147] In the example of Figure 13, two FETs 102 and islands 115 are shown to be formed from an active Si layer 12 which is implemented over a BOX layer 104. The BOX layer is shown to be implemented over the handle wafer 106 having the doped regions 117. In some embodiments, such doped regions (117) can be implemented to be laterally positioned generally under gaps between the FETs 102 and/or the islands 115.

[0148] Figure 13 further shows that in some embodiments, the handle wafer 106 having doped regions such as the foregoing doped regions 117 can be biased as described herein through one or more conductive features 108 such as vias. As described herein, such conductive features 108 can be coupled to other portions of FET(s), to a separate terminal, or any combination thereof, so as to provide biasing to the handle wafer substrate 106 to achieve one or more desired operating functionalities for the FET(s).

[0149] In the example of Figure 13, a given conductive feature 108 can interact with a FET 102 through the handle wafer 106. For example, the BOX layer being interposed between the FET 102 and the handle wafer 106 can result in a capacitance C therebetween. Further, a resistance R can exist between the end of the conductive feature 108 and the BOX/handle wafer interface. Accordingly, a series RC coupling can be provided between the conductive feature 108 and the underside of the FET 102. Thus, providing a bias signal to handle wafer 106 through the conductive feature 108 can provide a desirable operating environment for the FET 102.

[0150] In the example of Figure 13, a given conductive feature 108 is depicted as being laterally separated from the nearest FET 102 so as to include at least one doped region 117 in the handle wafer 106. Accordingly, the resulting resistive path (with resistance R) can be relatively long. Thus, the resistance R can be a high resistance.

[0151] Referring to the examples of Figures 10-13, it is noted that in some embodiments, a given conductive feature 108 can be implemented so as to be laterally separated from the nearest FET 102 by a separation distance. Such a separation distance can be, for example, at least 1 μm , 2 μm , 3 μm , 4 μm , 5 μm , 6 μm , 7 μm , 8 μm , 9 μm , or 10 μm . In some embodiments, the separation distance can be in a range of 5 μm to 10 μm . For the purpose of description, it will be understood that such a separation distance can be, for example, a distance between the closest portions of the conductive feature 108 and the corresponding FET 102 in the active Si layer (12).

[0152] Described herein are, among others, examples related to SOI FET devices having a contact layer. Figures 14A and 14B show side sectional and plan views of an example SOI FET 100 having such a contact layer (260), in the context of the example SOI FET 100 of Figures 8A and 8B. Examples of how such a contact layer can be formed, as well as how such a contact layer can be configured in different manners, are described herein in greater detail.

[0153] In some embodiments, a contact layer having one or more features as described herein can be implemented on a side of a BOX layer opposite from the side on which a FET is formed. In the context of the FET being formed on the front or upper side of such a BOX layer, the contact layer can be implemented on the back or lower side of the BOX. Accordingly, relational terms “back,” “backside,” “lower,” “lower side,” etc. referring to position of a contact layer will be understood in the foregoing context.

[0154] It will also be understood that a contact layer having one or more features as described herein can also be referred to as a conductive contact layer, a substrate contact layer, a conductive layer, or some combination thereof. In some embodiments, such a contact layer can be implemented to be between a BOX layer and a substrate contact layer. In some embodiments, such a contact layer can be implemented on the backside of a BOX layer without a substrate layer. Accordingly, it will be understood that

the foregoing examples of interchangeable terms for the contact layer (including the substrate contact layer) can refer to implementations with or without a substrate layer.

[0155] In the example of Figure 14, the contact layer 260 is depicted as being in electrical contact with the conductive feature 108. Such a conductive feature (108) can allow the contact layer 260 to be in electrical contact with, for example, a substrate node. As described herein, such a substrate node can be electrically connected to a bias circuit and/or be coupled to one or more portions of the FET. Although various examples are described herein in the context of the contact layer 260 being electrically connected through one or more through-BOX conductive feature (such as the conductive feature 108 of Figure 14), it will be understood that a contact layer (such as the contact layer 260 of Figure 14) can be electrically connected in other configurations so as to provide an electrical connection to a bias circuit and/or one or more portions of a corresponding FET.

[0156] Figure 15 shows that in some embodiments, a contact layer 260 having one or more features as described herein can be implemented in an FET device 100 that is similar to the example of Figure 11 (e.g., in which a trap-rich layer (14 in Figure 10) is substantially absent). Accordingly, in some embodiments, the contact layer 260 can be in substantially direct contact with the BOX layer 104 on one side, and in substantially direct contact with the Si handle layer 106 on the other side.

[0157] In the example of Figure 15, the conductive features (e.g., vias) 108 are depicted as extending through the BOX layer 104 and contacting the contact layer 260. As described herein, such conductive features can be coupled to other electrical connections associated with the active Si device 102.

[0158] Figure 16 shows that in some embodiments, an electrical connection to a contact layer 260 can be implemented without being coupled to such other electrical connections associated with the active Si device 102. For example, a conductive feature 108 (such as a via) is shown to extend through the BOX layer 104 so as to form a contact with the contact layer 260. The upper portion of the through-BOX conductive feature 108 is shown to be electrically connected to a terminal 113 that is separate from a terminal 112.

[0159] In some embodiments, the electrical connection between the separate terminal 113 and the contact layer 260 (through the conductive feature 108) can be configured to allow, for example, separate biasing or controlling of a region underneath the

active Si device 102 to achieve a desired operating functionality for the active Si device 102. Examples related to such operating functionality are described herein in greater detail.

[0160] In the examples of Figures 15 and 16, the through-BOX conductive features (108) are depicted as either being coupled to electrical connections associated with the active Si device 102, or as being separate from such electrical connections. It will be understood that other configurations can also be implemented. For example, one or more through-BOX conductive features (108) can be coupled to one node of the active Si device 102 (e.g., source, drain or gate), but not other node(s). Non-limiting examples of circuit representations of such coupling (or non-coupling) between a node associated with the contact layer 260 and other nodes of the active Si device are disclosed herein in greater detail.

[0161] Figure 17 shows that in some embodiments, a contact layer 260 having one or more features as described herein can be implemented in an FET device 100 that is similar to the example of Figure 10 (e.g., in which a trap-rich layer 14 is present). In the example of Figure 17, the contact layer 260 can be implemented to be between the trap-rich layer 14 and the BOX layer 104.

[0162] In the example of Figure 17, the contact layer 260 is shown to be coupled to one or more portions of the active Si device 102 (e.g., through one or more through-BOX conductive features 108). It will be understood that in some embodiments, the contact layer of Figure 17 can be coupled to a separate terminal such as the separate terminal 113 of Figure 16.

[0163] Figures 18 and 19 show that in some embodiments, a contact layer 260 having one or more features as described herein can be implemented in an FET device 100 that is similar to the example of Figure 13 (e.g., in which a plurality of doped regions 117 are present). In the example of Figure 18, the contact layer 260 can be implemented to be substantially between the plurality of doped regions 117 and the BOX layer 104. In the example of Figure 19, the contact layer 260 can be configured to allow the plurality of doped regions 117 to be substantially in contact with the BOX layer 104. In some embodiments, such a configuration can be achieved by, for example, the contact layer 260 having a plurality of openings to allow the corresponding doped regions 117 to be in

contact with the BOX layer 104. An example of such a perforated configuration of the contact layer 260 is described herein in greater detail.

[0164] In the examples of Figures 18 and 19, the contact layer 260 can be coupled to one or more portions of an active device 102, be coupled to a separate terminal, or be configured in some combination thereof, similar to the examples of Figures 15 and 16.

Examples Related to Fabrication of SOI FET Devices

[0165] Figures 20 and 22 show processes 130 and 200 that can be implemented to fabricate an SOI device having one or more features as described herein. Figures 21 and 23 show examples of various stages of the fabrication processes of Figures 20 and 22. In some embodiments, some or all of the various process steps can be implemented utilizing wafer processing technologies.

[0166] In some embodiments, fabrication of an SOI device having one or more features as described herein can include fabrication of a wafer having an electrical connection formed between a contact layer and a terminal. An example of a wafer that can be utilized to achieve such a connection between the contact layer and the terminal is shown in Figure 21 as 146, and examples of process steps in Figure 20 can be implemented to achieve such a wafer configuration.

[0167] In block 132 of Figure 20, an SOI substrate can be formed or provided. In state 140 of Figure 21, such an SOI substrate can include an Si substrate 106 such as an Si handle wafer, an oxide layer 104 over the Si substrate 106, and an active Si layer 12 over the oxide layer 104. Such an SOI substrate may or may not have a trap-rich layer (e.g., 14 in Figures 9 and 10) between the oxide layer 104 and the Si substrate 106. Similarly, such an SOI substrate may or may not have doped regions (e.g., 117 in Figure 13) in the Si substrate 106.

[0168] In block 134 of Figure 20, one or more FETs can be formed with the active Si layer. In state 142 of Figure 21, such a FET is depicted as 150.

[0169] In block 136 of Figure 20, one or more conductive features such as vias can be formed through the oxide layer, to the Si substrate, and relative to the FET(s). In state 144 of Figure 21, such a conductive via is depicted as 108. As described herein, such an electrical connection through the oxide layer 104 to the Si substrate 106 can also

be implemented utilizing other conductive features such as one or more conductive trenches.

[0170] In the example of Figures 20 and 21, it will be understood that blocks 134 and 136 may or may not be performed in the example sequence shown. In some embodiments, conductive feature(s) such as a deep trench can be formed and filled with poly prior to the formation of the FET(s). In some embodiments, such conductive feature(s) can be formed (e.g., cut and filled with a metal such as tungsten (W) after the formation of the FET(s). It will be understood that other variations in sequences associated with the example of Figures 20 and 21 can also be implemented.

[0171] In block 138 of Figure 20, electrical connections can be formed for the conductive vias and the FET(s). In state 146 of Figure 21, such electrical connections are depicted as a metallization stack collectively indicated as 110. Such a metal stack can electrically connect the FET(s) 150 and the conductive vias 108 to one or more terminals 112. In the example state 146 of Figure 21, a passivation layer 114 is shown to be formed to cover some or all of the metallization stack 110.

[0172] Referring to Figures 22 and 23, process 200 can be a continuation of the process 130 associated with Figures 20 and 21 (e.g., both processes implemented at one fabrication facility), a separate process that utilizes as an input a wafer (e.g., configuration 146 in Figure 21) resulting from the process 130 (e.g., two processes implemented at different fabrication facilities), or any combination thereof. Accordingly, in block 202 of the process 200 of Figure 22A, an SOI wafer having an electrical connection for a substrate layer can be formed or provided. In Figure 23A, state 146 can be similar to state 146 of Figure 21.

[0173] In block 204 of Figure 22A, a carrier layer can be formed or attached on the front side of the SOI wafer. For the purpose of description, the front side of the SOI wafer can include the side opposite from the substrate layer. In state 250 of Figure 23A, such a carrier layer is depicted as 252. As described herein, such a carrier layer on the front side of the SOI wafer can allow fabrication steps to be performed on the back side to facilitate formation of a contact layer.

[0174] In some embodiments, the carrier layer can be a temporarily attached layer, or a permanently attached layer. In some embodiments, the carrier layer can be any

material suitable for being attached (temporarily or permanently) to one side of a wafer so as to allow one or more process steps to be performed on the other side of the wafer. Such a carrier layer can include, for example, another wafer, silicon, glass, quartz, silicon carbide, sapphire, etc. Such a carrier layer can be attached to the front side of the SOI wafer utilizing, for example, a spun-on adhesive.

[0175] In block 206 of Figure 22A, some or all of the substrate layer can be removed from the back side of the SOI wafer. In Figure 23A, such a substrate layer is depicted as 106 in state 250. In state 254, such a substrate layer is shown to be removed so as to expose a surface 256.

[0176] In some embodiments, the substrate layer can be removed sufficiently to expose the conductive feature(s) 108 such as conductive via(s). In some embodiments, such removal of the substrate layer may or may not expose the oxide layer 104. Such removal of the substrate layer can be achieved by, for example, grinding, chemical mechanical polishing (CMP), selective etching using an appropriate chemistry, or some combination thereof.

[0177] In block 208 of Figure 22A, a contact layer can be formed on the surface resulting from the removal of the substrate layer. In state 258 of Figure 23A, such a contact layer is depicted as 260 formed on the exposed surface 256.

[0178] As described herein, such a contact layer can be formed so as to be in electrical contact with the conductive feature(s) 108. In some embodiments, the contact layer 260 can include one or more layers that can be, for example, patterned, deposited, implanted, and/or formed by surface treatment on the exposed surface 256 of the oxide layer 104. Such a contact layer on the oxide layer 104 can have, for example, conductive, resistive, dielectric, inductive, rectifying, semi-insulating, semiconducting, trap and/or hole type properties.

[0179] In block 210 of Figure 22B, an interface layer can be formed over the contact layer. In state 262 of Figure 23B, such an interface layer is depicted as 264 formed so as to substantially cover the contact layer 260 and the surface 256. In some embodiments, such an interface layer (264) can be configured to facilitate attachment of a replacement substrate layer.

[0180] In block 212 of Figure 22B, a replacement substrate layer can be formed on or attached to the interface layer. In state 266 of Figure 23B, such a replacement substrate layer is depicted as 268.

[0181] In some embodiments, the substrate layer 268 can be a wafer, and such a wafer can be wafer-bonded to the oxide layer 104 of the SOI wafer, with or without the interface layer 104. Such wafer-bonding can be achieved by one or more wafer-bonding techniques. In some embodiments, the replacement substrate wafer can include, for example, silicon, glass, quartz, sapphire, silicon carbide, and/or gallium arsenide. Other materials can also be utilized for the replacement substrate wafer.

[0182] In block 214 of Figure 22B, the carrier layer can be removed from the SOI wafer's front side. In state 270 of Figure 23B, the front side of the SOI wafer is shown to have the carrier layer removed so as to substantially expose the terminals 112. Such removal of the carrier layer from the front side of the SOI wafer can be facilitated by the replacement substrate layer 268 now providing, among others, handle layer functionality.

[0183] In the example state 270 of Figure 23B, it is assumed that the carrier layer about the terminal 112 was a temporary layer. Such a temporary layer can be removed substantially completely from the front side of the SOI wafer. In some embodiments, at least some of the carrier layer can remain on the front side of the SOI wafer. In some embodiments, the front side of the SOI wafer can be further processed.

[0184] In the fabrication example described in reference to Figures 22 and 23, layer transfer techniques are utilized. However, it will be understood that use of other process techniques can be utilized to form a contact layer on or near the back side surface of an oxide layer of an SOI device.

[0185] In some embodiments, a contact layer as described herein can be utilized to, for example, provide bias for the substrate of an SOI device. In some embodiments, a contact layer as described herein can also be utilized for other applications. For example, Figure 24 shows that a contact layer 260 can be configured to be utilized as a back-gate to a transistor. Such a back-gate can provide one or more functionalities such as assisting in depleting or increasing charge in the active channel of an SOI FET 100. In some embodiments, the contact layer 260 can be dimensioned appropriately (e.g., depicted as dimension 280) to provide such back-gate functionality. In some embodiments, the contact

layer 260 can be separated from the active channel of an SOI FET 100 by a desired distance 282 to provide a desired functionality such as the back-gate functionality. In some embodiments, such a separation distance (282) can be achieved by, for example, a selected thickness of the BOX layer 104. In some embodiments, both of the dimension 280 and the separation distance 282 can be selected appropriately to achieve one or more functionalities for the FET.

[0186] Figures 25A and 25B show additional examples of how a contact layer 260 having one or more features as described herein can be dimensioned to provide one or more desirable functionalities. In the example of Figure 25A, the contact layer 260 is depicted as having a rectangular footprint shape dimensioned to be in electrical contact with a conductive feature 108, and to provide at least some overlap with a gate region associated with a FET 102.

[0187] Figure 25B shows that in some embodiments, a footprint shape of a contact layer can be selected to facilitate one or more functionalities. For example, suppose that an additional overlap is desired between a substrate contact layer and a gate region of the FET 102 (e.g., compared to the example of Figure 25A). To achieve such an increased overlap, a contact layer 260 can include an extended area 290 (e.g., depicted as additional areas above and below the original rectangular shape of the contact layer 260) to accommodate such an additional overlap.

[0188] In some embodiments, other design parameters associated with a contact layer can be implemented to achieve one or more desired functionalities. For example, design parameters such as contact layer material(s), thickness of the oxide layer, and/or the biasing networks can be configured appropriately for devices such as MOSFET devices to lower resistance, improve linearity performance, lower threshold voltage, increase breakdown voltage, and/or improve isolation performance of the transistor.

[0189] In the various examples described in reference to Figures 14, 24 and 25, the contact layer 260 is depicted as being located generally under a circuit element such as a FET. However, it will be understood that a contact layer having one or more features as described herein can also be implemented in other configurations. For example, different patterns of electrical connections can be implemented for substrates. In some

embodiments, contact layers can be configured to facilitate such patterns of electrical connections for substrates; and such patterns may or may not be under circuit elements.

[0190] Figures 26A-26F show non-limiting examples of how contact layers having one or more features as described herein can be implemented relative to circuit elements. In each of the examples, a contact layer 260 is shown to be electrically connected through one or more conductive vias 108; however, it will be understood that such electrical connections can also be implemented by other conductive features such as trenches.

[0191] Figure 26A shows an example where a contact layer 260 can be located generally below a circuit element 300. Such a configuration can represent, for example, the examples described herein in reference to Figures 14, 24 and 25.

[0192] Figure 26B shows an example where a contact layer 260 can be a strip that forms a perimeter around a circuit element 300. In some embodiments, such a configuration can be implemented with, for example, an example pattern of conductive vias that generally surround the circuit element 300.

[0193] Figures 26C and 26D show examples where contact layers 260 can be strips that form partial perimeters about their respective circuit elements 300. For example, Figure 26C shows a U-shape configuration, and Figure 26D shows an L-shaped configuration. In some embodiments, such configurations can be implemented with, for example, example patterns of conductive vias that partially surround the circuit element 300.

[0194] Figure 26E shows an example where a contact layer 260 can be a strip that forms a segment at or near a side of a circuit element 300. In some embodiments, such a configuration can be implemented with, for example, an example pattern of conductive vias that form a segment at or near a side of the circuit element 300.

[0195] Figure 26F shows an example where a contact layer 260 can have a relatively small pad shape that is not necessarily a strip. Such a configuration can be utilized in applications where relatively discrete contact layer is desired. In some embodiments, such a configuration can be implemented with, for example, an example pattern of one or more conductive vias grouped in a discrete manner.

[0196] It will be understood that contact layers having one or more features as described herein can also be configured in other ways. For example, there may be more than one contact layers for a given circuit element.

[0197] Figure 27 shows that in some embodiments, a contact layer 260 can include one or more openings. Such a configuration can, for example, accommodate features or regions formed on a handle wafer layer (e.g., Si handle wafer). For example, and in the context of the example configuration of Figure 19 (in which a plurality of doped regions 117 are provided on the handle wafer 106, the contact layer 260 of Figure 19 can include a plurality of openings as shown in Figure 27 to accommodate such doped regions.

[0198] In the example of Figure 27, such openings in the contact layer 260 are shown to substantially expose the corresponding doped regions. In some embodiments, such openings can also be dimensioned to partially expose corresponding doped regions.

[0199] In the example of Figure 27, the contact layer 260 can be electrically connected to one or more portions of an FET and/or a terminal through, for example, one or more conductive vias 108. It will be understood that other numbers and/or other arrangements of conductive vias can be implemented.

Examples Related to Biasing and/or Coupling of SOI FET Devices

[0200] Figure 28 shows that in some embodiments, an SOI FET device 100 having one or more features as described herein can have its contact layer biased by, for example, a substrate bias network 152. Various examples related to such a substrate bias network are described herein in greater detail.

[0201] In the example of Figure 28, other nodes such as the gate and the body of the SOI FET device 100 can also be biased by their respective networks. Among others, examples related to such gate and body bias networks can be found in PCT Publication No. WO 2014/011510 entitled CIRCUITS, DEVICES, METHODS AND COMBINATIONS RELATED TO SILICON-ON-INSULATOR BASED RADIO-FREQUENCY SWITCHES, the disclosure of which is hereby expressly incorporated by reference herein in its entirety.

[0202] Figures 29-31 show that in some embodiments, SOI FETs having one or more features as described herein can be implemented in RF switching applications.

[0203] Figure 29 shows an example of an RF switching configuration 160 having an RF core 162 and an energy management (EM) core 164. Additional details concerning

such RF and EM cores can be found in the above-referenced PCT Publication No. WO 2014/011510. The example RF core 162 of Figure 29 is shown as a single-pole-double-throw (SPDT) configuration in which series arms of transistors 100a, 100b are arranged between a pole and first and second throws, respectively. Nodes associated with the first and second throws are shown to be coupled to ground through their respective shunt arms of transistors 100c, 100d.

[0204] In the example of Figure 29, some or all of the transistors 100a-100d can include contact layers as described herein. Such contact layers can be utilized to provide desirable functionalities for the corresponding transistors.

[0205] Figure 30 shows an example of the RF core 162 of Figure 29, in which each of the switch arms 100a-100d includes a stack of FET devices. For the purpose of description, each FET in such a stack can be referred to as a FET, the stack itself can be collectively referred to as a FET, or some combination thereof can also be referred to as a FET. In the example of Figure 30, each FET in the corresponding stack one or more contact layers as described herein. It will be understood that some or all of the FET devices in the RF core 162 can include such contact layers.

[0206] Figure 31 shows an example of the biasing configuration 150 of Figure 28, implemented in a switch arm having a stack of FETs 100 as described in reference to Figure 30. In the example of Figure 31, each FET in the stack can be biased with a separate substrate bias network 152, the FETs in the stack can be biased with a plurality of substrate bias networks 152, all of the FETs in the stack can be biased with a common substrate bias network, or any combination thereof. Such possible variations can also apply to gate biasing (156) and body biasing (154).

[0207] Figure 32 shows that a pattern 261 of one or more contact layers 260 can be implemented to be electrically connected as described herein. In some embodiments, such a pattern of contact layers can also be electrically connected (depicted as 172) to, for example, a substrate bias network 152. In some embodiments, and as described herein, such a pattern of contact layers can be electrically connected to another node of the SOI FET device, with or without the substrate bias network 152. In some embodiments, some or all of the foregoing electrical connections for the contact layer(s) can be facilitated by

corresponding patterns of conductive features configured to provide substrate biasing functionality.

[0208] Figures 33-38 show non-limiting examples of the pattern 261 of one or more contact layers of Figure 32. In the examples of Figures 33-37, a pattern of such contact layer(s) (indicated as 170) is depicted as generally surrounding a corresponding circuit element. However, and as shown in Figures 38A-38E, such a pattern of contact layer(s) (indicated as 261) may or may not surround a corresponding circuit element.

[0209] In the examples of Figures 33-38, it will be understood that for some or all of such examples, the pattern of contact layer(s) can be electrically connected to another node of the SOI FET device, with or without the substrate bias network 152.

[0210] Figure 33 shows an example configuration 160 in which a pattern 170 of contact layers as described herein can generally form a ring shaped perimeter substantially around an entire die having an RF core 162 and an EM core 164. Accordingly, the RF core 162 and the EM core 164 collectively can be a circuit element associated with the pattern 170 of contact layers.

[0211] Figure 34 shows an example configuration 160 in which a pattern of contact layers as described herein can generally form a ring shaped distribution implemented substantially around each of an RF core 162 (pattern 170a) and an EM core 164 (pattern 170b) of a switching die. Accordingly, the RF core 162 can be a circuit element associated with the pattern 170a of contact layers, and the EM core 164 can be a circuit element associated with the pattern 170b of contact layers. Although both of the RF and EM cores are depicted as having respective patterns of contact layers, it will be understood that one pattern can have such contact layers while the other pattern does not. For example, the RF core can have such a pattern of contact layers while the EM core does not.

[0212] Figures 35-37 show examples of one or more patterns of contact layers as described herein that can be implemented for an RF core 162. Figure 35 shows an example configuration in which a pattern 170 of contact layers as described herein can generally form a ring shaped distribution implemented substantially around an assembly of series arms 100a, 100b and shunt arms 100c, 100d. Accordingly, the RF core 162 can be a circuit element associated with the pattern 170 of contact layers.

[0213] Figure 36 shows an example configuration in which a pattern of contact layers as described herein can generally form a ring shaped distribution implemented substantially around each of series arms 100a (pattern 170a), 100b (pattern 170b) and shunt arms 100c (pattern 170c), 100d (pattern 170d). Accordingly, each arm (100a, 100b, 100c or 100d) can be a circuit element associated with the corresponding pattern (170a, 170b, 170c or 170d) of contact layers.

[0214] Figure 37 shows an example configuration in which a pattern 170 of contact layers as described herein can generally form a ring shaped distribution implemented substantially around each FET in a given arm. Accordingly, each FET can be a circuit element associated with the corresponding pattern of contact layers.

[0215] In the examples of Figures 35-37, each component at different levels of the RF core is shown to be provided with a pattern of contact layers. For example, each arm in Figure 36 is shown to include a pattern of contact layers, and each FET in Figure 37 is shown to include a pattern of contact layers. It will be understood that not every one of such components necessarily needs to have such pattern of contact layers. Further, it will be understood that various combinations of the patterns of contact layers associated with different levels of the RF core can be combined. For example, an RF core can include a pattern of contact layers around the RF core itself, and one or more additional patterns of contact layers can also be implemented for selected arm(s) and/or FET(s).

[0216] As described herein, a pattern of contact layers can be implemented around a circuit element, partially around a circuit element, as a single feature, or any combination thereof.

[0217] Figures 38A-38E show non-limiting examples of such patterns. In such examples, the patterns are depicted as being electrically connected to their respective substrate bias networks. However, and as described herein, such patterns can be electrically connected to other part(s) of, for example, corresponding FET with or without such substrate bias networks.

[0218] Figure 38A shows an example in which a pattern 261 of one or more contact layers as described herein can be implemented around a circuit element, similar to the examples of Figures 33-37. Such a pattern can be electrically connected to a substrate bias network and/or another portion of the circuit element.

[0219] Figure 38B shows an example in which a pattern 261 of contact layers as described herein can be implemented partially around a circuit element. In the particular example of Figure 38B, such a partially surrounding pattern can be a U-shaped pattern in which one or more contact layers are implemented on three sides, but not on the fourth side relative to the circuit element. Such a pattern can be electrically connected to a substrate bias network and/or another portion of the circuit element.

[0220] Figure 38C shows another example in which a pattern 261 of contact layers as described herein can be implemented partially around a circuit element. In the particular example of Figure 38C, such a partially surrounding pattern can be an L-shaped pattern in which one or more contact layers are implemented on two adjacent sides, but not on the other two sides relative to the circuit element. Such a pattern can be electrically connected to a substrate bias network and/or another portion of the circuit element. In some embodiments, two sides having patterns of contact layers can be opposing sides.

[0221] Figure 38D shows yet another example in which a pattern 261 of contact layers as described herein can be implemented partially around a circuit element. In the particular example of Figure 38D, such a partially surrounding pattern can be a pattern in which one or more contact layers are implemented on one side, but not on the remaining three sides relative to the circuit element. Such a pattern can be electrically connected to a substrate bias network and/or another portion of the circuit element.

[0222] Figure 38E shows an example in which a pattern 261 of contact layers as described herein can be implemented as one or more discrete contact areas. In the particular example of Figure 38E, such a pattern can be a pattern in which a single contact layer is implemented relative to the circuit element. Such a pattern can be electrically connected to a substrate bias network and/or another portion of the circuit element.

[0223] In the examples of Figures 38A-38E, a given pattern 261 can include one or more discrete and/or contiguous contact layers. For the purpose of description, it will be understood that a contiguous pattern (e.g., two joined segments in the example of Figure 38C) can include contact layers that are electrically connected to a common substrate bias network and/or another common portion of the circuit element.

[0224] Figures 39A and 39B show that in some embodiments, there may be more than one pattern of contact layers implemented relative a circuit element. Such patterns of

contact layers can be electrically connected to separate substrate bias networks and/or portions of the circuit element, be electrically connected to a common substrate bias network and/or another common portion of the circuit element, or any combination thereof.

[0225] For example, Figure 39A shows a configuration in which two opposing sides relative to a circuit element are provided with first and second patterns 261 of contact layers. The first pattern can be electrically connected to a first substrate bias network 152a and/or a first portion of the circuit element, and the second pattern can be electrically connected to a second substrate bias network 152b and/or a second portion of the circuit element.

[0226] In another example, 39B shows a configuration in which two opposing sides relative to a circuit element are provided with first and second patterns 261 of contact layers, similar to the example of Figure 39A. Both of the first and second patterns 261 can be electrically connected to a common substrate bias network 152 and/or a common portion of the circuit element.

[0227] Figures 40-57 show non-limiting examples of substrate bias networks and/or other portions of an SOI FET device 100 that can be coupled with a contact layer of the SOI FET device 100. Such coupling with the contact layer can be facilitated by one or more patterns of conductive features as described herein. In some embodiments, such contact layers can provide one or more functionalities for the SOI FET device 100, including, for example, substrate biasing functionality, back-gate functionality, or some combination thereof.

[0228] Figure 40 shows an example in which a contact layer of an SOI FET device 100 can be electrically connected to a substrate bias network 152. Such a substrate bias network can be configured to allow application of a DC control voltage (V_{control}) to the contact layer.

[0229] Figure 41 shows an example in which a contact layer of an SOI FET device 100 can be electrically connected to a substrate bias network 152. Such a substrate bias network can be configured to allow application of a DC control voltage (V_{control}) to the contact through a resistance R (e.g., a resistor).

[0230] Figure 42 shows an example in which a contact layer of an SOI FET device 100 can be electrically connected to a gate node (e.g., back-side of the gate) of the

SOI FET device 100. In some embodiments, such a coupling may or may not include a resistance R (e.g., a resistor). In some embodiments, such a coupling may or may not be part of a substrate bias network 152 (if any).

[0231] Figure 43 shows an example in which a contact layer of an SOI FET device 100 can be electrically connected to a gate node of the SOI FET device 100 through a phase-shift circuit. In the example shown, the phase-shift circuit includes a capacitance (e.g., a capacitor); however, it will be understood that the phase-shift circuit can be configured in other manners. In some embodiments, such a coupling may or may not include a resistance R (e.g., a resistor). In some embodiments, such a coupling may or may not be part of a substrate bias network 152 (if any).

[0232] Figure 44 shows an example in which a contact layer of an SOI FET device 100 can be electrically connected to a gate node of the SOI FET device 100 through a phase-shift circuit, similar to the example of Figure 43. In the example of Figure 44, a substrate bias network 152 can be configured to allow application of a DC control voltage (V_{control}) to the contact layer. Such V_{control} can be applied directly to the contact layer, or through a resistance R1 (e.g., a resistor).

[0233] Figures 45-48 show non-limiting examples in which various couplings between a contact layer of an SOI FET device and another node of the SOI FET device can include a diode. Such a diode can be implemented to, for example, provide voltage-dependent couplings.

[0234] Figure 45A shows an example that is similar to the example of Figure 42, but with a diode D in series with the resistance R. In some embodiments, such a coupling between the contact layer the gate node can be implemented with or without the resistance R.

[0235] Figure 45B shows that in some embodiments, the polarity of the diode D can be reversed from the example of Figure 45A. It will be understood that such polarity reversal of the diode can also be implemented in the examples of Figures 46-48.

[0236] Figure 46 shows an example that is similar to the example of Figure 43, but with a diode D in parallel with a phase-shifting circuit (e.g., a capacitance C). In some embodiments, such a coupling between the contact layer and the gate node can be implemented with or without the resistance R.

[0237] Figure 47 shows an example that is similar to the example of Figure 42, but with a diode D in series with the resistance R. In some embodiments, a DC control voltage (V_{control}) can be applied directly to the contact layer, or through a resistance (e.g., a resistor).

[0238] Figure 48 shows an example that is similar to the example of Figure 46, but with biasing. Such biasing can be configured to allow application of a DC control voltage (V_{control}) to the contact layer directly or through a resistance R (e.g., a resistor).

[0239] In some embodiments, a contact layer connection having one or more features as described herein can be utilized to sense a voltage condition of the substrate. Such a sensed voltage can be utilized to, for example, compensate the voltage condition. For example, charge can be driven into or out of the substrate as needed or desired through the contact layer.

[0240] Figure 49 shows an SOI FET device 100 having a contact layer as described herein. Such a contact layer can be utilized to sense a voltage V associated with the substrate node. Figures 50-57 show non-limiting examples of how such sensed voltage can be utilized in various feedback and/or biasing configurations. Although various examples are described in the context of voltage V, it will be understood that one or more features of the present disclosure can also be implemented utilizing, for example, sensed current associated with the substrate.

[0241] Figures 50A-50D show examples of how a contact layer of an SOI FET device 100 can be coupled to another node of the SOI FET device 100. In some embodiments, such couplings can be utilized to facilitate the foregoing compensation based on the sensed substrate voltage of Figure 49. Figure 50A shows that a coupling 190 can be implemented between the contact layer and a gate node. Figure 50B shows that a coupling 190 can be implemented between the contact layer and a body node. Figure 50C shows that a coupling 190 can be implemented between the contact layer and a source node. Figure 50D shows that a coupling 190 can be implemented between the contact layer and a drain node. In some embodiments, the contact layer can be coupled to more than one of the foregoing nodes.

[0242] Figures 51A-51D show examples of how a contact layer of an SOI FET device 100 can be coupled to another node of the SOI FET device 100 through a phase-

shifting circuit (e.g., a capacitance) 192. In some embodiments, such couplings can be utilized to facilitate the foregoing compensation based on the sensed substrate voltage of Figure 49. Figure 51A shows that a coupling 190 having a phase-shifting circuit 192 can be implemented between the contact layer and a gate node. Figure 51B shows that a coupling 190 having a phase-shifting circuit 192 can be implemented between the contact layer and a body node. Figure 51C shows that a coupling 190 having a phase-shifting circuit 192 can be implemented between the contact layer and a source node. Figure 51D shows that a coupling 190 having a phase-shifting circuit 192 can be implemented between the contact layer and a drain node. In some embodiments, the contact layer can be coupled to more than one of the foregoing nodes.

[0243] Figures 52A-52D show examples that are similar to the examples of Figures 50A-50D. However, in each of the examples of Figures 52A-52D, a bias signal such as a DC control voltage (V_{control}) can be applied to the contact layer. Such V_{control} can be applied to the contact layer directly or through a resistance.

[0244] Figures 53A-53D show examples that are similar to the examples of Figures 51A-51D. However, in each of the examples of Figures 53A-53D, a bias signal such as a DC control voltage (V_{control}) can be applied to the contact layer. Such V_{control} can be applied to the contact layer directly or through a resistance.

[0245] Figures 54A-54D show examples of how a contact layer of an SOI FET device 100 can be coupled to another node of the SOI FET device 100 through a diode D. In some embodiments, such couplings can be utilized to facilitate the foregoing compensation based on the sensed substrate voltage of Figure 49. In some embodiments, a given diode can be reversed from the configuration as shown as needed or desired.

[0246] Figure 54A shows that a coupling 190 having a diode D can be implemented between the contact layer and a gate node. Figure 54B shows that a coupling 190 having a diode D can be implemented between the contact layer and a body node. Figure 54C shows that a coupling 190 having a diode D can be implemented between the contact layer and a source node. Figure 54D shows that a coupling 190 having a diode D can be implemented between the contact layer and a drain node. In some embodiments, the contact layer can be coupled to more than one of the foregoing nodes.

[0247] Figures 55A-55D show examples of how a contact layer of an SOI FET device 100 can be coupled to another node of the SOI FET device 100 through a diode D and a phase-shifting circuit 192. In some embodiments, such diode D and the phase-shifting circuit 192 can be arranged in a parallel configuration. In some embodiments, such couplings can be utilized to facilitate the foregoing compensation based on the sensed substrate voltage of Figure 49. In some embodiments, a given diode can be reversed from the configuration as shown as needed or desired.

[0248] Figure 55A shows that a coupling 190 having a diode D and a phase-shifting circuit 190 can be implemented between the contact layer and a gate node. Figure 55B shows that a coupling 190 having a diode D and a phase-shifting circuit 190 can be implemented between the contact layer and a body node. Figure 55C shows that a coupling 190 having a diode D and a phase-shifting circuit 190 can be implemented between the contact layer and a source node. Figure 55D shows that a coupling 190 having a diode D and a phase-shifting circuit 190 can be implemented between the contact layer and a drain node. In some embodiments, the contact layer can be coupled to more than one of the foregoing nodes.

[0249] Figures 56A-56D show examples that are similar to the examples of Figures 54A-54D. However, in each of the examples of Figures 56A-56D, a bias signal such as a DC control voltage (V_{control}) can be applied to the contact layer. Such V_{control} can be applied to the contact layer directly or through a resistance.

[0250] Figures 57A-57D show examples that are similar to the examples of Figures 55A-55D. However, in each of the examples of Figures 57A-57D, a bias signal such as a DC control voltage (V_{control}) can be applied to the contact layer. Such V_{control} can be applied to the contact layer directly or through a resistance.

Examples Related to Switch Configurations

[0251] As described herein in reference to the examples of Figures 29, 30 and 33-37, FET devices having one or more features of the present disclosure can be utilized to implement an SPDT switch configuration. It will be understood that FET devices having one or more features of the present disclosure can also be implemented in other switch configurations.

[0252] Figures 58-68 show examples related to various switch configurations that can be implemented utilizing FET devices such as SOI FET devices having one or more features as described herein. For example, Figure 58 shows a switch assembly 255 implemented in a single-pole-single-throw (SPST) configuration. Such a switch can include an SOI FET device 100 implemented between a first port (Port1) and a second port (Port2).

[0253] Figure 59 shows that in some embodiments, the SOI FET device 100 of Figure 58 can include a contact layer feature as described herein. The source node of the SOI FET device 100 can be connected to the first port (Port1), and the drain node of the SOI FET device 100 can be connected to the second port (Port2). As described herein, the SOI FET device 100 can be turned ON to close the switch 255 (of Figure 58) between the two ports, and turned OFF to open the switch 250 between the two ports.

[0254] It will be understood that the SOI FET device 100 of Figures 58 and 59 can include a single FET, or a plurality of FETs arranged in a stack. It will also be understood that each of various SOI FET devices 100 of Figures 60-68 can include a single FET, or a plurality of FETs arranged in a stack.

[0255] Figure 60 shows an example of how two SPST switches (e.g., similar to the examples of Figures 58, 59) having one or more features as described herein can be utilized to form a switch assembly 255 having a single-pole-double-throw (SPDT) configuration. Figure 61 shows, in a SPDT representation, that the switch assembly 255 of Figure 60 can be utilized in an antenna switch configuration 265. It will be understood that one or more features of the present disclosure can also be utilized in switching applications other than antenna switching application.

[0256] It is noted that in various switching configuration examples of Figures 58-68, switchable shunt paths are not shown for simplified views of the switching configurations. Accordingly, it will be understood that some or all of switchable paths in such switching configurations may or may not have associated with them switchable shunt paths (e.g., similar to the examples of Figures 29, 30 and 33-37).

[0257] Referring to the examples of Figures 60 and 61, it is noted that such examples are similar to the examples described herein in reference to Figures 29, 30 and 33-37. In some embodiments, the single pole (P) of the switch assembly 250 of Figure 60 can be utilized as an antenna node (Ant) of the antenna switch 265, and the first and

second throws (T1, T2) of the switch assembly 255 of Figure 60 can be utilized as TRx1 and TRx2 nodes, respectively, of the antenna switch 265. Although each of the TRx1 and TRx2 nodes is indicated as providing transmit (Tx) and receive (Rx) functionalities, it will be understood that each of such nodes can be configured to provide either or both of such Tx and Rx functionalities.

[0258] In the examples of Figures 60 and 61, the SPDT functionality is shown to be provided by two SPST switches 100a, 100b, with the first SPST switch 100a providing a first switchable path between the pole P (Ant in Figure 61) and the first throw T1 (TRx1 in Figure 61), and the second SPST switch 100b providing a second switchable path between the pole P (Ant in Figure 61) and the second throw T2 (TRx2 in Figure 61). Accordingly, selective coupling of the pole (Ant) with either of the first throw T1 (TRx1) and the second throw T2 (TRx2) can be achieved by selective switching operations of the first and second SPST switches. For example, if a connection is desired between the pole (Ant) and the first throw T1 (TRx1), the first SPST switch 100a can be closed, and the second SPST switch 100b can be opened. Similarly, and as depicted in the example state in Figures 60 and 61, if a connection is desired between the pole (Ant) and the second throw T2 (TRx2), the first SPST switch 100a can be opened, and the second SPST switch 100b can be closed.

[0259] In the foregoing switching examples of Figures 60 and 61, a single TRx path is connected to the antenna (Ant) node in a given switch configuration. It will be understood that in some applications (e.g., carrier-aggregation applications), more than one TRx paths may be connected to the same antenna node. Thus, in the context of the foregoing switching configuration involving a plurality of SPST switches, more than one of such SPST switches can be closed to thereby connect their respective throws (TRx nodes) to the same pole (Ant).

[0260] Figure 62 shows an example of how three SPST switches (e.g., similar to the examples of Figures 58, 59) having one or more features as described herein can be utilized to form a switch assembly 255 having a single-pole-triple-throw (SP3T) configuration. Figure 63 shows, in a SP3T representation, that the switch assembly 255 of Figure 62 can be utilized in an antenna switch configuration 265. It will be understood that

one or more features of the present disclosure can also be utilized in switching applications other than antenna switching application.

[0261] Referring to the examples of Figures 62 and 63, it is noted that the SP3T configuration can be an extension of the SPDT configuration of Figures 60 and 61. For example, the single pole (P) of the switch assembly 255 of Figure 62 can be utilized as an antenna node (Ant) of the antenna switch 265, and the first, second and third throws (T1, T2, T3) of the switch assembly 255 of Figure 62 can be utilized as TRx1, TRx2 and TRx3 nodes, respectively, of the antenna switch 265. Although each of the TRx1, TRx2 and TRx3 nodes is indicated as providing transmit (Tx) and receive (Rx) functionalities, it will be understood that each of such nodes can be configured to provide either or both of such Tx and Rx functionalities.

[0262] In the examples of Figures 62 and 63, the SP3T functionality is shown to be provided by three SPST switches 100a, 100b, 100c, with the first SPST switch 100a providing a first switchable path between the pole P (Ant in Figure 63) and the first throw T1 (TRx1 in Figure 63), the second SPST switch 100b providing a second switchable path between the pole P (Ant in Figure 63) and the second throw T2 (TRx2 in Figure 63), and the third SPST switch 100c providing a third switchable path between the pole P (Ant in Figure 63) and the third throw T3 (TRx3 in Figure 63). Accordingly, selective coupling of the pole (Ant) with one of the first throw T1 (TRx1), the second throw T2 (TRx2), and the third throw T3 (TRx3) can be achieved by selective switching operations of the first, second and third SPST switches. For example, if a connection is desired between the pole (Ant) and the first throw T1 (TRx1), the first SPST switch 100a can be closed, and each of the second and third SPST switches 100b, 100c can be opened. If a connection is desired between the pole (Ant) and the second throw T2 (TRx2), the second SPST switch 100b can be closed, and each of the first and third SPST switches 100a, 100c can be opened. Similarly, and as depicted in the example state in Figures 62 and 63, if a connection is desired between the pole (Ant) and the third throw T3 (TRx3), each of the first and second SPST switches 100a, 100b can be opened, and the third SPST switch 100c can be closed.

[0263] In the foregoing switching examples of Figures 62 and 63, a single TRx path is connected to the antenna (Ant) node in a given switch configuration. It will be understood that in some applications (e.g., carrier-aggregation applications), more than one

TRx paths may be connected to the same antenna node. Thus, in the context of the foregoing switching configuration involving a plurality of SPST switches, more than one of such SPST switches can be closed to thereby connect their respective throws (TRx nodes) to the same pole (Ant).

[0264] Based on the foregoing examples of SPST, SPDT and SP3T configurations of Figures 58-63, one can see that other switching configurations involving a single pole (SP) can be implemented utilizing SOI FET devices having one or more features as described herein. Thus, it will be understood that a switch having a SPNT can be implemented utilizing one or more SOI FET devices as described herein, where the quantity N is a positive integer.

[0265] Switching configurations of Figures 60-63 are examples where a single pole (SP) is connectable to one or more of a plurality of throws to provide the foregoing SPNT functionality. Figures 64-67 show examples where more than one poles can be provided in switching configurations. Figures 64 and 65 show examples related to a double-pole-double-throw (DPDT) switching configuration that can utilize a plurality of SOI FET devices having one or more features as described herein. Similarly, Figures 66 and 67 show examples related to a triple-pole-triple-throw (3P3T) switching configuration that can utilize a plurality of SOI FET devices having one or more features as described herein.

[0266] It will be understood that a switching configuration utilizing a plurality of SOI FET devices having one or more features as described herein can include more than three poles. Further, it is noted that in the examples of Figures 64-67, the number of throws (e.g., 2 in Figures 64 and 65, and 3 in Figures 66 and 67) are depicted as being the same as the corresponding number of poles for convenience. However, it will be understood that the number of throws may be different than the number of poles.

[0267] Figure 64 shows an example of how four SPST switches (e.g., similar to the examples of Figures 58, 59) having one or more features as described herein can be utilized to form a switch assembly 255 having a DPDT configuration. Figure 65 shows, in a DPDT representation, that the switch assembly 255 of Figure 64 can be utilized in an antenna switch configuration 265. It will be understood that one or more features of the present disclosure can also be utilized in switching applications other than antenna switching application.

[0268] In the examples of Figures 64 and 65, the DPDT functionality is shown to be provided by four SPST switches 100a, 100b, 100c, 100d. The first SPST switch 100a is shown to provide a switchable path between a first pole P1 (Ant1 in Figure 65) and a first throw T1 (TRx1 in Figure 65), the second SPST switch 100b is shown to provide a switchable path between a second pole P2 (Ant2 in Figure 65) and the first throw T1 (TRx1 in Figure 65), the third SPST switch 100c is shown to provide a switchable path between the first pole P1 (Ant1 in Figure 65) and a second throw T2 (TRx2 in Figure 65), and the fourth SPST switch 100d is shown to provide a switchable path between the second pole P2 (Ant2 in Figure 65) and the second throw T2 (TRx2 in Figure 65). Accordingly, selective coupling between one or more of the poles (antenna nodes) with one or more of the throws (TRx nodes) can be achieved by selective switching operations of the four SPST switches 100a, 100b, 100c, 100d. Examples of such switching operations are described herein in greater detail.

[0269] Figure 66 shows an example of how nine SPST switches (e.g., similar to the examples of Figures 58, 59) having one or more features as described herein can be utilized to form a switch assembly 255 having a 3P3T configuration. Figure 67 shows, in a 3P3T representation, that the switch assembly 255 of Figure 66 can be utilized in an antenna switch configuration 265. It will be understood that one or more features of the present disclosure can also be utilized in switching applications other than antenna switching application.

[0270] Referring to the examples of Figures 66 and 67, it is noted that the 3P3T configuration can be an extension of the DPDT configuration of Figures 64 and 65. For example, a third pole (P3) can be utilized as a third antenna node (Ant3), and a third throw (T3) can be utilized as a third TRx node (TRx3). Connectivity associated with such third pole and third throw can be implemented similar to the examples of Figures 64 and 65.

[0271] In the examples of Figures 66 and 67, the 3P3T functionality is shown to be provided by nine SPST switches 100a-100i. Such nine SPST switches can provide switchable paths as listed in Table 1.

Table 1

SPST switch	Pole	Throw
100a	P1	T1
100b	P2	T1
100c	P3	T1
100d	P1	T2
100e	P2	T2
100f	P3	T2
100g	P1	T3
100h	P2	T3
100i	P3	T3

Based on the example of Figures 66 and 67, and Table 1, one can see that selective coupling between one or more of the poles (antenna nodes) with one or more of the throws (TRx nodes) can be achieved by selective switching operations of the nine SPST switches 100a-100i.

[0272] In many applications, switching configurations having a plurality of poles and a plurality of throws can provide increased flexibility in how RF signals can be routed therethrough. Figures 68A-68E show examples of how a DPDT switching configuration such as the examples of Figures 64 and 65 can be operated to provide different signal routing functionalities. It will be understood that similar control schemes can also be implemented for other switching configurations, such as the 3P3T examples of Figures 66 and 67.

[0273] In some wireless front-end architectures, two antennas can be provided, and such antennas can operate with two channels, with each channel being configured for either or both of Tx and Rx operations. For the purpose of description, it will be assumed that each channel is configured for both Tx and Rx operations (TRx). However, it will be understood that each channel does not necessarily need to have such TRx functionality. For example, one channel can be configured for TRx operations, while the other channel can be configured for Rx operation. Other configurations are also possible.

[0274] In the foregoing front-end architectures, there may be relatively simple switching states including a first state and a second state. In the first state, the first TRx channel (associated with the node TRx1) can operate with the first antenna (associated with the node Ant1), and the second TRx channel (associated with the node TRx2) can operate with the second antenna (associated with the node Ant2). In the second state,

connections between the antenna nodes and the TRx nodes can be swapped from the first state. Accordingly, the first TRx channel (associated with the node TRx1) can operate with the second antenna (associated with the node Ant2), and the second TRx channel (associated with the node TRx2) can operate with the first antenna (associated with the node Ant1).

[0275] In some embodiments, such two states of the DPDT switching configuration can be controlled by a one-bit logic scheme, as shown in the example logic states in Table 2.

Table 2

State	Control logic	TRx1-Ant1 connection	TRx1-Ant2 connection	TRx2-Ant1 connection	TRx2-Ant2 connection
1	0	Yes	No	No	Yes
2	1	No	Yes	Yes	No

[0276] The first state (State 1) of the example of Table 2 is depicted in Figure 68A as 271a, where the TRx1-Ant1 connection is indicated as path 275a, and the TRx2-Ant2 connection is indicated as path 277a. A control signal, representative of the control logic of Table 2, provided to the assembly (273) of the four SPST switches (100a, 100b, 100c, 100d) is collectively indicated as Vc(s). Similarly, the second state (State 2) of the example of Table 2 is depicted in Figure 68B as 271b, where the TRx1-Ant2 connection is indicated as path 277b, and the TRx2-Ant1 connection is indicated as path 275b.

[0277] In some front-end architectures having a DPDT switching configuration, it may be desirable to have additional switching states. For example, it may be desirable to have only one path active among the two TRx channels and the two antennas. In another example, it may be desirable to disable all signal paths through the DPDT switch. Examples of 3-bit control logic that can be utilized to achieve such examples switching states are listed in Table 3.

Table 3

State	Control logic (Vc1, Vc2, Vc3)	TRx1-Ant1 connection	TRx1-Ant2 connection	TRx2-Ant1 connection	TRx2-Ant2 connection
1	0, 0, 0	No	No	No	No
2	0, 0, 1	Yes	No	No	Yes
3	0, 1, 0	Yes	No	No	No
4	0, 1, 1	No	Yes	Yes	No
5	1, 0, 0	No	Yes	No	No

[0278] The first state (State 1) of the example of Table 3 is depicted in Figure 68E as 271e, where all of the TRx-Ant paths are disconnected. A control signal indicated as Vc(s) in Figure 68E and as listed in Table 3 can be provided to the assembly (272) of the four SPST switches (100a, 100b, 100c, 100d) to effectuate such a switching state.

[0279] The second state (State 2) of the example of Table 3 is depicted in Figure 68A as 271a, where the TRx1-Ant1 connection is indicated as path 275a, and the TRx2-Ant2 connection is indicated as path 277a. A control signal indicated as Vc(s) in Figure 68A and as listed in Table 3 can be provided to the assembly (273) of the four SPST switches (100a, 100b, 100c, 100d) to effectuate such a switching state.

[0280] The third state (State 3) of the example of Table 3 is depicted in Figure 68C as 271c, where the TRx1-Ant1 connection is indicated as path 275c, and all other paths are disconnected. A control signal indicated as Vc(s) in Figure 68C and as listed in Table 3 can be provided to the assembly (273) of the four SPST switches (100a, 100b, 100c, 100d) to effectuate such a switching state.

[0281] The fourth state (State 4) of the example of Table 3 is depicted in Figure 68B as 271b, where the TRx1-Ant2 connection is indicated as path 277b, and the TRx2-Ant1 connection is indicated as path 275b. A control signal indicated as Vc(s) in Figure 68B and as listed in Table 3 can be provided to the assembly (273) of the four SPST switches (100a, 100b, 100c, 100d) to effectuate such a switching state.

[0282] The fifth state (State 5) of the example of Table 3 is depicted in Figure 68D as 270d, where the TRx1-Ant2 connection is indicated as path 277d, and all other paths are disconnected. A control signal indicated as Vc(s) in Figure 68D and as listed in Table 3 can be provided to the assembly (273) of the four SPST switches (100a, 100b, 100c, 100d) to effectuate such a switching state.

[0283] As one can see, other switching configurations can also be implemented with the DPDT switch of Figures 68A-68E. It will also be understood that other switches such as 3P3T of Figures 66 and 67 can be controlled by control logic in a similar manner.

Cavity and Trench/Opening Formation

[0284] Various characteristics of substrates or other components of RF devices can contribute to non-linearity in performance. As an example, characteristics in silicon and silicon-on-insulator (SOI) technologies that can lead to degradation in performance may include substrate resistivity and/or dielectric permittivity of the substrate. Such characteristics may be particularly problematic when dealing with relatively high-frequency and radio frequency (RF) applications that utilize silicon and/or SOI technologies. Specifically, the resistivity and permittivity of the substrate are factors that can affect losses in the device. Increasing the resistivity and lowering the permittivity of the substrate may help lower such signal losses of devices. Furthermore, selectively increasing the resistivity and lowering the dielectric permittivity between circuit elements of a device may also improve the isolation and linearity of the device.

[0285] The losses described above can lead to non-linearity that can negatively impact performance in a number of ways. For example, certain components of an SOI or other type of semiconductor structure may be susceptible to cross-talk with neighboring electrical components laterally and/or vertically through semiconductor substrate or other layer/component. In certain embodiments, SOI and/or other types of semiconductor devices may include contacts for electrically connecting to passive elements, such as inductors, capacitors, or the like, which may generally have performance factor, or Q value, characteristics that provide a measurement of their efficiency. Maximizing the Q value can be achieved through minimizing both the resistance of the passive device (e.g., inductor) as well as the energy loss into the substrate and surrounding dielectric material when energized. The use of low dielectric constant (i.e., low-k) materials in the construction of planar inductor coils may be used to at least partially decrease the radio frequency (RF) energy lost into the surrounding material, thus improving the inductor Q value, especially at relatively high frequencies. In certain embodiments, relatively highly-engineered substrates, rather than traditional bulk substrate in layer-transfer processes, may be implemented to at least partially reduce parasitic bulk capacitance and/or improve active device linearity.

[0286] The formation of cavities and/or openings in semiconductor device structures may also be used in semiconductor processing to replace at least some of the material surrounding inductors, laterally and/or vertically, with air, dielectric or vacuum, which may exhibit substantially low k value characteristics, thereby potentially reducing RF loss when such cavities/openings are strategically placed around or near certain circuit elements; cavities may improve both passive and active device performance. The terms “cavity” and “opening” are used herein according to their broad and ordinary meanings and may refer to any space (e.g., three-dimensional space), via, or region that includes air, dielectric, or other material or vacuum contained within one or more physical barriers; generally, a “cavity” may not have semiconductor substrate or dielectric disposed therein, at least in a region characterized as the “cavity.” Cavities and/or openings may be referred to herein as silicon-on-nothing (SON) structures. The term “trench” is also used herein according to its broad and ordinary meaning, and may be used to describe a recess, cut-out, opening, cavity, concavity, or the like, and may be used substantially interchangeably herein with the terms opening and/or cavity in certain contexts and in connection with certain embodiments.

[0287] Cavities and/or openings may be formed at the wafer-level or at the die level, using various approaches. For example, disclosed herein are devices and methods associated with the creation of cavities and/or openings nearby critical passive elements by creating them above and/or underneath such elements. Certain embodiments disclosed provide for the formation of backside via SON structures and methods of fabricating the same.

[0288] Backside via technology can be used to increase the resistivity and lower the permittivity of substrates. By selectively utilizing backside via technology on silicon and SOI-based devices, the substrate resistivity can be increased and the permittivity can be lowered on circuits and discrete elements in circuits. Various methods may be implemented for integrating backside via technology into silicon and SOI-based devices. For example, some embodiments involve a SOI wafer device that has a through-wafer via opening area directly underneath at least a portion of a device that contains passive components that are desired to be isolated. Such a device may be created in part by starting with a front-side substantially completed silicon or SOI wafer, wherein the wafer is first thinned, after which

the backside of the wafer may be patterned in order to create an opening in, for example, photoresist in the area where a backside isolation/opening is desired. The silicon in the photoresist opening may then be selectively etched to the backside of the oxide (BOX) layer of the SOI device using any suitable techniques (e.g., wet etching with potassium hydroxide or tetramethyl ammonium hydroxide, etc.). The opening may then be filled using one or more materials, such as a thin polysilicon layer followed by a low K dielectric.

[0289] In certain embodiments, the performance of the device may be varied through the use of different shapes/geometry with respect to the openings, different fill materials, and/or different fill material thicknesses. The opening/via structures described in the various embodiments disclosed herein may be positioned under and/or over a passive area of a device. Additionally or alternatively, openings can be selectively fabricated under and/or over active areas of circuits and devices, between active areas, between active and passive areas, or otherwise positioned. Vias/openings may also be formed in a variety of shapes and patterns on devices and circuits to optimize performance and/or mechanical strength.

[0290] Figure 69A shows a process 3700 that can be implemented to form one or more dielectric-filled openings in an SOI device or structure having one or more features as described herein. The embodiment shown in Figure 69A may provide for dielectric-filled opening creation under one or more passive (or active) elements of an SOI device structure. Figure 69B shows examples of various stages of the fabrication processes of Figure 69A. By creating backside openings in semiconductor devices and filling such openings with dielectric material having a dielectric constant value of approximately 2-4, or less, device performance may be improved in certain embodiments. In the examples of Figures 69A and 69B, it will be understood that the various blocks, or stages, may or may not be performed in the example sequences illustrated. Furthermore, various of the illustrated and described steps may be omitted in certain embodiments, or additional steps may be implemented that are not explicitly described while remaining within the scope of the present disclosure.

[0291] At block 3702, the process 3700 involves providing an SOI wafer 3801, or portion thereof, having one or more device and/or connections, as shown at stage 3801. The associated example wafer structure 3801 may correspond to certain SOI processes

disclosed above. Specifically, the structure 3801 may include one or more of a bulk substrate 3806, buried oxide (BOX) layer 3804, active semiconductor device(s) 3850, through-BOX via(s) 3808, electrical connections (e.g., metal stack) 3810, passivation layer 3814, and/or other features.

[0292] The substrate (e.g., silicon) layer 3806 may provide stability to the structure 3801, thereby allowing for formation of certain of the remaining layers that may not be formable without being associated with a mechanically-stabilizing substrate/wafer. For example, in certain embodiments, the passivation layer/area 3814 may be approximately 10 μm thick, wherein the substrate layer 3806 is substantially thicker (e.g., approximately 600 μm thick) to provide mechanical stability to the passivation layer 3814 and associated components. The passivation layer/area 3814 may comprise one or more dielectric layers. In certain contexts, an upper-most layer or portion of the one or more dielectric layers that make up the passivation layer/area 3814 may be referred to as a/the passivation layer.

[0293] In certain embodiments, wherein a plurality of elements are printed on a single die/chip, it may be desirable to at least partially prevent or reduce cross-talk between such elements. For example, separate elements may cross-talk through the substrate layer 3806, where one or more components carrying RF signal(s) may capacitively couple to the substrate 3806, such that the substrate 3806 may carry such signal(s) laterally and couple to neighboring elements, possibly leading to performance degradation.

[0294] At block 3704, the process 3700 involves at least partially thinning or removing the backside substrate layer 3806. For example, as shown in structure 3803, the backside substrate 3806 may be thinned to result in a substrate layer 3811 thinner than the substrate layer 3806 shown in structure 3801. At block 3706, the process 3700 involves selectively removing a portion of the substrate 3811 to form an opening 3874, which may expose at least a portion of the oxide layer 3804. The opening 3874 may comprise a hole or trench etched in the substrate 3811, which may extend all the way through the substrate layer to the backside of the oxide layer 3804, or alternatively may extend only part of the way through the substrate 3811, or may extend all the way through the substrate, but may not expose the oxide layer 3804 due to the presence of an intermediate material, such as a nitride or dielectric layer covering at least a portion of the backside of the oxide layer 3804.

The positioning of the opening 3874 may be implemented to achieve desired RF isolation in the semiconductor die. For example, the opening 3874 may be disposed at least partially under a passive device or element, and/or an active element (e.g., the active device(s) 3850), depending on the isolation needs of the circuit. Therefore, the patterned opening 3874 may be disposed in regions where improved linearity performance is desired. To such end, the wafer 3805 may undergo photo image processing to define the desirable pattern in the substrate 3811 where the opening is desired.

[0295] The process 3700 may further involve applying a layer of dielectric material 3870 at least partially over the opening 3874 at block 3708. The dielectric layer 3870 may comprise, for example, borosilicon glass, polysilicon, silicon, or other type of material. In certain embodiments, the dielectric layer 3870 includes a relatively thin polysilicon layer followed by a low-K dielectric material. The dielectric layer 3870 may comprise polyimide in certain embodiments.

[0296] In certain embodiments, the dielectric layer 3870, or portion thereof, may be used as an attachment medium for attaching a replacement substrate (not shown) and/or to provide structural protection for the opening. The dielectric layer 3870 may be applied to the wafer backside over the opening 3874 and/or surrounding substrate 3811. The bottom surface of the dielectric layer 3870 may be substantially planar over the opening area, or may be slightly recessed in an area associated with the opening/trench 3874 as a result of surface tension, pressure, or other factor(s). The dielectric material 3870 may further serve to keep contaminants from coming in contact with certain features of the structure 3807, such as with the oxide layer 3804. In certain embodiments, the dielectric material 3870 is a spin-on dielectric application.

[0297] Certain embodiments disclosed herein provide for creation of openings/vias/trenches that are not filled with dielectric, but are instead covered to provide an air cavity in the desired region of the device. For example, a front-side completed silicon or SOI wafer may be first thinned using any suitable technology. The backside of the wafer may then be patterned so that there is an opening in the photoresist in the area where the backside opening is desired. The silicon in the photoresist opening may then be selectively etched to the oxide layer (BOX) of the SOI device using any suitable technique (e.g., wet etching with potassium hydroxide or tetramethyl ammonium hydroxide, or other

technology). An air cavity may then be created in the selected area using any suitable technique, such as by applying a laminate, b-stage or c-stage epoxy onto the backside of the wafer and then curing the material. The performance of the device can be varied through the use of different shapes/geometry for the openings, different wafer thicknesses, and/or different encapsulating materials. The opening/via/trench structures described in the various embodiments disclosed herein may be positioned under and/or over a passive area of a device. Additionally or alternatively, openings can be selectively fabricated under and/or over active areas of circuits and devices, between active areas, between active and passive areas, or otherwise positioned. Vias/openings/trenches may also be formed in a variety of shapes and patterns on devices and circuits to optimize performance and/or mechanical strength.

[0298] Figure 70 shows a process 3900 that can be implemented to form one or more cavities in an SOI device or structure having one or more features as described herein. Figure 71 shows examples of various stages/structures of the fabrication processes of Figure 70. The embodiments disclosed in Figures 70 and 71 may be implemented to provide opening creation above, beneath and/or around certain electrical element(s), such as passive element(s) of an SOI device. In the examples of Figures 70 and 71, it will be understood that the various blocks, or stages, may or may not be performed in the example sequences illustrated. Furthermore, various of the illustrated and described steps may be omitted in certain embodiments, or additional steps may be implemented that are not explicitly described while remaining within the scope of the present disclosure.

[0299] At block 3902, the process 3900 involves providing at least a portion of a SOI wafer or die having one or more devices and/or connections formed or otherwise associated therewith, as described in various embodiments above. Certain of the features illustrated in Figure 71 may be similar in certain respects to certain features illustrated in figures described above, and therefore, for simplicity, detailed description of such features may not be provided here.

[0300] The substrate layer 4006 may provide stability to the structure 4001, thereby allowing for formation of certain of the remaining layers that may not be formable without being associated with a mechanically stabilizing substrate/wafer. For example, in certain embodiments, the passivation layer/area 4014 may be approximately 10 μm thick,

wherein the substrate layer 4006 is substantially thicker (e.g., approximately 600 μm thick) to provide mechanical stability to the passivation layer 4014 and associated components. The passivation layer/area 4014 may comprise one or more dielectric layers. In certain contexts, an upper-most layer or portion of the one or more dielectric layers that make up the passivation layer/area 4014 may be referred to as a/the passivation layer. In certain embodiments, wherein a plurality of elements are printed on a single die/chip, it may be desirable to at least partially prevent or reduce cross-talk between such elements. For example, separate elements may cross-talk through the substrate layer 4006, where one or more components carrying RF signal(s) may capacitively couple to the substrate 4006, such that the substrate 4006 may carry such signal(s) laterally and couple to neighboring element(s), possibly leading to performance degradation.

[0301] At block 3904, the process 3900 involves at least partially thinning or removing the backside substrate layer 4006. For example, as shown in structure 4003, the backside substrate 4006 may be thinned to result in a substrate layer 4011 thinner than the substrate layer 4006 shown in structure 4001.

[0302] Certain embodiments disclosed herein provide for the creation of a trench or cavity in a substrate layer by patterning the substrate layer 4011 itself. For example, patterning may be done using various established photolithography techniques, or the like. At block 3906, the process 3900 involves selectively removing a portion of the substrate 4011 to form an opening or trench 4074, which may expose at least a portion of the oxide layer 4004, or alternatively may extend only part of the way through the substrate 4011, or may extend all the way through the substrate, but may not expose the oxide layer 4004 due to the presence of an intermediate material, such as a nitride or dielectric layer covering at least a portion of the backside of the oxide layer 4004. The positioning of the opening 4074 may be implemented to achieve desired RF isolation in the semiconductor die. For example, the opening 4074 may be disposed at least partially under a passive device or element, and/or an active element, depending on the isolation needs of the circuit. Therefore, the patterned opening 4074 may be disposed in regions where improved linearity performance is desired.

[0303] The process 3900 may further involve applying a cap layer 4009 at least partially over the opening 4074 at block 3908 to form a cavity 4075. The cap layer 4009

may be applied to the wafer backside on top of the opening 4074 and/or surrounding substrate 4011. In certain embodiments, the cap layer 4009 is permanently bonded to the wafer 4007 and provides structural support for the wafer. In certain embodiments, the cap layer 4009, and may comprise a tape layer, rigid structure, or other material or structure. The cap layer 4009 may advantageously comprise dielectric properties that are more electrically insulating than silicon, and may have a dielectric constant value of approximately 2-4 or less in certain embodiments. Furthermore, the cap layer 4009 may comprise a tape having markings thereon that may be used to help with laser marking, reducing edge chip-out, or for other purposes.

[0304] The cap layer 4009 may be a film or tape. For example, the layer 4009 may comprise an adhesive strip, film, structure, or the like. In certain embodiments, the layer 4009 may comprise a laminate material, which may be associated with an epoxy-type material. The layer 4009 may be less than 50 μm in thickness, such as approximately 25 μm , or less. In certain embodiments, the layer 4009 comprises a plastic or polymer film.

[0305] The cavity 4075 may have any shape and/or configuration. Furthermore, the cavity 4075 may be positioned below or adjacent to one or more active devices, such as the FET 4050. The cavity may further be positioned such that one or more active devices is at least partially disposed within, or exposed within, the cavity. Furthermore, the cavity 4075 may be positioned below or adjacent to one or more passive devices, such as an inductor. The cavity may further be positioned such that one or more passive devices is at least partially disposed within, or exposed within, the cavity.

[0306] It should be understood that the illustrated dimensions of Figure 71 are for illustrative purposes only, and the various layers and/or components of Figure 71 are not drawn to scale, and relative thicknesses and/or widths of the various layers and/or components may be substantially greater or less in implementation than shown.

[0307] While described above are processes and embodiments for patterning for cavity, trench and/or opening creation on a backside of a wafer, the description below in connection with Figures 72-75 may describe patterning for cavity and/or opening creation on a front-side of a wafer.

[0308] Figure 72 shows a process 4100 that can be implemented to form one or more electrically-isolating openings on a front side of a wafer in a device or structure having

one or more features as described herein. Figure 73 shows examples of various stages of the fabrication processes of Figure 72. In the examples of Figures 72 and 73, it will be understood that the various blocks, or stages, may or may not be performed in the example sequences illustrated. Furthermore, various illustrated and/or described steps may be omitted in certain embodiments, or additional steps may be implemented that are not explicitly described while remaining within the scope of the present disclosure. Certain of the features illustrated in Figure 73 may be similar in certain respects to certain features illustrated in figures described above, and therefore, for simplicity, detailed description of such features may not be provided here.

[0309] At block 4102, the process 4100 involves providing at least a portion of an SOI wafer having one or more devices and/or connections formed or otherwise associated therewith, as described in various embodiments above. The process 4100 may provide for creation of an opening structure above, for example, a passive element of an SOI device. An electrical element 4212, such as a passive device, for example (e.g., inductor, capacitor, etc.) may be disposed on a front side of the wafer structure 4201. In addition, a handle wafer layer 4216 may be disposed on the front side of the wafer structure 4201 at least partially above the electrical element 4212.

[0310] Certain embodiments disclosed herein provide for the creation of an opening in a substrate layer by patterning the substrate layer (e.g., the handle wafer 4216) itself. For example, patterning may be done using various established photolithography techniques, prior to bonding the original wafer to its final substrate. At block 4104, the process 4100 involves selectively removing a portion of the handle wafer 4216 to form an opening or trench 4274, which may expose at least a portion of the passivation layer 4214 and/or electrical element 4212, or alternatively may extend only part of the way through the substrate 4216, or may extend all the way through the substrate, but may not expose the passivation layer due to the presence of an intermediate material, such as a nitride or other dielectric layer covering at least a portion of the passivation layer 4214. The positioning of the opening/trench 4274 may be implemented to achieve desired RF isolation in the semiconductor die, such as over one or more passive or active devices, or may be positioned such that one or more active or passive devices are at least partially within the opening/trench 4274.

[0311] The process 4100 may further involve applying a layer of dielectric material 4270 at least partially over the opening/trench 4274 at block 4106. The dielectric layer 4270 may comprise, for example, borosilicon glass, polysilicon, silicon, or other type of material. In certain embodiments, the dielectric layer 4270 includes a relatively thin polysilicon layer followed by a low-K dielectric material. In certain embodiments, the dielectric layer 4270 may be used as an attachment medium for attaching a replacement substrate (not shown) and/or to provide structural protection for the opening. The dielectric layer 4270 may be applied to the front side of the wafer on top of the opening 4274 and/or surrounding substrate 4216.

[0312] Figure 74 shows a process 4300 that can be implemented to form one or more electrically-isolating cavities in an SOI device or structure having one or more features as described herein. Figure 75 shows examples of various stages of the fabrication processes of Figure 74. In the examples of Figures 74 and 75, it will be understood that the various blocks, or stages, may or may not be performed in the example sequences illustrated. Furthermore, various of the illustrated and/or described steps may be omitted in certain embodiments, or additional steps may be implemented that are not explicitly described while remaining within the scope of the present disclosure. Certain of the features illustrated in Figure 75 may be similar in certain respects to certain features illustrated in figures described above, and therefore, for simplicity, detailed description of such features may not be provided here.

[0313] At block 4302, the process 4300 involves providing at least a portion of an SOI wafer having one or more devices and/or connections formed or otherwise associated therewith, as described in various embodiments above. The process 4300 may provide for cavity creation above, for example, a passive element, or active element (e.g., FET 4450), of an SOI device using single-layer transfer. An electrical element 4412, such as a passive device, for example (e.g., inductor, capacitor, etc.) may be disposed on a front-side of the wafer structure 4401. In addition, a handle wafer layer 4416 may be disposed on the front side of the wafer structure 4401 at least partially above the electrical element 4412.

[0314] Certain embodiments disclosed herein provide for the creation of an opening or trench in the handle wafer layer 4416 by patterning the layer itself. For example, patterning may be done using various established photolithography techniques, such as

prior to bonding the original wafer to its final substrate. At block 4304, the process 4300 involves selectively removing a portion of the handle wafer 4416 to form an opening or trench 4474, which may expose at least a portion of the passivation layer 4414 and/or electrical element 4412. In certain embodiments, the opening/trench 4474 may extend only part of the way through the substrate 4216, or may extend all the way through the substrate, but may not expose the passivation layer 4414 due to the presence of an intermediate material, such as a nitride or other dielectric layer covering at least a portion of the passivation layer 4414. The positioning of the opening 4474 may be implemented to achieve desired RF isolation in the semiconductor die, such as over and/or above at least part of a passive or active (e.g., FET 4450) device.

[0315] The process 4300 may further involve applying a cap layer 4409 at least partially over the opening 4474 at block 4306 to form a cavity 4475. The cap layer 4409 may be applied to the front side of the wafer on top of the opening 4474 and/or surrounding substrate 4416. In certain embodiments, the cap layer 4409 is permanently bonded to the wafer 4205 and provides structural support for the wafer. In certain embodiments, the cap layer 4409 may comprise a tape layer, rigid structure, or other material or structure. The cap layer 4409 may advantageously comprise dielectric properties that are more electrically insulating than silicon, and may have a dielectric constant value of approximately 2-4 or less in certain embodiments. Furthermore, the cap layer 4409 may comprise a tape having markings thereon that may be used to help with laser marking, reducing edge chip-out, or for other purposes.

[0316] The cap layer 4409 may be a film or tape. For example, the layer 4409 may comprise an adhesive strip, film, structure, or the like. In certain embodiments, the layer 4409 may comprise a laminate material, which may be associated with an epoxy-type material. The layer 4409 may be less than 50 μm in thickness, such as approximately 25 μm , or less. In certain embodiments, the layer 4409 comprises a plastic or polymer film.

[0317] The cavity 4475 may have any shape and/or configuration. Furthermore, the cavity 4475 may be positioned below or adjacent to one or more active devices, such as the FET 4450. The cavity may further be positioned such that one or more active devices is at least partially disposed within, or exposed within, the cavity. Furthermore, the cavity 4475 may be positioned below or adjacent to one or more passive devices, such as

an inductor. The cavity may further be positioned such that one or more passive devices is at least partially disposed within, or exposed within, the cavity.

[0318] It should be understood that the illustrated dimensions of Figure 75 are for illustrative purposes only, and the various layers and/or components of Figure 75 are not drawn to scale, and relative thicknesses and/or widths of the various layers and/or components may be substantially greater or less in implementation than shown.

[0319] Figures 76A-76C show embodiments of die structures 4500A, 4500B, 4500C that include generally rectangular-shaped cavities 4575A, 4575B, 4575C. Figure 76A shows an embodiment of a die structure 4500A that includes a plurality of cavities 4575A formed in substantially geometrically alignment over at least portions of RF core and energy management (EM) core regions of the die 4500A.

[0320] Figure 76B shows an embodiment of a die wherein cavities 4575 are arranged to cover at least a portion of an RF core region of the die, while an EM core portion of the die is substantially free of cavities in at least certain regions thereof. In the embodiment of Figure 76C, cavities 4575C may be arranged in clusters (e.g., cluster 4577), which may be positioned around, or at least partially overlapping with, certain devices that are desired to be isolated to some degree.

[0321] While generally rectangular-shaped cavities are illustrated in Figures 76A-76C, it should be understood that cavities of any shape or configuration may be implemented within the scope of the present disclosure. Figures 77A-77C show embodiments of die structures 4600A, 4600B, 4600C that include generally hexagonally-shaped cavities 4675A, 4675B, 4675C. Figure 77A shows an embodiment of a die structure 4600A that includes a plurality of cavities 4675A formed in substantially geometrically alignment over at least portions of RF core and EM core regions of the die 4600A.

[0322] Figure 77B shows an embodiment of a die wherein cavities 4675 are arranged to cover at least a portion of an RF core region of the die, while an EM core portion of the die is substantially free of cavities in at least certain regions thereof. In the embodiment of Figure 77C, cavities 4675C may be arranged in clusters (e.g., cluster 4677), which may be positioned around, or at least partially overlapping with, certain devices that are desired to be isolated to some degree.

Examples of Implementations in Products

[0323] Various examples of FET-based circuits and bias/coupling configurations described herein can be implemented in a number of different ways and at different product levels. Some of such product implementations are described by way of examples.

Semiconductor Die Implementation

[0324] Figures 78A-78D schematically show non-limiting examples of such implementations on one or more semiconductor die. Figure 78A shows that in some embodiments, a switch circuit 820 and a bias/coupling circuit 850 having one or more features as described herein can be implemented on a die 800. Certain of the switch and/or bias/coupling circuitry may be designed as to be isolated by one or more cavities formed according to one or more embodiments disclosed herein. Figure 78B shows that in some embodiments, at least some of the bias/coupling circuit 850 can be implemented outside of the die 800 of Figure 78A.

[0325] Figure 78C shows that in some embodiments, a switch circuit 820 having one or more features as described herein can be implemented on a first die 800a, and a bias/coupling circuit 850 having one or more features as described herein can be implemented on a second die 800b. Figure 78D shows that in some embodiments, at least some of the bias/coupling circuit 850 can be implemented outside of the first die 800a of Figure 78C.

Packaged Module Implementation

[0326] In some embodiments, one or more die having one or more cavity features described herein can be implemented in a packaged module. An example of such a module is shown in Figures 79A (plan view) and 79B (side view). Although described in the context of both of the switch circuit and the bias/coupling circuit being on the same die (e.g., example configuration of Figure 79A), it will be understood that packaged modules can be based on other configurations.

[0327] A module 810 is shown to include a packaging substrate 812. Such a packaging substrate can be configured to receive a plurality of components, and can include, for example, a laminate substrate. The components mounted on the packaging substrate 812 can include one or more dies. In the example shown, a die 800 having a switching circuit 820 and a bias/coupling circuit is shown to be mounted on the packaging

substrate 812. The die 800 can be electrically connected to other parts of the module (and with each other where more than one die is utilized) through connections such as connection-wirebonds 816. Such connection-wirebonds can be formed between contact pads 818 formed on the die 800 and contact pads 814 formed on the packaging substrate 812. In some embodiments, one or more surface mounted devices (SMDs) 822 can be mounted on the packaging substrate 812 to facilitate various functionalities of the module 810.

[0328] In some embodiments, the packaging substrate 812 can include electrical connection paths for interconnecting the various components with each other and/or with contact pads for external connections. For example, a connection path 832 is depicted as interconnecting the example SMD 822 and the die 800. In another example, a connection path 832 is depicted as interconnecting the SMD 822 with an external-connection contact pad 834. In yet another example a connection path 832 is depicted as interconnecting the die 800 with ground-connection contact pads 836.

[0329] In some embodiments, a space above the packaging substrate 812 and the various components mounted thereon can be filled with an overmold structure 830. Such an overmold structure can provide a number of desirable functionalities, including protection for the components and wirebonds from external elements, and easier handling of the packaged module 810.

[0330] Figure 80 shows a schematic diagram of an example switching configuration that can be implemented in the module 810 described in reference to Figures 79A and 79B. In the example, the switch circuit 820 is depicted as being an SP9T switch, with the pole being connectable to an antenna and the throws being connectable to various Rx and Tx paths. Such a configuration can facilitate, for example, multi-mode multi-band operations in wireless devices.

[0331] The module 810 can further include an interface for receiving power (e.g., supply voltage VDD) and control signals to facilitate operation of the switch circuit 820 and/or the bias/coupling circuit 850. In some implementations, supply voltage and control signals can be applied to the switch circuit 820 via the bias/coupling circuit 850.

Wireless Device Implementation

[0332] In some implementations, a device and/or a circuit having one or more features described herein can be included in an RF device such as a wireless device. Such a device and/or a circuit can be implemented directly in the wireless device, in a modular form as described herein, or in some combination thereof. In some embodiments, such a wireless device can include, for example, a cellular phone, a smart-phone, a hand-held wireless device with or without phone functionality, a wireless tablet, etc.

[0333] Figure 81 schematically depicts an example wireless device 900 having one or more advantageous features described herein. In the context of various switches and various biasing/coupling configurations as described herein, a switch 920 and a bias/coupling circuit 950 can be part of a module 910. In some embodiments, such a switch module can facilitate, for example, multi-band multip-mode operation of the wireless device 900.

[0334] In the example wireless device 900, a power amplifier (PA) module 916 having a plurality of PAs can provide an amplified RF signal to the switch 920 (via a duplexer 920), and the switch 920 can route the amplified RF signal to an antenna. The PA module 916 can receive an unamplified RF signal from a transceiver 914 that can be configured and operated in known manners. The transceiver can also be configured to process received signals. The transceiver 914 is shown to interact with a baseband sub-system 910 that is configured to provide conversion between data and/or voice signals suitable for a user and RF signals suitable for the transceiver 914. The transceiver 914 is also shown to be connected to a power management component 906 that is configured to manage power for the operation of the wireless device 900. Such a power management component can also control operations of the baseband sub-system 910 and the module 810.

[0335] The baseband sub-system 910 is shown to be connected to a user interface 902 to facilitate various input and output of voice and/or data provided to and received from the user. The baseband sub-system 910 can also be connected to a memory 904 that is configured to store data and/or instructions to facilitate the operation of the wireless device, and/or to provide storage of information for the user.

[0336] In some embodiments, the duplexer 918 can allow transmit and receive operations to be performed simultaneously using a common antenna (e.g., 924). In Figure 81, received signals are shown to be routed to "Rx" paths (not shown) that can include, for example, a low-noise amplifier (LNA).

[0337] A number of other wireless device configurations can utilize one or more features described herein. For example, a wireless device does not need to be a multi-band device. In another example, a wireless device can include additional antennas such as diversity antenna, and additional connectivity features such as Wi-Fi, Bluetooth, and GPS.

General Comments

[0338] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The word "coupled", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0339] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while

processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0340] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0341] While some embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A method for fabricating a radio-frequency (RF) device, the method comprising:
 - providing a field-effect transistor (FET) formed over a an oxide layer formed on a substrate layer; and
 - removing at least a portion of the substrate layer to form an opening exposing at least a portion of a backside of the oxide layer, the opening being positioned to enhance RF performance for one or more components of the RF device.
2. The method of claim 1 further comprising thinning the substrate layer prior to said removing the at least a portion of the substrate layer.
3. The method of claim 1 further comprising covering at least a portion of the substrate layer and the opening with a covering to form a cavity.
4. The method of claim 3 wherein the covering is a laminate film.
5. The method of claim 3 wherein the covering is a plastic lid structure.
6. The method of claim 3 wherein the covering is an additional replacement substrate layer.
7. The method of claim 1 further comprising at least partially filling the opening with a dielectric filler.
8. The method of claim 7 further comprising covering at least a portion of a backside of the substrate layer with the dielectric filler to form a dielectric layer.
9. The method of claim 8 further comprising applying a replacement substrate layer to the dielectric layer to provide mechanical stability for the RF device.
10. The method of claim 1 further comprising applying a handle wafer to the RF device to provide mechanical stability for the RF device.
11. A radio-frequency (RF) device comprising:

a field-effect transistor (FET) implemented over an oxide layer;
a patterned semiconductor substrate layer on which the oxide layer is formed, the substrate layer including a backside trench defined at least in part by side wall portions of the substrate layer; and
one or more electrical connections connected to the FET.

12. The RF device of claim 11 wherein the substrate layer is a thinned substrate layer.

13. The RF device of claim 11 further comprising a replacement substrate layer disposed on a backside of the substrate layer and covering the trench to form a cavity.

14. The RF device of claim of claim 11 further comprising dielectric filler material contained within the trench.

15. The RF device of claim 14 further comprising a dielectric layer disposed on a backside of the substrate layer.

16. A wireless device comprising:
a transceiver configured to process radio-frequency (RF) signals;
an RF module in communication with the transceiver, the RF module including a switching device having a field-effect transistor (FET) implemented over an oxide layer and a patterned semiconductor substrate layer including an opening defined at least in part by a side wall of the substrate layer and a portion of a backside of the oxide layer, the switching device further including one or more electrical connections connected to the FET; and
an antenna in communication with the RF module, the antenna configured to facilitate transmitting and/or receiving of the RF signals.

17. The wireless device of claim 16 wherein the substrate layer is a thinned substrate layer.

18. The wireless device of claim 16 further comprising a replacement substrate layer disposed on a backside of the substrate layer and covering the opening to form a cavity.

19. The wireless device of claim 16 further comprising dielectric filler contained within the opening.

20. The wireless device of claim 19 further comprising a dielectric layer disposed on a backside of the substrate layer.

21. A radio-frequency (RF) module comprising:
a packaging substrate configured to receive a plurality of devices; and
a switching device mounted on the packaging substrate, the switching device including a field-effect transistor (FET) implemented over an oxide layer and a patterned semiconductor substrate layer including an opening defined at least in part by a side wall of the substrate layer and a portion of a backside of the oxide layer, the switching device further including one or more electrical connections connected to the FET.

22. The RF module of claim 21 wherein the substrate layer is a thinned substrate layer.

23. The RF module of claim 21 further comprising a replacement substrate layer disposed on a backside of the substrate layer and covering the opening to form a cavity.

24. The RF module of claim 21 further comprising dielectric filler contained within the opening.

25. The module of claim 24 further comprising a dielectric layer disposed on a backside of the substrate layer.

26. A method of fabricating a radio-frequency (RF) device comprising:
providing a field-effect transistor (FET) formed over an oxide layer;
forming one or more electrical connections to the FET;

forming one or more dielectric layers over at least a portion of the electrical connections;

electrically coupling an electrical element to the FET via the one or more electrical connections;

disposing a handle wafer layer on at least a portion of the one or more dielectric layers, the handle wafer layer being at least partially over the electrical element; and

removing at least a portion of the handle wafer layer to form an opening exposing at least a portion of the electrical element.

27. The method of claim 26 further comprising thinning the handle wafer layer prior to said removing the at least a portion of the handle wafer layer.

28. The method of claim 26 further comprising covering at least a portion of the handle wafer layer and the opening with a covering to form a cavity.

29. The method of claim 28 wherein the covering is a laminate film.

30. The method of claim 28 wherein the covering is a plastic lid structure.

31. The method of claim 28 wherein the covering is an additional replacement substrate layer.

32. The method of claim 26 further comprising at least partially filling the opening with a dielectric material.

33. The method of claim 32 further comprising covering at least a portion of the handle wafer layer with the dielectric material to form a dielectric layer.

34. The method of claim 33 further comprising applying a replacement substrate layer to the dielectric layer to provide mechanical stability for the RF device.

35. The method of claim 26 wherein the electrical element is a surface acoustic wave (SAW) device.

36. The method of claim 26 wherein the electrical element is a bulk acoustic wave (BAW) device.

37. The method of claim 26 further comprising at least partially removing the substrate layer to expose at least a portion of a backside of an oxide layer disposed between the FET and the substrate layer.

38. The method of claim 37 further comprising disposing an electrical contact structure on the backside of the oxide layer to provide electrical contact to the one or more electrical connections through a through-oxide via.

39. The method of claim 37 further comprising disposing a substrate contact layer on the backside of the oxide layer.

40. A radio-frequency (RF) device comprising:
a field-effect transistor (FET) implemented over an oxide layer;
one or more electrical connections to the FET;
one or more dielectric layers formed over at least a portion of the electrical connections;
an electrical element electrically coupled to the FET via the one or more electrical connections;
a handle wafer layer disposed on at least a portion of the one or more dielectric layers, the handle wafer layer including a topside trench defined at least in part by sidewall portions of the handle wafer layer, the trench exposing at least a portion of the electrical element.

41. The RF device of claim 40 further comprising a covering that covers at least a portion of the handle wafer layer and the trench to form a cavity.

42. The RF device of claim 41 wherein the covering is a laminate film.

43. The RF device of claim 40 further comprising a dielectric material that at least partially fills the trench.

44. The RF device of claim 43 further comprising a replacement substrate layer applied to the dielectric material to provide mechanical stability for the RF device.

45. A wireless device comprising:

a transceiver configured to process radio-frequency (RF) signals;

an RF module in communication with the transceiver, the RF module including a switching device having a field-effect transistor (FET) implemented over an oxide layer, one or more electrical connections to the FET, one or more dielectric layers formed over at least a portion of the electrical connections, an electrical element electrically coupled to the FET via the one or more electrical connections, a handle wafer layer disposed on at least a portion of the one or more dielectric layers, the handle wafer layer including a topside trench defined at least in part by sidewall portions of the handle wafer layer, the trench exposing at least a portion of the electrical element; and

an antenna in communication with the RF module, the antenna configured to facilitate transmitting and/or receiving of the RF signals.

46. The wireless device of claim 45 wherein the RF module further includes a covering that covers at least a portion of the handle wafer layer and the trench to form a cavity.

47. The wireless device of claim 45 wherein the RF module further comprises a dielectric material that at least partially fills the trench.

48. A method of fabricating a radio-frequency (RF) device comprising:

providing a field-effect transistor (FET) formed over an oxide layer;

forming one or more electrical connections to the FET;

forming one or more dielectric layers over at least a portion of the electrical connections;

disposing a handle wafer layer on at least a portion of the one or more dielectric layers; and

removing at least a portion of the handle wafer layer to form an opening at least partially above the FET.

49. The method of claim 48 further comprising thinning the handle wafer layer prior to said removing the at least a portion of the handle wafer layer.

50. The method of claim 48 further comprising covering at least a portion of the handle wafer layer and the opening with a covering to form a cavity.

51. The method of claim 50 wherein the covering is a laminate film.

52. The method of claim 50 wherein the covering is a plastic lid structure.

53. The method of claim 50 wherein the covering is an additional replacement substrate layer.

54. The method of claim 48 further comprising at least partially filling the opening with a dielectric material.

55. The method of claim 54 further comprising covering at least a portion of the handle wafer layer with the dielectric material to form a dielectric layer.

56. The method of claim 55 further comprising applying a replacement substrate layer to the dielectric layer to provide mechanical stability for the RF device.

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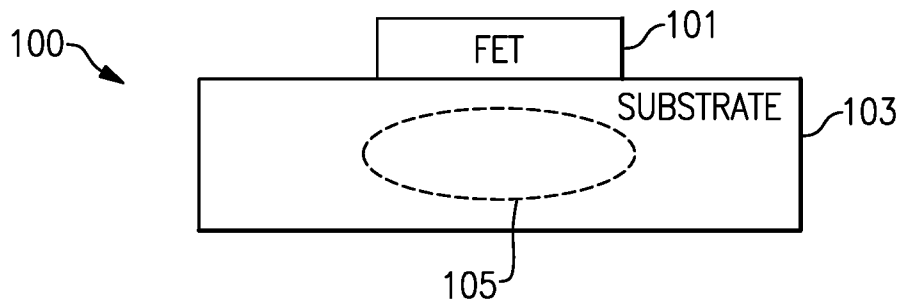


FIG. 1

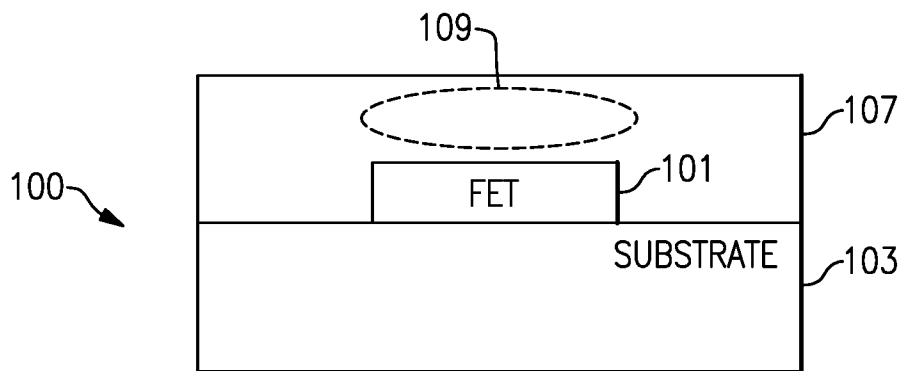


FIG. 2

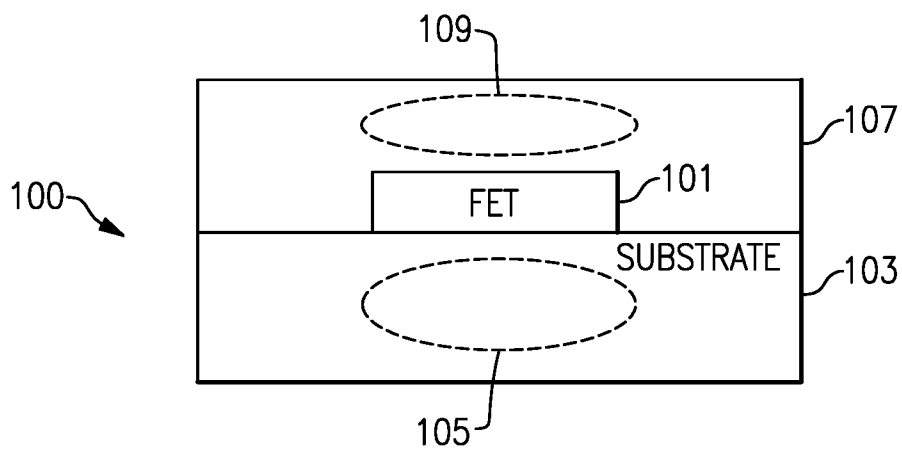


FIG. 3

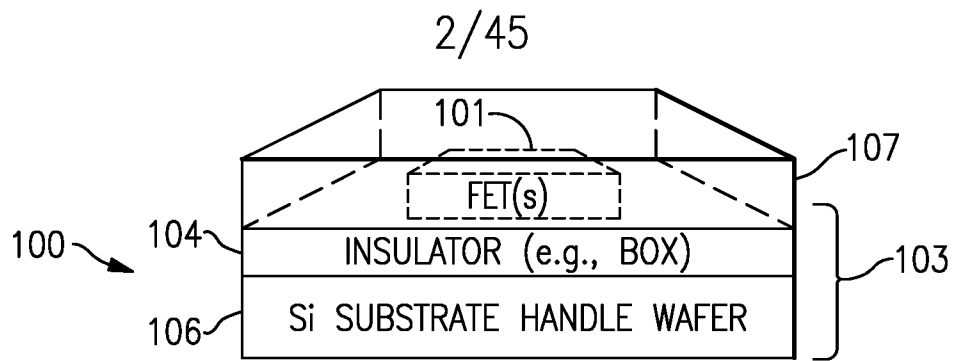


FIG. 4

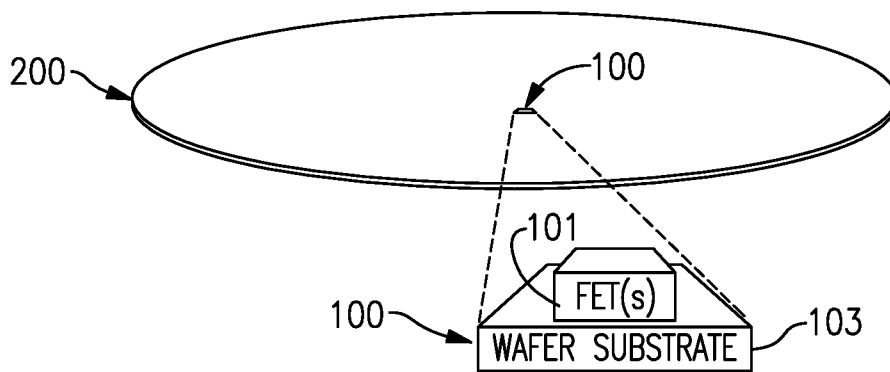


FIG. 5

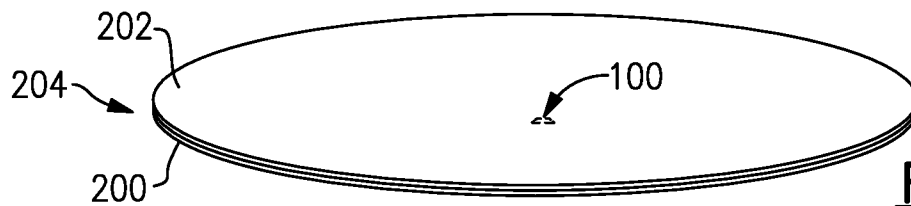


FIG. 6A

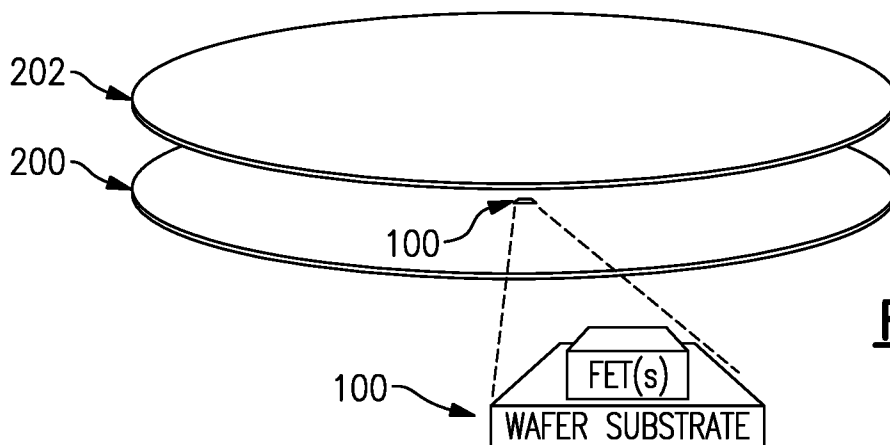


FIG. 6B

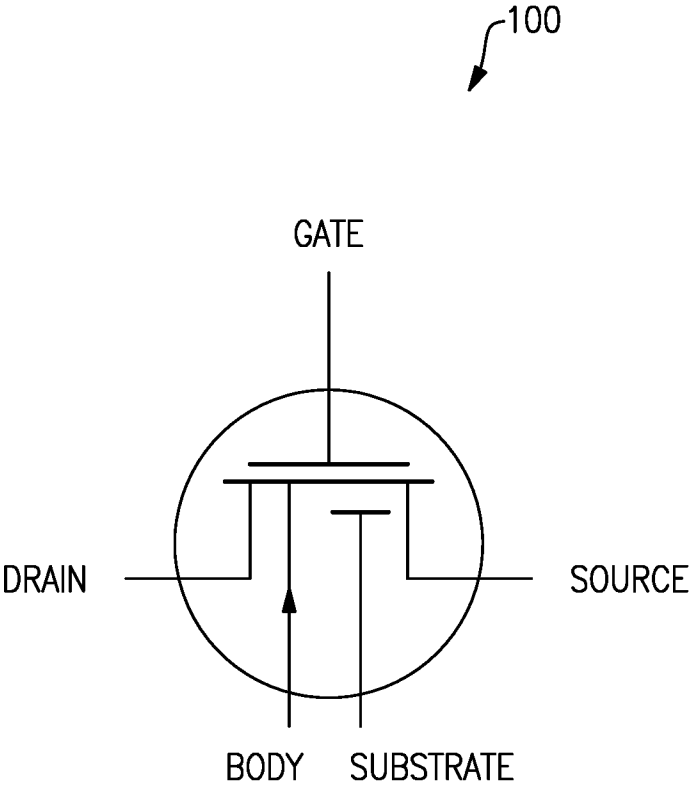


FIG.7

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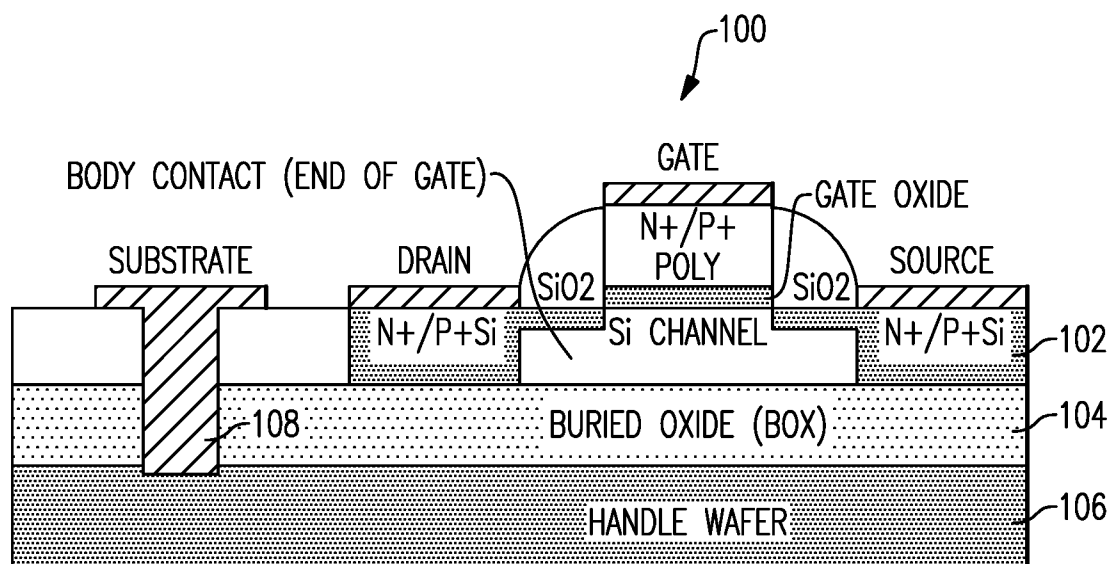


FIG. 8A

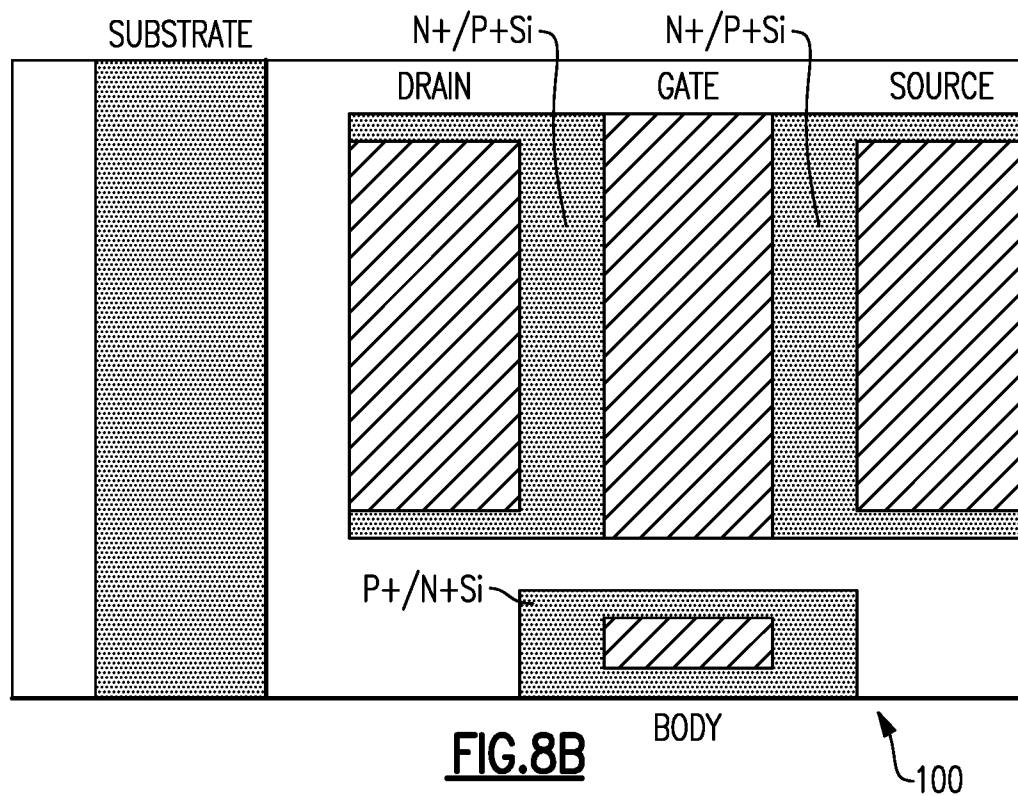


FIG. 8B

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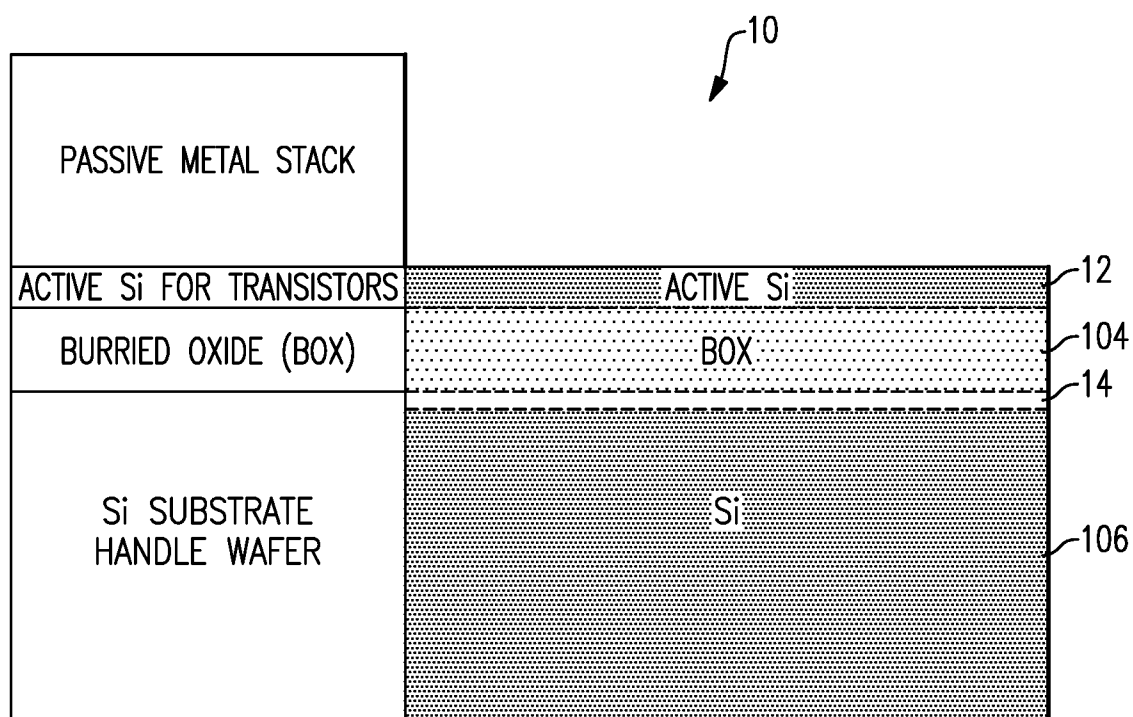


FIG. 9

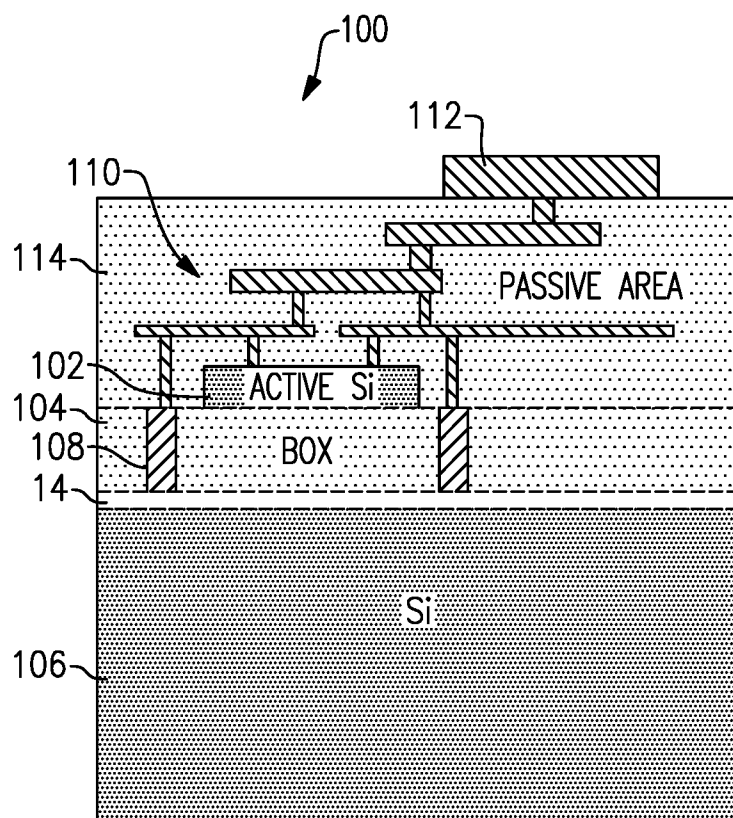


FIG. 10

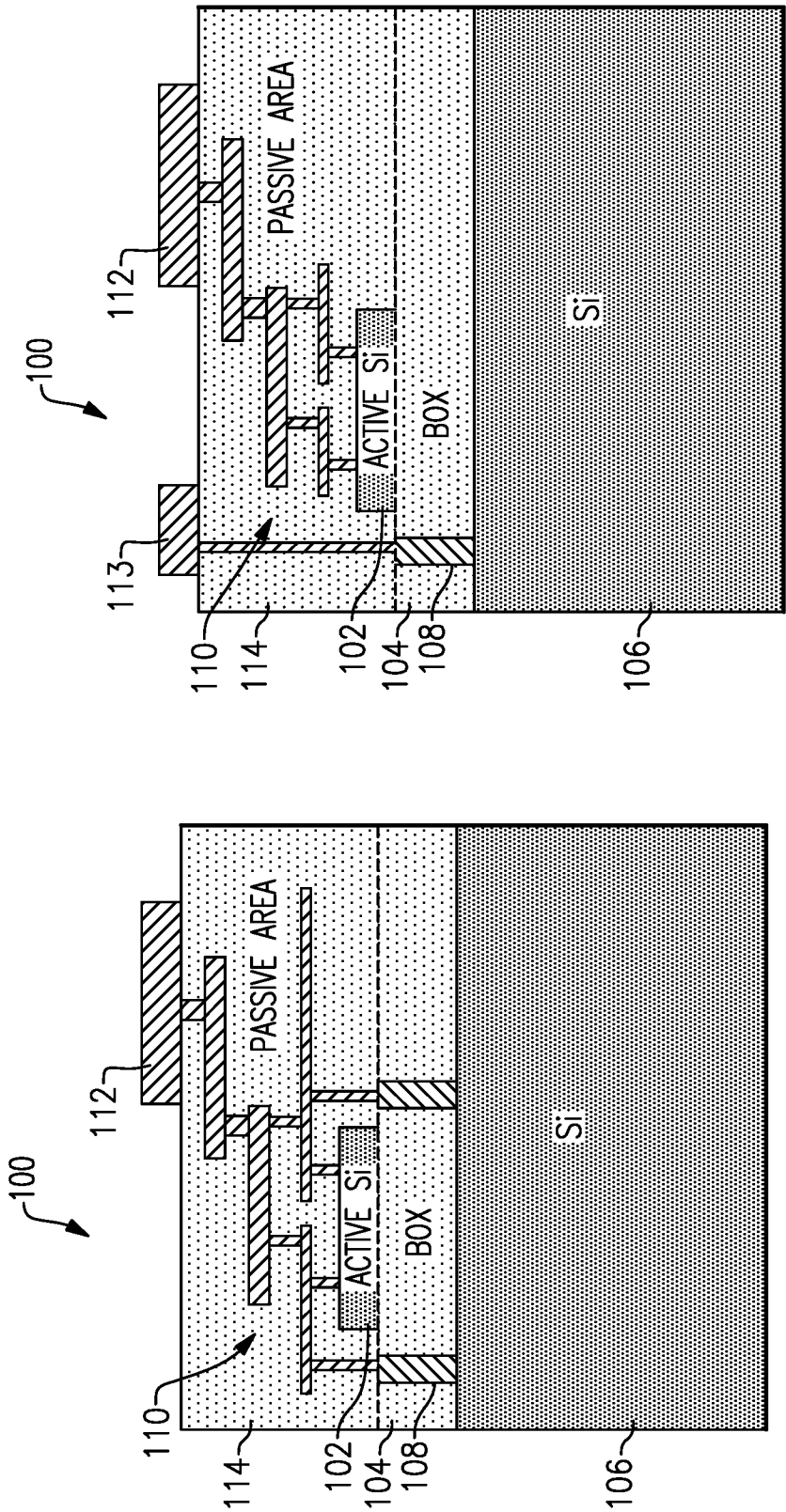


FIG.11

FIG.12

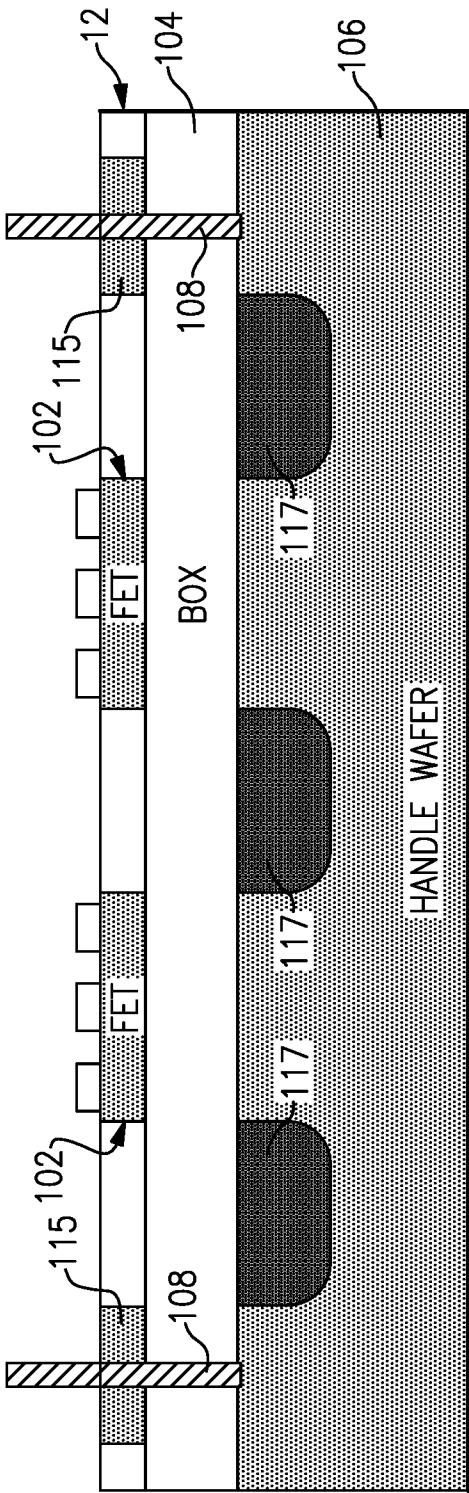


FIG.13

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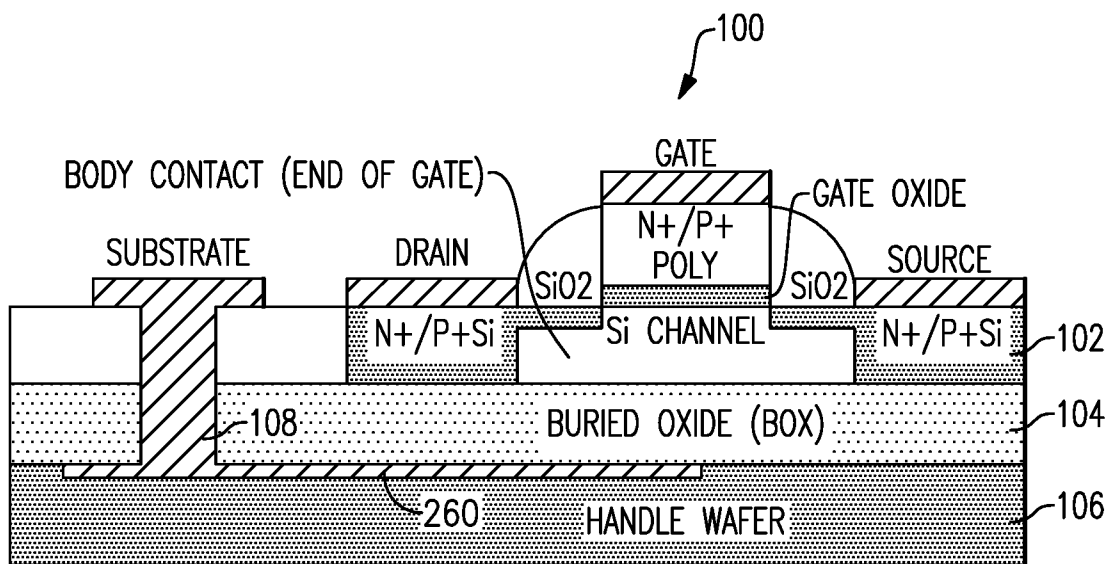


FIG. 14A

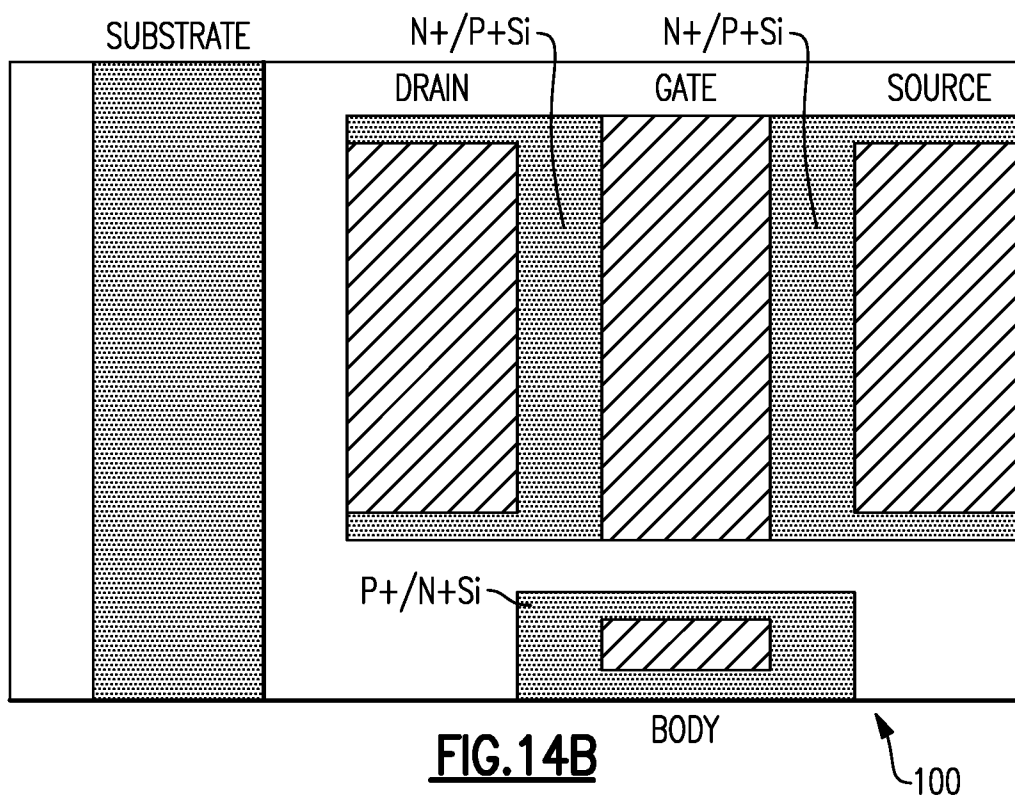


FIG. 14B

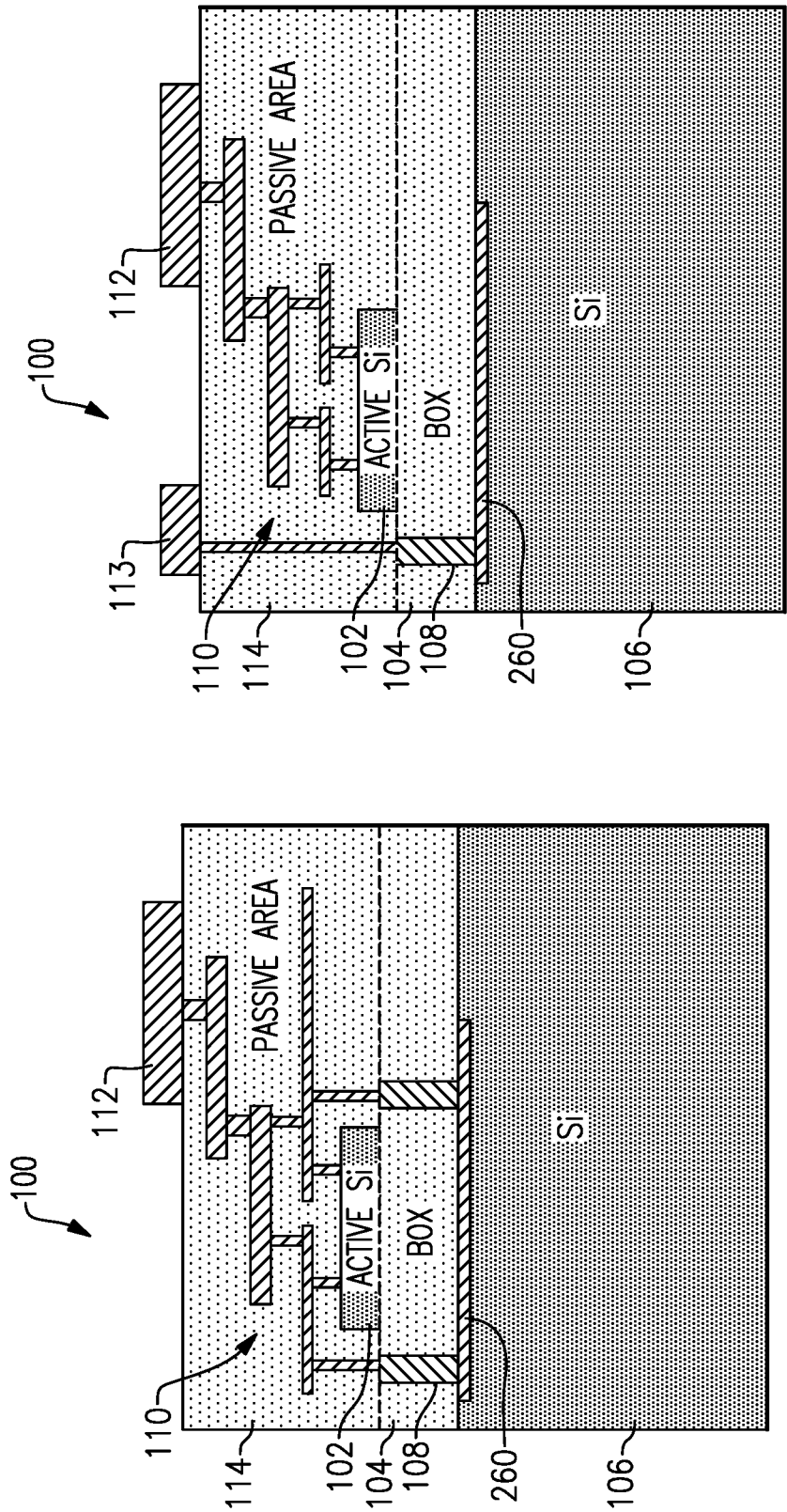


FIG.15

FIG.16

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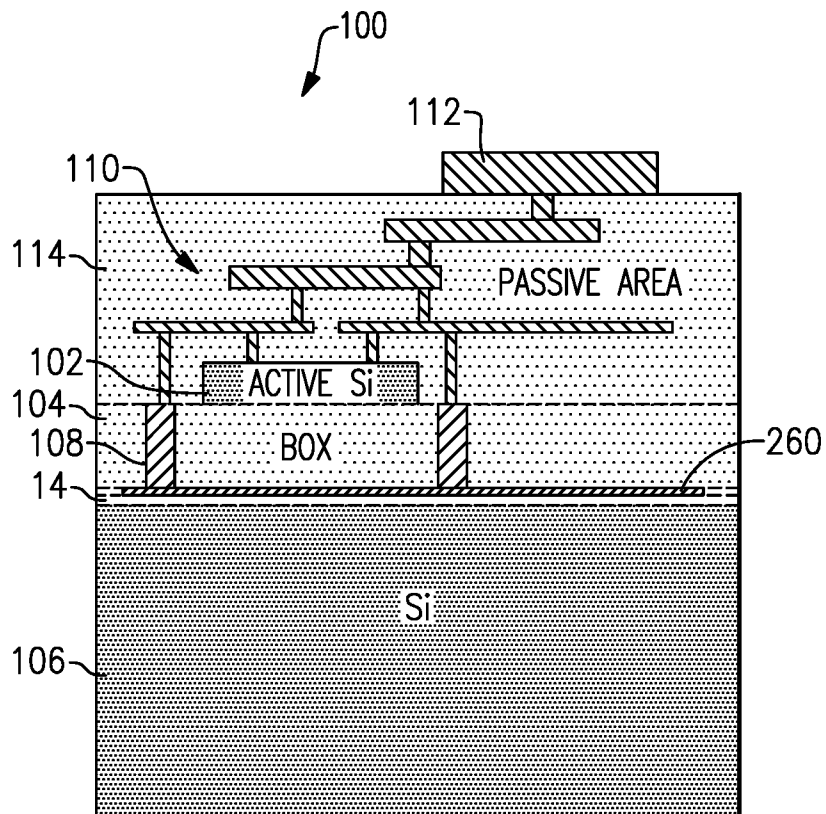


FIG.17

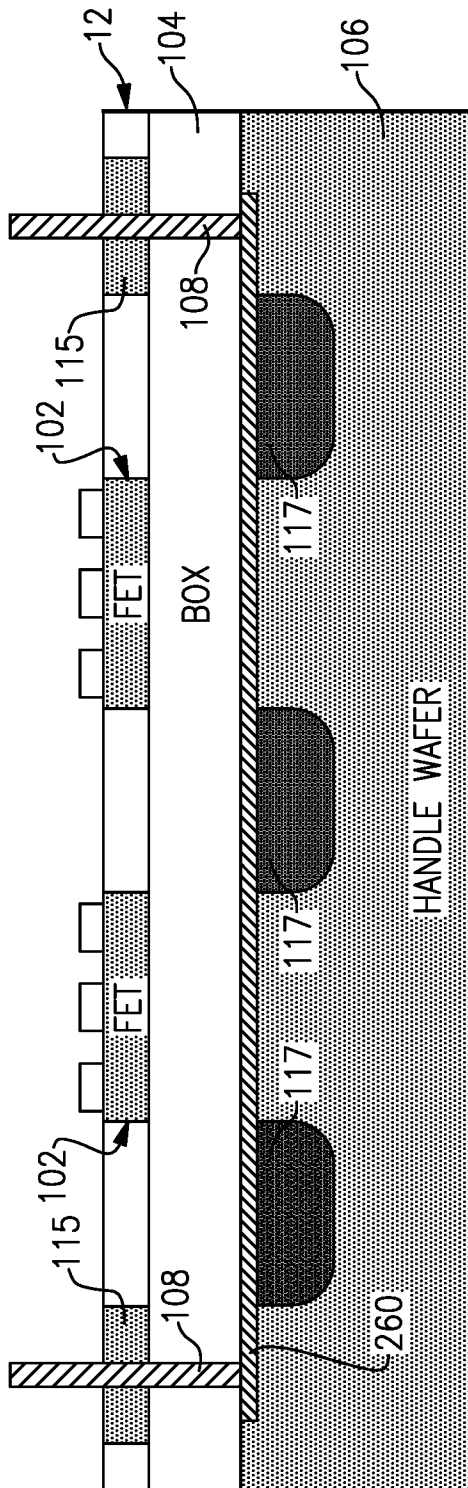


FIG. 18

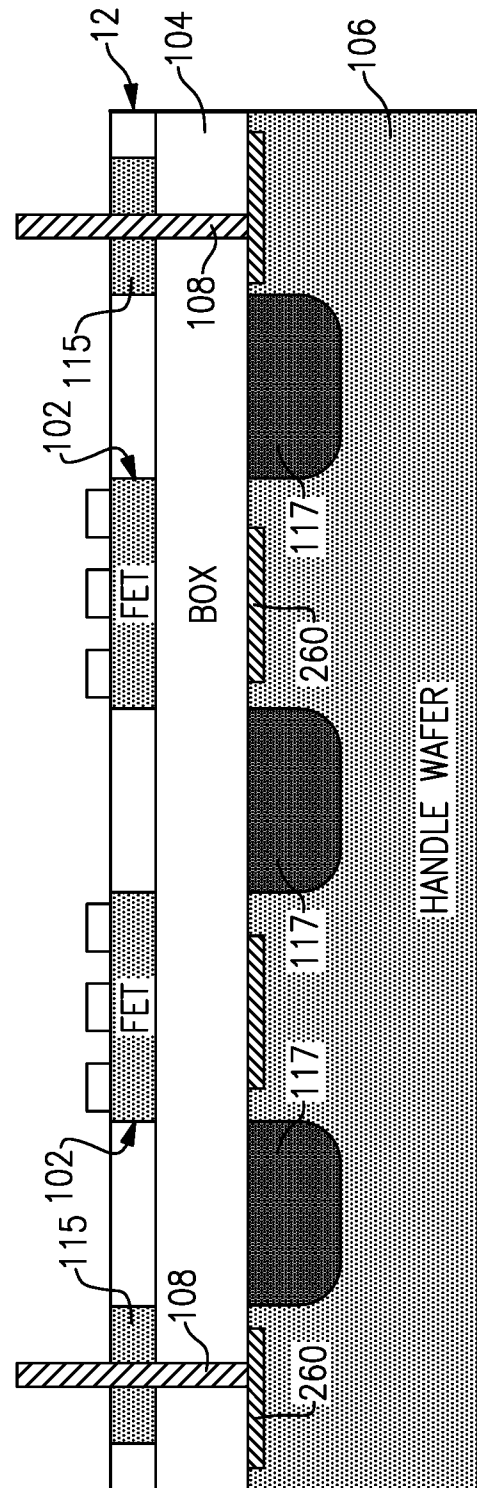
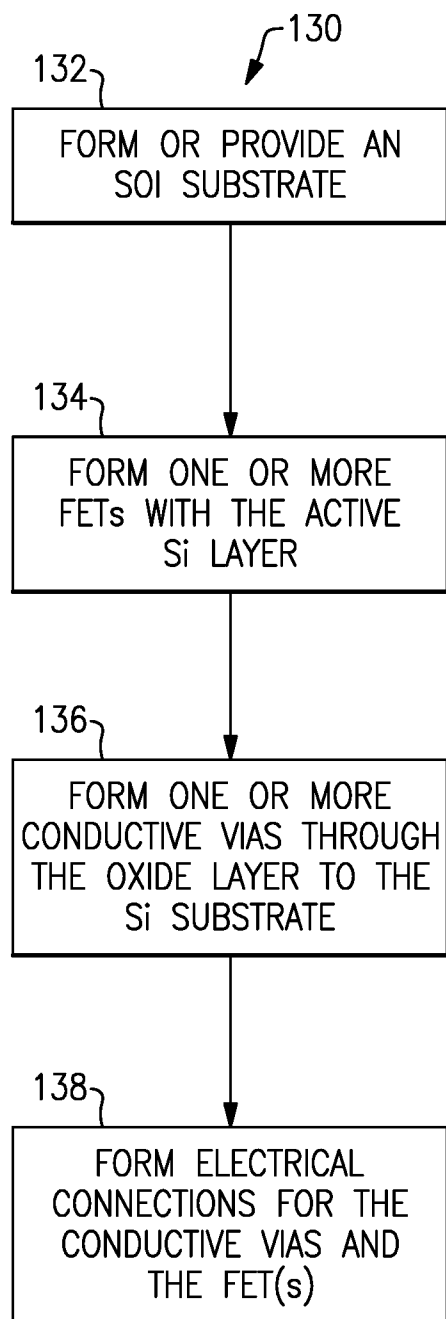
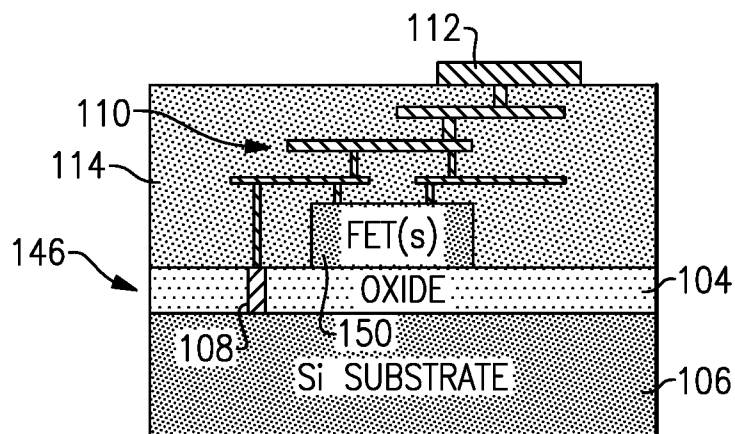
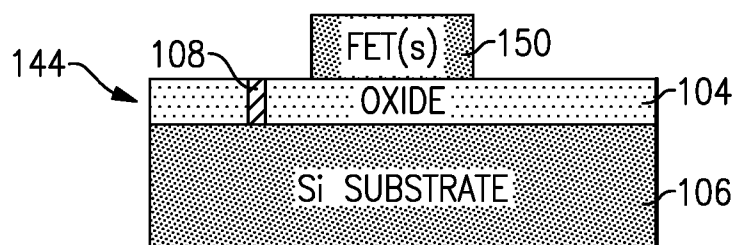
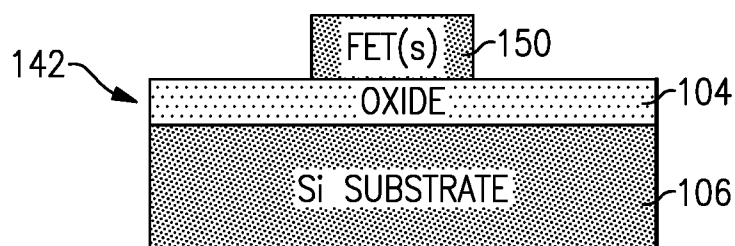
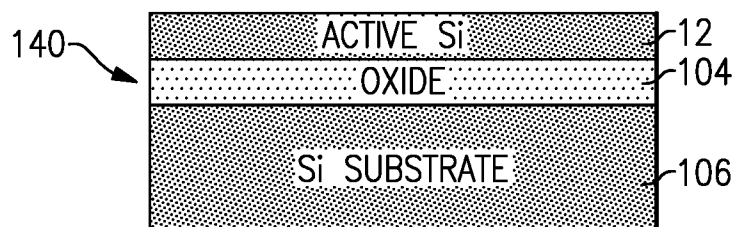
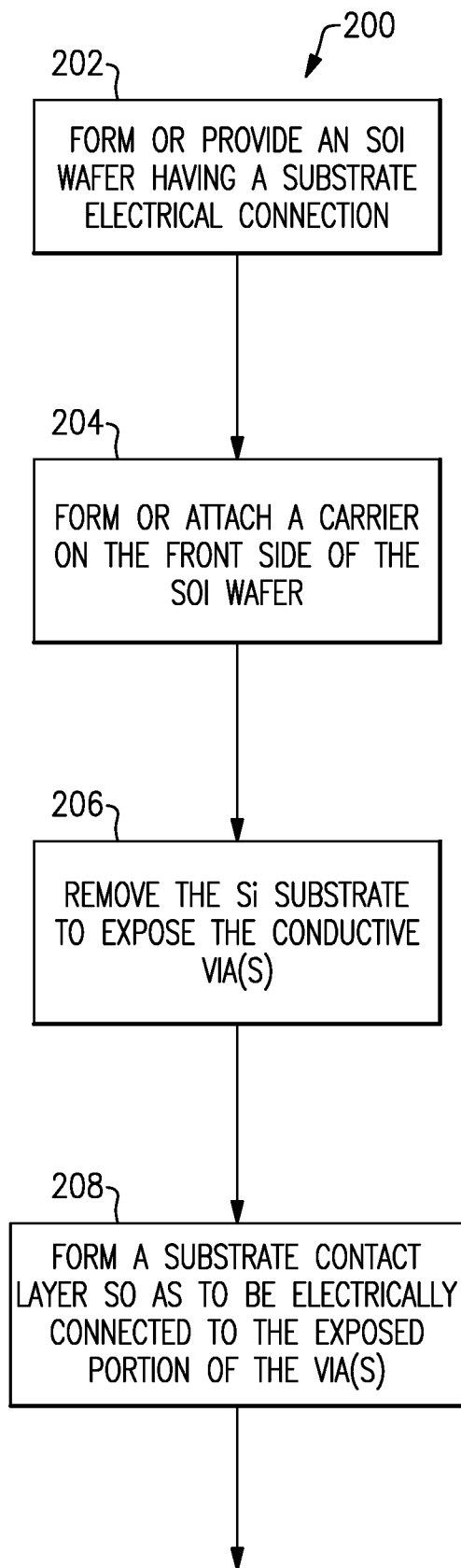
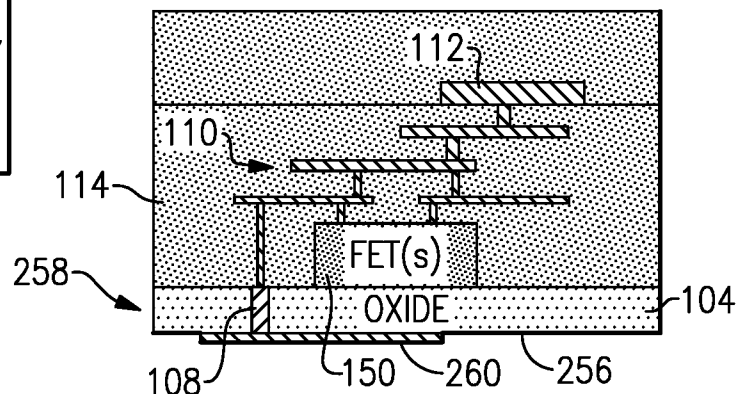
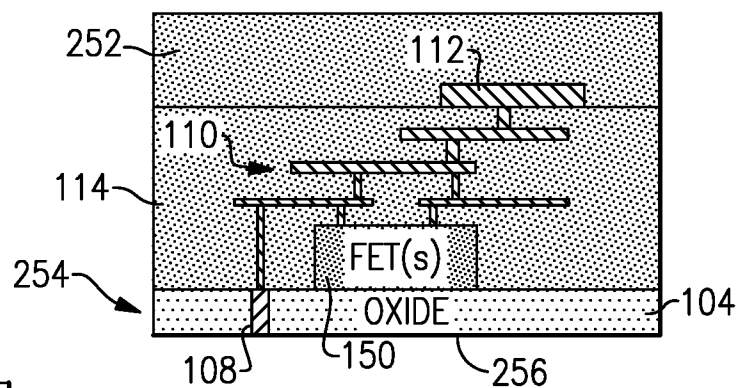
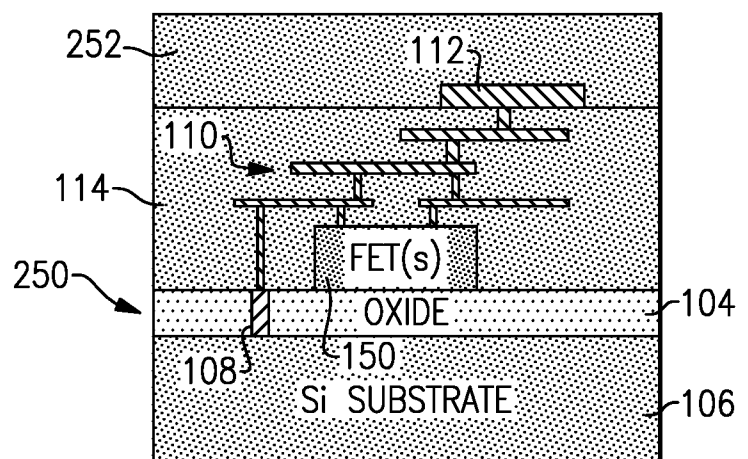
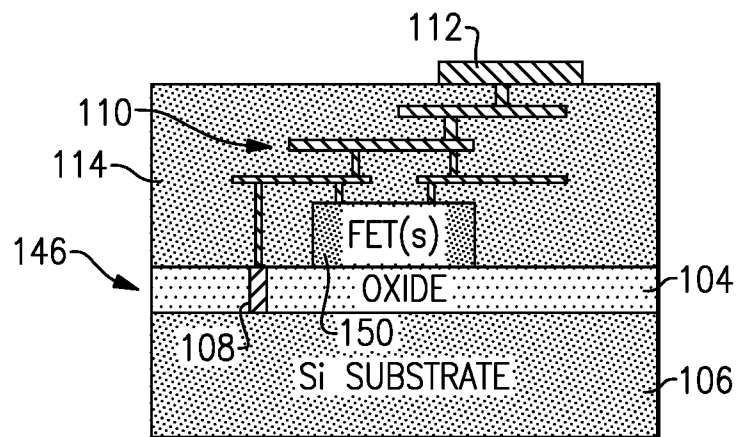


FIG. 19

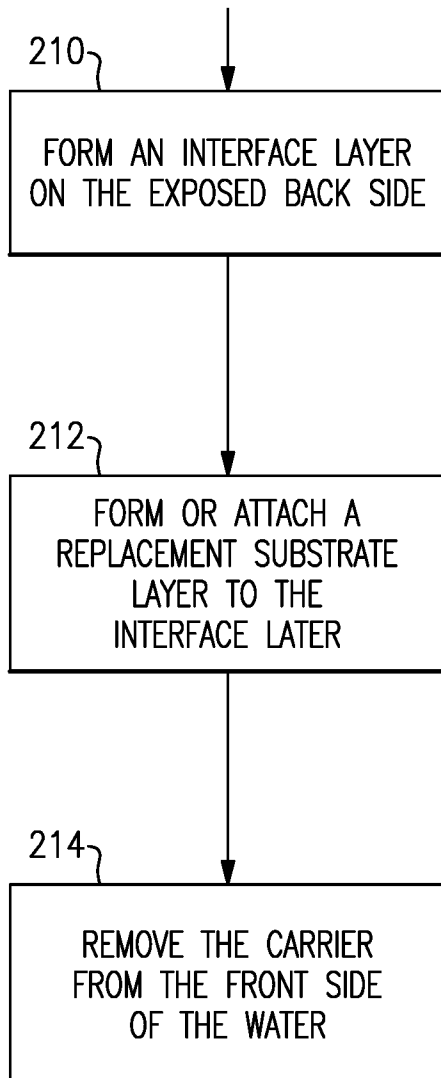
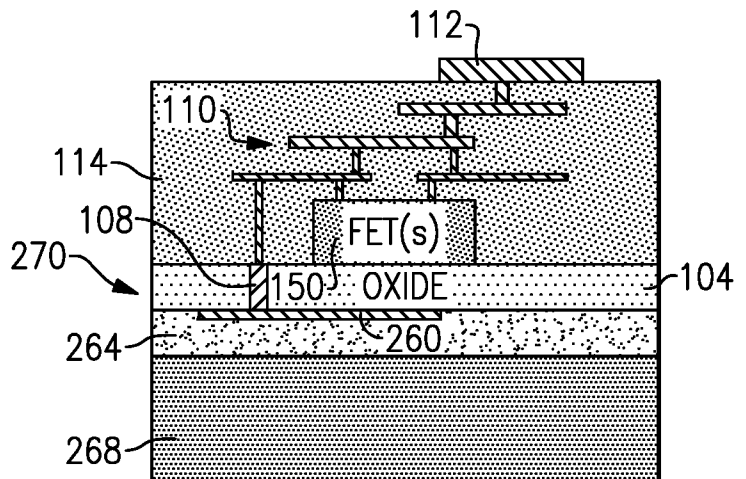
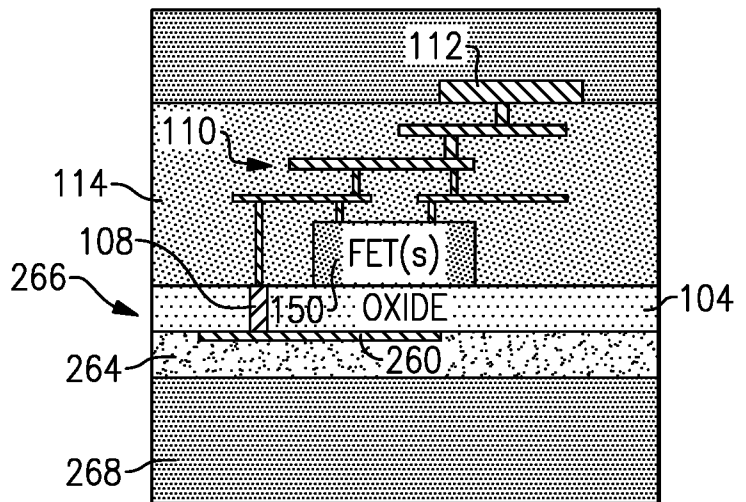
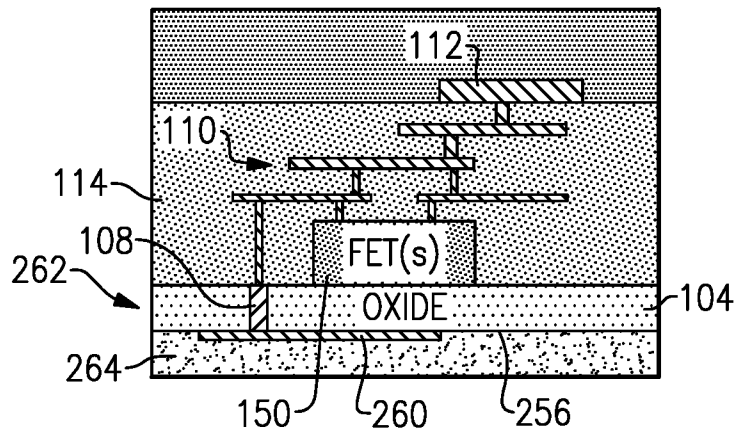
12/45

**FIG.20****FIG.21**

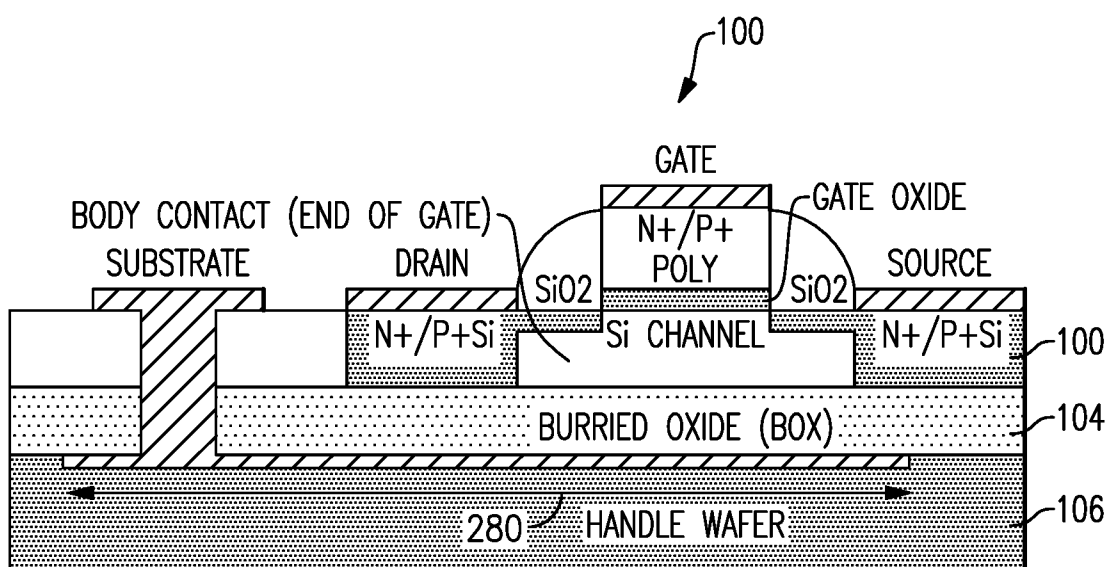
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**FIG.22A****FIG.23A**

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**FIG.22B****FIG.23B**

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**FIG.24**

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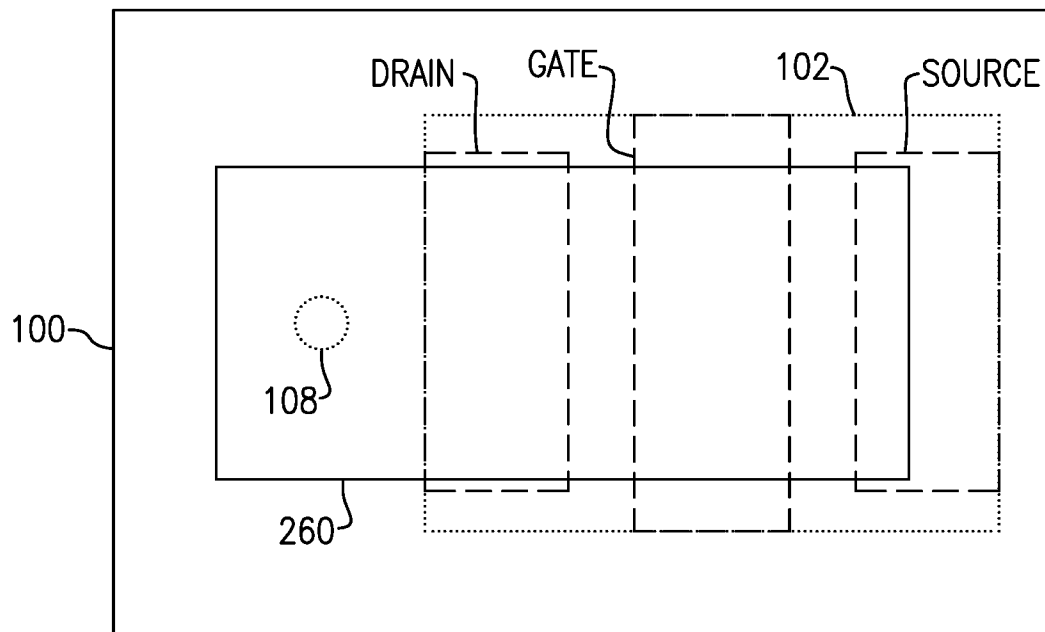


FIG. 25A

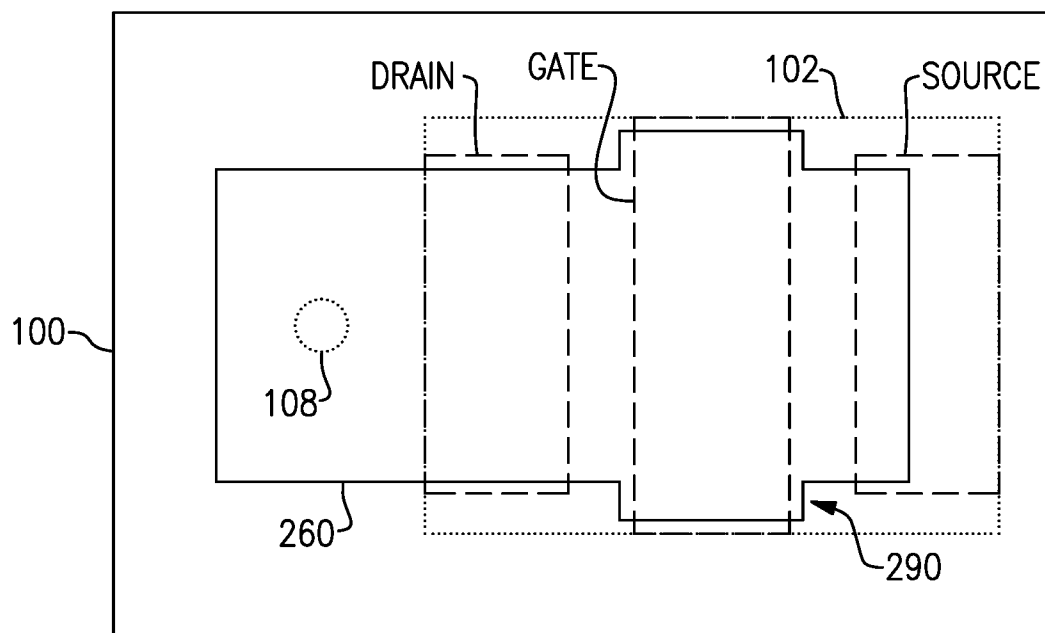


FIG. 25B

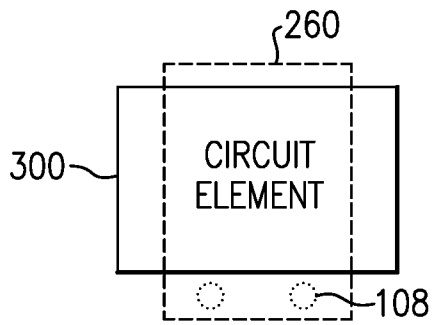


FIG. 26A

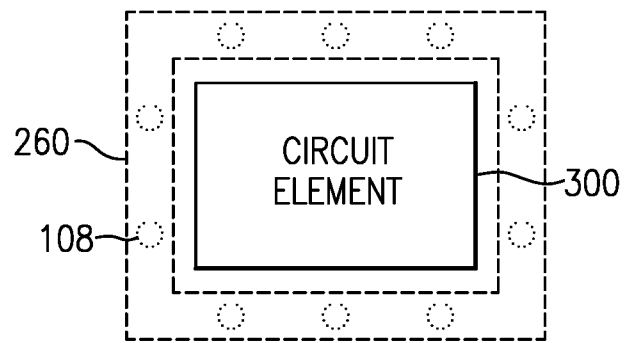


FIG. 26B

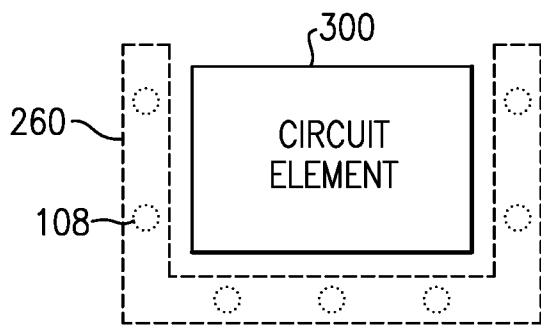


FIG. 26C

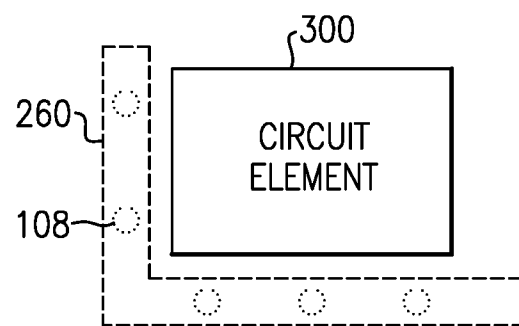


FIG. 26D

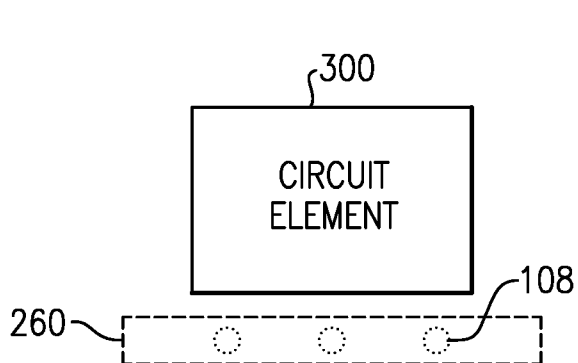


FIG. 26E

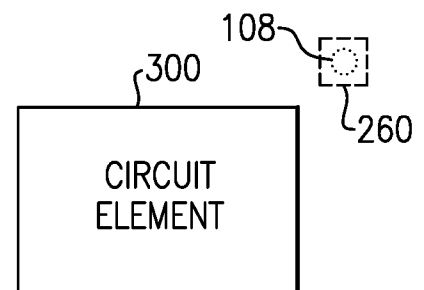


FIG. 26F

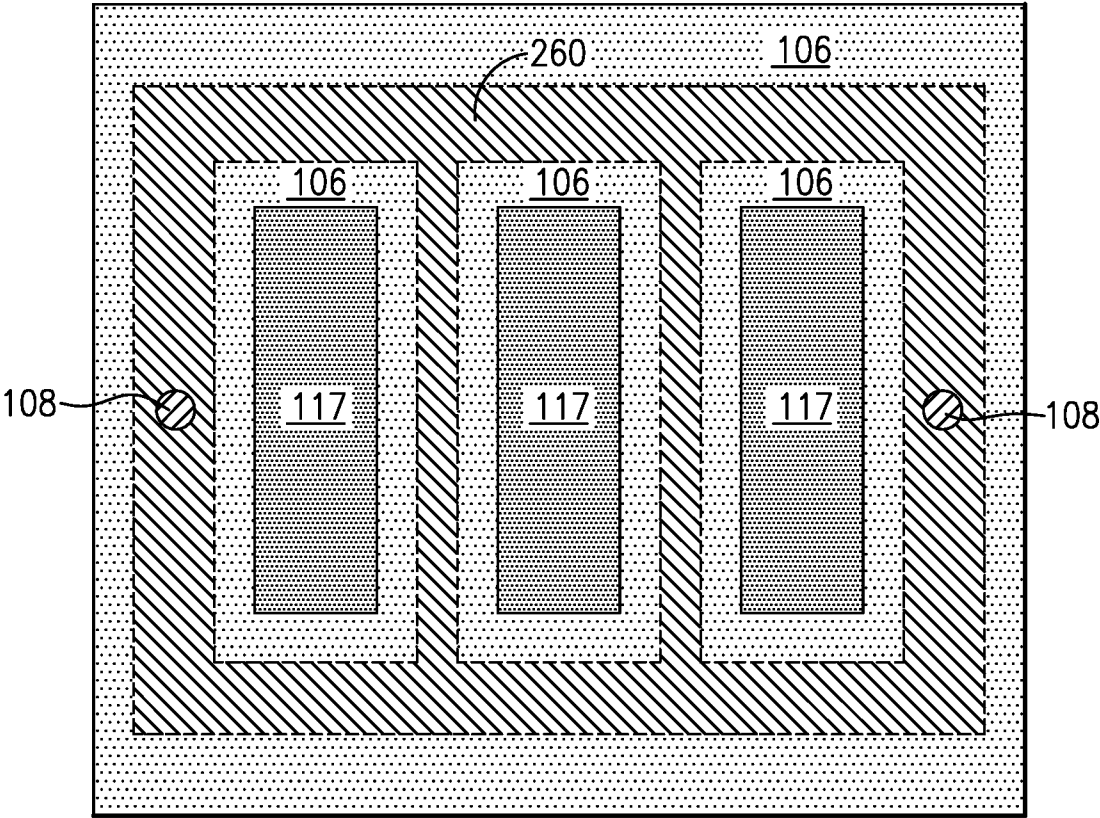
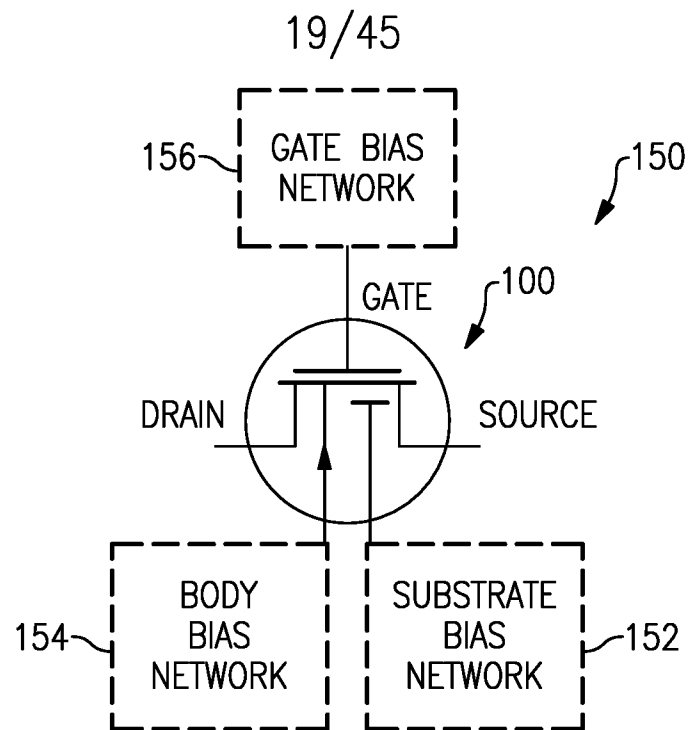
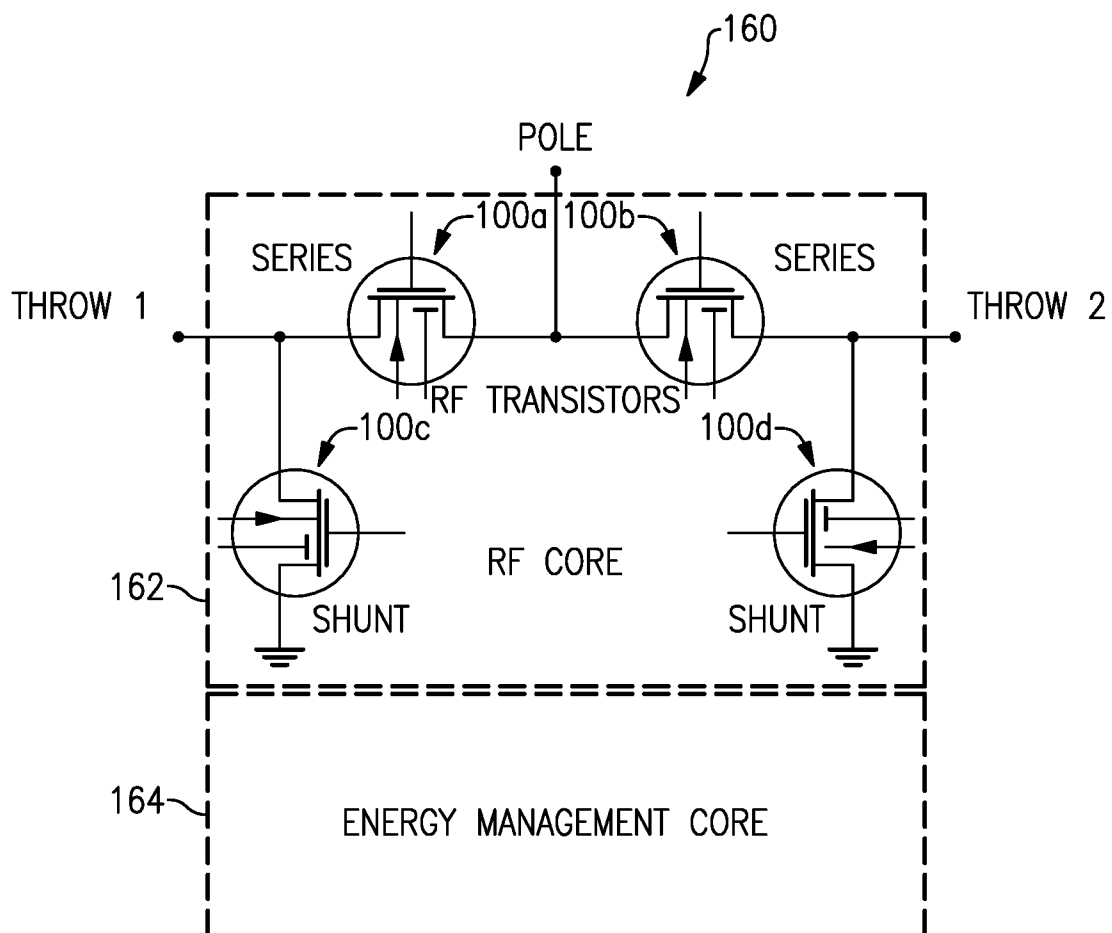


FIG.27

**FIG.28****FIG.29**

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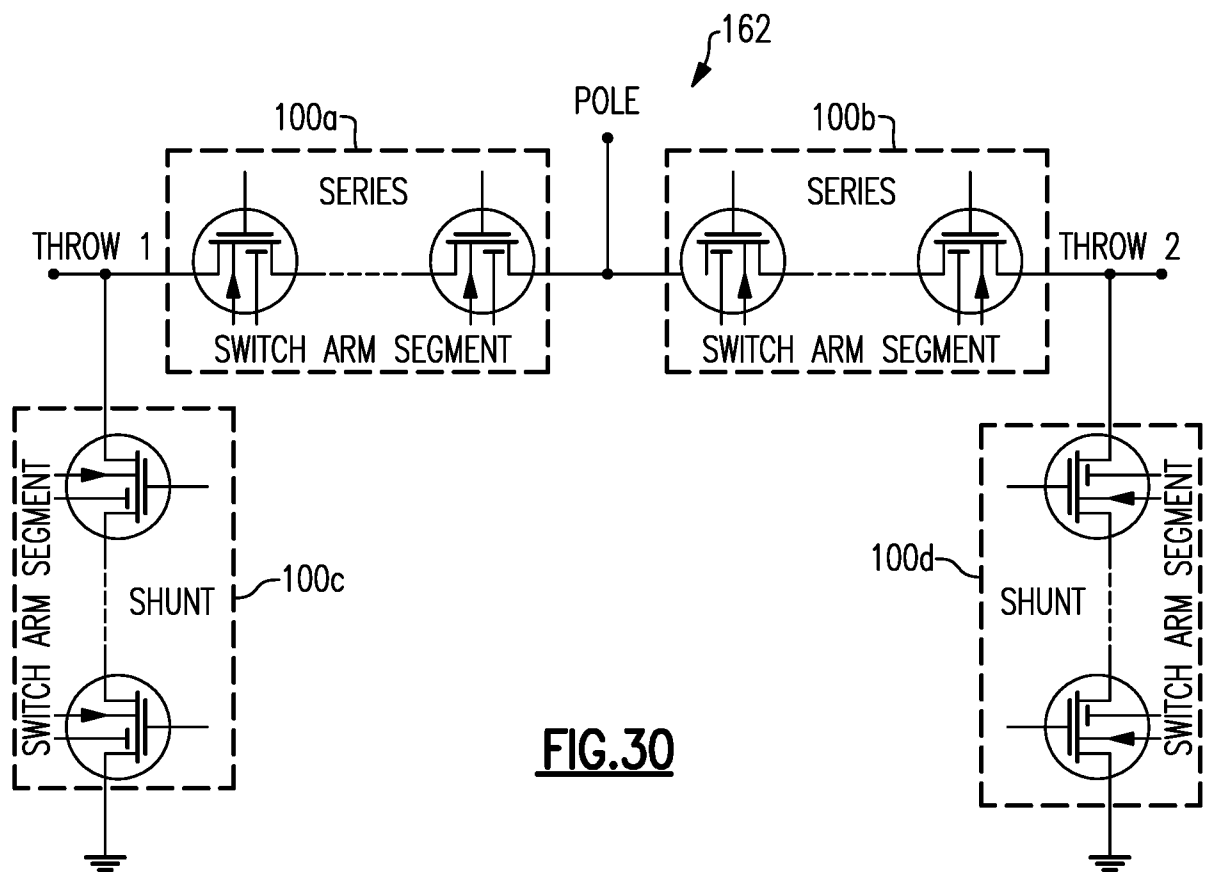


FIG.30

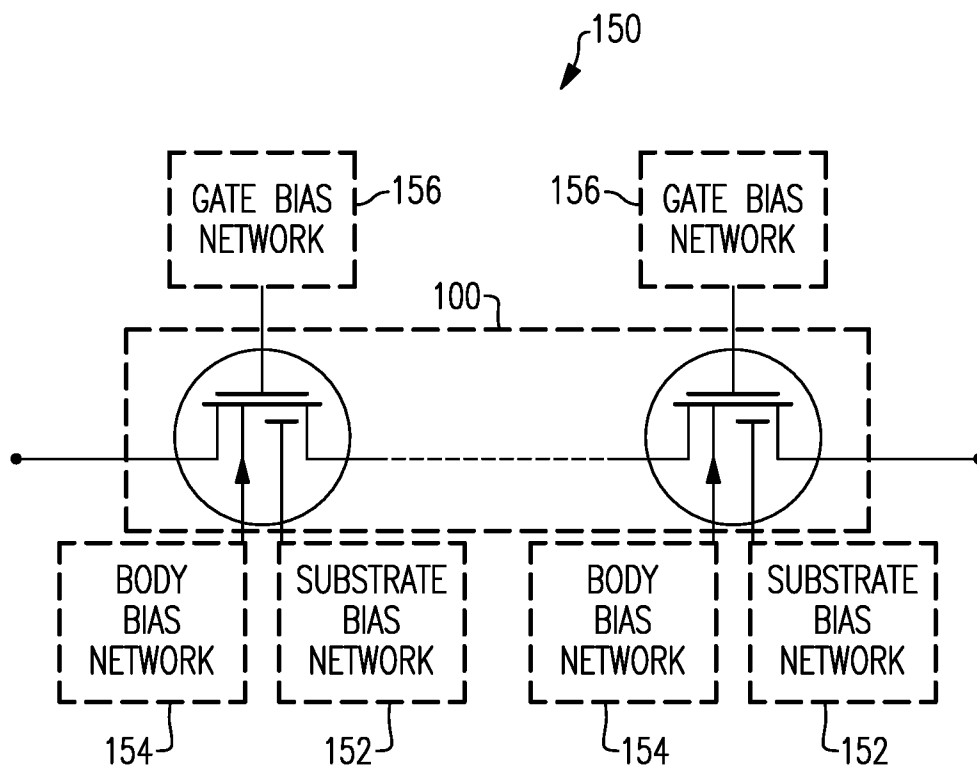
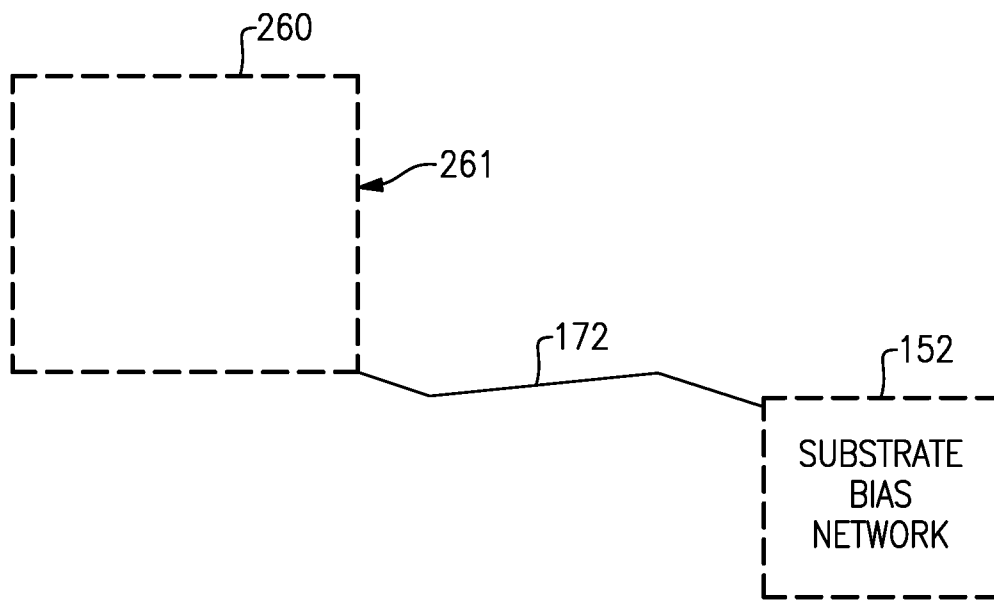


FIG.31

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**FIG.32**

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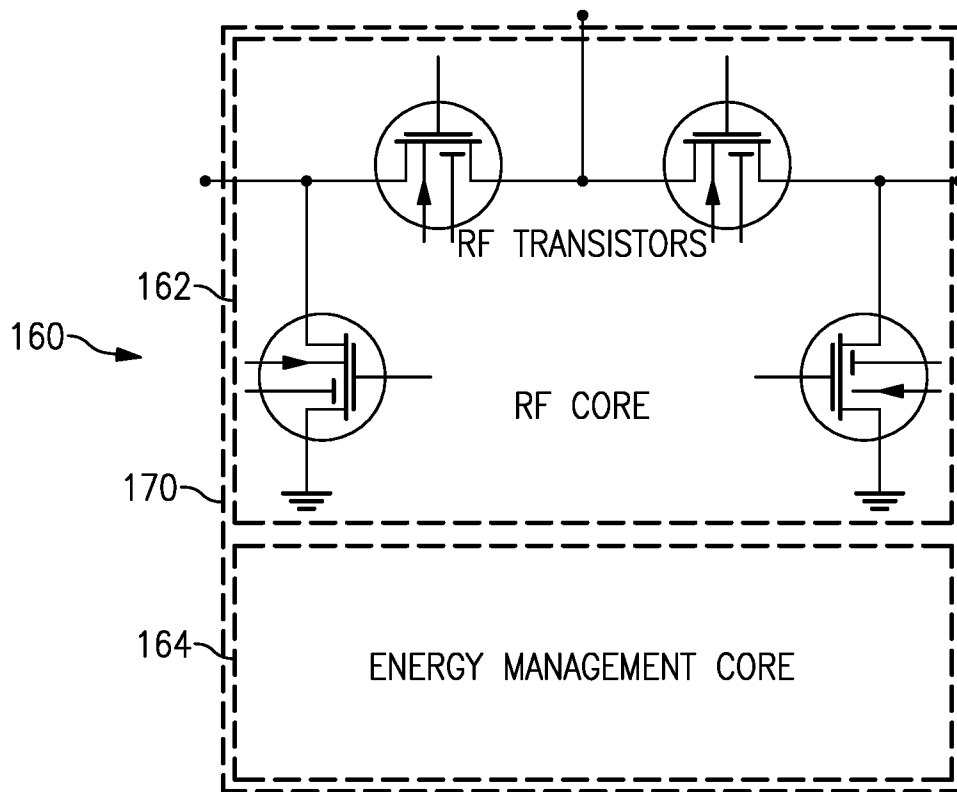


FIG.33

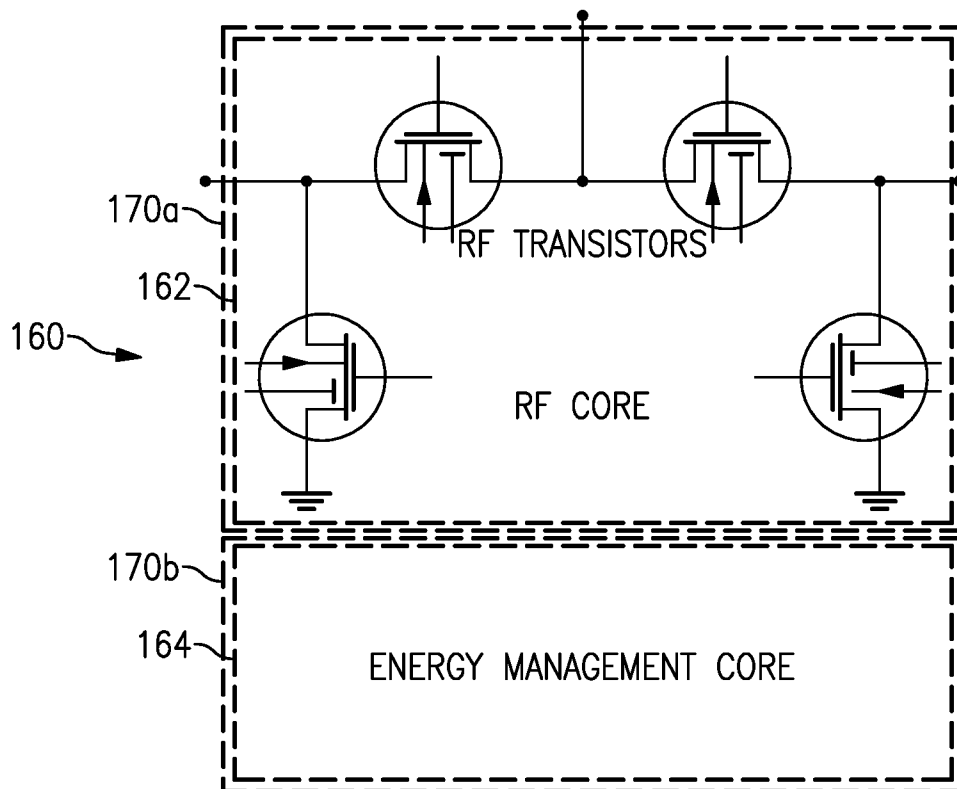


FIG.34

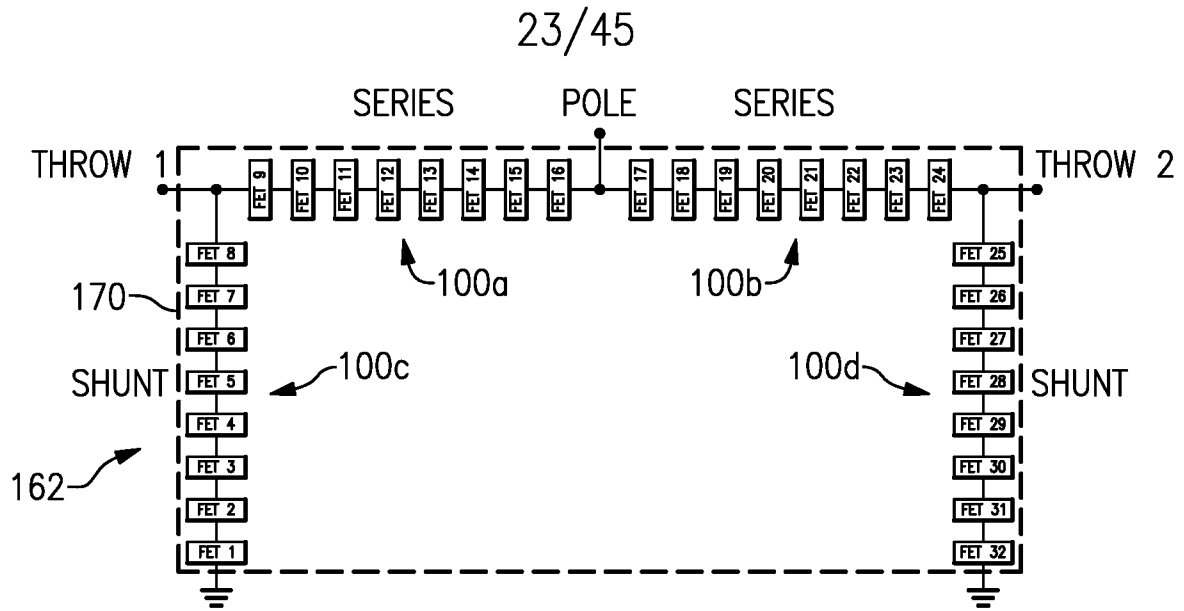


FIG. 35

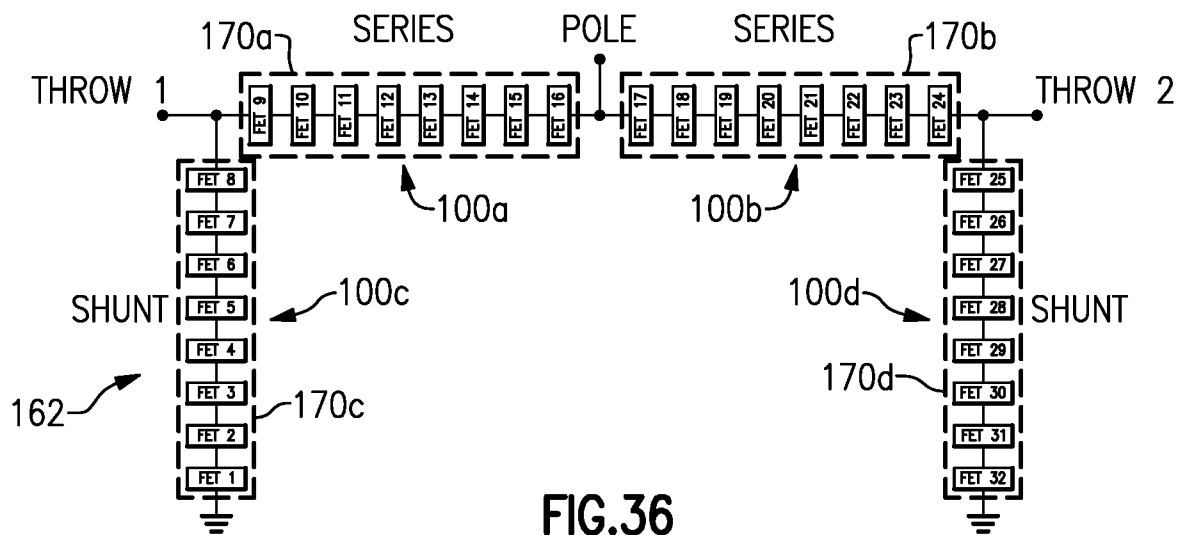


FIG. 36

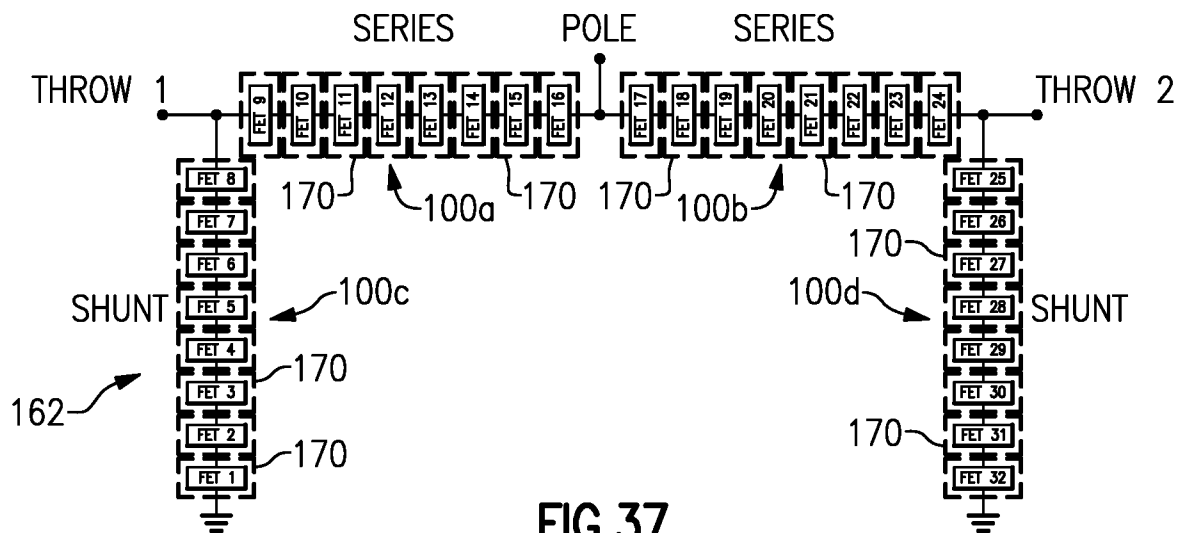
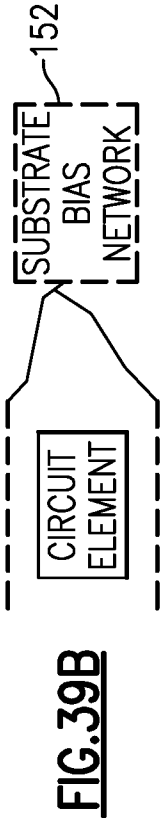
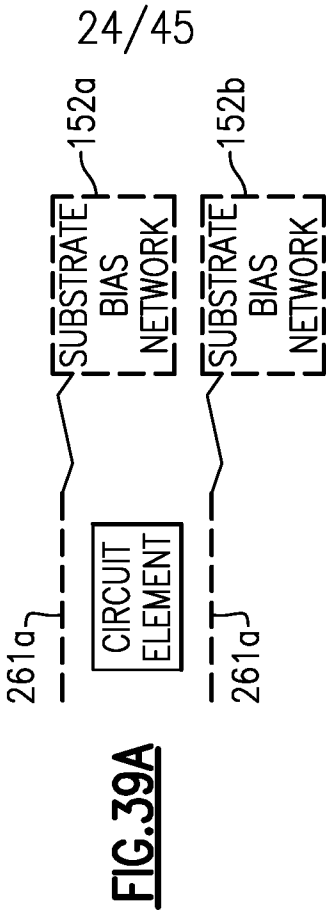
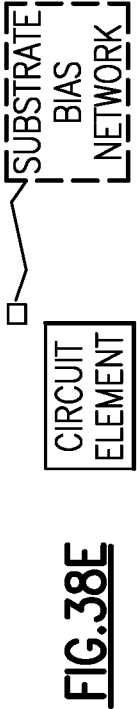
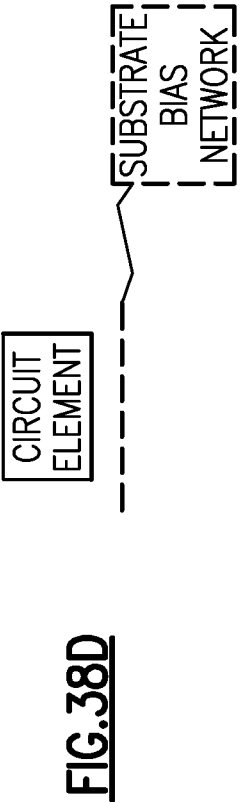
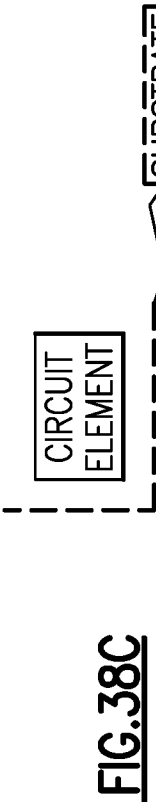
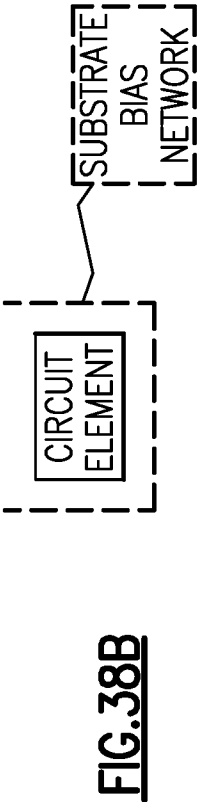
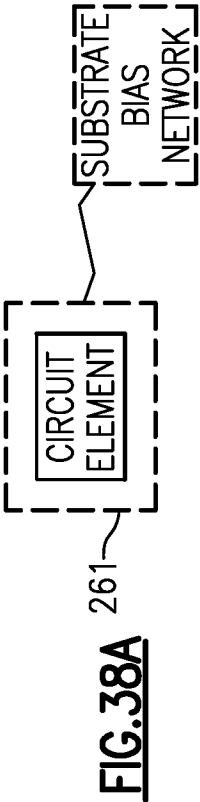


FIG. 37



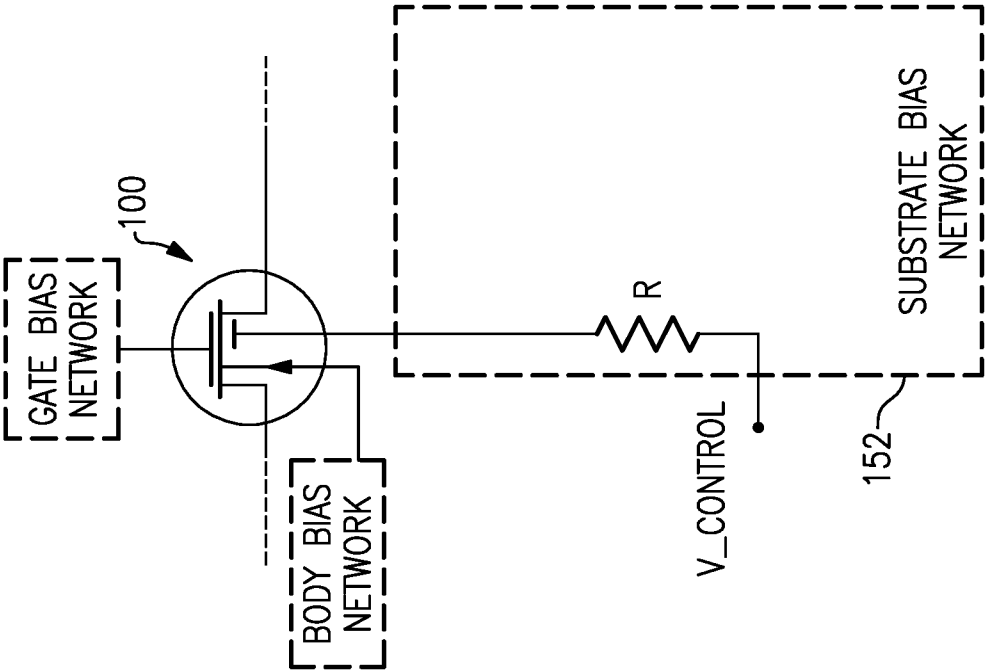


FIG.41

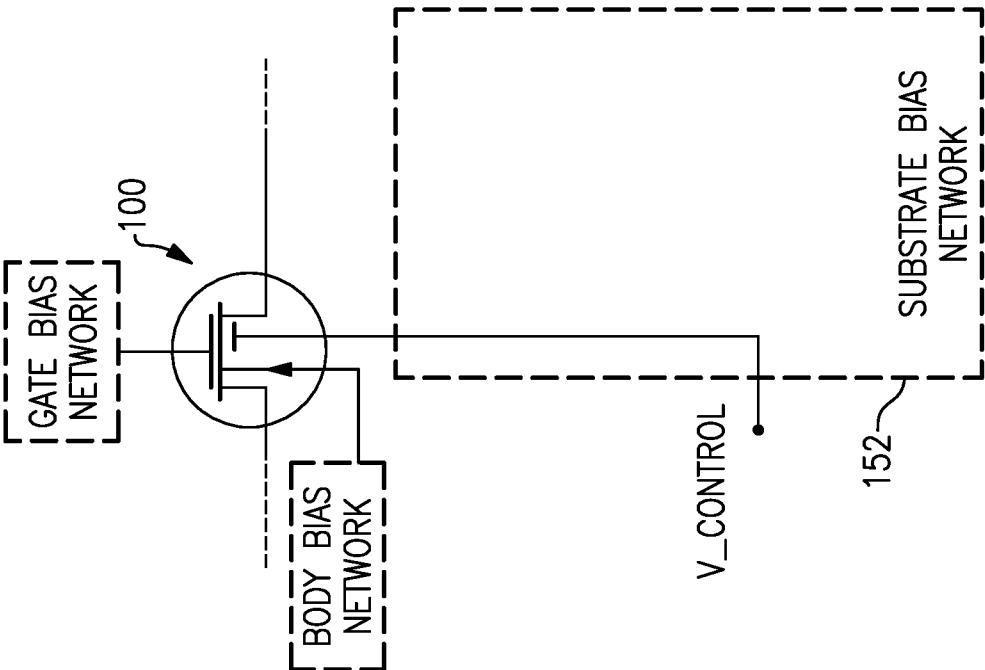


FIG.40

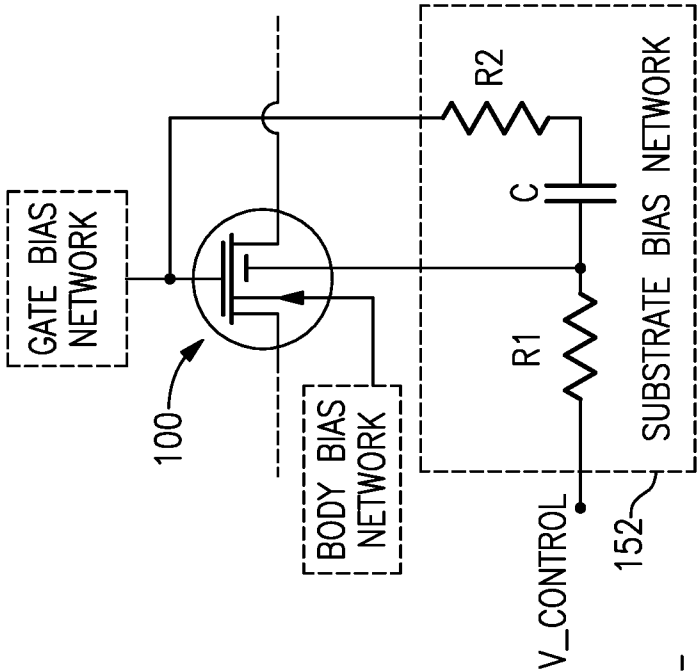


FIG.44

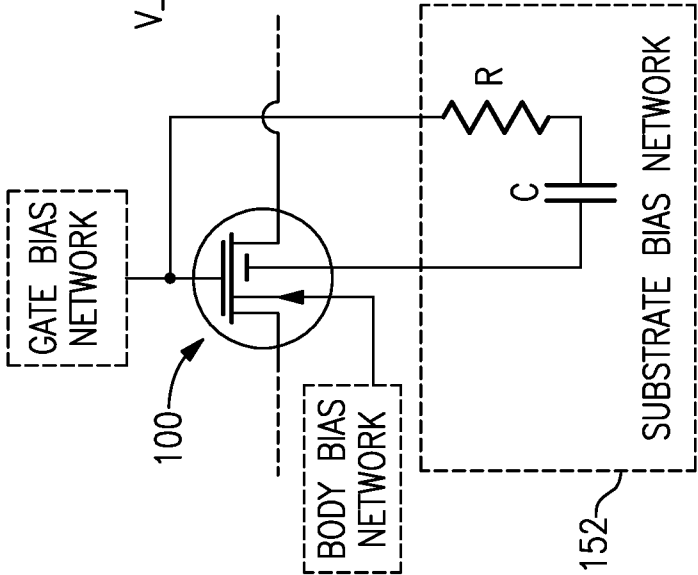


FIG.43

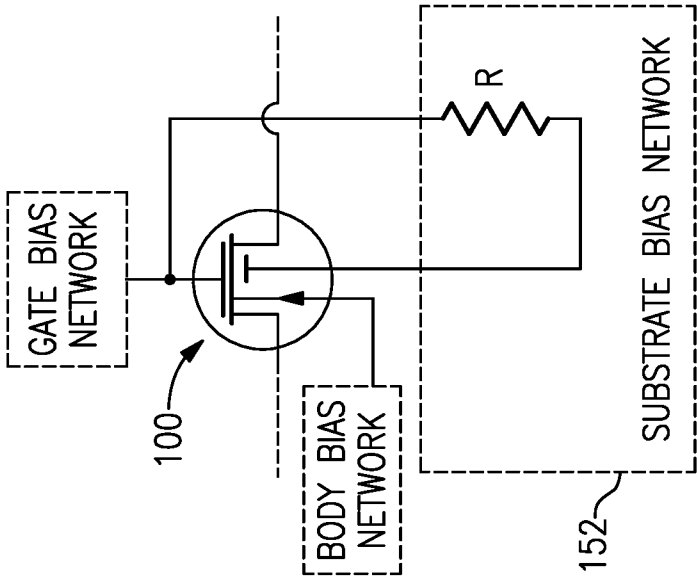


FIG.42

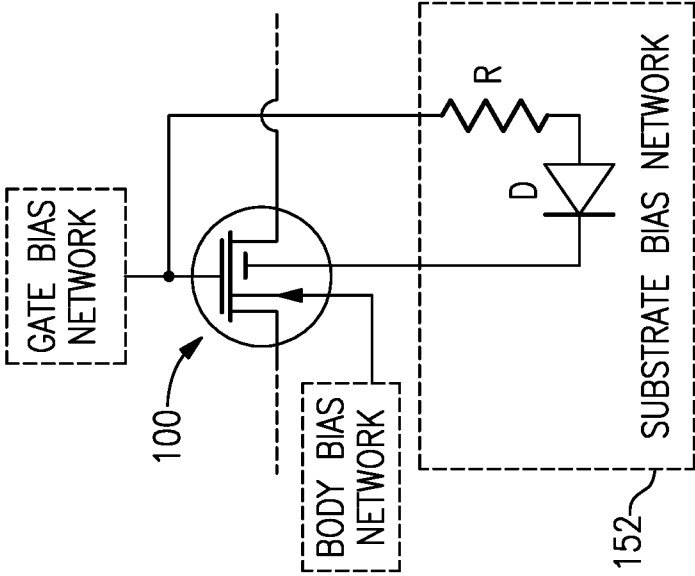


FIG. 45B

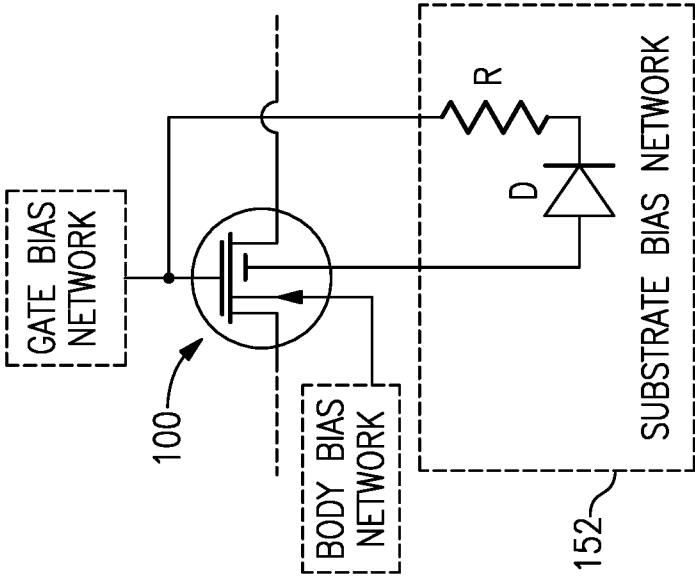
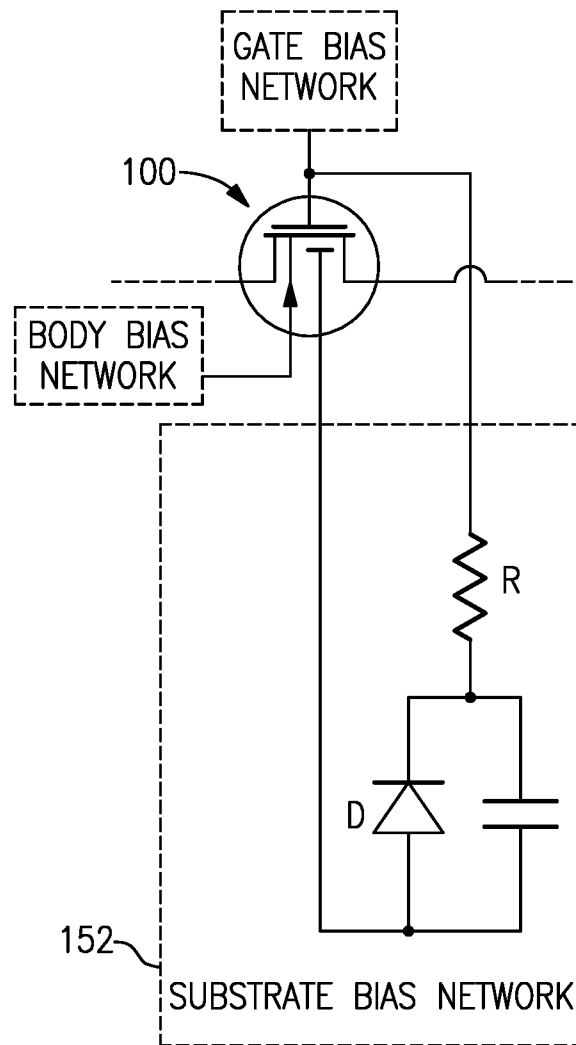


FIG. 45A

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**FIG.46**

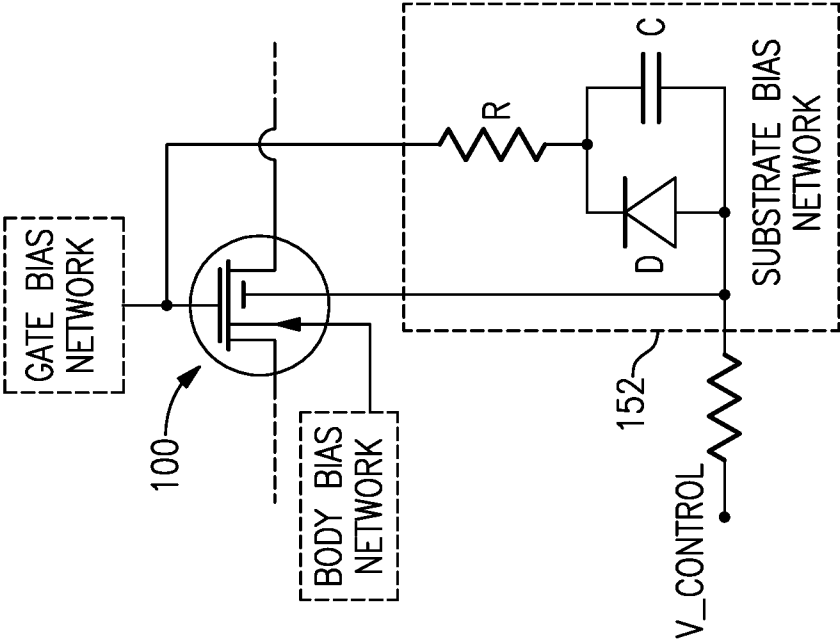


FIG. 48

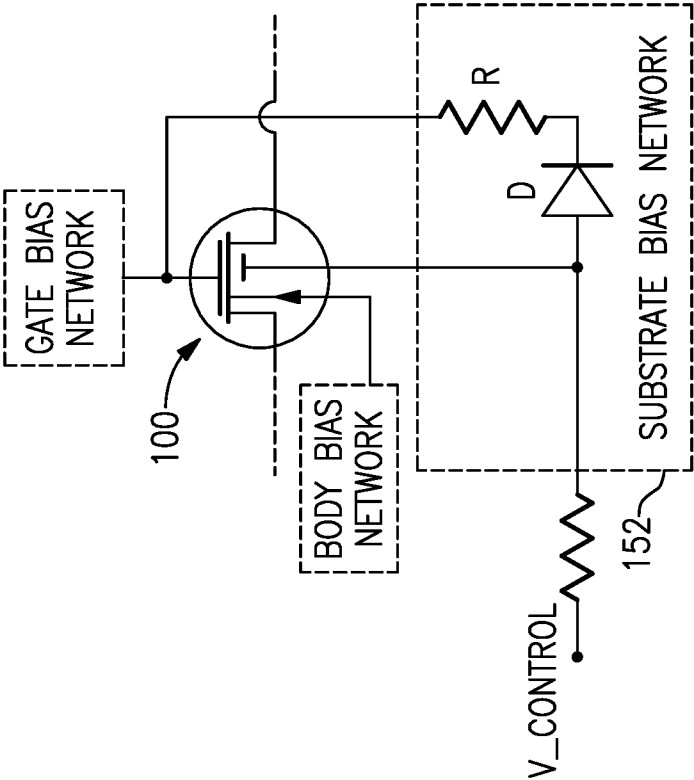
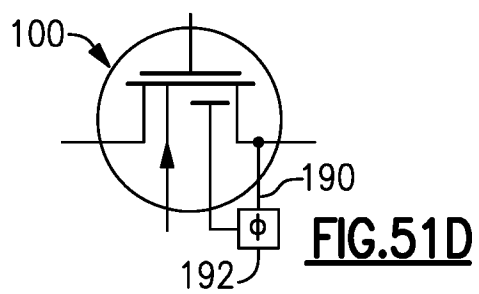
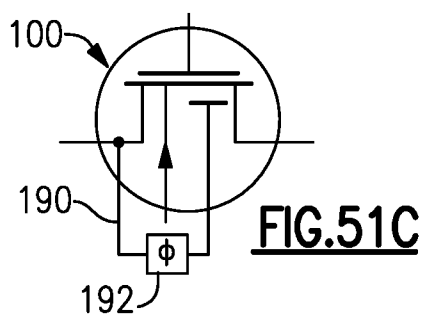
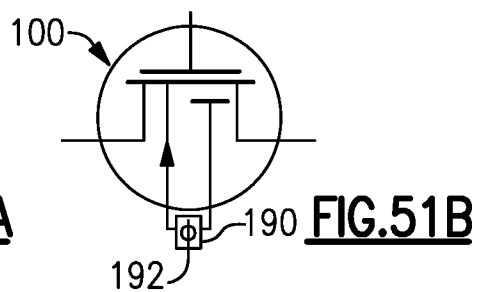
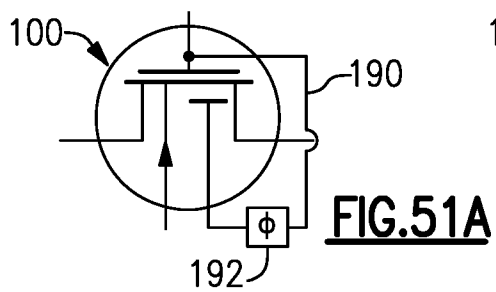
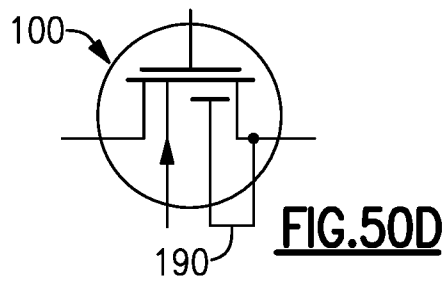
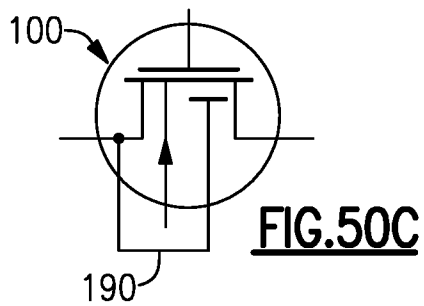
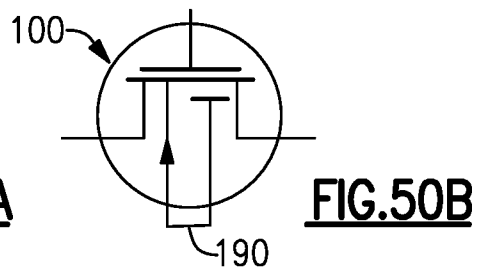
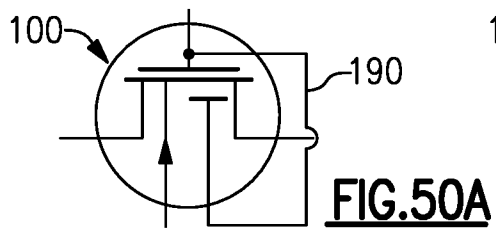
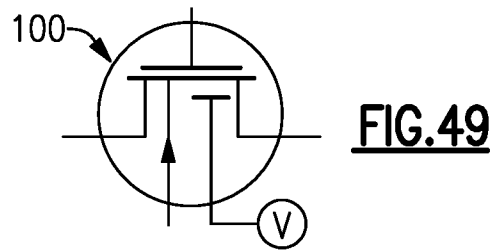
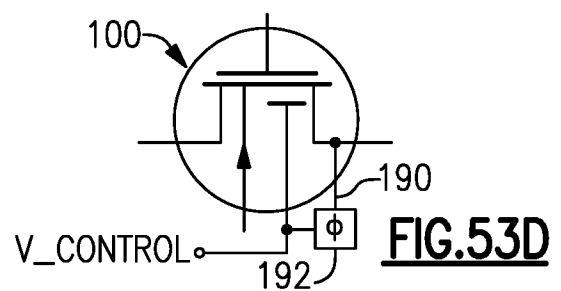
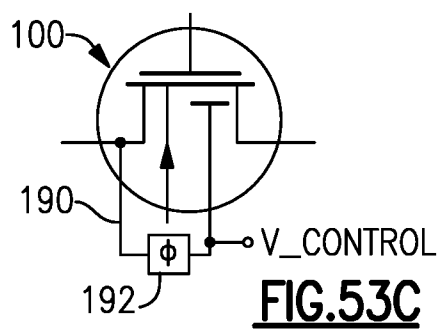
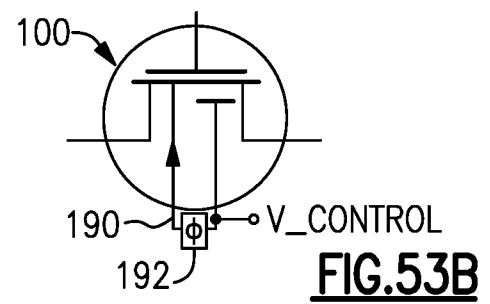
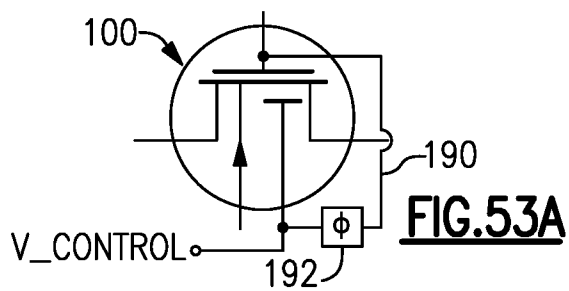
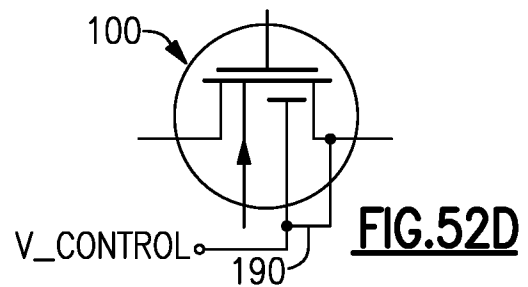
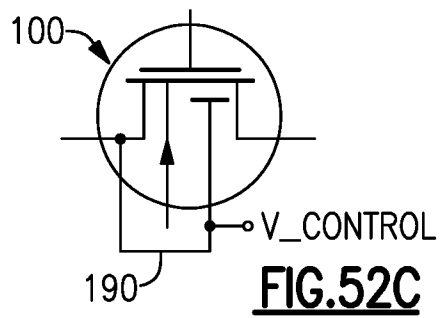
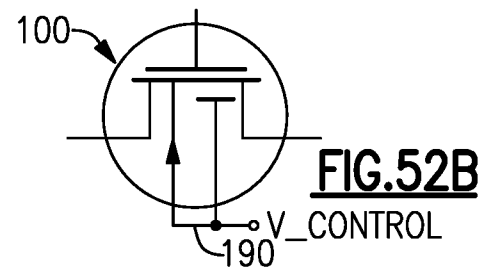
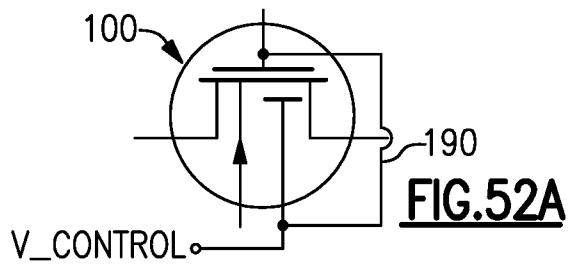


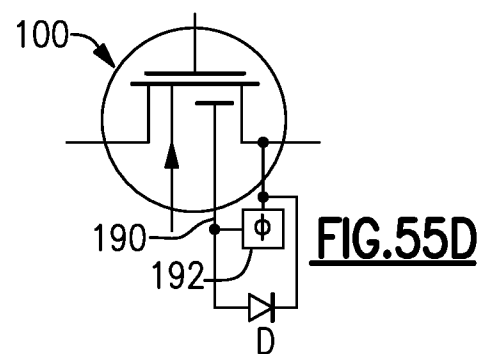
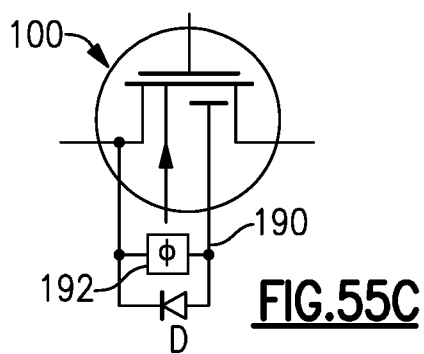
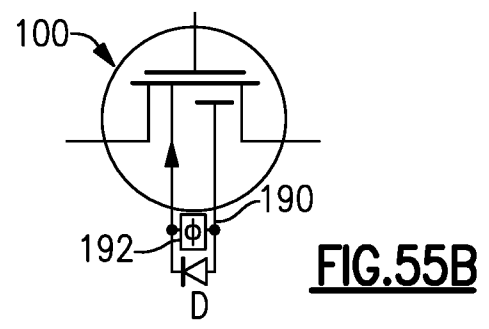
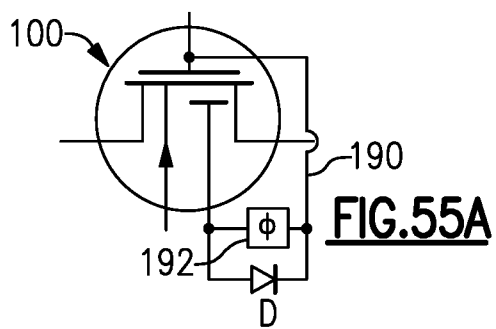
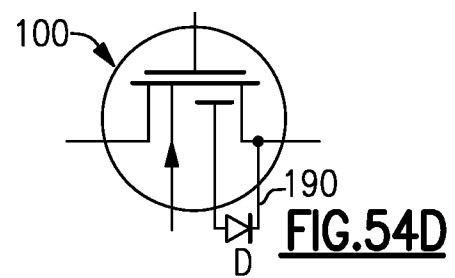
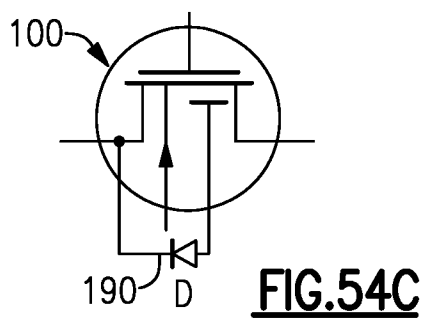
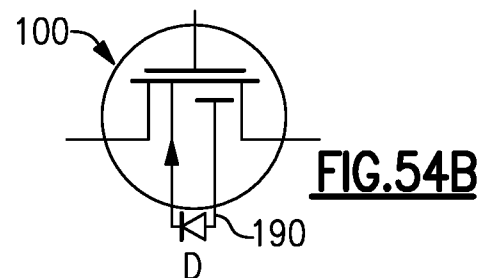
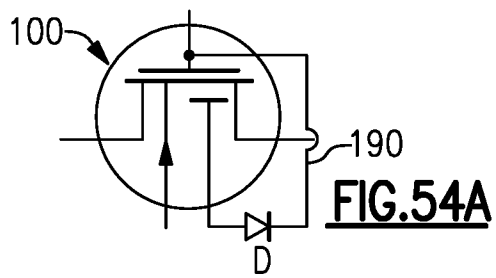
FIG. 47

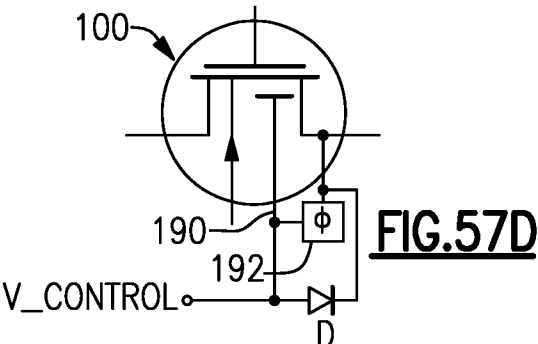
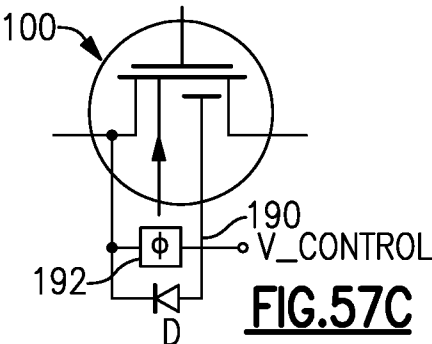
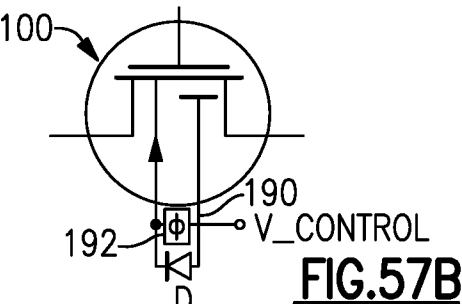
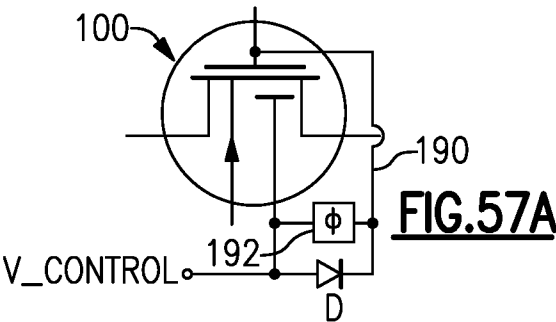
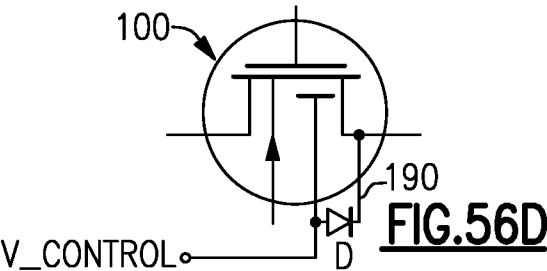
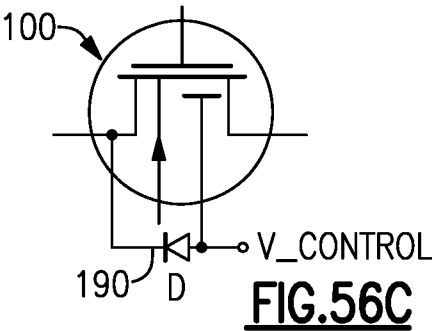
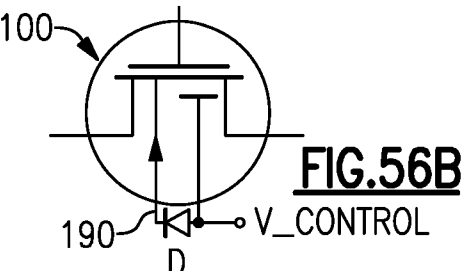
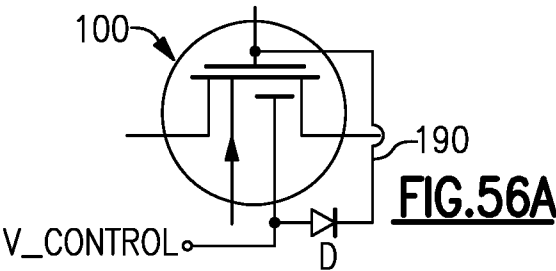
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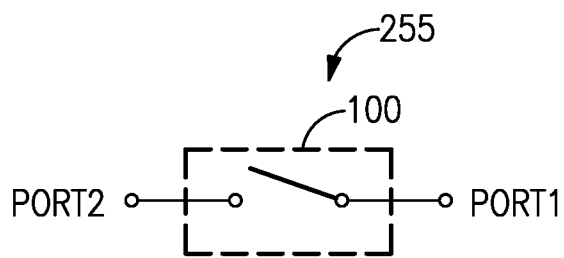


FIG. 58

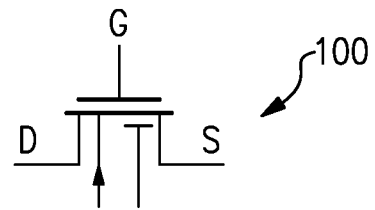


FIG. 59

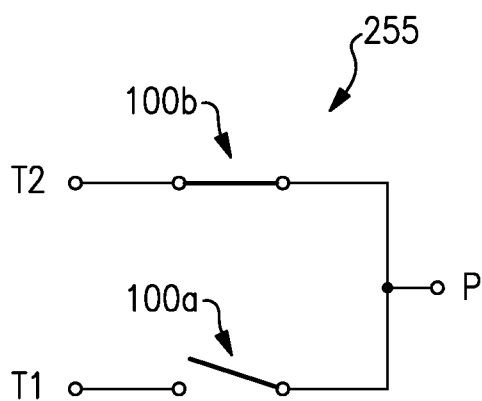


FIG. 60

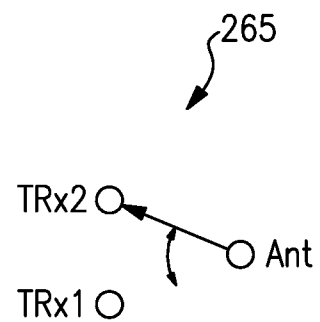


FIG. 61

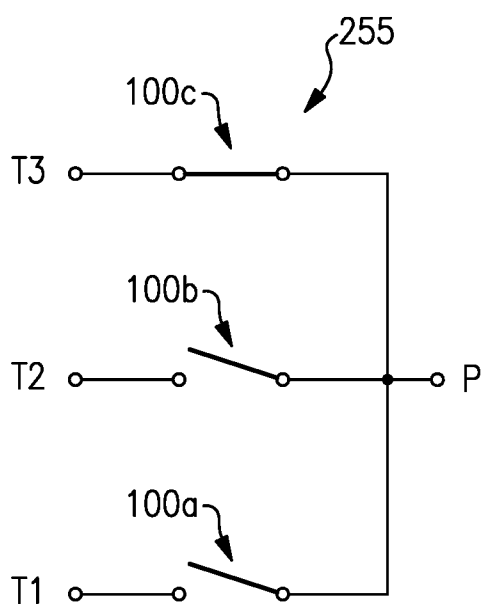


FIG. 62

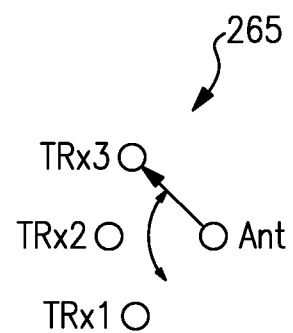


FIG. 63

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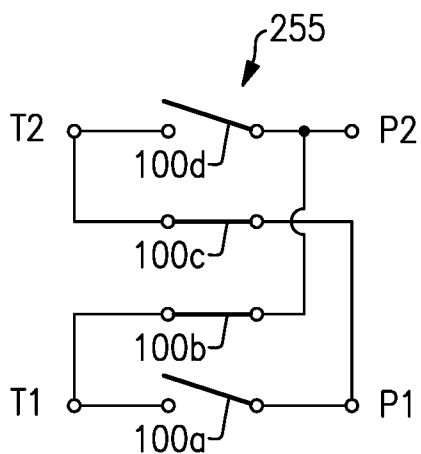


FIG.64

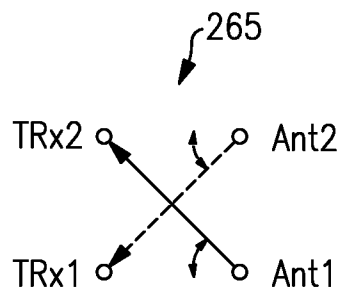


FIG.65

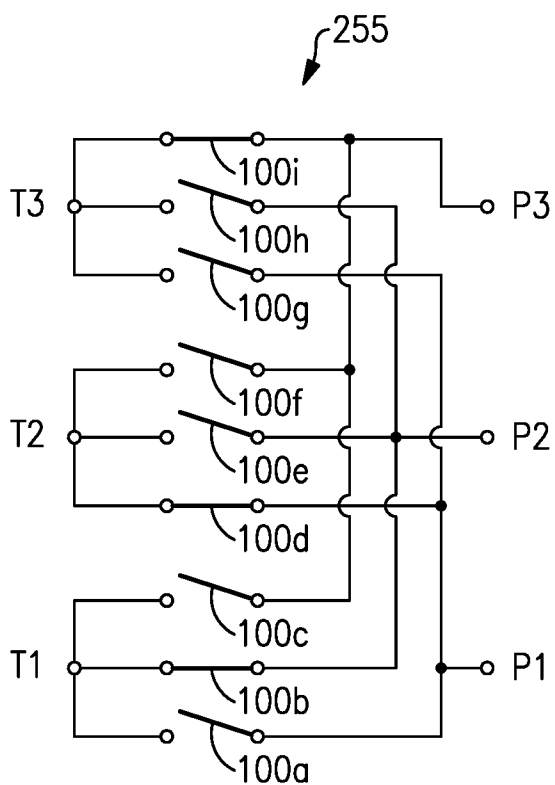


FIG.66

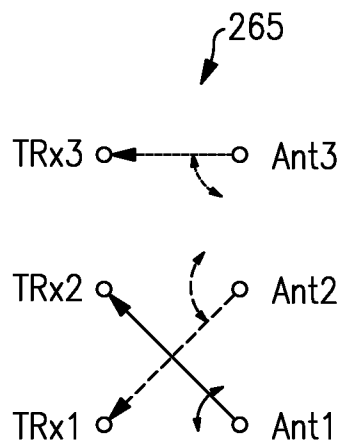
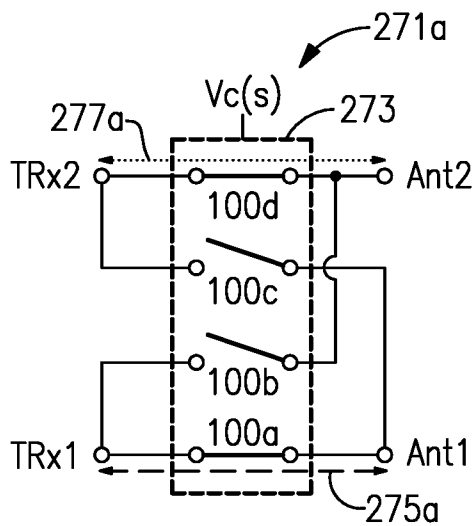
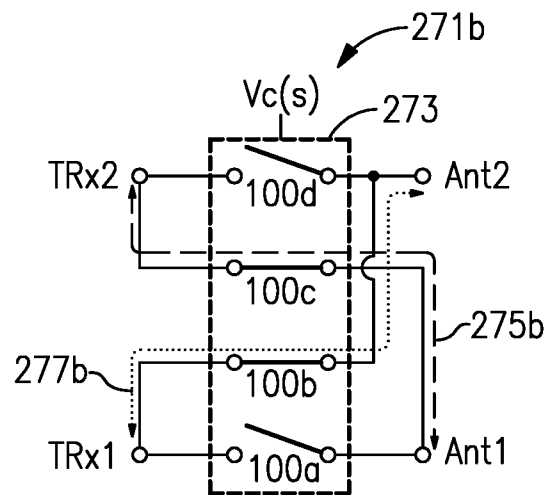
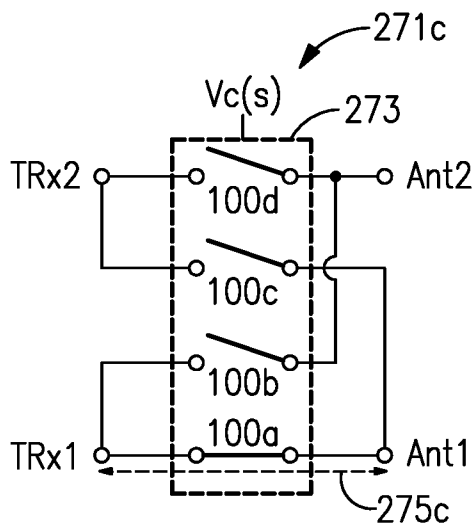
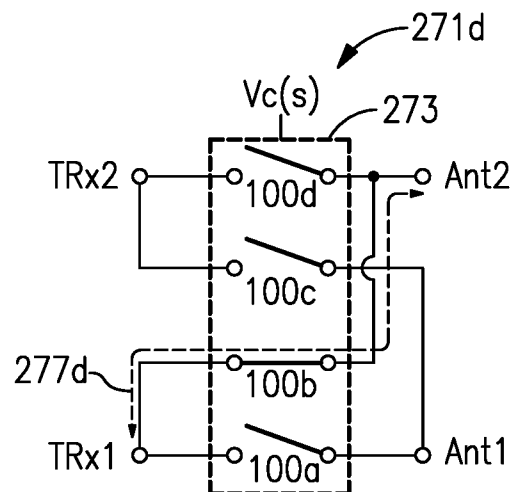
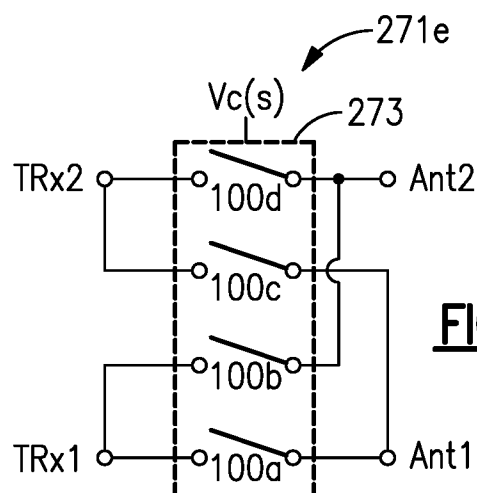


FIG.67

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**FIG. 68A****FIG. 68B****FIG. 68C****FIG. 68D****FIG. 68E**

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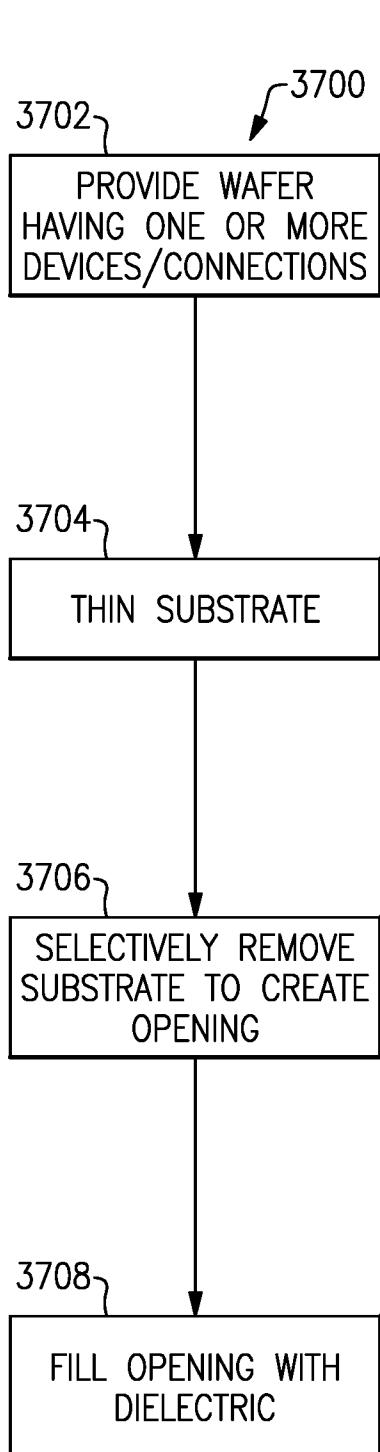


FIG.69A

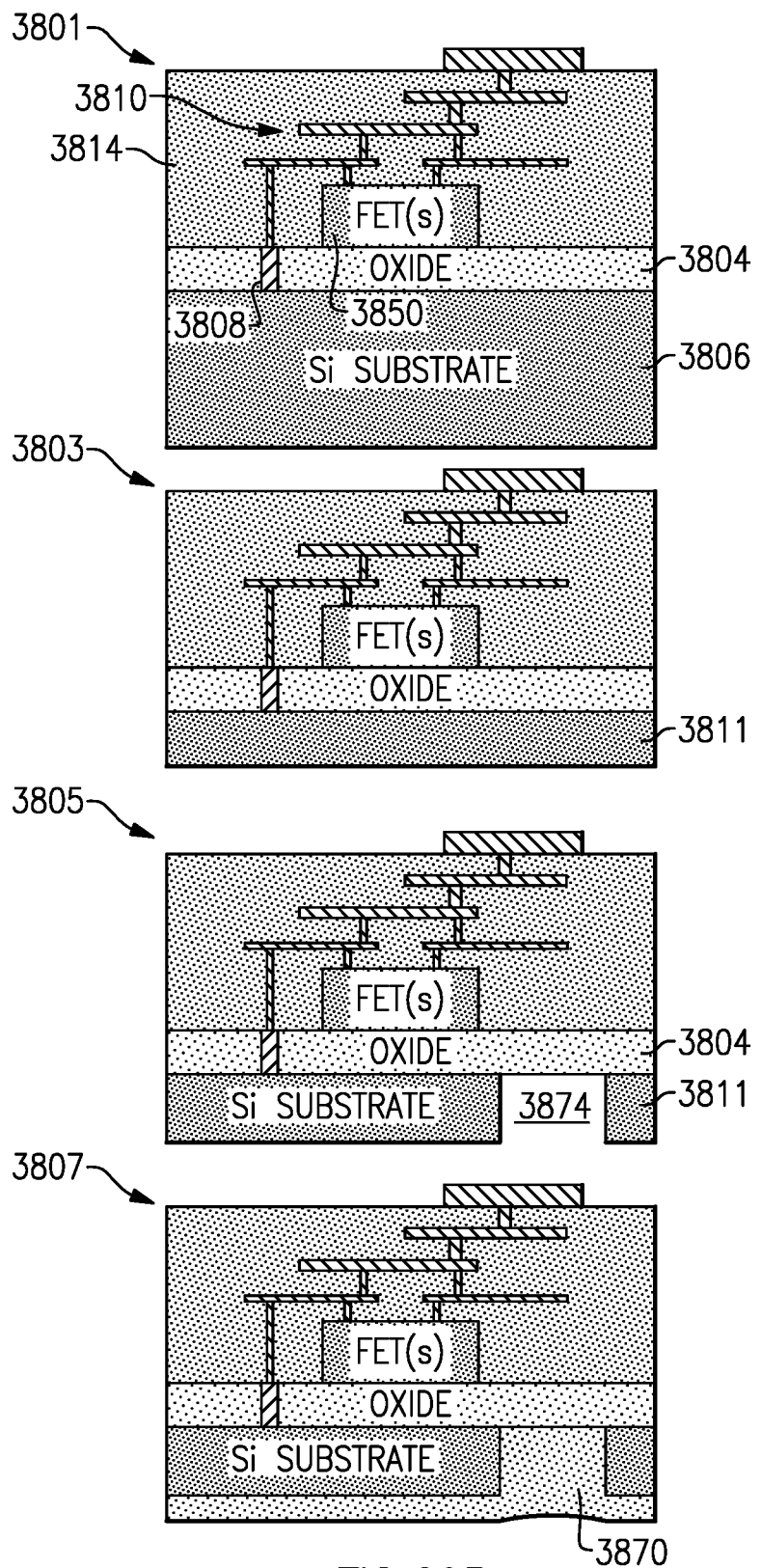
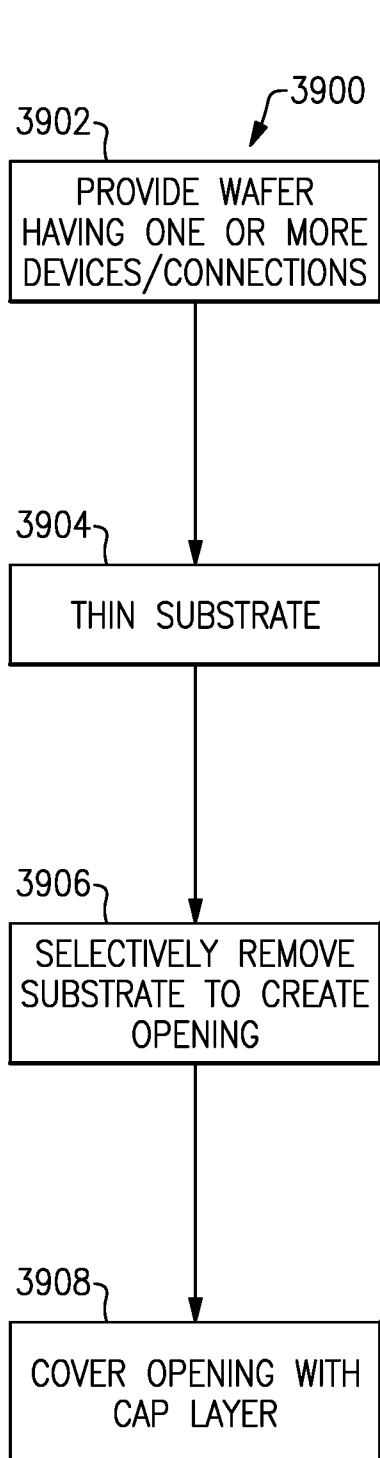
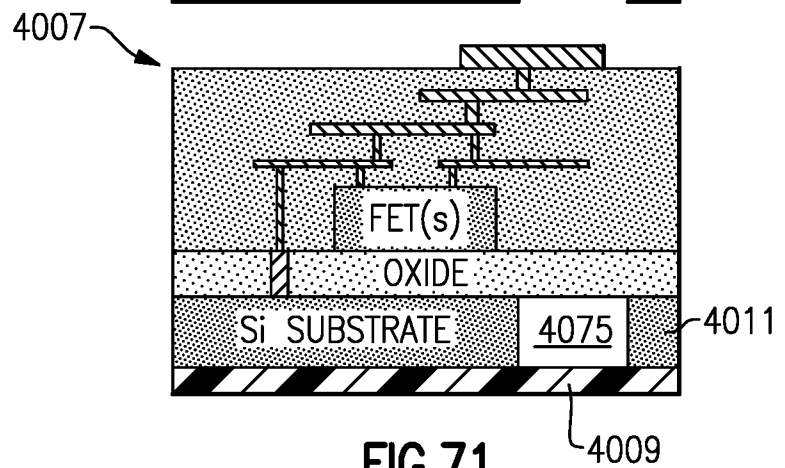
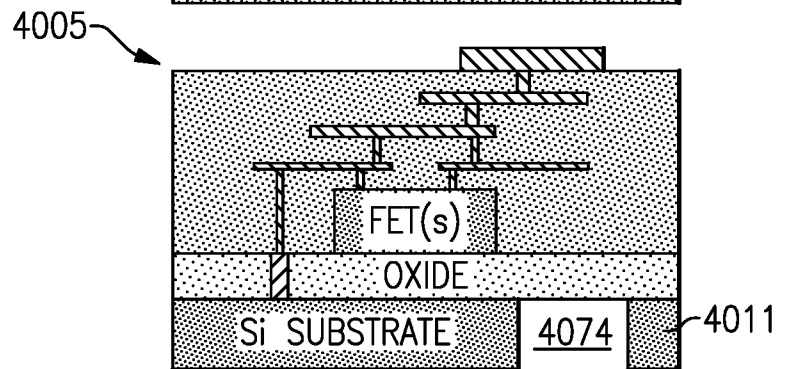
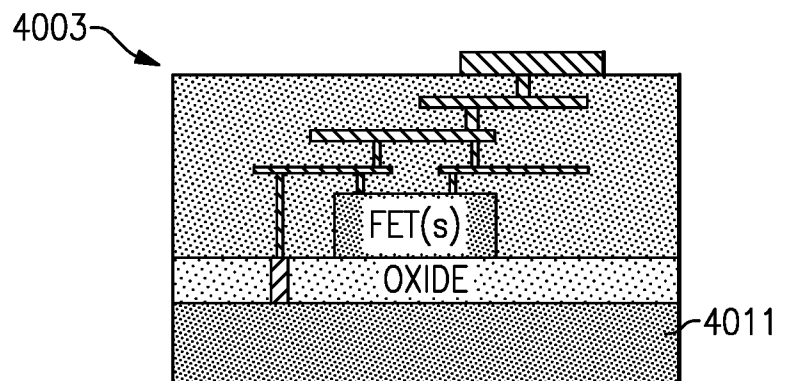
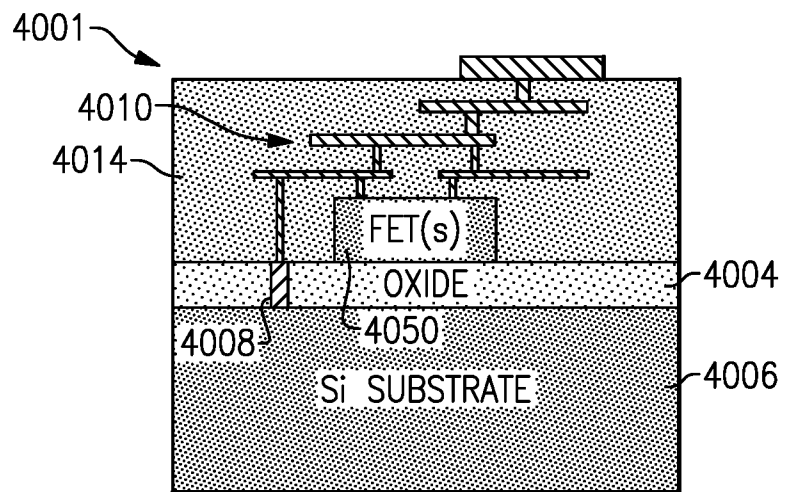
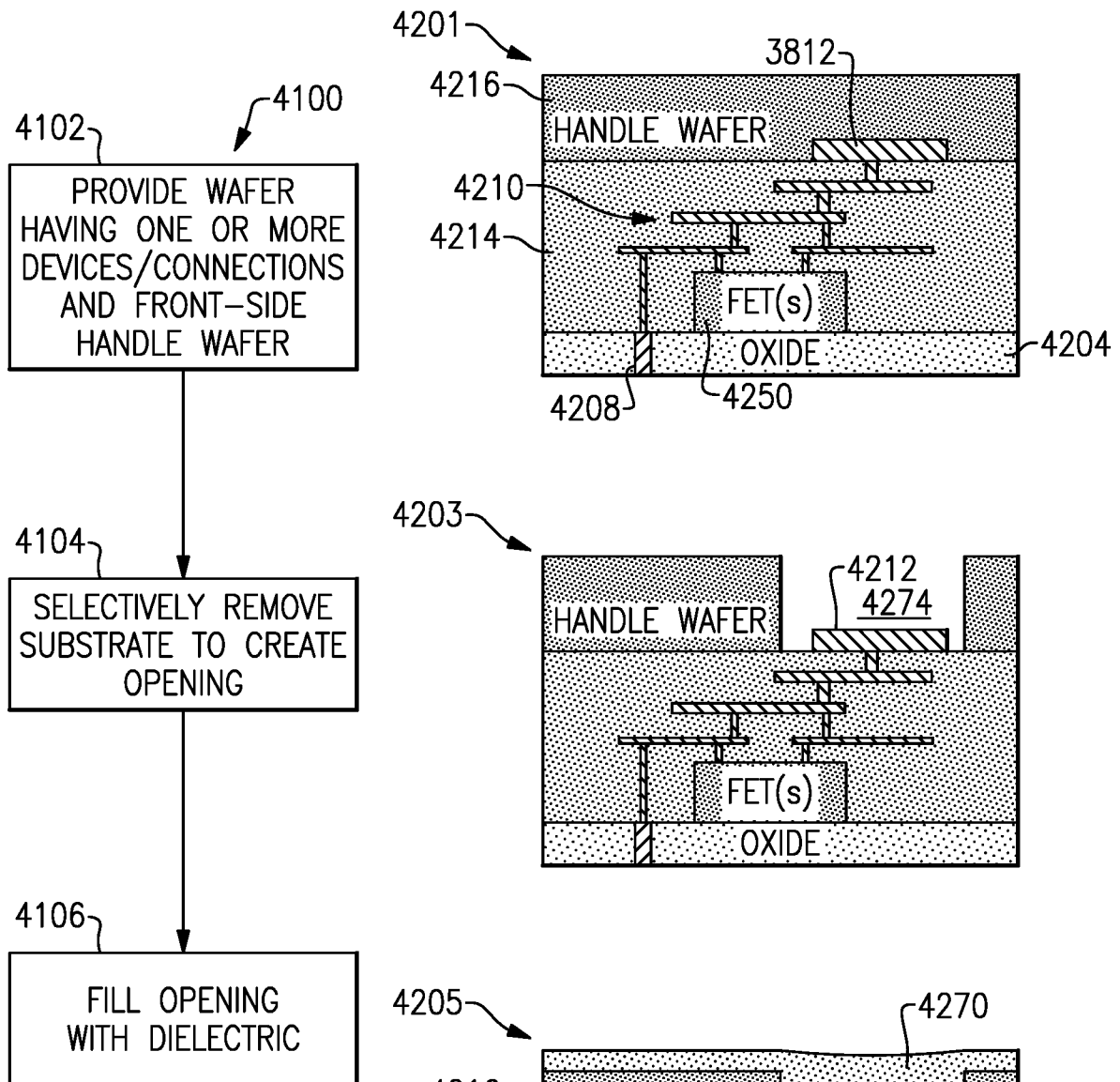


FIG.69B

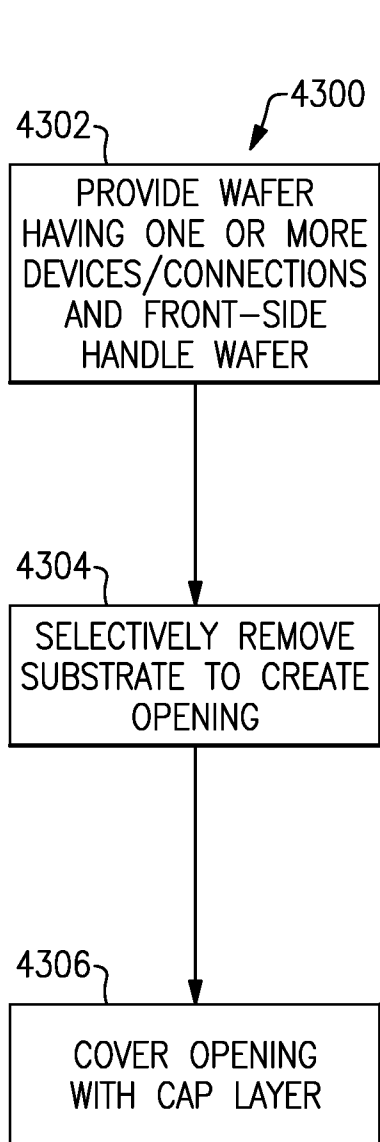
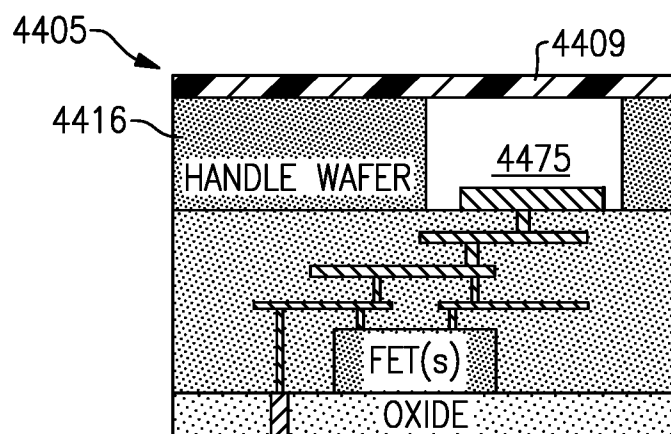
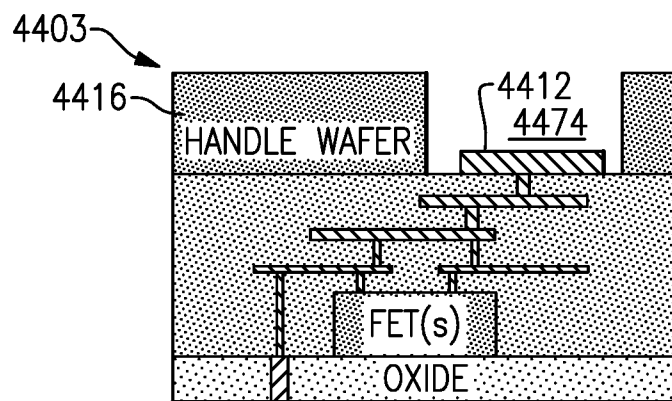
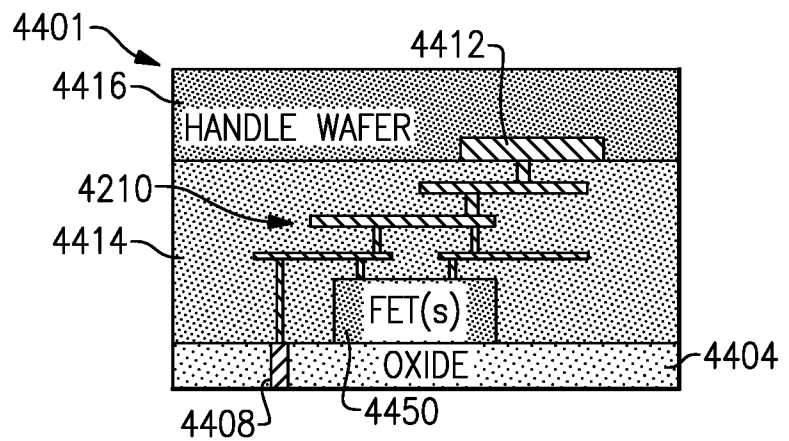
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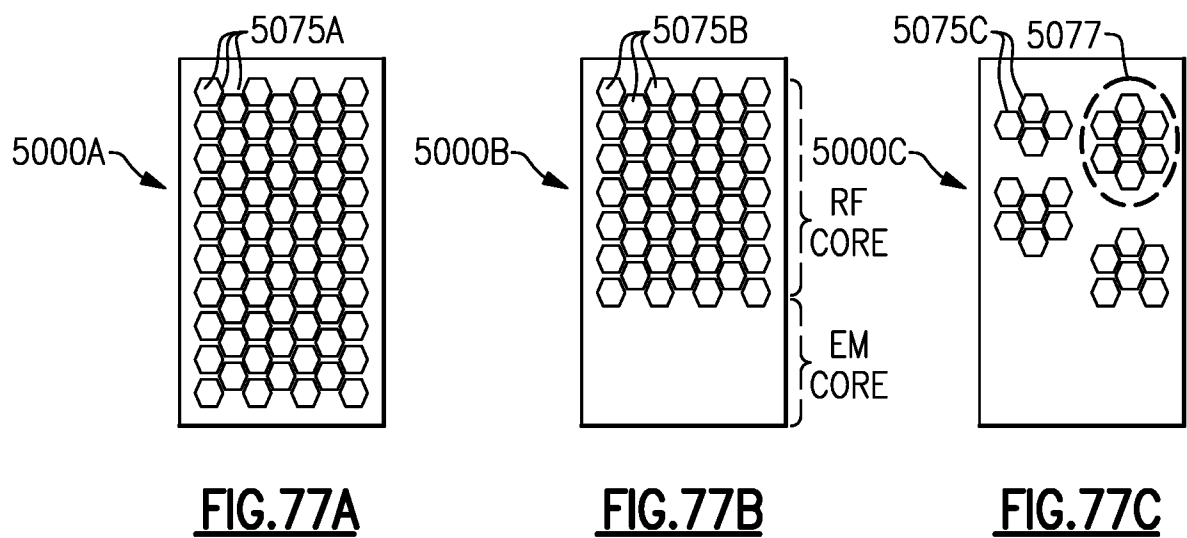
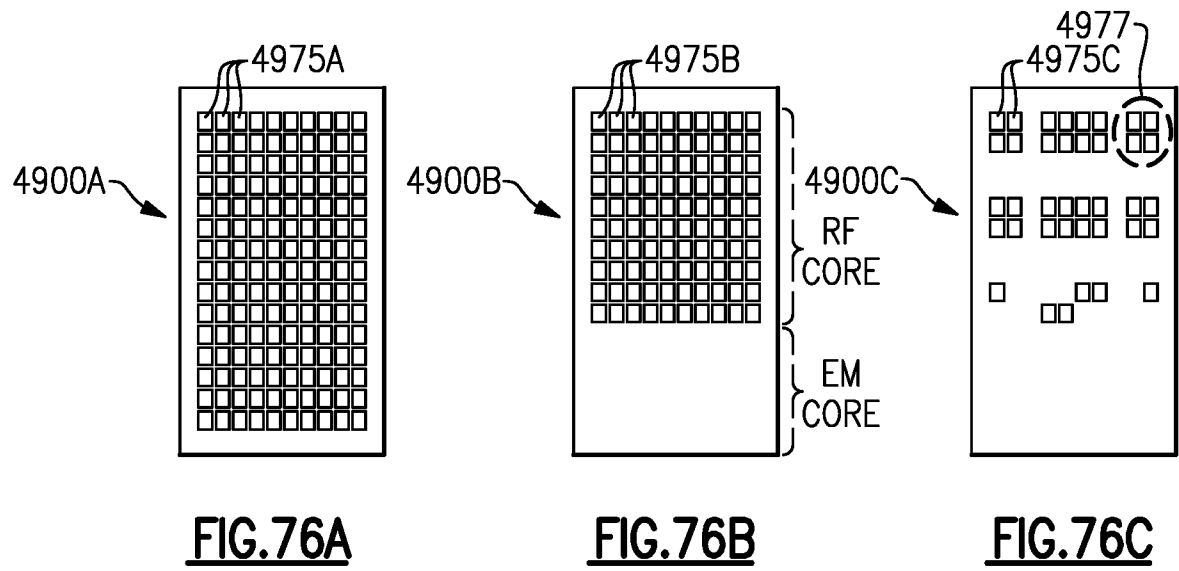
**FIG.70****FIG.71**

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**FIG.72****FIG.73**

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**FIG.74****FIG.75**



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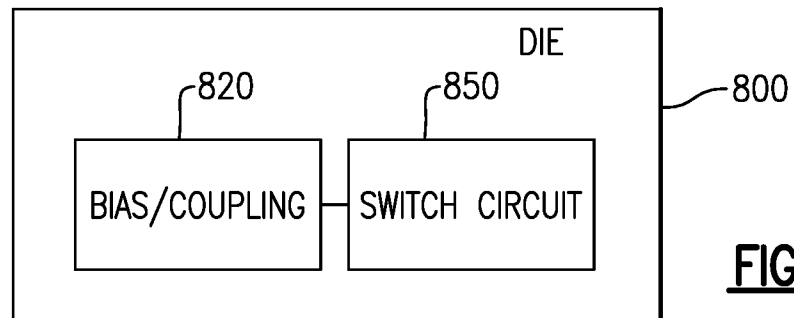


FIG. 78A

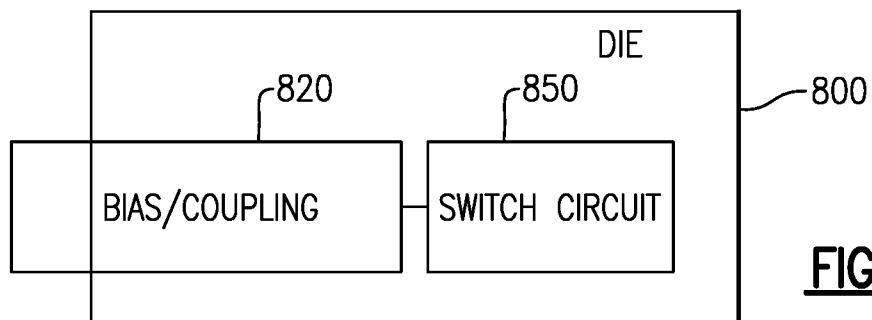


FIG. 78B

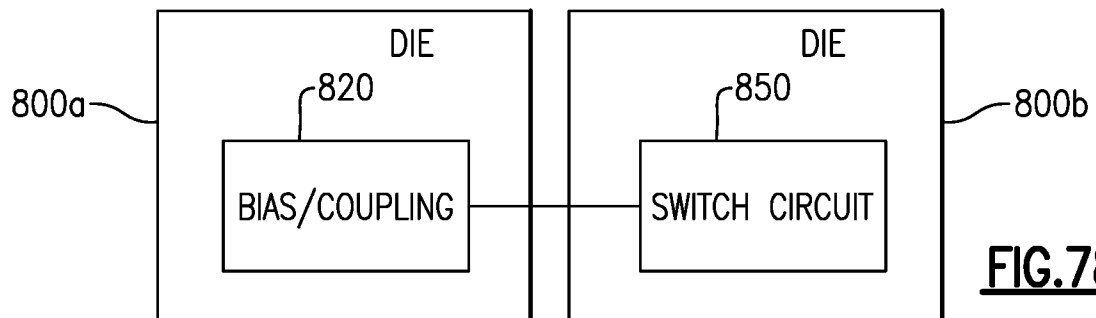


FIG. 78C

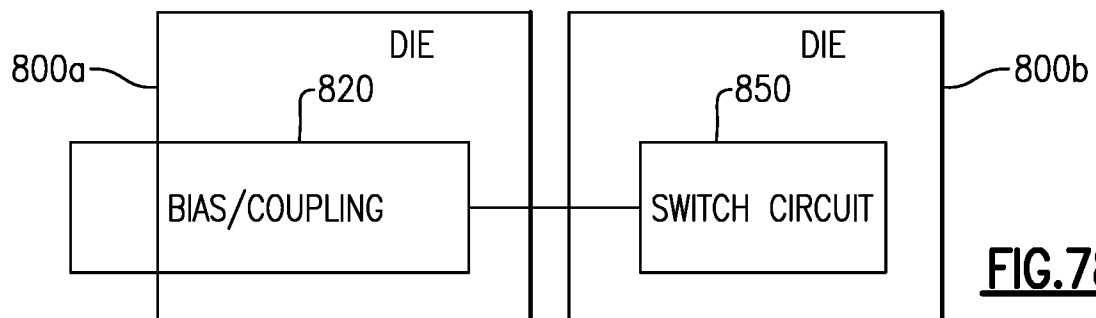


FIG. 78D

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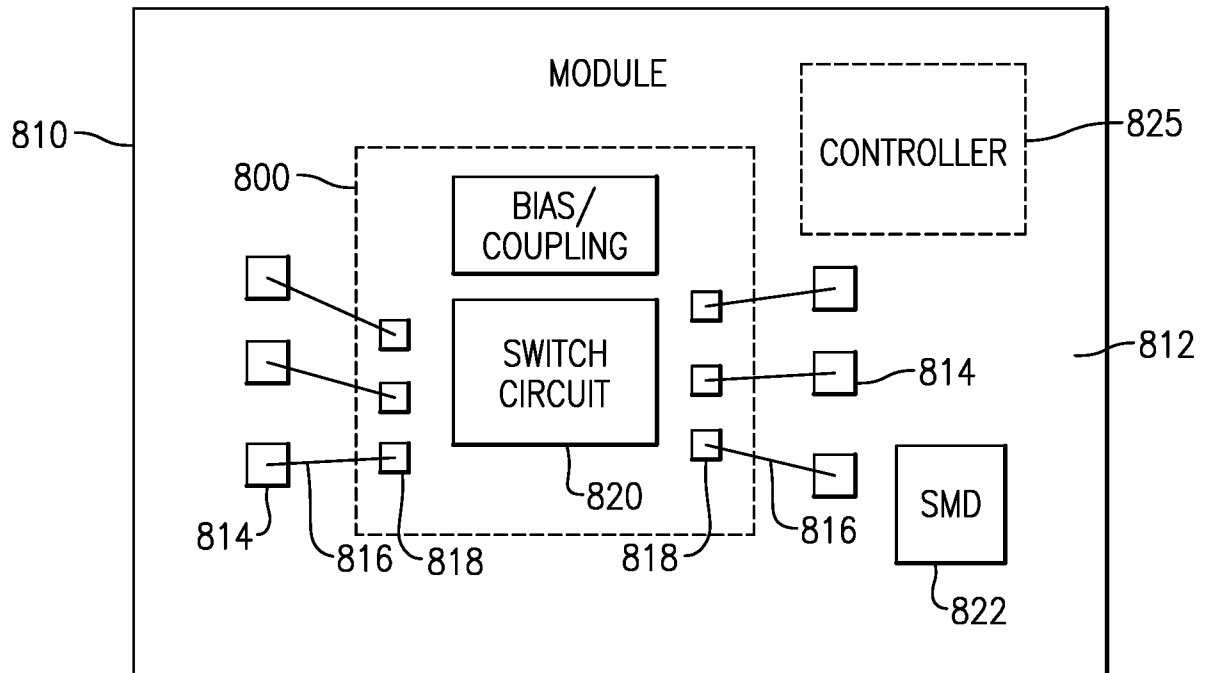


FIG.79A

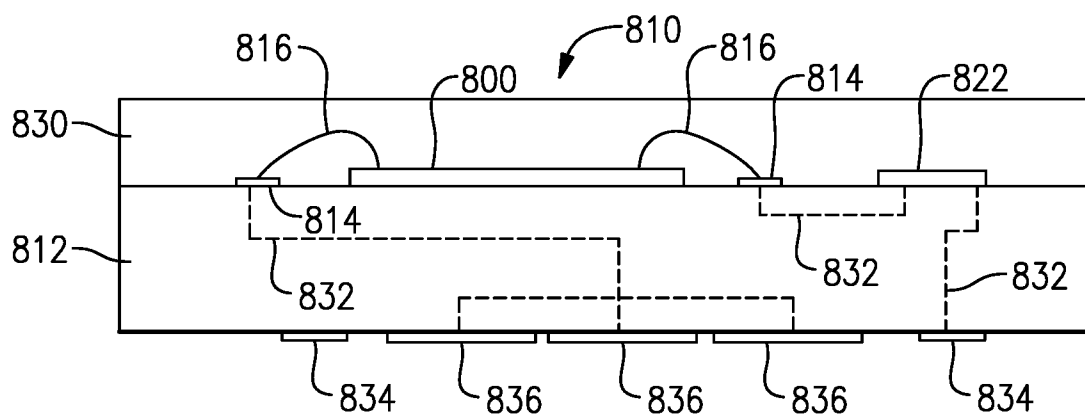
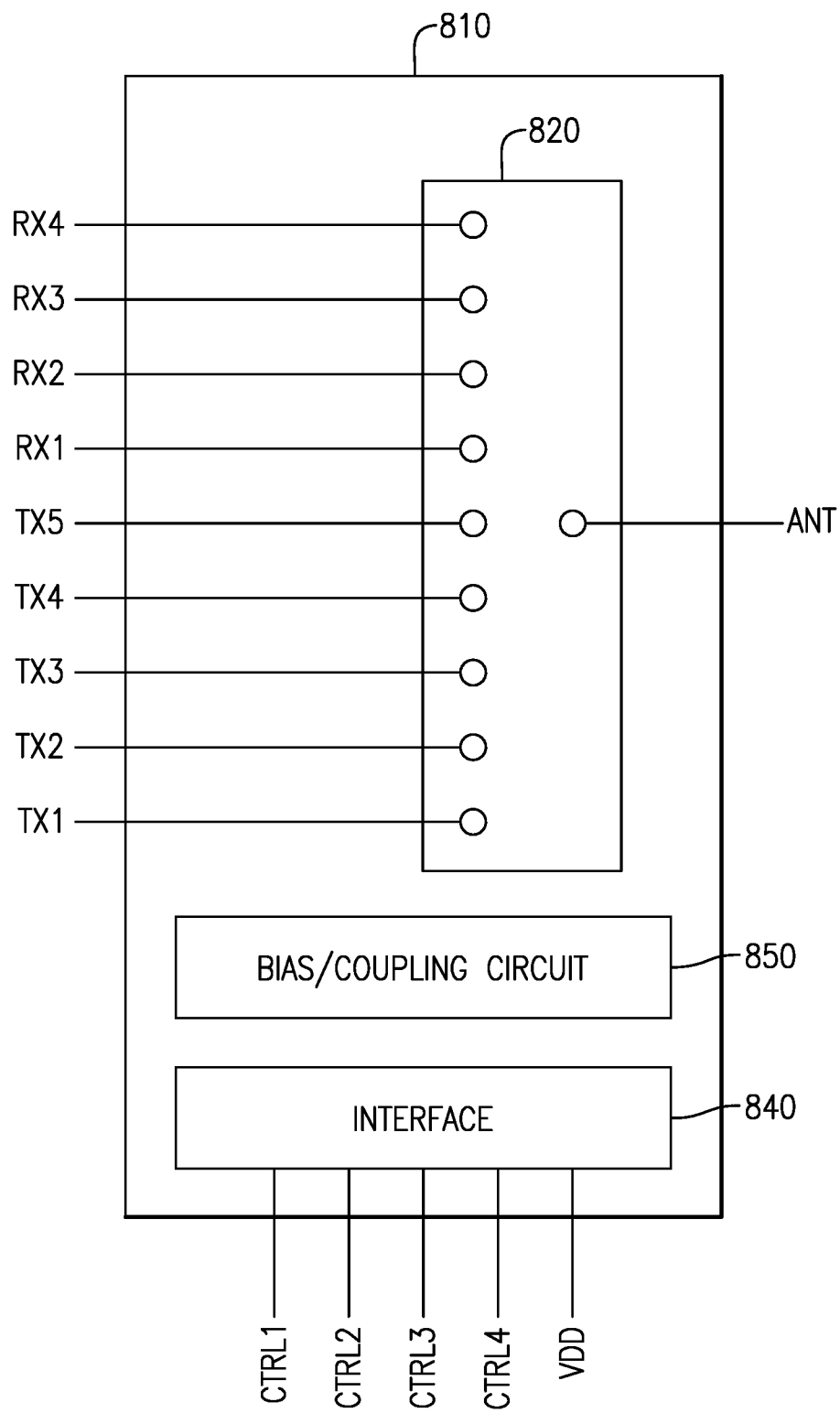


FIG.79B

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**FIG.80**

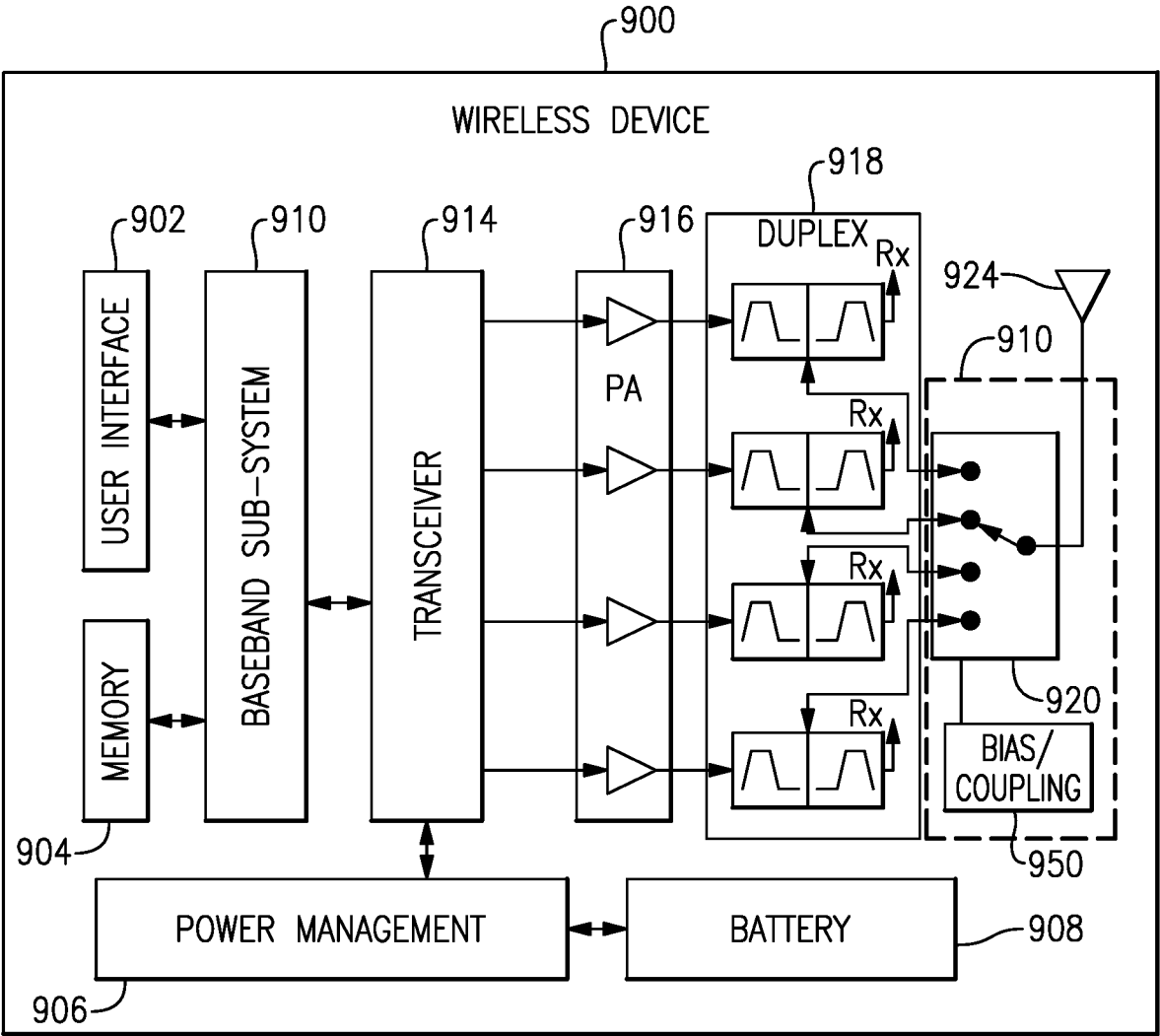


FIG.81

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/032436**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/768(2006.01)I, H01L 21/762(2006.01)I, H01L 29/78(2006.01)I**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; H01L 27/108; H01L 29/06; H01L 21/02; H01L 21/762; H01L 27/07; H01L 21/00; H01L 27/12; H01L 29/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: RF, switch, SOI, trench, opening

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 8421082 B1 (XIAO "CHARLES" YANG) 16 April 2013 See abstract, column 1, lines 37-56, column 7, line 47-column 10, line 17 and figures 4A-5B	1-7, 10-25, 48-54
Y		8, 9, 55, 56
A		26-47
Y	US 2012-0038024 A1 (ALAN B. BOTULA et al.) 16 February 2012 See abstract, paragraph [0021] and figures 4, 15.	8, 9, 55, 56
A	US 2009-0053860 A1 (GARRETT A. STORASKA et al.) 26 February 2009 See abstract, paragraphs [0014]-[0017] and figure 2B.	1-56
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Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

08 August 2016 (08.08.2016)

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08 August 2016 (08.08.2016)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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