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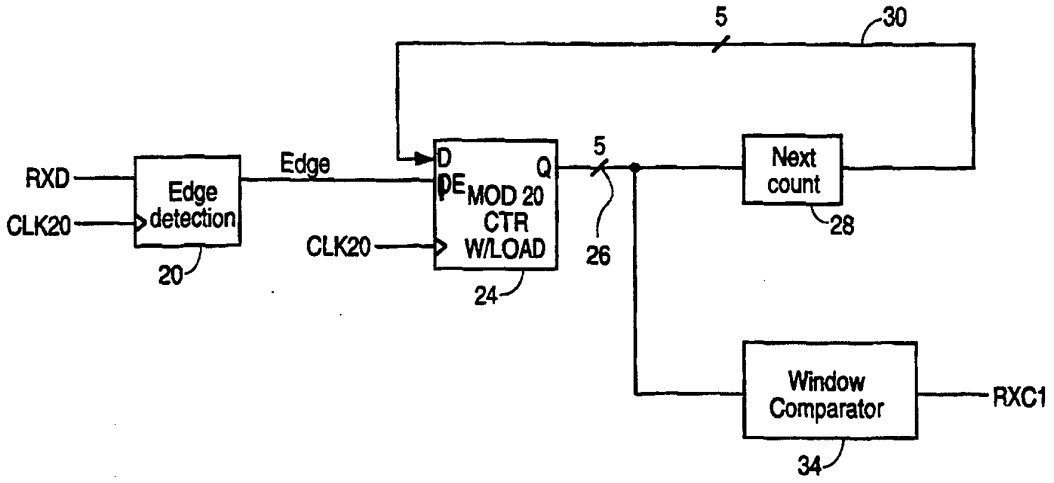

(57) Abstract

A modeless digital non-return to zero (NRZ) clock recovery circuit uses a high speed clock signal to oversample incoming digital data and divide each bit cell into a number of subcells. When a data transition occurs in the input data, logic in the circuit (20) determines whether the transition has occurred in an appropriate time window. If the data transition is several subcells out of alignment, a larger modification is made to align the output clock signal to the data transition. In any case, the clock adjustment occurs within one clock cycle of the high speed clock signal. The circuit includes a counter (24) with parallel enable, and combinatorial logic (28) determines the next counter state. The counter (24) is loaded with the correct state value on every detected edge transition of the input data stream. Logic synchronizes the incoming data stream and high speed clock, and synthesizes the output clock signal from the counter state information.

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NRZ CLOCK RECOVERY WITH INSTANT LOCK

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to clock signal recovery and specifically to a clock signal recovery circuit for use with a non-return to zero (NRZ) signal.

DESCRIPTION OF THE PRIOR ART

It is well known that data communication systems require a circuit to extract timing information from a received serial bit data stream. Most such data streams consist of data packets, each of which is prefixed by a preamble (a fixed pattern header) that aids the receive clock recovery circuit in finding and extracting the clock signal. Some systems encode the data in a special way so that the clock signal ("clock") may be easily extracted from the received data stream.

The serial bit data stream is typically a sequence of digital ones and zeroes. A local area network system such as Ethernet encodes the data by Manchester encoding to enable the clock recovery circuit to extract the clock signal from the received serial bit stream. Ethernet includes at the beginning of each data packet a preamble which is the 64-bit sequence 1, 0, 1, 0, 1, 0. This preamble indicates that data follows, and also is used to synchronize the clock recovery mechanism in the receiver, using the square wave 1, 0, 1, 0 pattern. Following the preamble is the start of frame delimiter which in Ethernet is the pattern 1, 0, 1, 0, 1, 0, 1, 1. This delimiter is the starting marker for the beginning of the actual data. The start of frame delimiter indicates to the receiver to switch out of the hunting mode into the normal receive

mode, at which point the clock recovery is relatively "tight", requiring that the edges of the data transition fall within certain well defined timing boundaries. In this case, excessive timing jitter will cause failure of the normal receive mode and reversion to the hunting mode.

Clock recovery circuits have two desirable properties. First, such a circuit should quickly lock on to (synchronize to) the incoming data stream. This is often called the "hunting" mode, when the circuit is hunting for received data transitions and waiting, e.g. for a start of frame delimiter.

The second desirable property of a clock recovery circuit is input jitter tolerance in the normal receive mode. After the circuit has determined that it is receiving a data packet, it makes assumptions about where in each bit cell (timing window) valid data transitions i.e., pulse leading or trailing edges, are expected to occur. If a "rogue" transition occurs outside the expected portion of the bit cell, the circuit is able to compensate in the normal receive mode only very slowly. When the compensation is inadequate, data errors will occur, and the circuit may revert to the hunting mode.

The disadvantage of Manchester encoding is that it requires twice the actual signal bandwidth to transmit a given amount of data, for instance requiring 20 MHz of bandwidth to send 10 megabits per second of data.

Also, a system such as Ethernet typically uses analog clock recovery circuitry, including a phase lock loop and an associated analog filter to lock onto the received signal. This analog circuitry is typically complex and expensive. In contrast, the remainder of the receiver is typically digital circuitry. A typical Ethernet receiver therefore requires approximately 15 bits of data to synchronize (acquire the clock signal). Thus a significant amount of data is lost during the

synchronization process.

Therefore, it would be desirable to have a non-return to zero clock recovery circuit which does not require Manchester encoding (with its wasted bandwidth) or analog circuitry, and which does not have the disadvantage of operating in two distinct modes, with the ensuing slow synchronization.

SUMMARY OF THE INVENTION

Modeless (single mode) clock recovery uses a high speed clock signal to oversample an incoming data stream and divide each bit cell of the data stream into a particular number of subcells. When a data transition (a timing transition) occurs in the incoming data stream, digital logic determines whether the transition has occurred at an appropriate time (window) in the bit cell. If so, no modification is made to a receive clock signal synchronized to the high speed clock signal. If the data transition is slightly out of bounds from the window, a small modification is made to the time of the receive clock signal to bring it into alignment with the data stream. If the incoming data transition is several subcells (substantially) out of bounds from the window, a larger modification is made to align the receive clock signal to the data stream. In each case the clock adjustment occurs immediately, i.e. within one clock cycle of the high speed clock.

In one embodiment, the clock recovery circuit uses a modulo 20 counter with a parallel enable (load) input feature which is actuated by the timing transitions in the data stream, and associated combinatorial logic which determines the next counter state. The counter is loaded with the "correct" state value on every detected data transition. Additional logic synchronizes the incoming data transitions with the high speed clock signal and

synthesizes the receive clock signal from the counter state information. The incoming digital bit stream is an NRZ waveform which does not require Manchester encoding.

The clock recovery scheme in accordance with the invention is useful with a wireless hybrid asynchronous and time bounded local area network, i.e. a radio (or infra-red or other medium) type of LAN, and also with other applications requiring recovery of clock signals. Advantageously the circuit and method in accordance with the invention will acquire lock (synchronize) within one clock time of the high speed clock. The clock recovery circuitry in one embodiment is all digital.

In one embodiment, an input flip-flop and an output flip-flop provide deglitching and a window comparator correctly aligns the receive clock with the sampled data stream.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a timing diagram in accordance with the present invention.

Figure 2 shows a block diagram of a circuit in accordance with the present invention.

Figure 3 shows detail of the circuit of Figure 2.

Figures 4a, 4b, 4c and 4d show detail of the circuit of Figure 3.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 shows a timing diagram in accordance with the present invention. For example, an incoming serial bit data stream is at 0.5 MHz maximum frequency, so that each bit cell has a duration of 1 microsecond (as shown at the lower axis of Figure 1 depicting one bit cell). This one bit cell clock period is divided by an external high speed clock signal into 20 subcells, each of 50 nanoseconds duration as indicated by the upper horizontal

axis in Figure 1. If a detected timing edge at a station (receiver) of a LAN is in the first part of the bit cell (labelled "Edge" in Figure 1) i.e., in subcells 0 through 6, synchronization exists and no further action is required. If the detected timing edge is in another portion of the bit cell of Figure 1, then synchronization takes place by adjusting the subsequent receive clock pulse. In this example if the timing edge occurs in bit subcells 6 through 17, the adjustment is made. If the timing edge is in cells 17-20, no adjustment is made. Thus the output ("receive clock") signal RXC1 goes high during bit subcells 6 through 17 to provide the timing output signal.

It is to be understood that these values are exemplary only. Thus a high speed clock, in this case a 20 MHz clock signal, defines the bit subcell timing. It is also to be understood that the division of the bit subcell into 20 subcells is exemplary, and that other bit cell divisions such as into 10 subcells would also be operative.

A window comparator (as explained below) determines that if the count of a counter incremented by the high speed clock is between the values of 6 and 17, the receive clock (output) signal RXC1 will be high, and otherwise the receive clock signal is low. As explained below, if the detected edge of the incoming data occurs in the first 6 subcells, synchronization already exists; otherwise, if the incoming edge is detected in bit subcells 6 through 17, the counter is reloaded with a value that will effectively make it stay a few more counts; this pushes the occurrence of the subsequent edge into the first 6 subcells. Moreover, as explained above, the logic which performs the timing adjustment provides a variable output so as to ensure that the next edge is detected in the first 6 bit subcells of the high speed clock.

A circuit in accordance with the invention in Figure 2 includes an edge detector 20 which receives two signals, one of which is the received incoming data serial bit stream RXD and the second of which is a high speed clock signal CLK20, in this case a 20 MHz clock signal from an external source such as an oscillator. Signal RXD is digitized (in one embodiment) by a conventional slicer (not shown) so that upon receipt of an analog signal the slicer determines whether each successive portion of the signal is a 1 value or a 0 value. The slicer includes an analog comparator which averages the voltage value between the value assigned to digital 1 and the value assigned to digital 0 and determines a mid point. Any incoming signal above the mid point is assigned digital value 1, and any incoming signal below the mid point is assigned digital value 0. The slicer resets its midpoint threshold for each data frame i.e., each message data packet.

Edge detector 20 outputs an "Edge" signal to the PE (parallel enable) input terminal of modulo 20 counter 24, which has as a second input (to its clock terminal) the high speed clock signal CLK20. The output signal of counter 24 (i.e. the current count) is provided on a five line (in this case) bus 26 to Next Count combinatorial logic 28 which provides the adjustment as described above for the subsequent count. This adjustment is then provided on five line bus 30 to the data input terminals D of counter 24. The output of counter 24 on bus 26 is also provided to one set of input terminals of window comparator 34 which determines (as described above) whether the count has occurred within a given window within each bit cell i.e., counts 6 through 17. If so, the output receive clock signal RXC1 is generated. For instance, output signal RXC1 is a clock signal for use by a LAN station to be synchronized to input signal RXD.

It is to be understood that next count logic 28

provides the adjustment only if it is determined that the edge has not occurred within the first 6 bit subcells as illustrated in Figure 1; otherwise next count logic 28 provides no adjustment. In this case the detected edge has no effect on counter 24, and output signal RXC1 is synchronized to the high speed clock signal CLK20.

Detail of the circuit of Figure 2 in one embodiment is illustrated in Figure 3. Edge detector 20 of Figure 2 includes input flip-flop 40 which receives the input, data RXD from the slicer (not shown) at its data input terminal D and high speed clock signal CLK20 at its clock input terminal. Flip-flop 40 is a D-type flip-flop provided for de-glitching purposes. The output signal on the Q terminal of flip-flop 40 is provided to exclusive OR gate 42, the second input of which is the RXD signal. Thus the "Edge" signal which is the output of exclusive OR gate 42 is provided only if the most recent signal RXD is opposite to the previously clocked-in signal to flip-flop 40. Thus the exclusive OR gate 42 goes high indicating presence of an edge.

The Edge signal is provided to modulo 20 counter 24 at its PE (parallel enable) terminal. Hence modulo 20 counter 24 is a counter with a "load" feature. Modulo 20 counter 24 counts up from zero to 19 and provides its counted output on terminals Q0 through Q4 on five line bus 26 to both window comparator 34 and to the next state logic 28. Next state logic 28 has corresponding input terminals Q0 through Q4 and provides output signals on terminals N0 through N4.

Detail of next state logic 28 is shown in Figures 4a, 4b, 4c and 4d. The intermediate signals Q0B through Q4B as shown are generated by inverters. (The inverter for signal Q4B performs the same function, but has more "power" so it can drive more outputs.) Thus the combinatorial logic in next state logic 28 as illustrated

in Figures 4a-4d provides the variable count adjustments depending on the value of the count output by counter 24. These count adjustments provided on terminals N0 through N4 are fed back to the D input terminals D0 to D4 of counter 24 by five line bus 30 to adjust the count variably. The combinatorial logic shown in Figures 4a-4d hence is composed exclusively of AND gates, OR gates and inverters.

Window comparator 34 includes a first five bit comparator 50, and a second five bit comparator 52. The B input terminals B0 to B4 of comparator 50 are hard-wired to a set of buffers providing a fixed value of six. The B input terminals B0 to B4 of comparator 52 are hard wired to a second set of buffers providing a fixed value of seventeen. Thus comparator 52 is a greater than six comparator and comparator 52 is a less than seventeen comparator. The output signals of each of comparators 50, 52 are provided as input signals to AND gate 56 which provides an the output signal to the output of data terminal D of flip flop 60 which is a deglitcher. The output signal on terminal Q of flip flop 60 is the signal RXC1 which is the receive clock signal.

Thus the actual "intelligence" in the circuit of Figure 3 is provided by the combinatorial logic of Figures 4a through 4d. Explanation of the function of this logic is shown generally in Figure 1.

More specifically, the logic of Figures 4a through 4d provides the count adjustment of Table I:

TABLE I

Value of Q (count)	Value of N (correction)	Next Count - Adjusted Value of Q
0	0	1
1	1	1
2	1	2
3	1	3
4	2	3
5	2	4
6	2	5
7	3	5
8	3	6
9	3	7
10	11	0
11	3	15
12	3	16
13	3	17
14	2	17
15	2	18
16	2	19
17	1	19
18	1	0
19	0	0

The reset signals for flip flop 40 and counter 20 (to terminals R and RD respectively) are provided when the circuit is powered up. In this particular embodiment since high speed clock signal CLK20 is at 20 MHz and counter 20 is a modulo 20 counter, receive clock signal RCX1 is a 1 MHz signal.

The output de-glitching flip flop 60 provides a one count delay. Thus, in another embodiment where deglitching is of less concern flip flop 60 is eliminated and the upper comparator 50 set to sense a count greater than seven.

To describe the operation of the circuit of Figure 3 in another way, the circuit only operates if an edge occurs on the input data bit stream. If an edge occurs and it is inside the desired window at the first part (e.g. subcells 0 to 6) of the one microsecond (in this case) duration of each bit cell, the output clock signal

is already synchronized to the high speed external clock signal and no further action is needed. If otherwise, that is if the edge is detected in the central part (subcells 7 to 17) of the bit cell, the count is adjusted by loading a value into the counter from the next state logic so that the output counter value is what is desired, i.e. indicating a count in bit subcells 0 to 6. Thus the next count is the current count plus a predetermined value from next state logic 28.

The above description is illustrative and not limiting; further modifications will be apparent to one of ordinary skill in the art and the invention is limited only by the appended claims.

I claim:

1. A method of recovering a timing transition from serial data, comprising the steps of:

providing a clock signal;

oversampling the serial data at a rate determined by the clock signal;

determining if the oversampled timing transition occurs in a predetermined interval defined by the clock signal;

providing an output signal synchronized to the clock signal if the timing transition occurs in the predetermined interval; and

if the timing transition does not occur in the predetermined interval, providing the output signal at a time variably related to the timing transition, thereby synchronizing the output signal to the timing transition.

2. The method of Claim 1, wherein the timing transition is an edge of a non-return to zero signal.

3. The method of Claim 1, wherein the step of oversampling comprises:

dividing the serial data into a plurality of cells; and

dividing each of the plurality of cells into a plurality of subcells, one subcell occurring for each pulse of the clock signal.

4. The method of Claim 1, wherein the second step of providing occurs within one timing transition interval.

5. The method of Claim 1, wherein the predetermined interval is of a constant length.

6. An apparatus for recovery of timing transition signals from serial data, comprising:

an edge detector for detecting timing transitions in the serial data, and providing an edge signal in response;

a counter for counting a clock signal and which is enabled by the edge signal;

a logic network for variably incrementing the counter when the counter is enabled by the edge signal; and

a window comparator for providing an output signal only when the counter output signal is within a predetermined range of values, thereby synchronizing the output signal to the timing transitions.

7. The apparatus of Claim 6, wherein the logic network variably increments the counter only if the timing transitions occur outside of a predetermined interval, and the amount of the increment is larger the farther the timing transitions are from a boundary of the predetermined interval.

8. The apparatus of Claim 6, wherein the edge detector comprises:

a flip-flop for receiving the serial data at its data input terminal and receiving the clock signal at its clock input terminal; and

an exclusive OR gate having two input terminals and receiving the serial data at one input terminal and an output signal of the flip-flop at its second input terminal.

9. The apparatus of Claim 6, wherein the counter receives the edge signal at a parallel enable input

terminal and the clock signal at a clock input terminal, and provides an output signal to the logic network, an output signal of the logic network being provided to data input terminals of the counter.

10. The apparatus of Claim 6, further comprising a flip-flop for receiving the output signal from the window comparator.

11. The apparatus of Claim 6, wherein the counter counts to a maximum value of N, and the ratio of the clock signal frequency to a maximum frequency of the serial is N.

12. The apparatus of Claim 6, wherein the logic network includes only combinatorial logic elements.

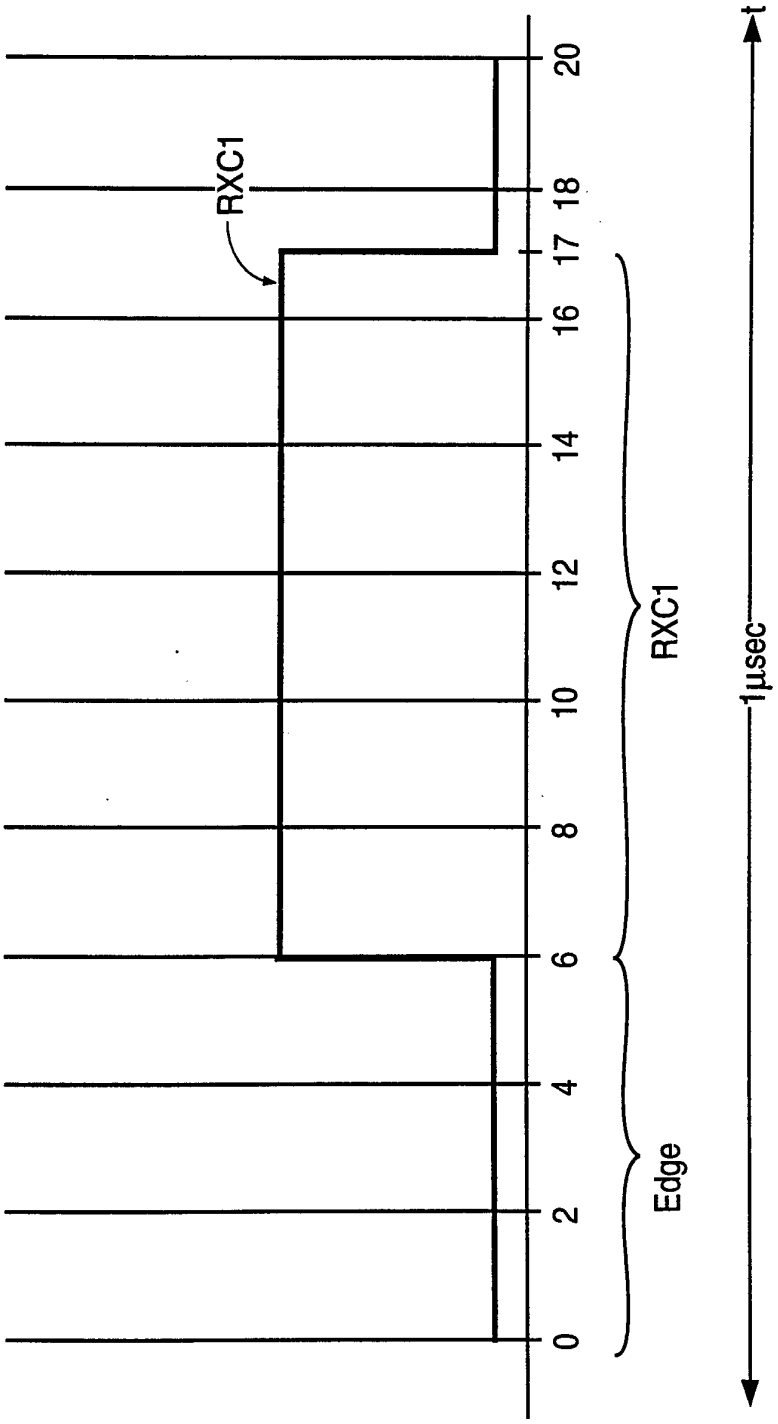

FIG. 1

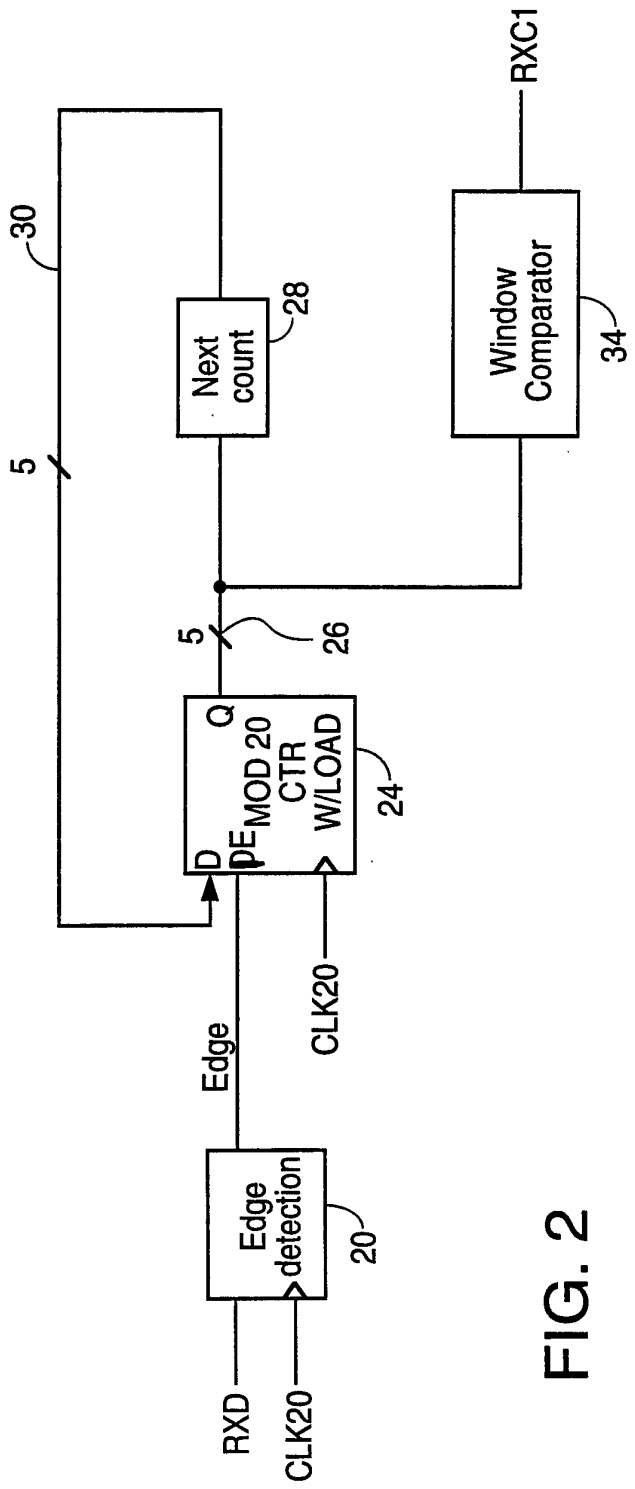
RXC1
30
Next count
28
Window Comparator
34
5
5
26
Q
D
PE
MOD 20 CTR W/LOAD
24
Edge
CLK20
Edge detection
20
RXD
CLK20

FIG. 2

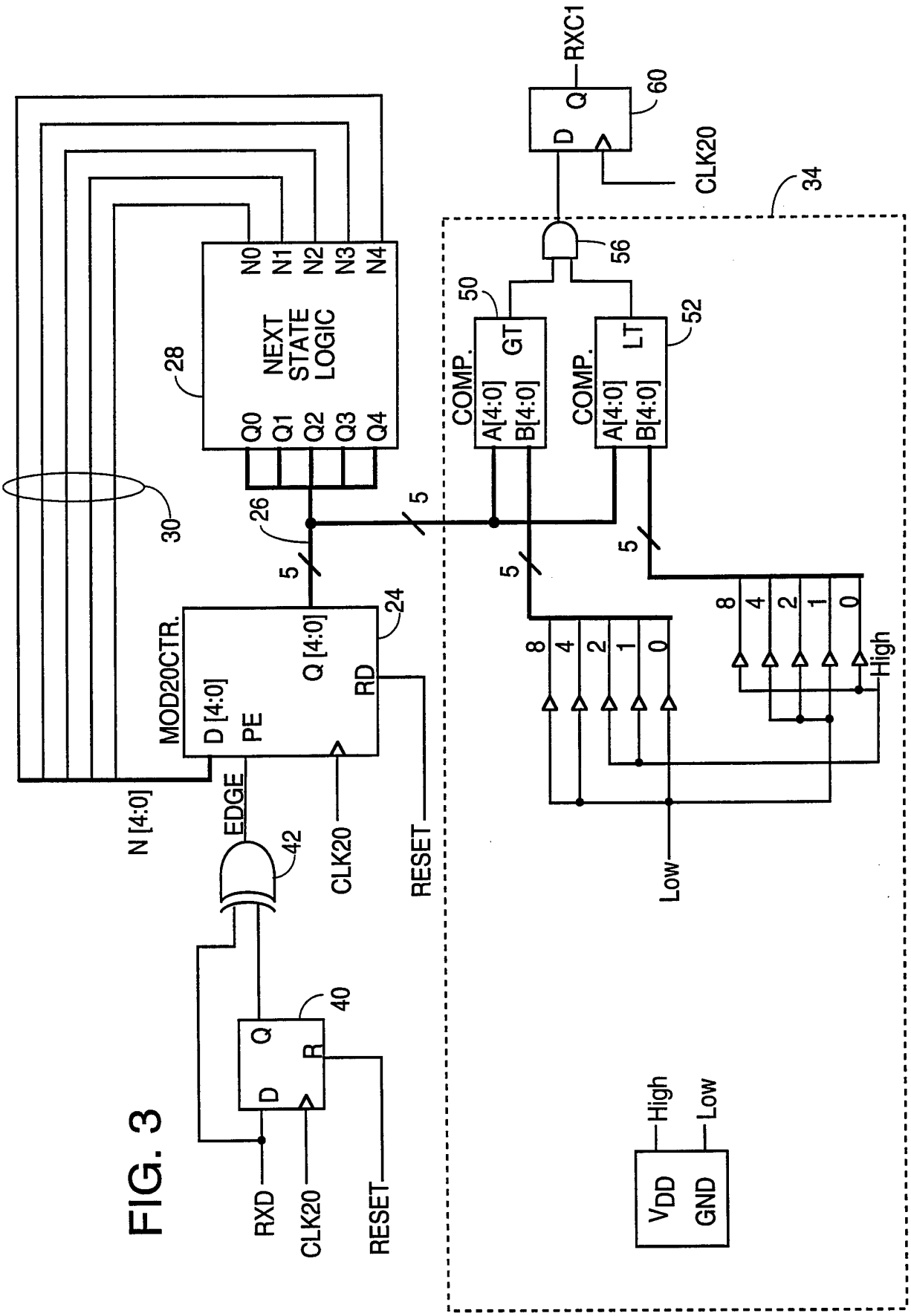
RXC1
60
D
Q
CLK20
34
56
50
52
COMP.
A[4:0]
B[4:0]
GT
LT
28
NEXT STATE LOGIC
N0
N1
N2
N3
N4
Q0
Q1
Q2
Q3
Q4
30
26
5
MOD20CTR.
D [4:0]
PE
Q [4:0]
RD
24
8
4
2
1
0
High
Low
N [4:0]
EDGE
42
CLK20
RESET
40
Q
D
R
RXD
CLK20
RESET
VDD
GND
High
Low

FIG. 3

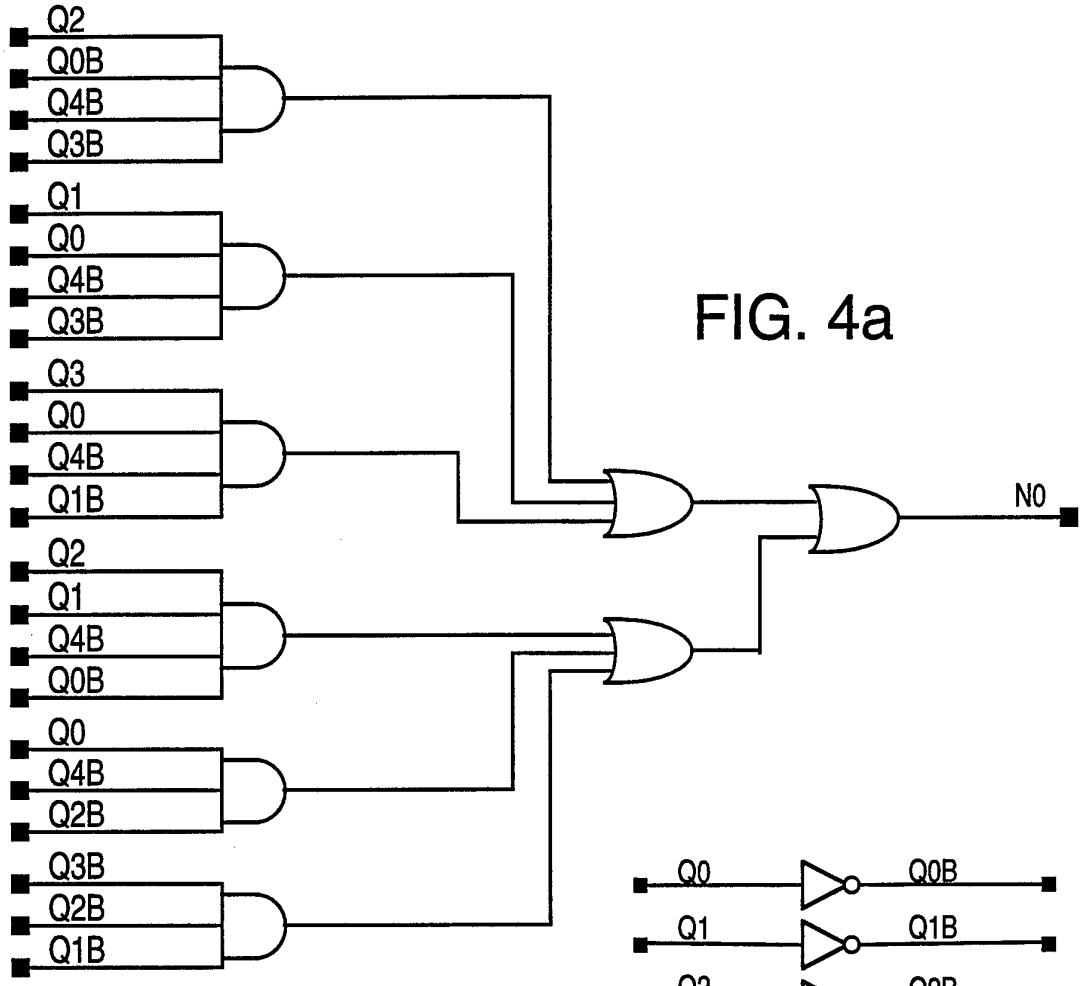

FIG. 4a

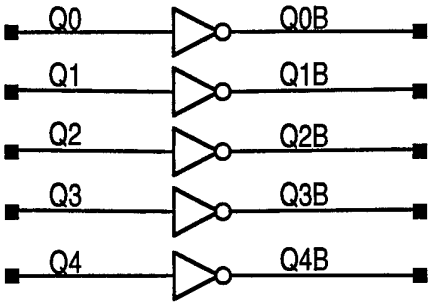

FIG. 4b

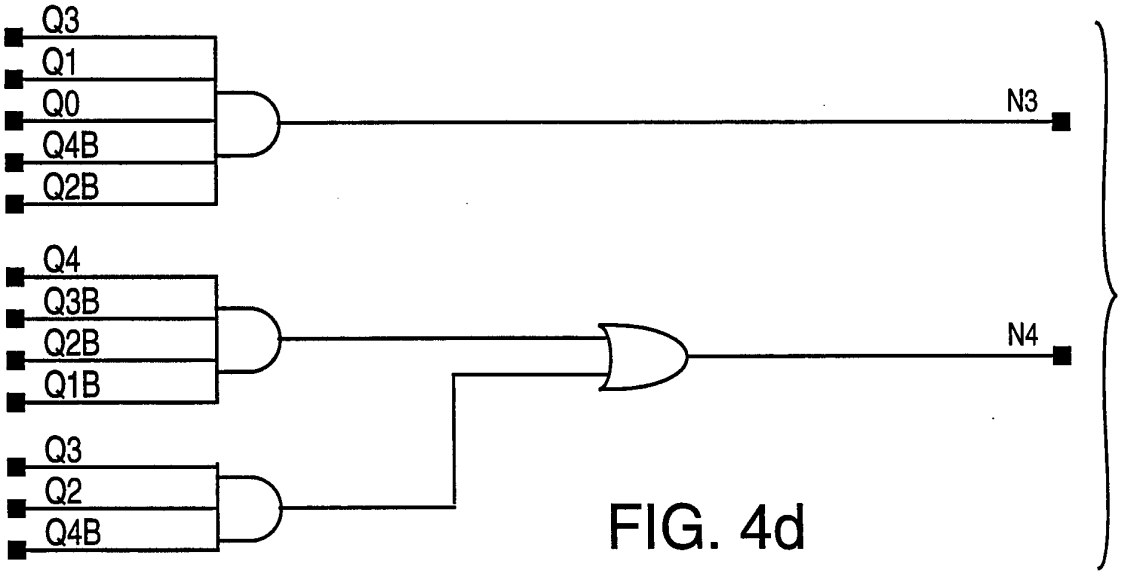

FIG. 4d

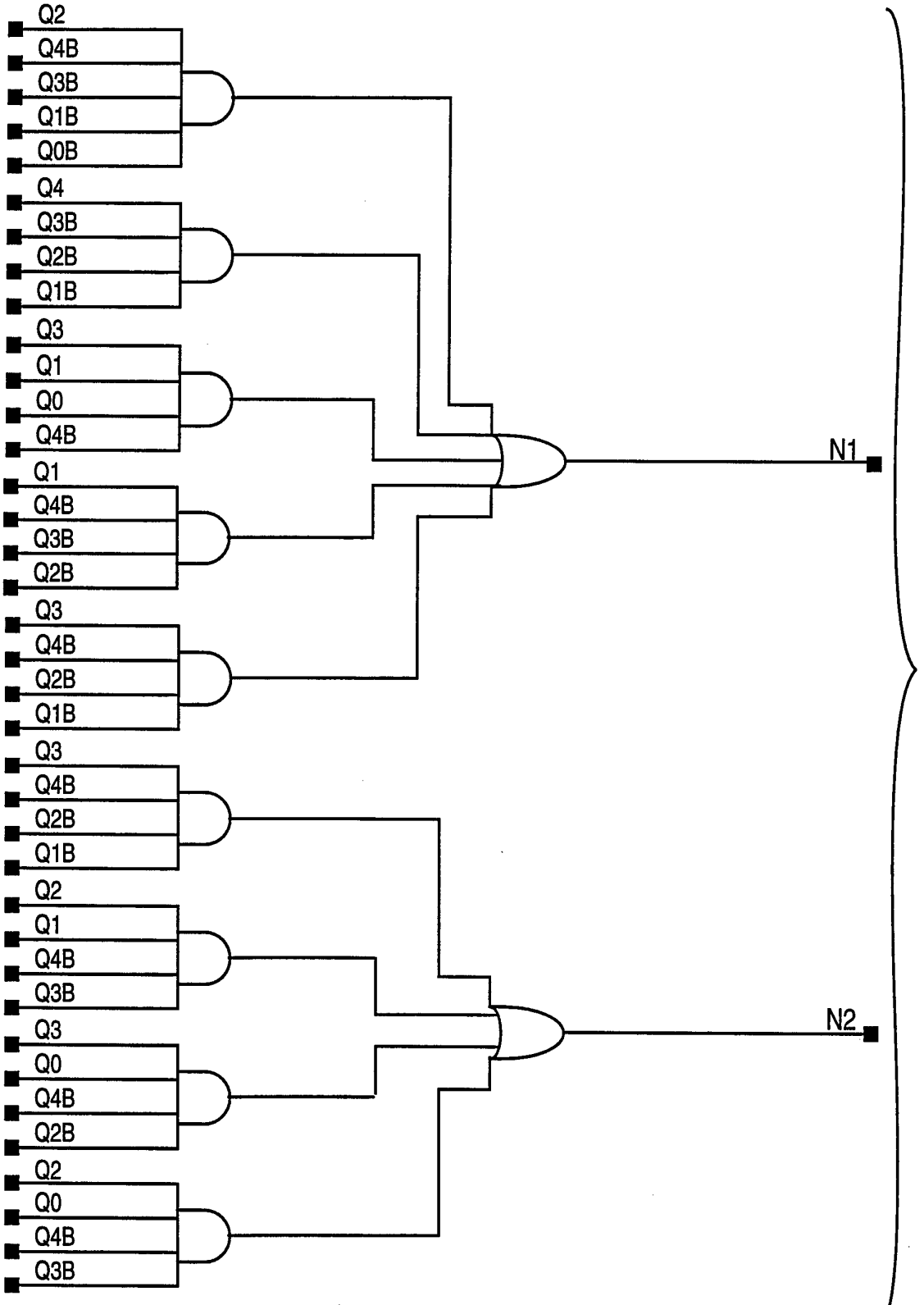
Q2
Q4B
Q3B
Q1B
Q0B
Q4
Q3B
Q2B
Q1B
Q3
Q1
Q0
Q4B
Q1
Q4B
Q3B
Q2B
Q3
Q4B
Q2B
Q1B
Q3
Q4B
Q2B
Q1B
Q2
Q1
Q4B
Q3B
Q3
Q0
Q4B
Q2B
Q2
Q0
Q4B
Q3B
N1
N2

FIG. 4c

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/07001

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : H04L 7/02; H03D 3/24
US CL : 375/110, 119
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/110, 119, 111, 113, 4; 341/68, 69; 360/ 41, 44

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---- Y	US, A, 5,185,768 (FERRAIOLO ET AL.) 09 February 1993, see col. 4, line 1 through col. 7, line 43, and figure 2.	1-2, 4-7 ------- 8
Y	US, A, 4,694,196 (HASLEY ET AL.) 15 September 1987, see figure 1.	8
A	US, A, 5,197,082 (UDA ET AL.) 23, March 1993, see abstract and figure 2.	1-12
A	US, A, 5,197,086 (JACKSON ET AL.) 23 March 1993, see abstract and figure 1.	1-12

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"O"	document referring to an oral disclosure, use, exhibition or other means		
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