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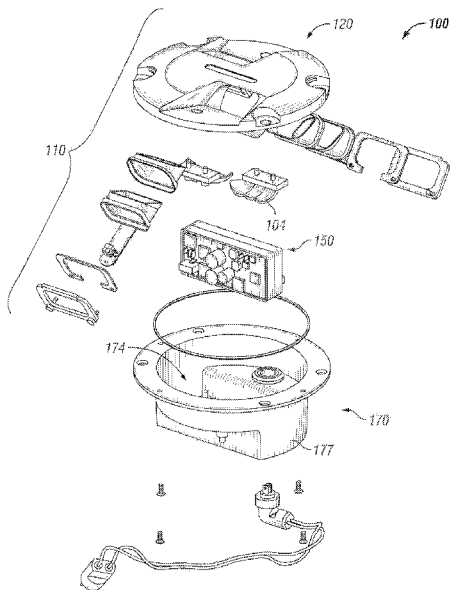


FIG. 1

(57) Abstract: The present disclosure provides techniques for power factor correction on a constant current system and also provides power line communications on the same power factor correction circuit. In one example embodiment, through controlled charging and draining of an input capacitor, the power factor correction circuit generates an input voltage which is in phase with the input current. Communication data is also embedded in the input voltage and/or input current by further charging and draining of the input capacitor according to a controlled switching scheme which includes both input current phase data and corresponding communication signals.



POWER FACTOR CORRECTION FOR CONSTANT CURRENT INPUT WITH POWER LINE COMMUNICATION

TECHNICAL FIELD

[0001] The present disclosure relates generally to power line communication on a power factor correction circuit. Specifically, the present disclosure relates to techniques for providing power line communication and power factor correction in a system having a constant current input.

BACKGROUND

[0002] Power factor correction is often used in electric power systems and between power sources and loads in order to synchronize the input current and the input voltage before it is delivered to the load. Power factor correction can provide many benefits to the electric power system and the load, such as prolonged life and energy efficiency.

[0003] Traditionally, power factor correction circuitry is designed as voltage based power factor correction. Such circuitry is used in constant voltage systems, and the input current waveform is made to match the input voltage waveform. However, in certain industries, such as airfield lighting, the existing infrastructure requires current based systems which require a constant current power source rather than a constant voltage power source. Specifically, in the area of airfield lighting, constant current systems are traditionally used because of the need for consistent brightness across the plurality of light fixtures coupled in series and being powered by the same power source. Because a constant current power supply can provide the same level of current to each of the light fixtures, it became the standard form of power distribution in the area of airfield lighting. Though lighting technology has become more sophisticated in recent years, the infrastructure has remained a current based system. However, power factor correction techniques used for voltage based systems which receive a constant voltage generally cannot be used for current based systems.

[0004] Additionally, in many modern lighting systems, light fixtures are able to communicate with a central controller. For example, a light fixture may send a signal to the central controller indicative of operational data or error. The central controller may also send a signal to a light fixture containing an operational command or status request. In the airport lighting industry, such communication can be done through power line communication, in which communication and control signals can be sent between the central controller and light

fixtures. Typically, an amplifier is used to add a higher frequency communication signal on top of the power line signal, such as a typical 60 hertz power line signal. A receiver is then used at the receiving end to decode the communication signal. Consequently, such communication systems typically require additional hardware and present several challenges, such as attenuation, error checking, and slow hardware.

SUMMARY

[0005] In an example embodiment of the present disclosure, a power factor correction circuit with power line communication includes an input capacitor configured to receive an input current from a constant current source and produce an input voltage, and a switching device coupled to the input capacitor, wherein the switching device switches between an OFF state and an ON state. The input voltage rises when the switching device is in the OFF state and drops when the switching device is in the ON state. The circuit includes a controller coupled to the switching device, wherein the controller controls switching of the switching device, and the switching of the switching device shapes the input voltage to be in phase with the input current. The switching of the switching device generates disturbances on the input voltage and input current, the disturbances having communication data.

[0006] In another example embodiment of the present disclosure, a controller for a power factor correction (PFC) circuit with power line communication includes a controller configured to receive an input current from a PFC circuit, an output voltage from the PFC circuit, and a communication signal. The controller generates a sine wave reference synchronized with the input current and adds the communication signal to the sine wave reference. The controller comprises a feedback controller configured to compare the output voltage to a reference voltage and produce a feedback controller output, wherein the feedback controller output increases when output voltage is below the reference voltage and decreases when the output voltage is above the reference voltage. The feedback controller output is multiplied with the summation of the sine wave reference and the communication signal to produce a control signal. A pulse width modulation (PWM) generator receives the control signal and converts the control signal into a corresponding PWM signal, wherein the PWM signal controls at least a portion of the PFC circuit. The PFC circuit shapes an input voltage to be in phase with the input current, and the input current, input voltage, or both include communication data reflective of the communication signal.

[0007] In another example embodiment of the present disclosure, a method of controlling a power factor correction (PFC) circuit having power line communication

includes receiving an output voltage from a PFC circuit, receiving a reference voltage indicative of a desired power level of the output voltage, comparing the output voltage to the reference voltage, generating a feedback controller output based on the difference between the output voltage and the reference voltage. The method further includes receiving a sine wave reference synchronized with an input current from the PFC circuit, receiving a communication signal to be transmitted over the PFC circuit, summing the sine wave reference and the communication signal, and multiplying the feedback controller output by the sum of the sine wave reference and the communication signal to produce a sine control signal. The method also includes controlling the PFC with the sine control signal and shaping an input voltage to be in phase with the input current.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the disclosure and the advantages thereof, reference is now made to the following description, in conjunction with the accompanying figures briefly described as follows:

[0009] Figure 1 illustrates a light fixture powered by a constant current system and having a power factor correction circuit with power line communication, in accordance with an example embodiment of the present disclosure;

[0010] Figure 2 illustrates a schematic diagram of a power factor correction circuit with power line communication for a constant current system, in accordance with an example embodiment of the present disclosure;

[0011] Figure 3 illustrates a diagram of a controller of the power factor correction circuit with power line communication of Figure 1, in accordance with an example embodiment of the present disclosure; and

[0012] Figure 4 illustrates a flow chart of a method of current-based power factor correction, in accordance with an example embodiment of the present disclosure; and

[0013] Figure 5 illustrates a flow chart of a method of controlling a power factor correction circuit with power line communication, in accordance with an example embodiment of the present disclosure.

[0014] The drawings illustrate only example embodiments of the disclosure and are therefore not to be considered limiting of its scope, as the disclosure may admit to other equally effective embodiments. The elements and features shown in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of

example embodiments of the present disclosure. Additionally, certain dimensions may be exaggerated to help visually convey such principles.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0015] In the following paragraphs, the present disclosure will be described in further detail by way of examples with reference to the attached drawings. In the description, well known components, methods, and/or processing techniques are omitted or briefly described so as not to obscure the disclosure. As used herein, the “present disclosure” refers to any one of the embodiments of the disclosure described herein and any equivalents. Furthermore, reference to various feature(s) of the “present disclosure” is not to suggest that all embodiments must include the referenced feature(s). The present disclosure provides systems and methods of power factor correction and integrated power line communications operating on a constant current input source. The present disclosure is directed towards power distribution systems in the area of airfield lighting as an example application, but may be used with any other appropriate power distribution and power line communication system operating on a constant current input source.

[0016] In certain example embodiments, the present disclosure provides a power factor correction circuit having power line communication capabilities for use in systems with constant current input sources. In one example, the power factor correction circuit with power line communication is used in an airfield lighting system which includes a plurality of individual light fixtures. Each of the light fixtures receives a constant current power supply from a central power source and can communicate with a central controller. In certain example embodiments, each or a subset of the light fixtures includes the power factor correction circuit with power line communications disclosed herein, which improves the energy efficiency of the light fixtures as well as the effectiveness and reliability of communication.

[0017] Figure 1 shows an exploded perspective view of one such light fixture 100 in accordance with certain example embodiments. Referring now to Figure 1, the light fixture 100 is an example of an airport runway and/or taxiway light fixture. The light fixture 100 of Figure 1 includes a frame, a light source 104, and a power supply 150. The frame can include a cover 170 and optical housing 120. The light fixture 100 further includes an optical housing assembly 110. The optical housing assembly 110 includes the combination of one or more components associated with the mechanical structure and configuration of the optical

housing 120 and other optical components, such as a body, lens, diffuser, connectors, and the like.

[0018] In certain example embodiments, the cover 170 includes at least one wall 177 that forms a cavity 174. Inside of the cavity 174 can be positioned at least one or more light sources 104 and the power supply 150. The cover 170 can include one or more features (*e.g.*, ledges, apertures) that allow the various components disposed in the cavity 174 to fit and maintain electrical, mechanical, and/or thermal coupling with each other. The optical housing 120 protects the components disposed within the cavity 174, and can also secure the light sources 104 and the other internal components 130.

[0019] The power supply 150 includes one or more circuits and electrical components configured to receive the constant current input from the central power source, condition the received current, and drive the light sources 104. In certain example embodiments, the power supply includes the power factor correction circuit with power line communications disclosed herein. In certain example embodiments, the constant current input is conditioned for power factor correction before it is supplied to the light sources 104, thereby improving energy efficiency. Additionally, the power line communications provided by the power factor correction circuit allows the light fixture 100 to be controlled by a central controller and exchange data with the central controller.

[0020] Figure 2 illustrates a schematic diagram of a power factor correction (PFC) circuit with power line communications 200, in accordance with an example embodiment of the present disclosure. In certain example embodiments, the PFC circuit with power line communications 200 includes an input source 202, an input charging capacitor 204, a first inductor 212a, a first switching MOSFET 210a, and a first output diode 216a. The PFC circuit with power line communications 200 further includes a second inductor 212b, a second switching MOSFET 210b, a second output diode 216b, a controller 220, an output capacitor 214, and a DC output bus 224. The input source 202 provides a constant current power supply to the circuit 200. In certain example embodiments, the input source 202 provides a 6.6 amp, 60 hertz, sine wave. In certain example embodiments, the PFC circuit with power line communications 200 is largely identical to a PFC circuit for a constant current source. Specifically, the power line communication functions of the PFC circuit with power line communications 200 are readily carried out by a PFC circuit for a constant current source without additional communications hardware or cost.

[0021] PFC circuit with power line communications 200 provides power factor correction between the constant current power input source 202 and a load, such as a light

fixture. Specifically, the PFC circuit with power line communications 200 receives power from the constant current input source 202 and outputs DC power via the DC output bus 224 to a load. The PFC circuit with power line communications 200 shapes the waveform of the input voltage at the input charging capacitor 204 to follow and be synchronized with the waveform of the input current. In certain example embodiments, the waveform of the voltage is at least partially shaped by controlling the charging and draining of the input charging capacitor by the first and second MOSFETs 210a, 210b. The input source 202 provides a constant alternating current, which is positive during one half cycle and negative during the other half cycle. Rather than rectifying the input current by using a diode rectifier bridge, the PFC circuit with power line communications 200 utilizes two MOSFETs 210a, 210b, coupled to the circuit 200 in opposite directions. Typically, a diode rectifier bridge includes a plurality (e.g., 4) of diodes, which results in a relatively large power loss. Thus, the ability to handle an alternating current without the use of a rectifier bridge significantly increases energy efficiency. However, in certain example embodiments of the PFC circuit with power line communications 200, the circuit 200 includes a diode rectifier bridge for rectifying the input current. In such an embodiment, only one MOSFET is needed as the MOSFET will always be biased in the operation direction relative to the rectified current. In certain example embodiments, other appropriate switching devices are used in place of the MOSFETs.

[0022] For example, the first MOSFET 210a is in operation to control charging and draining of the input charging capacitor 204 when the input current is on the first half cycle (e.g., positive). During this time, the second MOSFET 210b, which is biased in the wrong direction when the current is in the first half cycle, acts as a short. Likewise, when the input current is in the second half cycle (e.g., negative), the second MOSFET 210b, which is now biased in the operational direction, can be switched to control the charging and draining of the input charging capacitor 204. During this time, the first MOSFET 210a, which is now biased in the wrong direction, acts as a short. In certain example embodiments, the first MOSFET 210a works in conjunction with the first inductor 212a and the first output diode 216a to produce a voltage having a waveform which matches the input current waveform. Likewise, the second MOSFET works in conjunction with the second inductor 212b and the second output diode 216b.

[0023] The following describes, in further detail, the operation of the PFC circuit with power line communications 200 for power factor correction purposes and how it is controlled to produce a voltage waveform which is matched to the input current. Subsequently, the

power line communication functions of the PFC circuit with power line communications 200 will be described.

[0024] The first and second MOSFETs 210a, 210b may sometimes be referred to generically as “the MOSFET 210”. The MOSFET 210 refers to either the first or second MOSFET 210a, 210b, depending on which half cycle the input current is in, as the first and second MOSFETs 210a, 210b are identical in their operation relative to their given half cycle. Thus, the general operation of both the first MOSFET 210a and the second MOSFET 210b is described in terms of the MOSFET 210 for sake of brevity. Likewise, the first and second inductors 212a, 212b, which are respectively associated with the first and second MOSFETs 210a, 210b, may be referred to as “the inductor 212.” Additionally, the first and second output diodes 216a, 216b, which are respectively associated with the first and second MOSFETs 210a, 210b, may be referred to as “the output diode 216.” The first MOSFET 210a and the second MOSFET 210b will be separately identified when a distinction is to be made.

[0025] Still referring to Figure 2, in certain example embodiments, the input source 202 is directly coupled to the input charging capacitor 204. The input current from the constant current input source 202 charges the input charging capacitor 204 when the MOSFET 210 is in an off state. In certain example embodiments, the MOSFET 210 is initially off. Thus, in this state, the input current from the constant current input source 202 charges the input charging capacitor 204. As the input current charges the input charging capacitor 204, a voltage rise occurs in the input charging capacitor 204. When the voltage rises to a certain threshold level, the MOSFET 210 is switched on. In certain example embodiments, the threshold level is determined by a reference voltage 222 such that the voltage at the input charging capacitor 204 is allowed to rise until it reaches the level of the reference voltage 222. In certain example embodiments, the controller 220 provides the reference voltage 222 and also receives a sensed voltage signal 226 of the voltage at the input charging capacitor 204. The controller 220 also receives a sensed current signal 206 from the input current. In certain example embodiments, the reference voltage 222 is indicative of the level of desired output power, or the amplitude of the voltage waveform. The controller 220 compares a sensed voltage signal 226 to the reference voltage 222 and controls the MOSFET 210 accordingly. The controller 220 will be described in further detail below with respect to Figure 3. The controller 220 sends a switching signal to both the first MOSFET 210a and the second MOSFET 210b. However, only one of the first and second MOSFETs 210a, 210b will be able to operate accordingly at one time.

[0026] When the voltage at the input charging capacitor 204 reaches the reference voltage 222, the MOSFET 210 is switched on. When the MOSFET 210 is switched on, current is drained from the input charging capacitor 204 and the voltage drops accordingly. Thus, voltage at the input charging capacitor 204 rises when the MOSFET 210 is off and drops when the MOSFET 210 is on, creating a waveform which follows the duty cycle of the MOSFET 210. During the time the MOSFET 210 is on, current rises in the inductor 222. Thus, when the MOSFET 210 is switched off again, the inductor flies back and delivers energy, which is rectified by the output diode 216, to the output capacitor 214. The voltage at the output capacitor 214 is provided to a DC output bus 224 and configured to be delivered to a load. As the MOSFET 210 switches at a high frequency (hundreds of kHz) according to a controlled duty cycle, the instantaneous voltage at the input charge capacitor 204 will match the reference voltage of each cycle. Thus, a sine wave input voltage in which the waveform is matched to the waveform of the input current is created over time. Specifically, for example, during the first half cycle, the first MOSFET 210a is switchable, by the controller 220, between the on state and the off state. During the second half cycle, the second MOSFET 210b is switchable, by the controller 220, between the on state and the off state.

[0027] In another example embodiment, the controller 220 does not necessarily monitor the input voltage 226. Rather, the switching device is provided with a pulse width modulation signal shaped like a sine wave regardless of the input voltage, which forces the input voltage to take on a waveform as defined by the pulse width modulation signal.

[0028] In another embodiment of the present disclosure, the PFC circuit with power line communications 200 includes a flyback configuration. In such an embodiment, the first and second inductors 212a, 212b are replaced with first and second transformers (not shown), respectively. The secondary windings of the first and second transformers provide the output voltage. However, because the transformers provide a variable transformer ratio, the level of output voltage can be controlled by adjusting the transformer ratio.

[0029] As briefly discussed, the PFC circuit with power line communications 200 is able to provide, carry, and read communication signals in addition to power line input without the addition of extra components or costs to the base PFC circuit 200. In certain embodiments, the base PFC circuit 200 is configured differently and contains different components for the purpose of carrying out power factor correction. Such modifications should not be seen as additional components for carrying out power line communications, but rather as embodiments of the disclosed base PFC circuit 200. Indeed, rather than using additional communications equipment to drive communication signals onto power lines, the

PFC circuit with power line communications 200 allows the duty cycle of the switching MOSFETs 110 in the PFC circuit 200 to be manipulated to create controlled voltage and current disturbances on the input voltage 226 and current 206. The voltage and current disturbances are or represent the communication signal to be transmitted. The communication signal is then read by the controller 220 or other processor at the load. In certain example embodiments, the communication signal to be transmitted is provided and embedded in the power signal by the controller 220 of the sending device, the details of which are further provided below with respect to Figure 3.

[0030] Figure 3 illustrates a diagrammatical representation of the controller 220 of Figure 2, in accordance with an example embodiment. The controller 220 provides switching control of the MOSFETs 210 for power factor correction purposes as well as power line communication purposes. For power factor correction purposes, the controller 220 includes a feedback controller 302 which receives, as inputs, a sense output voltage 303 from the DC output bus 224 and the reference voltage 222. The value of the reference voltage 222 is typically selected according to the desired amount of power to be provided at the DC output bus 224. The value of the sensed output voltage 303 is compared with the value of reference voltage 222. If the value of the sensed output voltage 303 is below the value of the reference voltage 222, the output 304 of the feedback controller 302 will increase. If the value of the sensed output voltage 303 is above the value of the reference voltage 222, the output 304 of the feedback controller 302 will decrease. The output 304 of the feedback controller 302 is then multiplied 306 by a sine wave reference 308. In certain example embodiments, the input current signal 206 is applied to the sine wave reference 308 to synchronize the sine wave reference 308 with the input current signal 206. Thus, the output 310 of the multiplication 306 of the sine wave reference 308 and the feedback controller output 304 is a sine control signal 310 which varies in amplitude with the feedback controller output 304.

[0031] In certain example embodiments, such as when a communication signal is to be sent over the power lines, a communication signal 314 is added to the sine wave reference 308. Thus, the summation 307 of the sine wave reference 308 and the communication signal 314 is synchronized with the input current waveform and also includes the communication signal 314. In such an embodiment, the summation 307 of the sine wave reference 308 and the communication signal 314 is multiplied with the feedback controller output 304 to produce a sine wave 310 which varies in amplitude with the feedback controller output 304, and includes input current synchronization 308 and the communication signal 314.

[0032] In certain example embodiments, the controller 220 further includes a pulse width modulation (PWM) generator 312. The PWM generator 312 receives as input, the sine control signal 310 and converts the sine control signal 310 into a pulse width modulation signal 316. The pulse width modulation signal 316 is used to drive the MOSFET 210 (Figure 2). In certain example embodiments, the duty cycle of the pulse width modulation signal 316 decreases to increase the input voltage 226, and the pulse modulation signal 316 increases to decrease the input voltage 226. At the peaks of the sine control signal 310, the pulse width modulation signal 316 is at its controlled minimum, and the input voltage is at its peak. Thus, the peaks of the input voltage waveform are matched to the peaks of the sine control signal 310, which has been synchronized with the input current 206. Therefore, the input voltage waveform is matched to that of the input current 206.

[0033] In certain example embodiments, the sine control signal 310 includes communication content 318 from of an embedded communication signal 314. As such, the PWM generator 312, upon receiving such a sine wave, will produce a variable duty cycle that not only controls MOSFET switching for power factor as described above, but also controls MOSFET switching to create a signal on the voltage waveform on the input voltage 226 which carries communication data 318 representative of the communication signal 314. Such communication data 318 can be seen as disturbances 318 on the input voltage 226 and current 206 waveforms, which can be seen and/or read by other devices, controllers, or processors in the load or in the system.

[0034] Figure 4 illustrates a method 400 of power factor correction for a constant current system, in accordance with an example embodiment. Figure 5 illustrates a method 500 of controlling the PFC circuit with power line communications 200, in accordance with an example embodiment. Specifically, in certain example embodiments, the method of power factor correction 400 is implemented via the power factor correction circuit of Figure 2 and the method of controlling 500 the PFC circuit with power line communications 200 is implemented via the controller 220 illustrated in Figure 3. Referring to Figures 2 and 4, the method 400 of power factor correction includes receiving an input current from a constant current input source 202 (step 402). The method 400 further includes allowing the input capacitor 204 to be charged (step 406). Specifically, in certain example embodiments, the MOSFET 210 is initially in the off state. As previously discussed, when the MOSFET 210 is in the off state, the input capacitor charges, and the input voltage increases. In certain example embodiments, the input voltage is constantly being monitored by the controller 220 via the input voltage sense 226. The method further includes determining whether the input

voltage has reached the reference voltage (block 408). In certain example embodiments, the reference voltage includes an amplitude indicative of the desired level of power output as well as a phase which is synchronized with the input current.

[0035] In order to make the determination, the controller 220 compares the value of the input voltage to the value of the reference voltage. If it is determined that the input voltage is less than the reference voltage, the method goes to step 406, in which the MOSFET 210 remains off and the input capacitor is allowed to charge. As discussed, the MOSFET 210 (first MOSFET 210a or second MOSFET 210b) that is operational depends on the half (positive or negative) of the input current cycle. In certain example embodiments, steps 406 and 408 are repeated until it is determined at step 408 that the input voltage has reached the reference voltage. In certain example embodiment, the controller 220 constantly monitors the input voltage and reacts when the sensed voltage value reaches a threshold representative of the reference voltage. When it is determined that the input has reached the reference voltage, the MOSFET 210 switches on (step 410).

[0036] Specifically, in certain embodiments, it is determined whether the input current is on the first half cycle (step 411). If the input is on the first half cycle, then the first MOSFET 210a is correctly biased and operational. Therefore, the first MOSFET 210a turns on (block 410a). If the input current is not on the first half cycle, then it must be on the second half cycle. In that case, the second MOSFET 210b turns on (step 410b). When the MOSFET 210 (either first MOSFET 210a or second MOSFET 210b) turns on, the input capacitor drains (step 412), and the input voltage drops. The method 400 further includes switching the MOSFET 210 off again (step 414) to allow the input voltage to rise again, forming a sinusoidal waveform. As explained above, MOSFET 210 refers to whichever one of the first MOSFET 210a and the second MOSFET 210b that is presently operational. The method 400 also includes continuously conditioning and outputting the input voltage via a DC output bus 224 (step 416). In certain example embodiments, the input voltage is filtered by the inductor 212 and rectified by the output diode 216. With such a method, the voltage output 226 of a constant current power correction circuit is made to match and follow the phase of the constant current input current. Thus, power efficiency is improved.

[0037] Referring to Figures 3 and 5, the method 500 of controlling the PFC circuit with power line communications 200 includes receiving the output voltage 303 from the PFC circuit 200 (step 502) and receiving the reference voltage 222 (step 504). In certain example embodiments, the output voltage 303 and the reference voltage 222 are received by the feedback controller 302. The method 500 further includes comparing the output voltage 303

to the reference voltage 222 (step 506). Accordingly, in certain example embodiments, the feedback controller 302 handles the comparison. The method 500 also includes generating a feedback controller output 304 from the comparison of the output voltage 303 and the reference voltage 222 (step 508). In comparing the output voltage 303 and the reference voltage 222, the method also determines whether the output voltage 303 is above or below the reference voltage 222 (step 510). If the output voltage 303 is above the reference voltage 222, then the feedback controller output 304 is decreased (step 512). If the output voltage 303 is below the reference voltage 222, then the feedback controller output 304 is increased (step 514). The method further includes multiplying 306 the feedback controller output 304 by the summation 307 of the sine wave reference 308 and the communication signal 314 to produce the sine control signal 310 (step 516). In certain example embodiments, the sine wave reference 308 has been synchronized with the input current waveform and thus includes the current phase. As such, the sine control signal 310 includes the desired amplitude data from the reference voltage 222, current phase data from the sine wave reference 308, and communication data from the communication signal 314. The method further includes converting the sine control signal 310 to a pulse width modulation (PWM) signal 316 (step 518). In certain example embodiments, the PWM generator performs step 518. The method also includes controlling the switching of the MOSFETs 210 through the PWM signal 316 (step 520). Thus, through the controlled switching of the MOSFETs 210, the input voltage 226 is formed to be in phase with the input current 206, have a desired amplitude as provided by the reference voltage, and contain communication data 318 as provided by the communication signal 314. In certain example embodiments, the method includes controlling the first and second MOSFETs 210a, 210b, depending on the half cycle of the input current. In certain other example embodiments, such as in a PFC circuit having a rectifier diode bridge, the method includes controlling a single MOSFET.

[0038] The present disclosure provides techniques for power factor correction with power line communications on a constant current system by matching the voltage waveform to the input current waveform. Although embodiments of the present disclosure have been described herein in detail, the descriptions are by way of example. The features of the disclosure described herein are representative and, in alternative embodiments, certain features and elements may be added or omitted. Additionally, modifications to aspects of the embodiments described herein may be made by those skilled in the art without departing from the spirit and scope of the present disclosure defined in the following claims, the scope

of which are to be accorded the broadest interpretation so as to encompass modifications and equivalent structures.

CLAIMS

What is claimed is:

1. A power factor correction circuit with power line communications, comprising:

an input capacitor configured to receive an input current from a constant current source and produce an input voltage;

a switching device coupled to the input capacitor, wherein the switching device switches between an OFF state and an ON state, and wherein the input voltage rises when the switching device is in the OFF state and drops when the switching device is in the ON state; and

a controller coupled to the switching device, wherein the controller controls switching of the switching device, and the switching of the switching device shapes the input voltage to be in phase with the input current, and wherein the switching of the switching device generates disturbances on the input voltage and input current, the disturbances having communication data.

2. The power factor correction circuit with power line communications of Claim 1, further comprising:

a rectifier diode bridge configured to receive the input current from the constant current source and rectify the input current.

3. The power factor correction circuit with power line communications of Claim 1, further comprising:

a first switching device coupled to the input capacitor, wherein the first switching device is operable during a first half cycle of the input current and shorted during a second half cycle of the input current, and switches between the OFF state and the ON state when operable;

a second switching device coupled to the input capacitor, wherein the second switching device is operable during the second half cycle of the input current and shorted during the first half cycle of the input current, and switches between the OFF state and the ON state when operable.

4. The power factor correction circuit with power line communications of Claim 1, wherein the switching device comprises a MOSFET.

5. The power factor correction circuit with power line communications of Claim 1, further comprising:

a DC output bus providing an output voltage, wherein the output voltage is a conditioned form of the input voltage, wherein the input voltage is in phase with the input current.

6. The power factor correction circuit with power line communications of Claim 5, further comprising:

a first inductor coupled to the input capacitor, wherein the first transformer provides the output voltage during the first half cycle of the input current; and

a second inductor coupled to the input capacitor, wherein the second transformer provides the output voltage during the second half cycle of the input current.

7. The power factor correction circuit with power line communications of Claim 1, wherein the controller produces a sine control waveform, the sine control waveform containing a desired voltage amplitude data, an input current phase data, and a communication data.

8. The power factor correction circuit with power line communications of Claim 7, wherein the controller comprises a pulse width modulation (PWM) generator which receives the sine control waveform and generates a corresponding PWM signal, wherein the PWM signal is used to control switching of the switching device.

9. A controller for a power factor correction (PFC) circuit with power line communications, comprising:

a controller configured to receive an input current from a PFC circuit, an output voltage from the PFC circuit, and a communication signal, wherein the controller generates a sine wave reference synchronized with the input current and adds the communication signal to the sine wave reference;

a feedback controller configured to compare the output voltage to a reference voltage and produce a feedback controller output, wherein the feedback controller output increases when the output voltage is below the reference voltage and decreases when the output voltage is above the reference voltage, and wherein the feedback controller output is multiplied with the summation of the sine wave reference and the communication signal to produce a control signal; and

a pulse width modulation (PWM) generator, wherein the PWM generator receives the control signal and converts the control signal into a corresponding PWM signal, wherein the PWM signal controls at least a portion of the PFC circuit, wherein the PFC circuit shapes the an input voltage to be in phase with the input current, and the input current, input voltage, or both include communication data reflective of the communication signal.

10. The controller for a power factor correction (PFC) circuit with power line communications of Claim 9, wherein the reference voltage represents a desired amplitude or power level of the output voltage.

11. The controller for a power factor correction (PFC) circuit with power line communications of Claim 9, wherein the PFC circuit comprises:

a MOSFET switchable between an OFF state and an ON state, wherein switching of the MOSFET shapes the input voltage, and wherein the PWM signal controls switching of the MOSFET.

12. The controller for a power factor correction (PFC) circuit with power line communications of Claim 11, wherein the MOSFET is switched ON when the output voltage reaches the reference voltage.

13. The controller for a power factor correction (PFC) circuit with power line communications of Claim 11, wherein the PFC circuit comprises an input capacitor configured to receive the input current from a constant current source and produce the input voltage, wherein when the MOSFET is in the OFF state, the input capacitor charges and the

input voltage rises, and when the MOSFET is in the ON state, the input capacitor drains and the input voltage drops.

14. The controller for a power factor correction (PFC) circuit with power line communications of Claim 9, wherein the communication signal is indicative of a system error, data, request, or update.

15. The controller for a power factor correction (PFC) circuit with power line communications of Claim 9, wherein the control signal contains a desired voltage amplitude data, an input current phase data, and a communication data.

16. A method of controlling a power factor correction (PFC) circuit having power line communications, comprising:

- receiving an output voltage from a PFC circuit;
- receiving a reference voltage indicative of a desired power level of the output voltage;
- comparing the output voltage to the reference voltage;
- generating a feedback controller output based on the difference between the output voltage and the reference voltage;
- receiving a sine wave reference synchronized with an input current from the PFC circuit;
- receiving a communication signal to be transmitted over the PFC circuit;
- summing the sine wave reference and the communication signal;
- multiplying the feedback controller output by the sum of the sine wave reference and the communication signal to produce a sine control signal; and
- controlling the PFC with the sine control signal and shaping an input voltage to be in phase with the input current.

17. The method of controlling a power factor correction (PFC) circuit having power line communications of Claim 16, further comprising:

- converting the sine control signal to a pulse width modulation (PWM) signal;

and

- controlling a switching device in the PFC circuit through the PWM signal, wherein switching of the switching device shapes the input voltage to be in phase with the input current, and causes disturbances on the output voltage and input current, wherein the disturbances contain communication data corresponding to the communication signal.

18. The method of controlling a power factor correction (PFC) circuit having power line communications of Claim 16, comprising:

- when the output voltage is above the reference voltage, decreasing the feedback controller output; and
- when the output voltage is below the reference voltage; increasing the feedback controller output.

19. The method of controlling a power factor correction (PFC) circuit having power line communications of Claim 18, further comprising:

when the input current is in a first half cycle, controlling a first switching device; and

when the input current is in a second half cycle, controlling a second switching device.

20. The method of controlling a power factor correction (PFC) circuit having power line communications of Claim 17, wherein the switching device comprises a MOSFET.

1/5

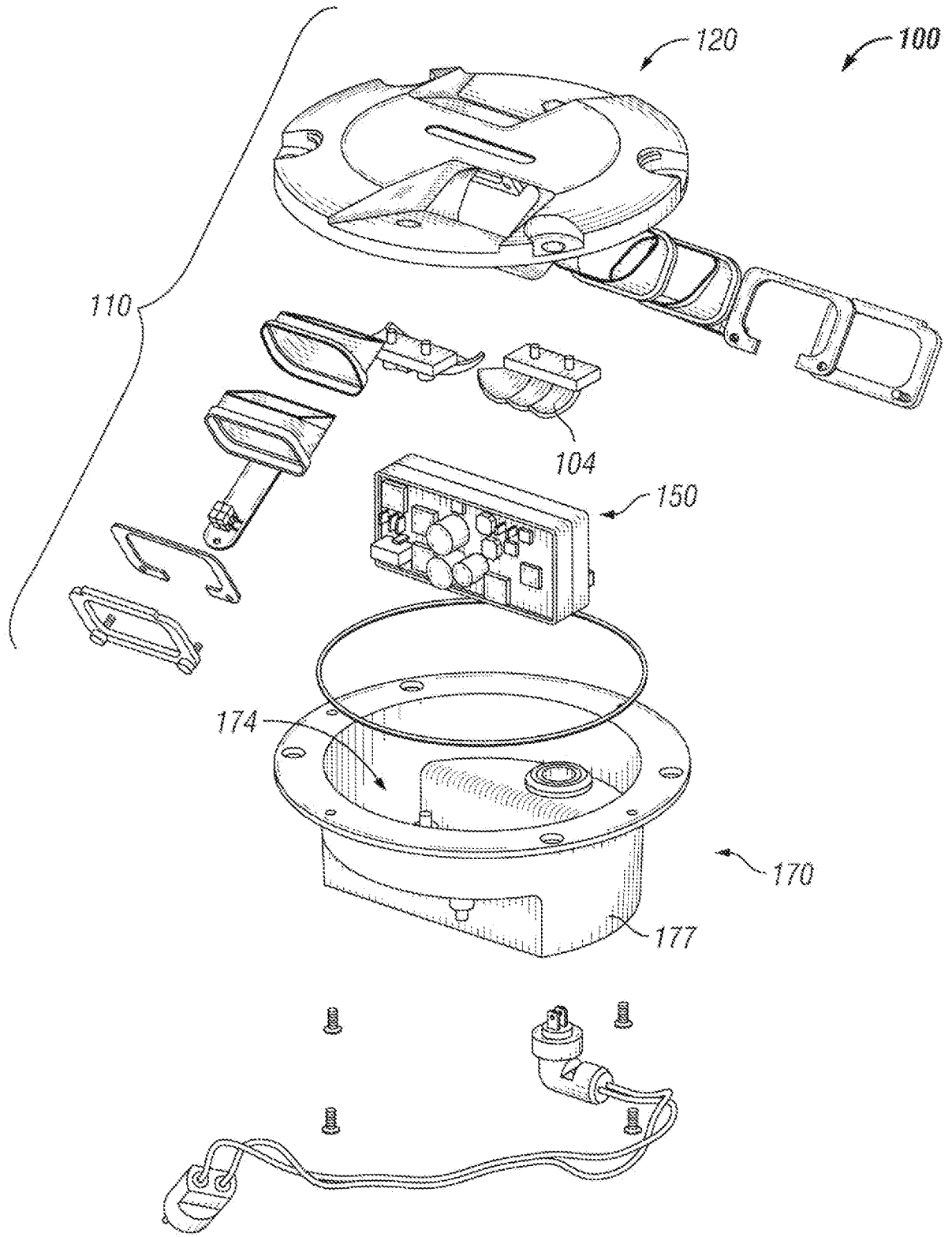


FIG. 1

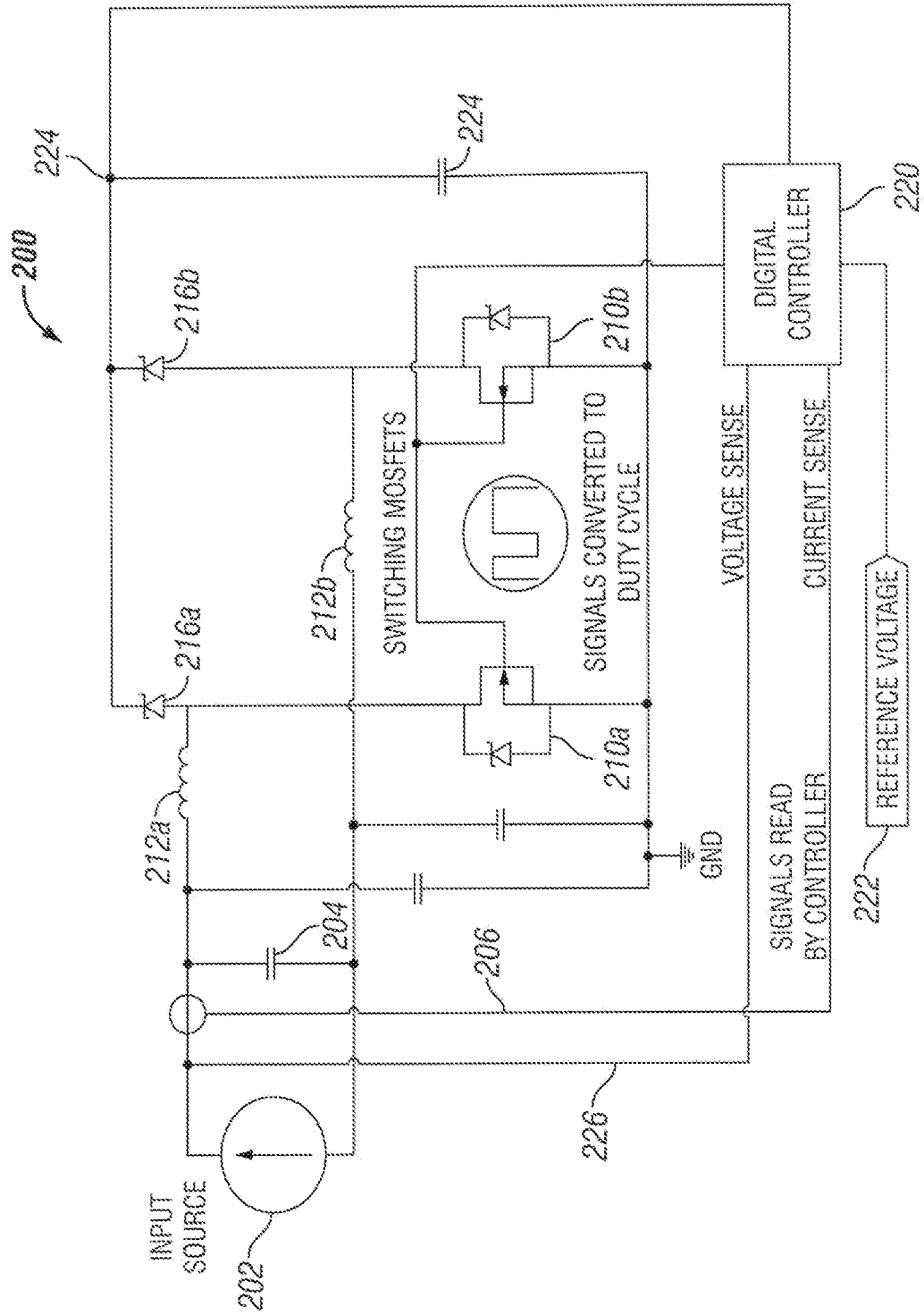


FIG. 2

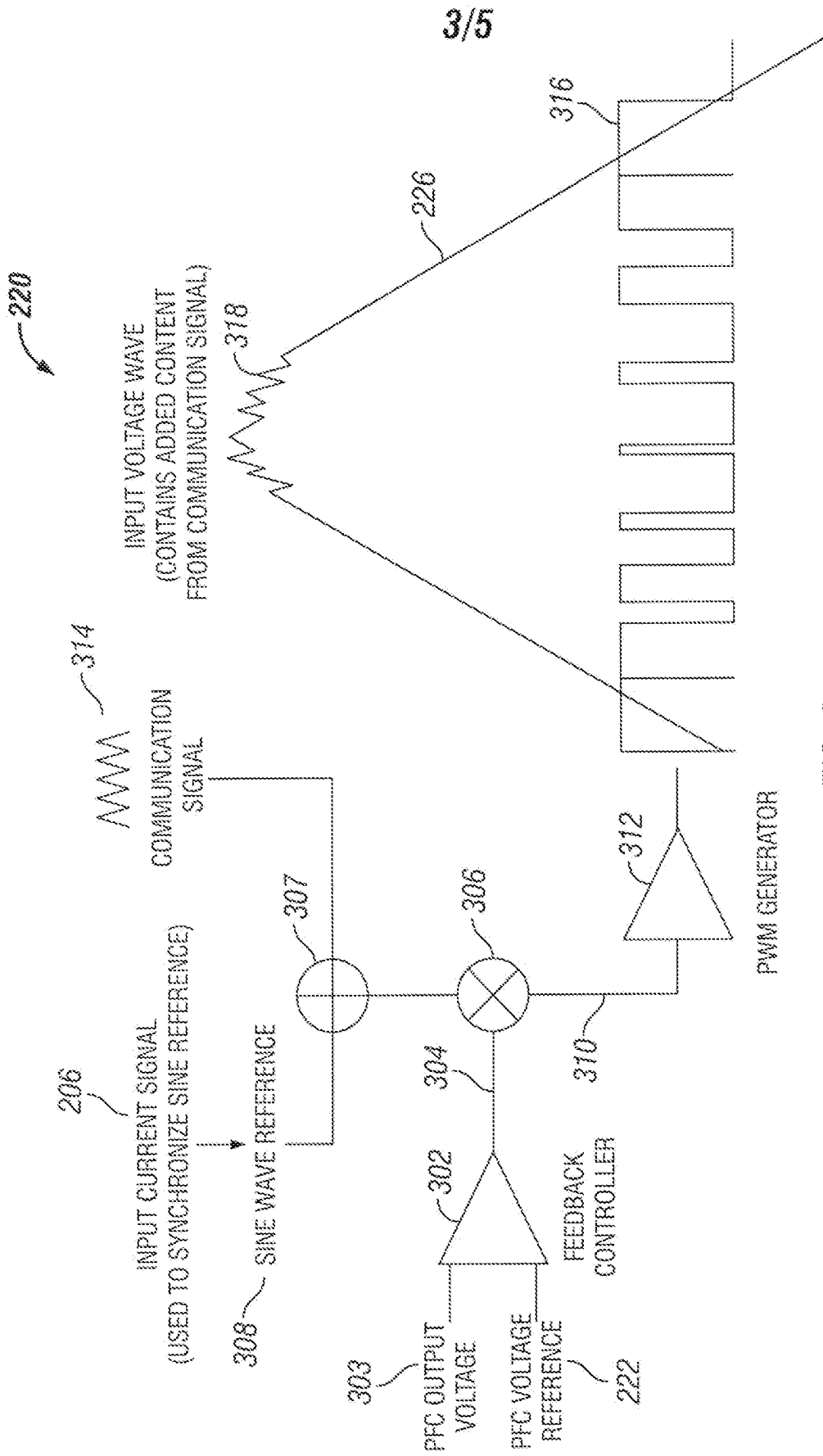


FIG. 3

4/5

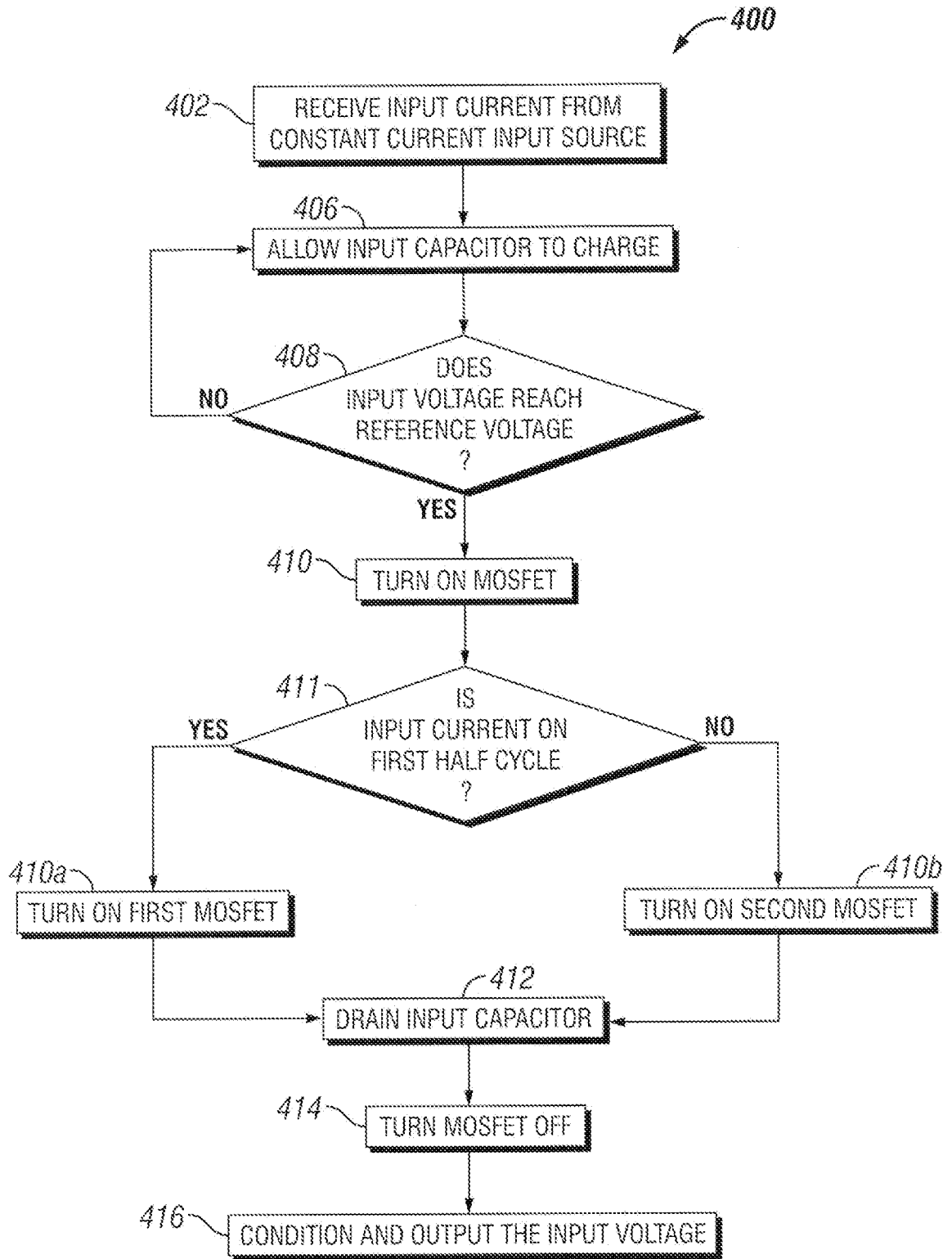


FIG. 4

5/5

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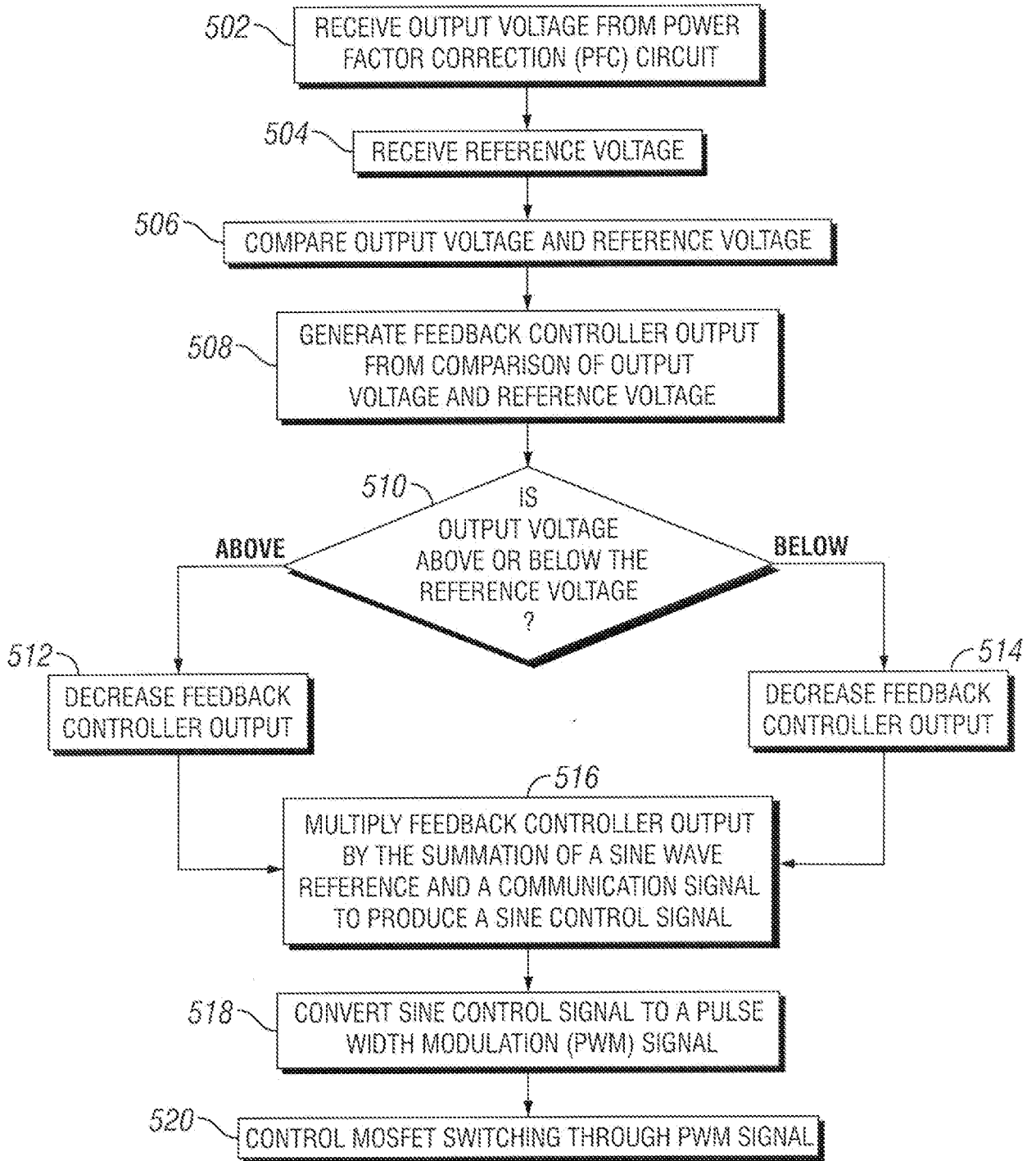


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/036248

A. CLASSIFICATION OF SUBJECT MATTER				
G05F 1/70 (2006.01) H02M 7/162 (2006.01)				
According to International Patent Classification (IPC) or to both national classification and IPC				
B. FIELDS SEARCHED				
Minimum documentation searched (classification system followed by classification symbols)				
G06F 17/00, 17/50, G05F 1/00-1/70, H02J 3/00, 3/12, 3/18, H02M 3/00, 7/00-7/162				
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched				
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)				
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS				
C. DOCUMENTS CONSIDERED TO BE RELEVANT				
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
X Y A	US 2008/0252268 A1 (INFINEON TECHNOLOGIES AUSTRIA) 16.10.2008, abstract, paragraphs [0002], [0005], [0032]-[0045], [0063]-[0070], [0084], claims 1, 13	1-2, 4-8 3 9-20		
Y	US 2011/0109283 A1 (INFINEON TECHNOLOGIES AUSTRIA) 12.05.2011, claim 22	3		
A	WO 2005/041393 A2 (PF1 INC) 06.05.2005	1-20		
A	US 6259613 B1 (SAMSUNG ELECTRONICS CO LTD) 10.07.2001	1-20		
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.				
* Special categories of cited documents: <table style="width: 100%; border: none;"> <tr> <td style="width: 50%; border: none;"> "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed </td> <td style="width: 50%; border: none;"> "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family </td> </tr> </table>			"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
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Date of the actual completion of the international search		Date of mailing of the international search report		
04 September 2014 (04.09.2014)		25 September 2014 (25.09.2014)		
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