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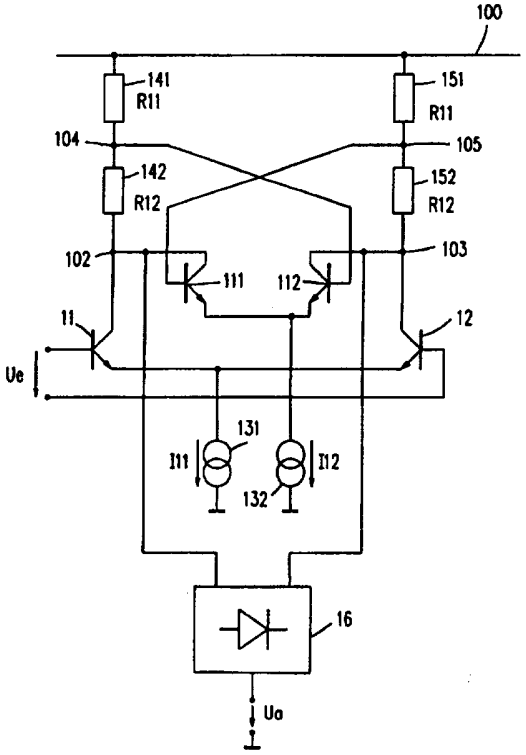
(54) Title: CIRCUIT ARRANGEMENT COMPRISING A LOGARITHMIC TRANSFER FUNCTION

(57) Abstract

A description is given of a circuit arrangement comprising a logarithmic transfer function between an input signal and an output signal in a predefined level range of the input signal, comprising a pair of amplifier elements forming a first differential amplifier, the main current paths of which amplifier elements are connected, on the one hand, to each other and to a first current source and on the other hand, to working impedances subdivided by respective taps, and the control terminals of which amplifier elements are supplied with the input signal; a pair of amplifier elements forming a second differential amplifier, the main current paths of which amplifier elements are connected, on the one hand, to each other and to a second current source and on the other hand, to the connections of the main current paths of the first differential amplifier and the working impedances, and whose control terminals are cross-connected to the taps of the working impedances; and a rectifier stage whose input is connected to the connections of the main current paths of the differential amplifiers and the working impedances and whose output signal is tapped from its output. This circuit arrangement has a very low power consumption and low circuit complexity.



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Circuit arrangement comprising a logarithmic transfer function

The invention relates to a circuit arrangement comprising a logarithmic transfer function.

In receiver circuits, for example, for pagers, need to have arrangements for controlling certain functions such as the mute mode, the indication of signal levels or the automatic gain control, by which arrangements the field strength of received signals (voltages, signal level) can be detected. Field strength detectors or voltage detectors used in this respect generally have a logarithmic transfer function between the (antenna) signal supplied thereto and their output signal, which output signal represents a measure for the detected field strength or voltage respectively. This means that when the input field strength or input voltage respectively, is plotted logarithmically against a linear representation of the output voltage of the detector, a substantially linear characteristic curve evolves in the diagram.

Such a diagram is shown in Fig. 1. The abscissa therein shows an input voltage Ue in a logarithmic scale. Among the ordinate in Fig. 1 is shown the associated output voltage Ua in a linear scale. In the level range between the input voltages Ue1 and Ue2 there is a characteristic curve in linear representation, i.e. a straight line, which represents a logarithmic relation between the input voltage Ue and the output voltage Ua, i.e. a logarithmic transfer function between these two voltages. The control region for the input voltage Ue when the voltage detector is in operation lies preferably between the voltage limits Ue1 and Ue2. Fig. 1 shows in this respect the transfer function of an ideal field strength detector or voltage detector, respectively.

Fig. 2 shows a possibility for an embodiment of a voltage detector which has a transfer function as shown in Fig. 1. This circuit arrangement comprises a plurality of correspondingly dimensioned differential amplifier stages 1, 2, ... n formed each by an emitter-coupled transistor pair 11, 12; 21, 22; ...; n1, n2, a respective emitter current source 13, 23, ..., n3 feeding each transistor pair and, for each of the transistors 11, 12; 21, 22; ...; n1, n2 a collector resistance 14, 15; 24, 25; ..., n4, n5 led to a shared power supply terminal 100. The base terminals of the individual transistor pairs 11, 12; ... n1, n2 form input terminals of the differential amplifier stages 1, ...n, the collector terminals of these

transistor pairs forming output terminals of the differential amplifier stages 1, ..., n. The differential amplifier stages 1, ..., n are connected to each other as a ladder network. The input of the first differential amplifier stage 1 is supplied with the input voltage Ue. The collector resistances 14, 15 of the first differential amplifier stage 1 have the resistance value R1, the collector resistances 24, 25 of the second differential amplifier stage 2 the resistance value R2, and so on; accordingly, the resistance values of the collector resistances n4, n5 of the n^{th} differential amplifier stage n are selected to be Rn. The emitter current sources 13, 23, ..., n3 produce the direct currents I1, I2, ..., In, respectively. The following dimensioning holds R1 = R2 = ... = Rn and I1 = I2 = ... = In i.e. all the differential amplifier stages 1, 2, ..., n have the same dimensioning, thus have the same gain and the same operating points.

The output signals of the differential amplifier stages 1, 2, ..., n are furthermore connected each to a rectifier stage 16, 17, ..., n6, respectively. Their (rectified) output signals are linearly added together in an adding circuit 101 and the sum is produced as output voltage Ua.

In the circuit arrangement shown in Fig. 2 the voltage range for the input voltage Ue between the voltage limits Ue1 and Ue2 depends on the number n of differential amplifier stages 1, 2, ..., n. However, there must be at least two differential amplifier stages available.

The use of a circuit arrangement as shown in Fig. 2, however, is very limited. For example, if the individual differential amplifier stages 1, 2, ..., n are dimensioned differently, or if each of the differential amplifier stages 1, 2, ..., n is followed by a respective high-pass filter, i.e. inserted into the ladder network, the circuit arrangement thus formed can no longer be used for obtaining a logarithmic characteristic curve.

On the other hand, the circuit arrangement shown in Fig. 2 represents a circuit complexity which, particularly for devices to be operated with low-capacity batteries, exceeds the limits of what is justifiable. This practically eliminates a use, for example, in a pager operating on a low battery voltage or in devices having comparable requirements as to energy supply and compact structure. The circuit arrangement shown in Fig. 2 does not satisfy the strict requirements made here with respect to a low power consumption and low circuit complexity. This circuit complexity would only be permitted to the extent of a differential amplifier stage 1, 2, ..., n in combination with an associated rectifier stage 16, 26,..., n6, respectively. With this limitation (n=1), the circuit arrangement shown in Fig. 2 does not provide the desired transfer function, however.

It is an object of the invention to provide a circuit arrangement having a logarithmic transfer function, which arrangement can be used, for example, as a voltage detector and has a very low power consumption and a very low circuit complexity.

This object is achieved according to the invention by a circuit arrangement comprising a logarithmic transfer function between an input signal and an output signal within a predefined level range of the input signal, comprising

- a pair of amplifier elements forming a first differential amplifier
  - the main current paths of which amplifier elements are connected,
    - on the one hand, to each other and to a first current source and
    - on the other hand, to working impedances subdivided by respective taps, and
  - the control terminals of which amplifier elements are supplied with the input signal,
- a pair of amplifier elements forming a second differential amplifier,
  - the main current paths of which amplifier elements are connected,
    - on the one hand, to each other and to a second current source and
    - on the other hand, to the connections of the main current paths of the first differential amplifier and the working impedances, and
  - whose control terminals are cross-connected to the taps of the working impedances, and
- a rectifier stage whose input is connected to the connections of the main current paths of the differential amplifiers and the working impedances and whose output signal is tapped from its output.

An exemplary embodiment with reference to which the invention may also be explained in general is shown in Fig. 3. A basic structure of this embodiment for the circuit arrangement according to the invention is derived from one of the differential amplifier stages 1, 2, ..., n of Fig. 2; accordingly, comparable or identical elements have like reference characters.

Compared to one of the differential amplifier stages 1, 2, ..., n of Fig. 2 - the first differential amplifier stage 1 being taken as an example in the following - the circuit arrangement according to the invention comprises a further transistor pair 111, 112, which is also structured in the form of an (emitted coupled) differential amplifier which is supplied with the direct current I12 by an emitter current source 132. In lieu of the emitter current source 13 of the differential amplifier stage 1 of Fig. 2, an emitter current source 131 occurs

having a direct current I11. The terminals facing away from the emitter current sources 131, 132 of the main current paths of the transistor pair 111, 112, in the example shown in Fig. 3 they are the collector terminals of the transistor pair 111, 112, are connected to nodes 102 and 103 respectively, in which nodes are connected the main current paths of the transistor pair 11, 12 having the associated collector resistances and which nodes represent output terminals of the differential amplifier formed by the transistor pair 11, 12. The collector resistances 14, 15 of the differential amplifier stage 1 in Fig. 2 i.e. the working impedances of the transistor pair 11, 12 are subdivided according to the invention by a tap 104, 105 respectively. The cross-connections of the transistor pair 111, 112 are connected to these taps 104, 105.

In this manner, the circuit complexity according to the invention is only slightly higher than for one of the differential amplifier stages 1, 2, ..., n shown in Fig. 2.

Compared to the differential amplifier stage 1 shown in Fig. 2, the working impedances divided each into sub-resistances 141, 142 and 151, 152 respectively, take the place of the collector resistances 14, 15. The sub-resistances 141, 151 have a resistance value R11 and the sub-resistances 142, 152 a resistance value R12. These resistance values may preferably be selected so that their sum R11 + R12 corresponds to the resistance value R1, which a collector resistance 14, 15 respectively, of a circuit arrangement as shown in Fig. 2 would have. Accordingly, the sum of the d.c. currents I11 + I12 of the emitter current sources 131 and 132 and the d.c. current I1 of the emitter current source 13 of Fig. 2 may preferably be selected to be the same. In that case, no additional power consumption is caused by the circuit arrangement according to the invention compared with the differential amplifier stage 1, 2, ..., n respectively, of Fig. 2.

The connection of the first and second differential amplifiers of the circuit arrangement according to the invention has (with respect to the nodes 102, 103 in Fig. 3) an output impedance which depends on the input signal (input voltage Ue). The consequent non-linearity between the input signal and the output signal accurately produces the logarithmic transfer function. The degree to which an exact logarithmic transfer function is approximated is decisively determined by the ratio of the values of the d.c. currents (I11, I12 respectively) produced by the first and the second current sources (131, 132 respectively, in Fig. 3). While assuming a certain ratio, the exact logarithmic transfer function may thus be approximated must accurately. The accuracy turns out to be larger as the ratio of the value of the d.c. current (I11) of the first current source (131) to that of the second current source 132 is selected lower. Preferably, this ratio is fixed at a value of at least approximately 3.

Choosing a smaller value for this ratio enhances the accuracy with which the logarithmic transfer function is obtained even more, but at the same time decreases thereby the stability of the circuit arrangement according to the invention. This means that the transfer function obtained for smaller values of said ratio is more logarithmic indeed, but that tolerances of the dimensioning of the individual circuit elements obtain more influence.

Fig. 4 shows a comparison of three characteristic curves between the logarithmically shown input voltage Ue and the linearly shown output voltage Ua. Curve a) shows the behavior of one of the differential amplifier stages 1, 2, ..., n of Fig. 2. Fig. b) shows by way of comparison the relation between the input voltage Ue and the output voltage Ua of the circuit arrangement according to the invention shown in the exemplary embodiment of Fig. 3, for the case where the ratio of the d.c. current I11 to the d.c. current I12 assumes the value 3. As against the case of curve a), curve b) in Fig. 4 shows a clearly linear variation which corresponds to an improved approximation of the exact logarithmic transfer function. Finally, for curve c) the above ratio of the currents I11 and I12 is set to the value 2. This again provides an improved approximation of the exact logarithmic variation of the transfer function compared with curve b).

Preferably, the first and second power sources (131, 132 in Fig. 3) and the working impedances (141, 142, 151, 152 in Fig. 3) are dimensioned so that even with the highest level of the input signal to be processed (input voltage Ue), a saturation of the differential amplifier (11, 12; 111, 112) is avoided, but that the second differential amplifier (111, 112) is slightly overloaded.

The circuit arrangement according to the invention may preferably be inserted into a logarithmic linearization stage. Such a linearization stage is preferably used in a level detector to obtain a more accurate characteristic curve and thus an improved detection accuracy. If such a level detector is used in an Automatic Gain Control (AGC), the function of this Automatic Gain Control would also become more precise. A preferred field of application for such circuit arrangements are pagers for which the exact mode of operation and the low power consumption with minimum circuit complexity is most favorable.

CLAIMS:

1. A circuit arrangement comprising a logarithmic transfer function between an input signal and an output signal in a predefined level range of the input signal, comprising

- a pair of amplifier elements forming a first differential amplifier
  - -- the main current paths of which amplifier elements are connected,
    - --- on the one hand, to each other and to a first current source and
    - --- on the other hand, to working impedances subdivided by respective taps, and
  - -- the control terminals of which amplifier elements are supplied with the input signal,
- a pair of amplifier elements forming a second differential amplifier,
  - -- the main current paths of which amplifier elements are connected,
    - --- on the one hand, to each other and to a second current source and
    - --- on the other hand, to the connections of the main current paths of the first differential amplifier and the working impedances, and
  - -- whose control terminals are cross-connected to the taps of the working impedances, and
- a rectifier stage whose input is connected to the connections of the main current paths of the differential amplifiers and the working impedances and whose output signal is tapped from its output.

2. A circuit arrangement as claimed in Claim 1, characterized in that the values of the currents produced by the first and second current sources have a predefined ratio to each other.

3. A circuit arrangement as claimed in Claim 2, characterized in that the ratio of the current value of the first current source to that of the second current source is at most 3.

4. A circuit arrangement as claimed in Claim 1, 2 or 3, characterized in that the first and second current sources and the operating impedances are dimensioned so that even with the largest level of the input signal to be processed a saturation of the differential

amplifier is avoided, but that the second differential amplifier is slightly overloaded.

5. A logarithmic linearization stage, characterized by a circuit arrangement as claimed in one of the preceding Claims.

6. A level detector, characterized by a logarithmic linearization stage as claimed in Claim 5.

7. An automatic gain control, characterized by a level detector as claimed in Claim 6.

8. A pager characterized by an automatic gain control as claimed in Claim 7.

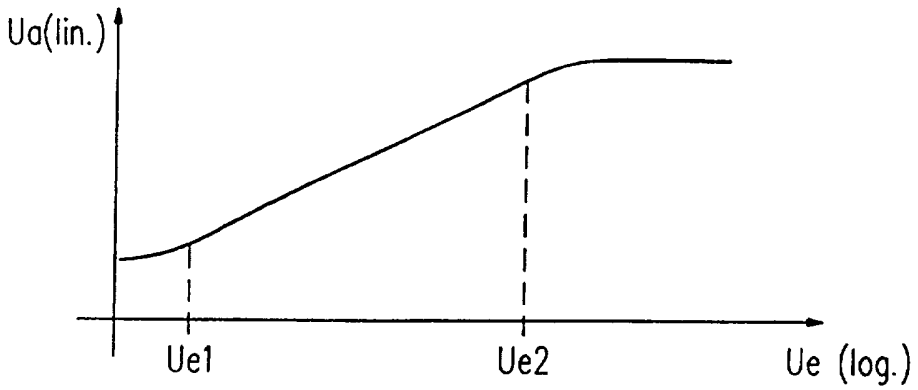
Ua(lin.)
Ue1
Ue2
Ue (log.)

Fig.1

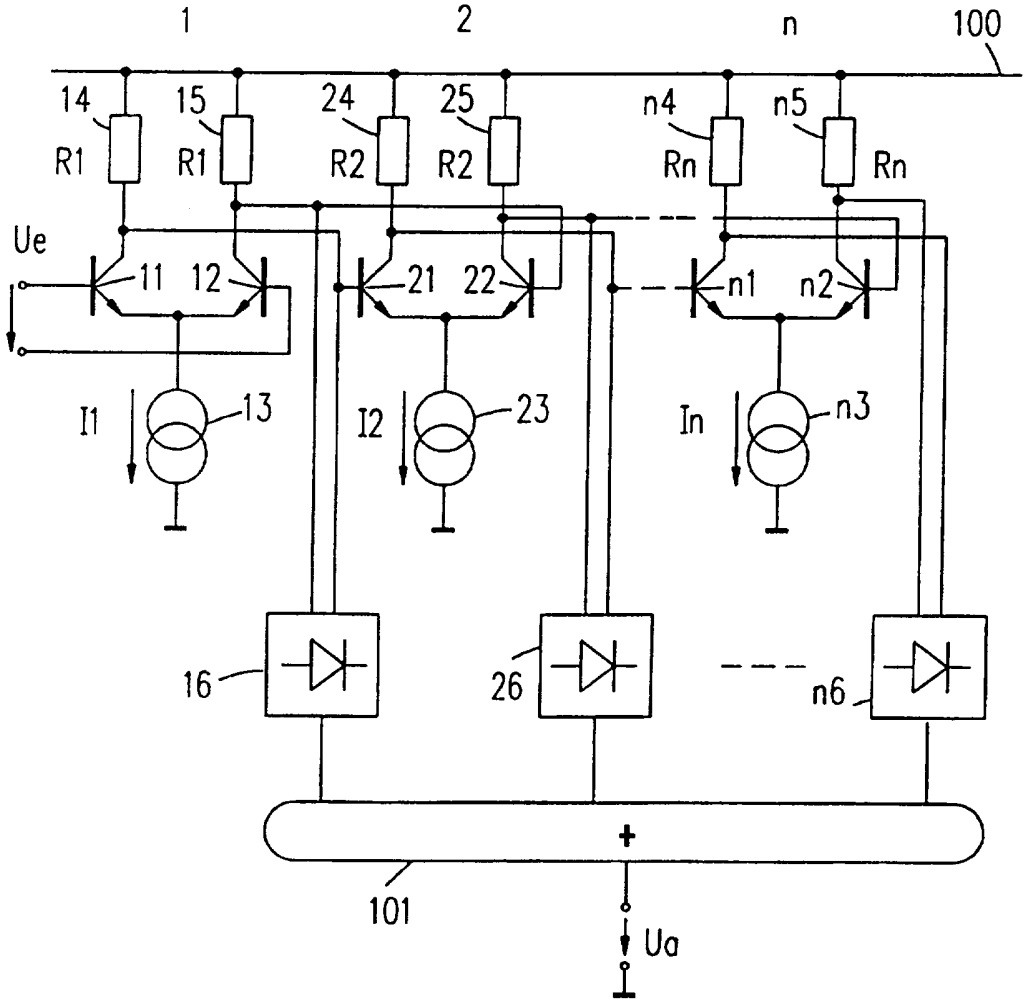
1
2
n
100
14
15
24
25
n4
n5
R1
R1
R2
R2
Rn
Rn
Ue
11
12
21
22
n1
n2
I1
13
I2
23
In
n3
16
26
n6
+
101
Ua

Fig.2

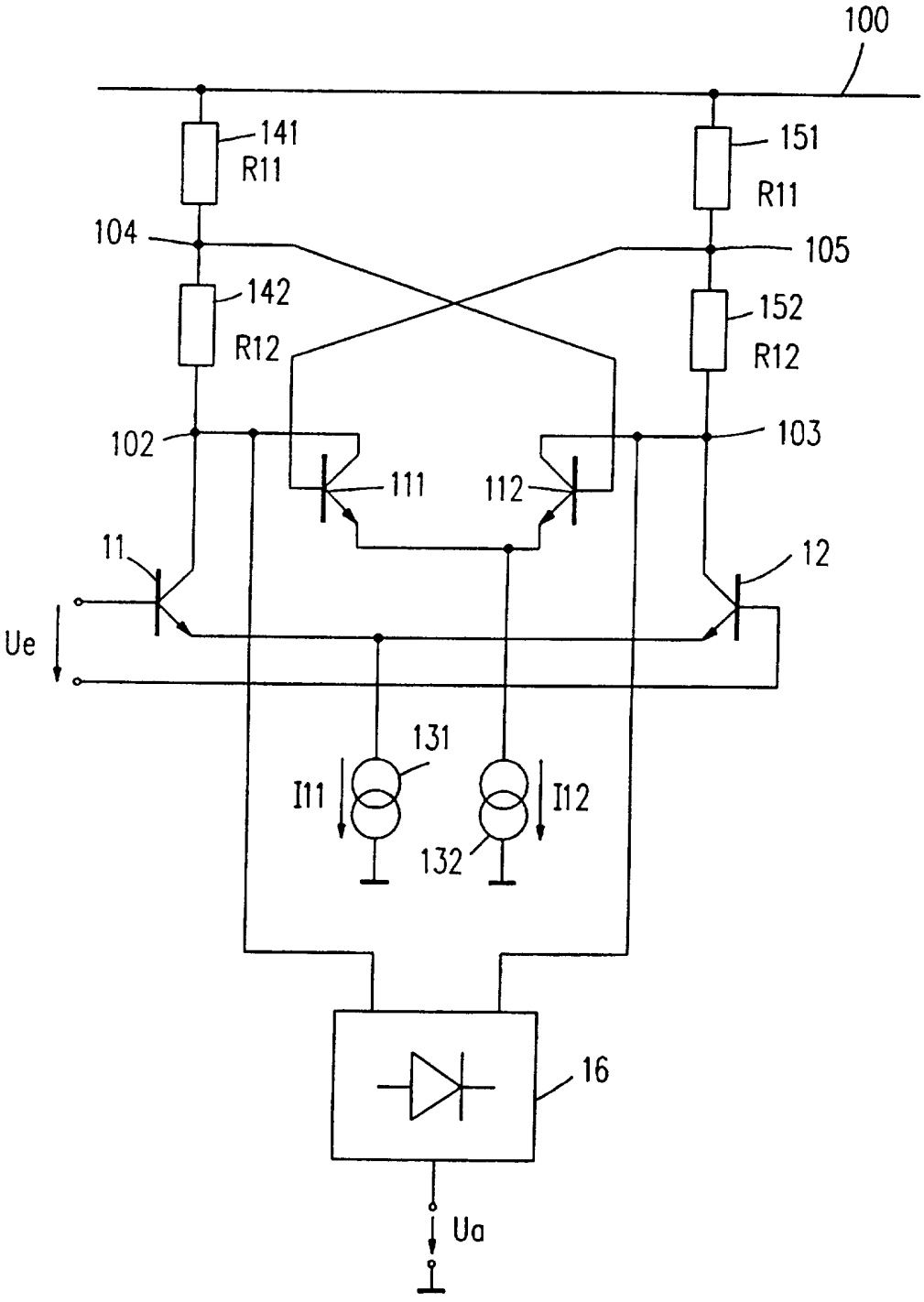
100
141
R11
151
R11
104
105
142
R12
152
R12
102
103
111
112
11
12
Ue
131
I11
I12
132
16
Ua

Fig.3

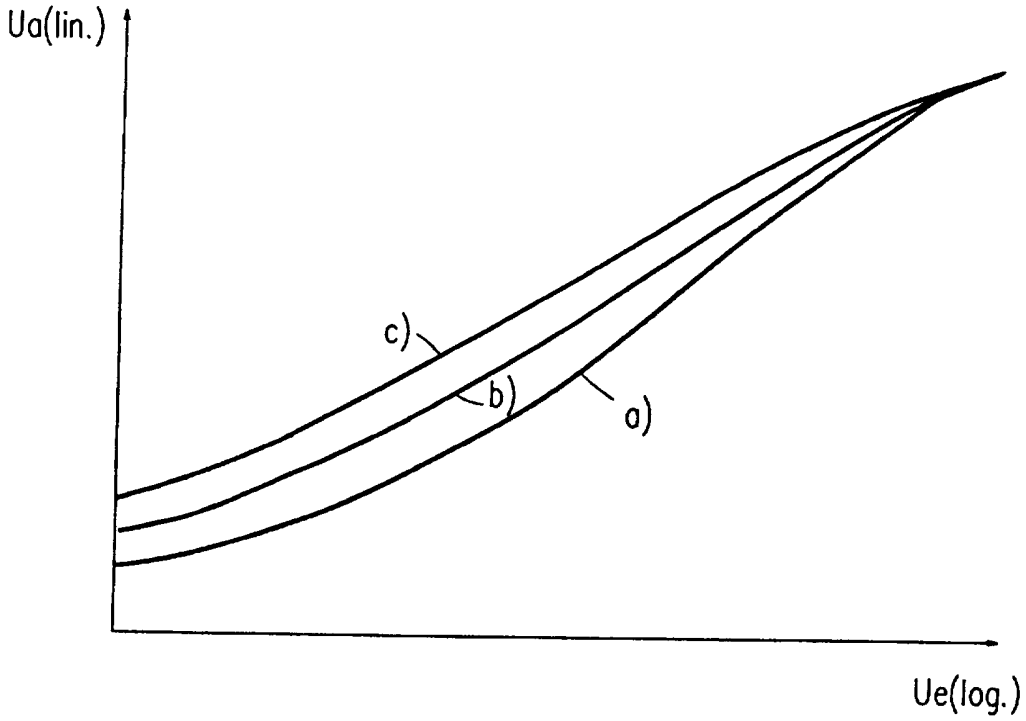

Fig.4